

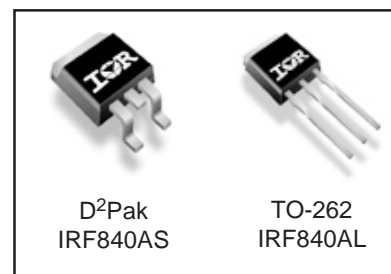
**Applications**

- Switch Mode Power Supply (SMPS)
- Uninterruptible Power Supply
- High Speed Power Switching

$V_{DSS}$	$R_{DS(on) \max}$	$I_D$
500V	0.85Ω	8.0A

**Benefits**

- Low Gate Charge Qg Results in Simple Drive Requirement
- Improved Gate, Avalanche and Dynamic dv/dt Ruggedness
- Fully Characterized Capacitance and Avalanche Voltage and Current
- Effective Coss Specified (See AN 1001)



**Absolute Maximum Ratings**

	Parameter	Max.	Units
$I_D @ T_C = 25^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10V$ ⑥	8.0	A
$I_D @ T_C = 100^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10V$ ⑥	5.1	
$I_{DM}$	Pulsed Drain Current ① ⑥	32	
$P_D @ T_C = 25^\circ\text{C}$	Power Dissipation	125	W
$P_D @ T_A = 25^\circ\text{C}$	Power Dissipation	3.1	
	Linear Derating Factor	1.0	W/°C
$V_{GS}$	Gate-to-Source Voltage	± 30	V
dv/dt	Peak Diode Recovery dv/dt ③ ⑥	5.0	V/ns
$T_J$	Operating Junction and	-55 to + 150	°C
$T_{STG}$	Storage Temperature Range		
	Soldering Temperature, for 10 seconds	300 (1.6mm from case )	

**Typical SMPS Topologies**

- Two Transistor Forward
- Haft Bridge
- Full Bridge

Notes ① through ⑥ are on page 10  
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# IRF840AS/L

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## Static @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	500	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.58	—	V/ $^\circ\text{C}$	Reference to $25^\circ\text{C}, I_D = 1\text{mA}$ ⑥
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	—	0.85	$\Omega$	$V_{GS} = 10V, I_D = 4.8A$ ④
$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	4.0	V	$V_{DS} = V_{GS}, I_D = 250\mu A$
$I_{DSS}$	Drain-to-Source Leakage Current	—	—	25	$\mu A$	$V_{DS} = 500V, V_{GS} = 0V$
		—	—	250		$V_{DS} = 400V, V_{GS} = 0V, T_J = 125^\circ\text{C}$
$I_{GSS}$	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS} = 30V$
	Gate-to-Source Reverse Leakage	—	—	-100		$V_{GS} = -30V$

## Dynamic @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$g_{fs}$	Forward Transconductance	3.7	—	—	S	$V_{DS} = 50V, I_D = 4.8A$
$Q_g$	Total Gate Charge	—	—	38	nC	$I_D = 8.0A$
$Q_{gs}$	Gate-to-Source Charge	—	—	9.0		$V_{DS} = 400V$
$Q_{gd}$	Gate-to-Drain ("Miller") Charge	—	—	18		$V_{GS} = 10V$ , See Fig. 6 and 13 ④⑥
$t_{d(on)}$	Turn-On Delay Time	—	11	—	ns	$V_{DD} = 250V$
$t_r$	Rise Time	—	23	—		$I_D = 8.0A$
$t_{d(off)}$	Turn-Off Delay Time	—	26	—		$R_G = 9.1\Omega$
$t_f$	Fall Time	—	19	—		$R_D = 31\Omega$ , See Fig. 10 ④⑥
$C_{iss}$	Input Capacitance	—	1018	—	pF	$V_{GS} = 0V$
$C_{oss}$	Output Capacitance	—	155	—		$V_{DS} = 25V$
$C_{rss}$	Reverse Transfer Capacitance	—	8.0	—		$f = 1.0\text{MHz}$ , See Fig. 5
$C_{oss}$	Output Capacitance	—	1490	—		$V_{GS} = 0V, V_{DS} = 1.0V, f = 1.0\text{MHz}$
$C_{oss}$	Output Capacitance	—	42	—		$V_{GS} = 0V, V_{DS} = 400V, f = 1.0\text{MHz}$
$C_{oss\ eff.}$	Effective Output Capacitance	—	56	—		$V_{GS} = 0V, V_{DS} = 0V \text{ to } 480V$ ⑤⑥

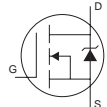
## Avalanche Characteristics

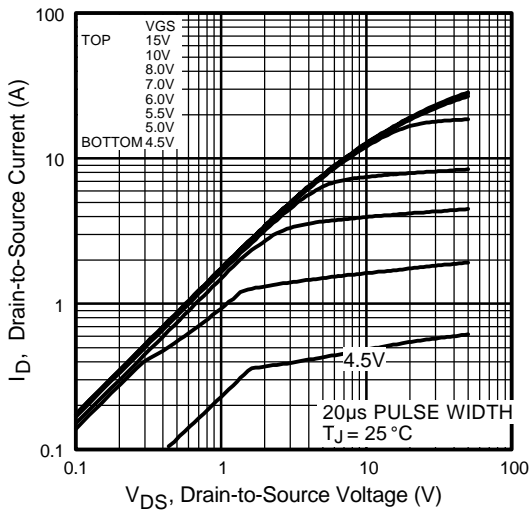
	Parameter	Typ.	Max.	Units
$E_{AS}$	Single Pulse Avalanche Energy②	—	510	mJ
$I_{AR}$	Avalanche Current①	—	8.0	A
$E_{AR}$	Repetitive Avalanche Energy①	—	13	mJ

## Thermal Resistance

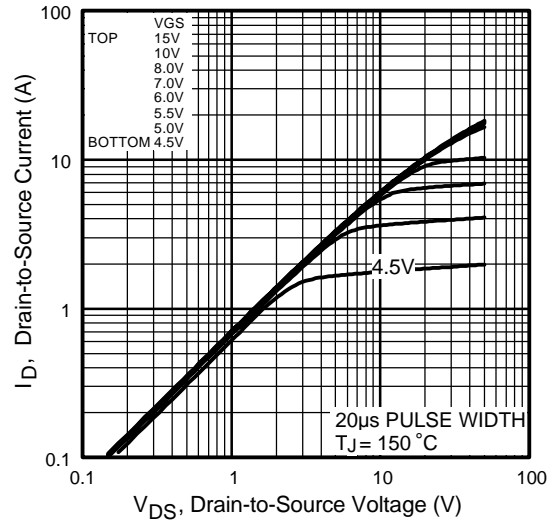
	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	1.0	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Junction-to-Ambient (PCB Mounted, steady-state)*	—	40	

## Diode Characteristics

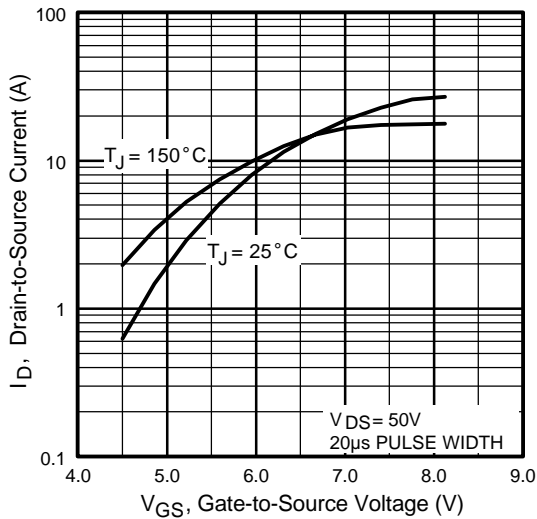
	Parameter	Min.	Typ.	Max.	Units	Conditions
$I_S$	Continuous Source Current (Body Diode)	—	—	8.0	A	MOSFET symbol showing the integral reverse p-n junction diode. 
$I_{SM}$	Pulsed Source Current (Body Diode) ①	—	—	32		
$V_{SD}$	Diode Forward Voltage	—	—	2.0	V	$T_J = 25^\circ\text{C}, I_S = 8.0A, V_{GS} = 0V$ ④
$t_{rr}$	Reverse Recovery Time	—	422	633	ns	$T_J = 25^\circ\text{C}, I_F = 8.0A$
$Q_{rr}$	Reverse Recovery Charge	—	2.0	3.0	$\mu\text{C}$	$di/dt = 100A/\mu\text{s}$ ④
$t_{on}$	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S+L_D$ )				



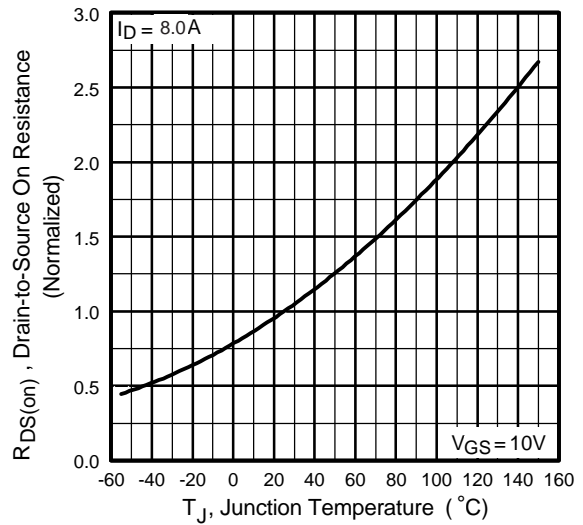
**Fig 1.** Typical Output Characteristics



**Fig 2.** Typical Output Characteristics

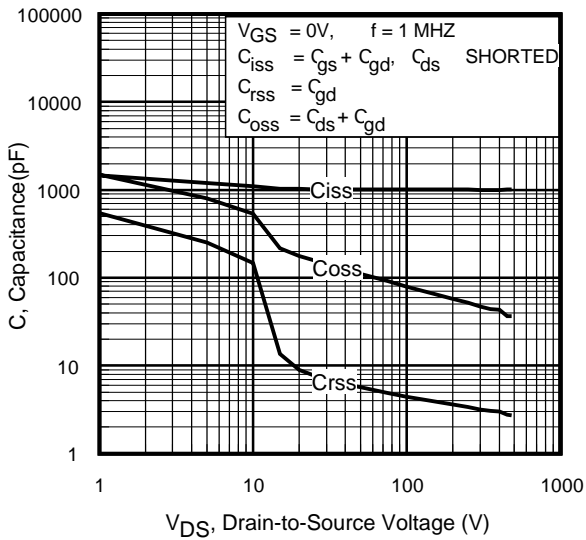


**Fig 3.** Typical Transfer Characteristics

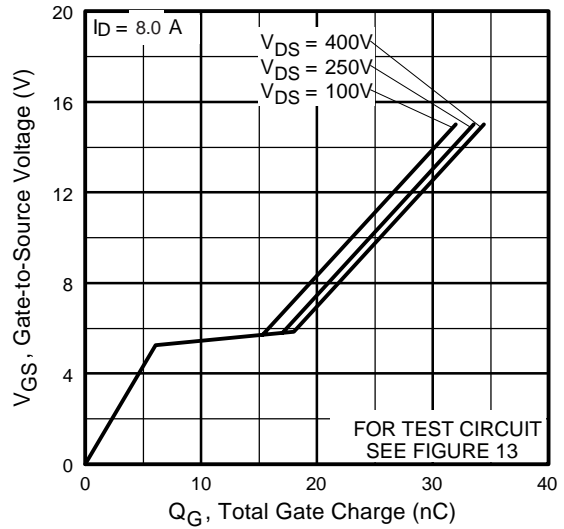


**Fig 4.** Normalized On-Resistance Vs. Temperature

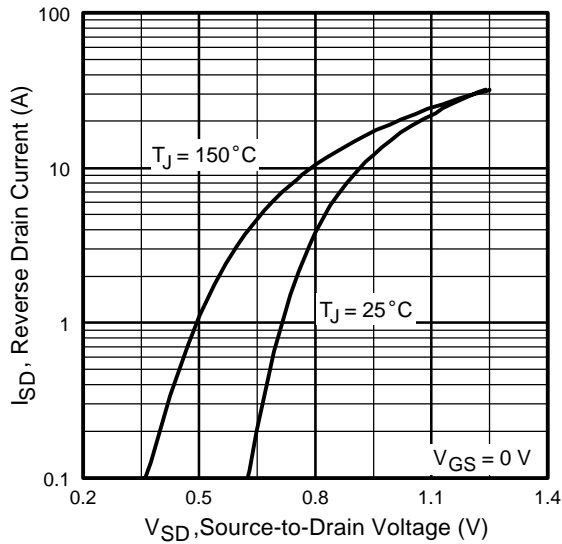
# IRF840AS/L



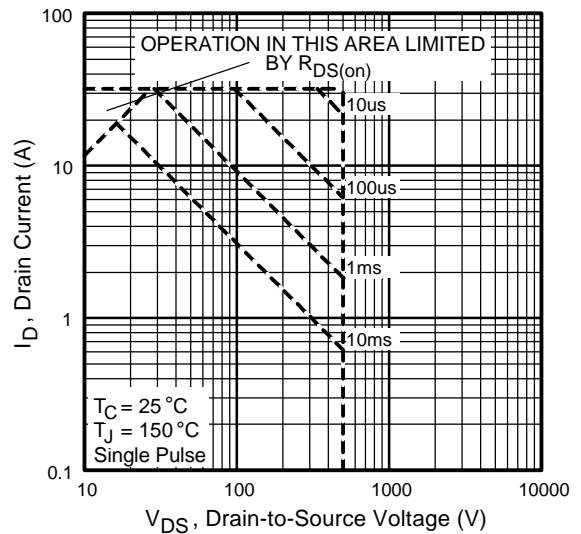
**Fig 5.** Typical Capacitance Vs. Drain-to-Source Voltage



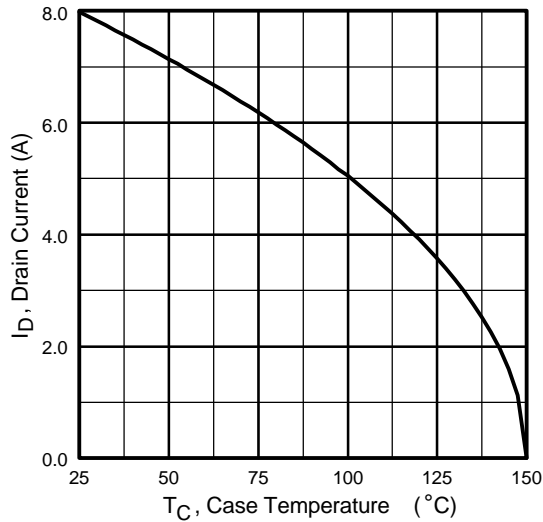
**Fig 6.** Typical Gate Charge Vs. Gate-to-Source Voltage



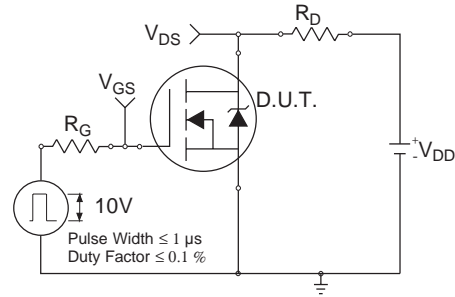
**Fig 7.** Typical Source-Drain Diode Forward Voltage



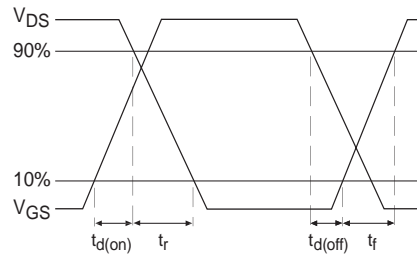
**Fig 8.** Maximum Safe Operating Area



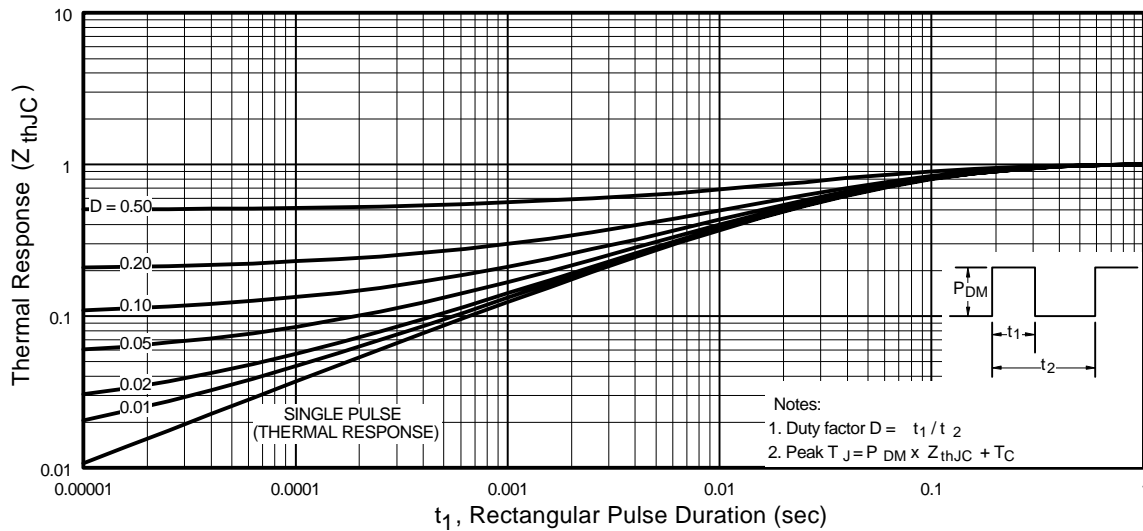
**Fig 9.** Maximum Drain Current Vs. Case Temperature



**Fig 10a.** Switching Time Test Circuit

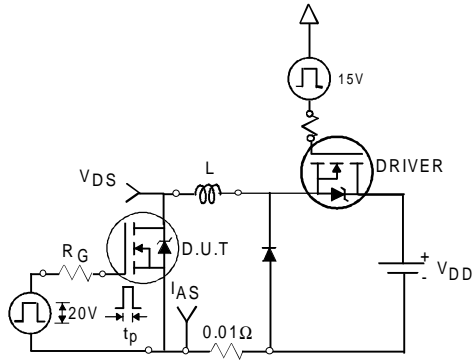


**Fig 10b.** Switching Time Waveforms

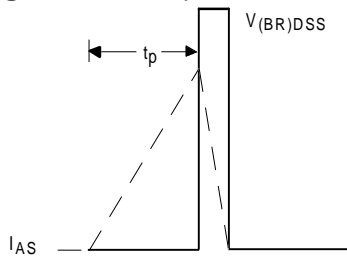


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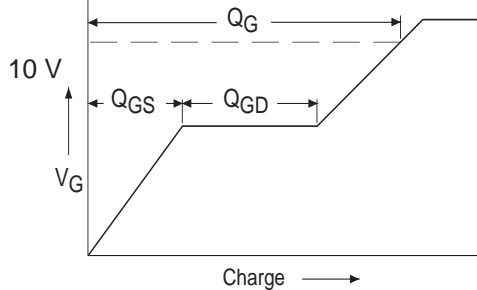
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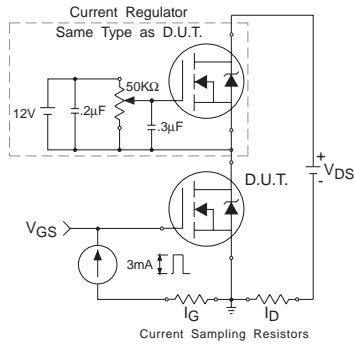
**Fig 12a.** Unclamped Inductive Test Circuit



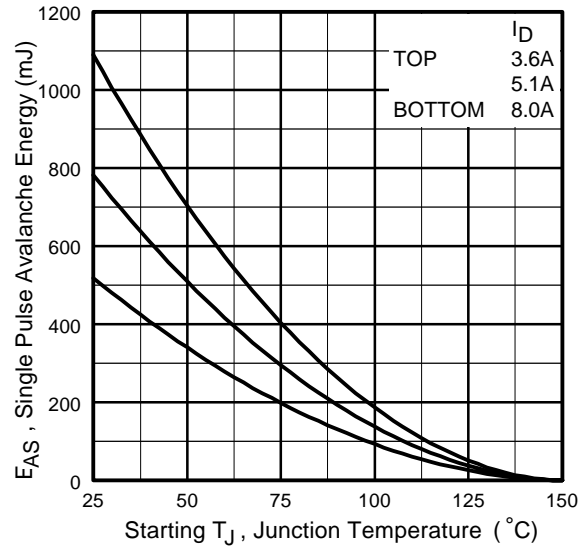
**Fig 12b.** Unclamped Inductive Waveforms



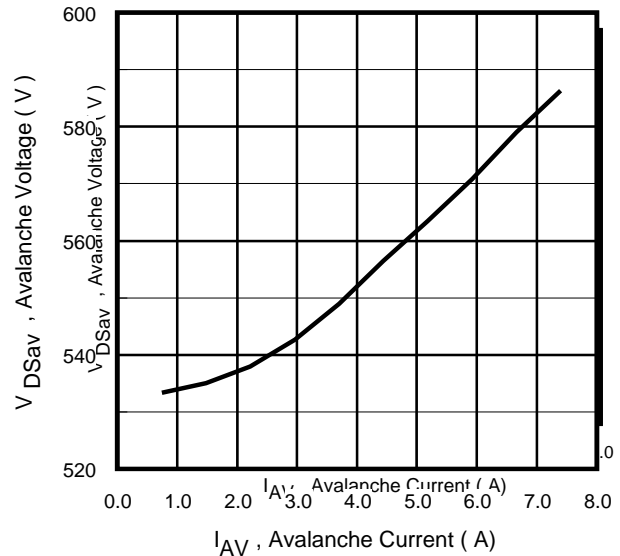
**Fig 13a.** Basic Gate Charge Waveform



**Fig 13b.** Gate Charge Test Circuit

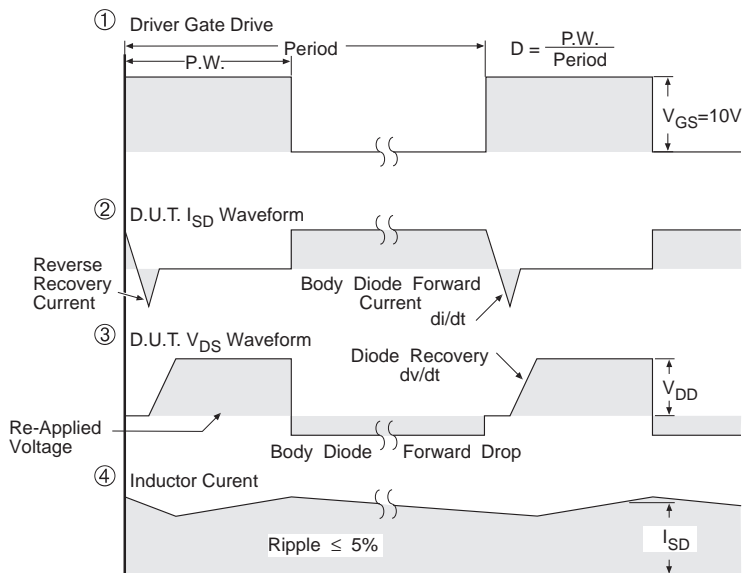


**Fig 12c.** Maximum Avalanche Energy Vs. Drain Current



**Fig 12d.** Typical Drain-to-Source Voltage Vs. Avalanche Current

**Peak Diode Recovery dv/dt Test Circuit**

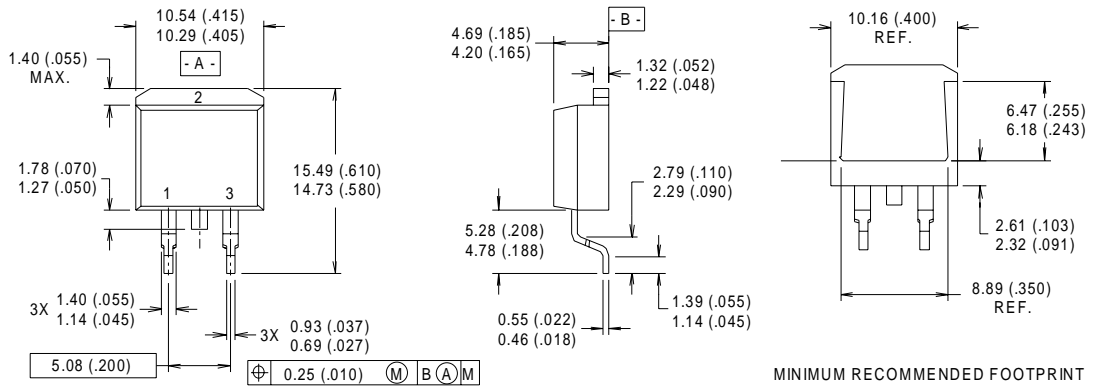


\*  $V_{GS} = 5V$  for Logic Level Devices

**Fig 14.** For N-Channel HEXFET<sup>®</sup> Power MOSFETs

# IRF840AS/L

## D<sup>2</sup>Pak Package Outline



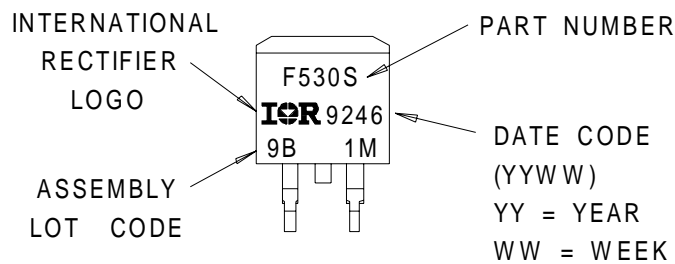
### NOTES:

- 1 DIMENSIONS AFTER SOLDER DIP.
- 2 DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
- 3 CONTROLLING DIMENSION : INCH.
- 4 HEATSINK & LEAD DIMENSIONS DO NOT INCLUDE BURRS.

### LEAD ASSIGNMENTS

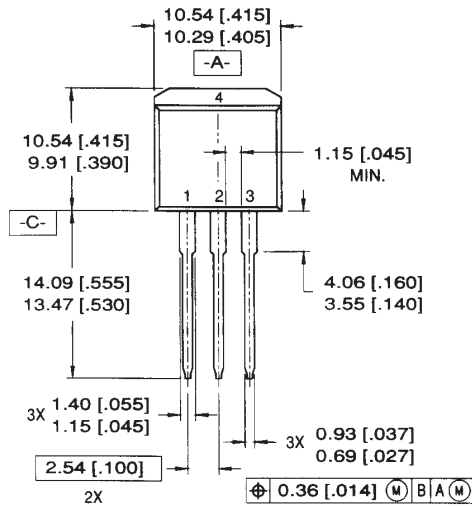
- 1 - GATE
- 2 - DRAIN
- 3 - SOURCE

## D<sup>2</sup>Pak Part Marking Information



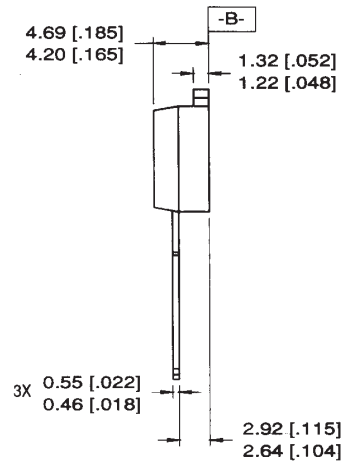


## TO-262 Package Outline



**LEAD ASSIGNMENTS**

1 = GATE	3 = SOURCE
2 = DRAIN	4 = DRAIN

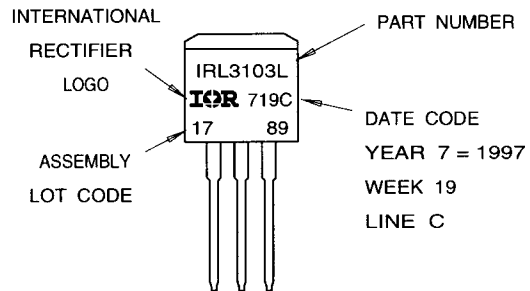


**NOTES:**

1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M-1982
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. HEATSINK & LEAD DIMENSIONS DO NOT INCLUDE BURRS.

## TO-262 Part Marking Information

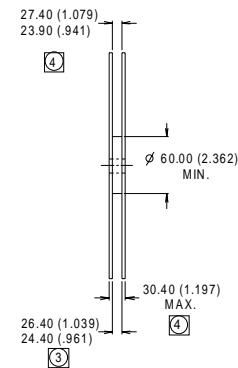
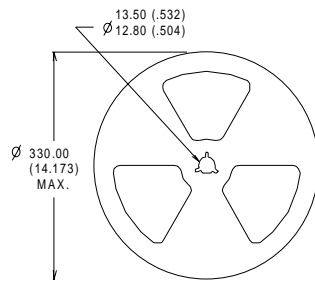
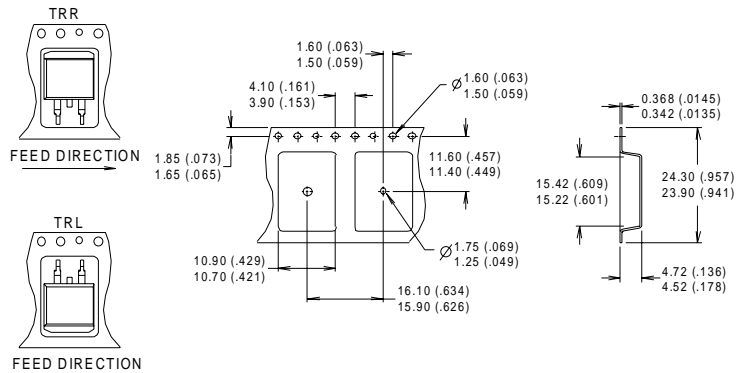
EXAMPLE: THIS IS AN IRL3103L  
 LOT CODE 1789  
 ASSEMBLED ON WW 19, 1997  
 IN THE ASSEMBLY LINE "C"



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## D<sup>2</sup>Pak Tape & Reel Information



- NOTES:
1. CONFORMS TO EIA-418.
  2. CONTROLLING DIMENSION: MILLIMETER.
  3. DIMENSION MEASURED @ HUB.
  4. INCLUDES FLANGE DISTORTION @ OUTER EDGE.

### Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11)
- ② Starting  $T_J = 25^\circ\text{C}$ ,  $L = 16\text{mH}$   
 $R_G = 25\Omega$ ,  $I_{AS} = 8.0\text{A}$ . (See Figure 12)
- ③  $I_{SD} \leq 8.0\text{A}$ ,  $di/dt \leq 100\text{A}/\mu\text{s}$ ,  $V_{DD} \leq V_{(BR)DSS}$ ,  
 $T_J \leq 150^\circ\text{C}$
- ④ Pulse width  $\leq 300\mu\text{s}$ ; duty cycle  $\leq 2\%$ .
- ⑤  $C_{oss}$  eff. is a fixed capacitance that gives the same charging time as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 80%  $V_{DSS}$
- ⑥ Uses IRF840A data and test conditions

\* When mounted on 1" square PCB (FR-4 or G-10 Material).

For recommended footprint and soldering techniques refer to application note #AN-994.

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**IR JAPAN:** K&H Bldg., 2F, 30-4 Nishi-Ikebukuro 3-Chome, Toshima-Ku, Tokyo Japan 171 Tel: 81 3 3983 0086

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**IR TAIWAN:** 16 Fl. Suite D. 207, Sec. 2, Tun Haw South Road, Taipei, 10673, Taiwan Tel: 886-2-2377-9936

Data and specifications subject to change without notice. 12/99