

MN103004J / 04K / F04K

Type	MN103004J / 04K / F04K	
Command ROM (×64-Bit)	192 KB / 128 KB / 256 KB (Flash)	
Data RAM (×32-Bit)	4 KB / 10 KB / 12 KB	
Minimum Instruction Execution Time	MN103004J / 04K:	30 ns (at 2.2 V, 33 MHz)
	MN103004J / 04K:	25 ns (at 3.0 V, 40 MHz)
	MN1030F04K:	36 ns (at 3.0 V, 28 MHz, 40 MHz (under development))
Interrupts	<ul style="list-style-type: none"> • RESET • IRQ × 8 • NMI × 1 • Timer × 22 • Input Capture × 14 • PWM × 4 • SIF × 16 • DMAC × 4 • WDT • A/D • System error 	
Timer Counter	<p>Timer Counter 0 to 3: 32-Bit × 1 (Interval Timer, Event Count, Toggle Output, Interrupt, A/D Conversion Trigger)</p> <p>Clock Source IOCLK, IOCLK/8, IOCLK/32, External Clock Input, Underflow of Timer Counter</p> <p>Interrupt Source Underflow of Timer Counter 0, 1, 2, 3</p> <p>Timer Counter 4 to 7: 32-Bit × 1 (Interval Timer, Event Count, Toggle Output, Interrupt, Clock Source for Serial I/F, Generation of Timer Synchronous Output Timing)</p> <p>Clock Source IOCLK, IOCLK/8, IOCLK/32, External Clock Input, Underflow of Timer Counter</p> <p>Interrupt Source Underflow of Timer Counter 4, 5, 6, 7</p> <p>Timer Counter 8 to B: 32-Bit × 1 (Interval Timer, Event Count, Toggle Output, Interrupt, Clock Source for Serial I/F, Generation of Timer Synchronous Output Timing)</p> <p>Clock Source IOCLK, IOCLK/8, IOCLK/32, External Clock Input, Underflow of Timer Counter</p> <p>Interrupt Source Underflow of Timer Counter 8, 9, A, B</p> <p>* Each of Timer Counters 0 to 3, 4 to 7, and 8 to B can be Changed to an 8-, 16-, or 24-Bit Timer Counter</p> <p>Timer Counter 10 to 13: 16-Bit × 4 (Interval Timer, Event Count, Toggle Output, Interrupt, DMA Start)</p> <p>Clock Source IOCLK, IOCLK/8, IOCLK/32, External Clock Input, Underflow of Timer Counter 0, 1, 2</p> <p>Interrupt Source Underflow of Timer Counter 10, 11, 12, 13</p> <p>Timer Counter 14, 15: 16-Bit × 2 (Interval Timer, Event Count, Toggle Output, PMW Output, Interrupt, Input Capture (2 Lines), One-Shot Output, External Trigger Start, Generation of Timer Synchronous Output Timing, DMA Start)</p> <p>Clock Source IOCLK, IOCLK/8, External Clock Input (2 Lines), Underflow of Timer Counter 0, 1, 2-Phase Encode</p> <p>Interrupt Source Overflow of Timer 14, 15, Underflow of Timer 14, 15, Coincidence of Compare Register with Binary Counter or at Capture</p> <p>Watchdog Timer: 16- to 25-Bit × 1ch</p>	
DMA Controller	<p>Number of Channels 2</p> <p>Unit of Transfer 8/16/32 bits</p> <p>Max Transfer Cycles 65535</p> <p>Starting Factor External Interrupt, Timer Factor, PNM Factor, Serial Transmission/Reception Factor, A/D Conversion finish, Software Factor</p> <p>Transfer Method 2-Bus Cycle Transfer</p> <p>Addressing Modes Fixed, Increment, Decrement</p> <p>Transfer Modes Word Transfer, Burst Transfer, Intermittent Transfer</p>	
Serial Interface	<p>Serial 0, 1: 7-, 8-Bit × 2 (Clock Synchronous Mode, Start-Stop Synchronous Mode, I²C Mode)</p> <p>Serial 2: 7-, 8-Bit × 1 (Start-Stop Synchronous Mode)</p> <p>Serial 3 to 7: 7-, 8-Bit × 5 (Clock Synchronous Mode)</p> <p>Clock Source (Clock Synchronous Mode, Start-Stop Synchronous Mode) IOCLK, Underflow of Timer Counter, External Clock (I²C Mode) IOCLK, Underflow of Timer Counter</p>	

I/O Pins	I/O	155	• Common use 137
	Input	16	• Common use 16
A/D Inputs		10-Bit × 16ch	
PWM		12-, 14-Bit resolution × 4ch (dedicated), 16-Bit resolution × 2ch (Common with Timer)	
ICR		28-Bit × 13ch + 16-Bit × 4ch (Common with Timer)	
OCR		16-Bit × 4ch (Common with Timer)	
Timer Synchronous Output		4-Bit (Synchronous Output) × 2ch	
Package		QFP208-P-2828A (MN103004J / 04K / F04K), FLGA239-C-1313 (MN103004K / F04K)	

Electrical Characteristics

MN103004J / 04K

Supply Current

Parameter	Symbol	Condition	Limit			Unit
			min	typ	max	
Operating Supply Current	IDD1	VDDH, VDDB, VDD, PVDD, AVDD = 3.0 V VI = VDDH (VDDB) or VSS At internal = 40 MHz Output released			150	mA
Supply current at stopping	IDD4	VDD, PVDD, AVDD = 3.6 V VI = VDDH (VDDB) or VSS Fosc = Oscillation stopped Output released			150*	μA

*FLGA239-C-1313 (Ta = -20 °C to +85 °C)

A/D Conversion Performance

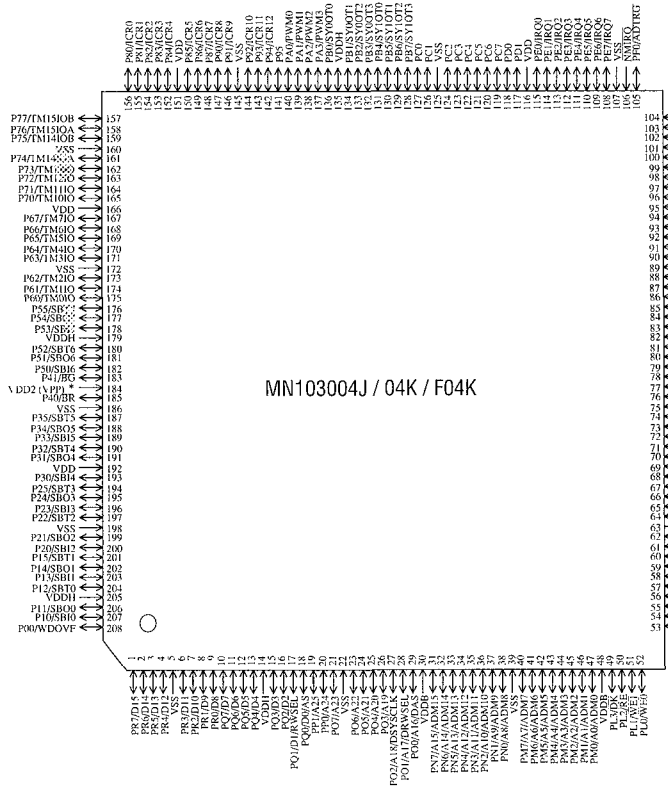
Parameter	Symbol	Condition	Limit			Unit
			min	typ	max	
Resolution					10	Bits
A/D conversion absolute Error		VREF+ = 3.0 V A/D conversion clock = 5 MHz			±7	LSB
A/D conversion relative Error					±5	LSB
A/D conversion time			2.8			μs

(Ta = -20 °C to +85 °C, AVDD = 3.0 V, AVSS = 0.0 V)

Support Tool

In-Circuit Emulator	PX-ICE103004
---------------------	--------------

Pin Assignment

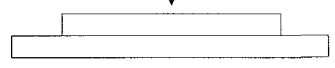


MN103004J / 04K / F04K

QFP208-P-2828A

* VDD2 for MN103004K or MN103004J and VPP for MN1030F04K

Perspective



		PE7 IRQ7	NMIRQ	PE1 IRQ1	PD0	PC4	PC1	PR1 SY00T1	PA2 PWM2	P94 ICR12	P91 ICR9	P84 ICR4	P80 ICR0		T		
		PE5 IRQ5		PE3 IRQ3	VDD	PC2	PB7 SY1OT3	PB3 SY00T3	PA0 PWM0	P92 ICR10	P85 ICR5	P82 ICR2			R		
AVDD		VSS		PE4 IRQ4	PC6	PC5	VSS	PB5 SY1OT1	PB0 SY00T0	VSS	VDD	P87 ICR7	P77 TM15IOB	P76 TM15IOA	P		
PG2 AN2	PG0 AN0	VREFH	PE6 IRQ6	PE2 IRQ2	PD1	PC3	PB6 SY1OT2	PA1 PWM1	P90 ICR8	P83 ICR3	P74 TM14IOA	P75 TM14IOB	P73 TM13IO	VSS	N		
PG3 AN3	PG5 AN5	PG1 AN1	PG4 AN4	PE0 IRQ0	PC7	PC0	PB2 SY00T2	PA3 PWM3	P95	P86 ICR6	P81 ICR1	P70 TM10IO	P72 TM12IO	VDD	P71 TM11IO	M	
PG7 AN7	PH1 AN9	PH2 AN10	PG6 AN6	PH3 AN11	PH0 AN8	PB4 SY1OT0		P93 ICR11	P67 TM7IO	P63 TM3IO	P65 TM5IO	VSS	P66 TM6IO	P64 TM4IO	L		
PH7 AN15	PH5 AN13	PH6 AN14	AVSS	PH0	PH4 AN12				P60 TM0IO	P54 SBO7	P62 TM2IO	P55 SBT7	P61 TM1IO	P53 SB1	K		
PI2	PI3	PI4	VDDH	PI1						P41 BG	VDDH	P51 SBO6	P52 SBT6	P50 SB16	I		
PI0 DWE	PI7	VSS	PI5	PI6						P35 SBT5	P34 SBO5	P40 BR	VDD2 (VPP)	VSS	H		
PK2 CS2 RAS2	PK0 CS0	PK1 CS1 RAS1	VDD	PI4	PJ2 DCAS1					P31 SBO4	P33 SB15	P30 SB14	P32 SBT4	VDD	P25 SBT3	G	
OSCO	PK4 SYSCLK	VDDH	PK3 CS3	PI3 CAS	PI1 DCAS0					P05 A21	P24 SBO3	P21 SBO2	P22 SBT2	P15 SBT1	P23 SB13	VSS	F
OSCI	VSS	PK7 FRQS	PK6 EXMOD0	PK5 EXMOD0	PN1 A9	PN3 A11	PN0 A16	PN2 A18	PN4 A24	PQ2 D2	PQ1 D9	PI3 SB11	P20 SB12	P14 SBO1	PI2 SBT0		E
MMOD1	RST	MMOD0	PVSS	PM4 A4	PN0 A8	PN4 A12	PN7 A23	PN3 A19	PQ0 D5	PQ5 D5	PQ7 D7	P10 SB10	VDDH	PI1 SBO0	P00 WDOVP		D
PVDD		PL1 WE1	PL3 DR	PM2 A2	PM6 A6	VSS	PN7 A15	VSS	PQ3 D3	VDDH	PR3 D11	PR4 D12	PR6 D14				C
		PL2 RE	PM0 A3	PM1 A5	PM5 A5	PN6 A14	VDDH	PQ6 A22	PP1 A22	PQ6 D6	PR0 D8	PR5 D13					B
		PL0 WE0	VDDH	PM7 A3	PM7 A7	PN2 A10	PN1 A17	PQ4 A20	PQ1 D1	PQ4 D4	PR2 D10	VSS	PR7 D15				A

FLGA239-C-1313

* H2 is VDD2 for MN103004K and VPP for MN1030F04K