

**TC74HC373AP, TC74HC373AF, TC74HC373AFW**

**OCTAL D-TYPE LATCH WITH 3-STATE OUTPUT**

The TC74HC373A is a high speed CMOS OCTAL LATCH with 3-STATE OUTPUT fabricated with silicon gate C<sup>2</sup>MOS technology.

It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation. These 8-bit D-type latches are controlled by a latch enable input (LE) and a output enable input ( $\overline{OE}$ ).

When the  $\overline{OE}$  input is high, the eight outputs are in a high impedance state.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.

**FEATURES:**

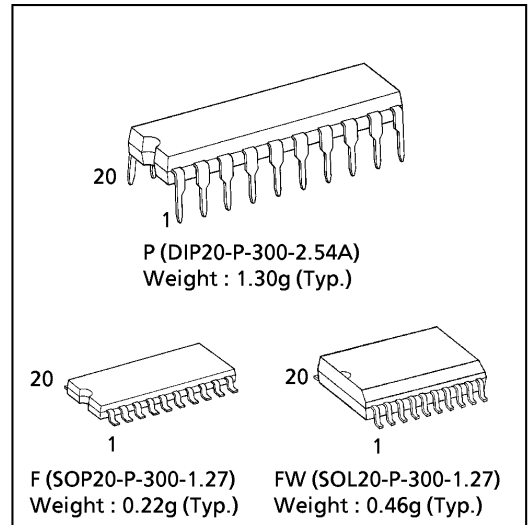
- High Speed..... $t_{pd} = 11\text{ns}(\text{typ.})$  at  $V_{CC} = 5\text{V}$
- Low Power Dissipation..... $I_{CC} = 4\mu\text{A}(\text{Max.})$  at  $T_a = 25^\circ\text{C}$
- High Noise Immunity..... $V_{NIH} = V_{NIL} = 28\% V_{CC} (\text{Min.})$
- Output Drive Capability..... 15 LSTTL Loads
- Symmetrical Output Impedance...  $|I_{OH}| = I_{OL} = 6\text{mA}(\text{Min.})$
- Balanced Propagation Delays.....  $t_{pLH} \approx t_{pHL}$
- Wide Operating Voltage Range...  $V_{CC} (\text{opr.}) = 2\text{V} \sim 6\text{V}$
- Pin and Function Compatible with 74LS373

**TRUTH TABLE**

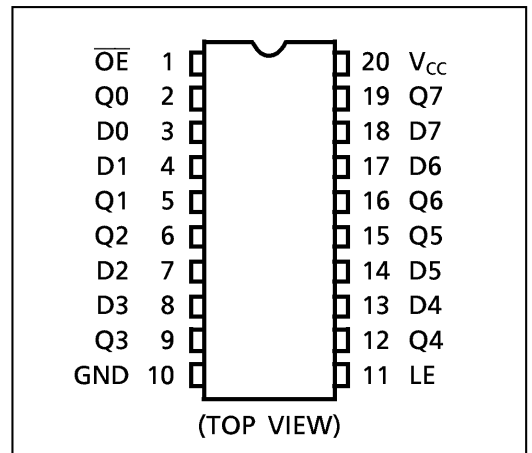
INPUTS			OUTPUTS
$\overline{OE}$	LE	D	Q
H	X	X	Z
L	L	X	$Q_n$
L	H	L	L
L	H	H	H

X : Don't Care  
 Z : High Impedance  
 $Q_n$  : Q outputs are latched at the time when the LE input is taken to a low logic level.

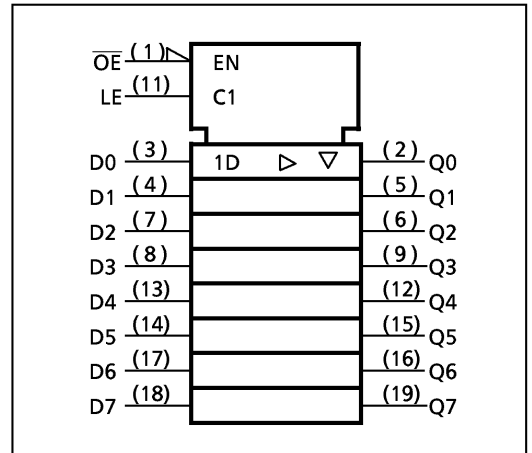
(Note) The JEDEC SOP (FW) is not available in Japan.



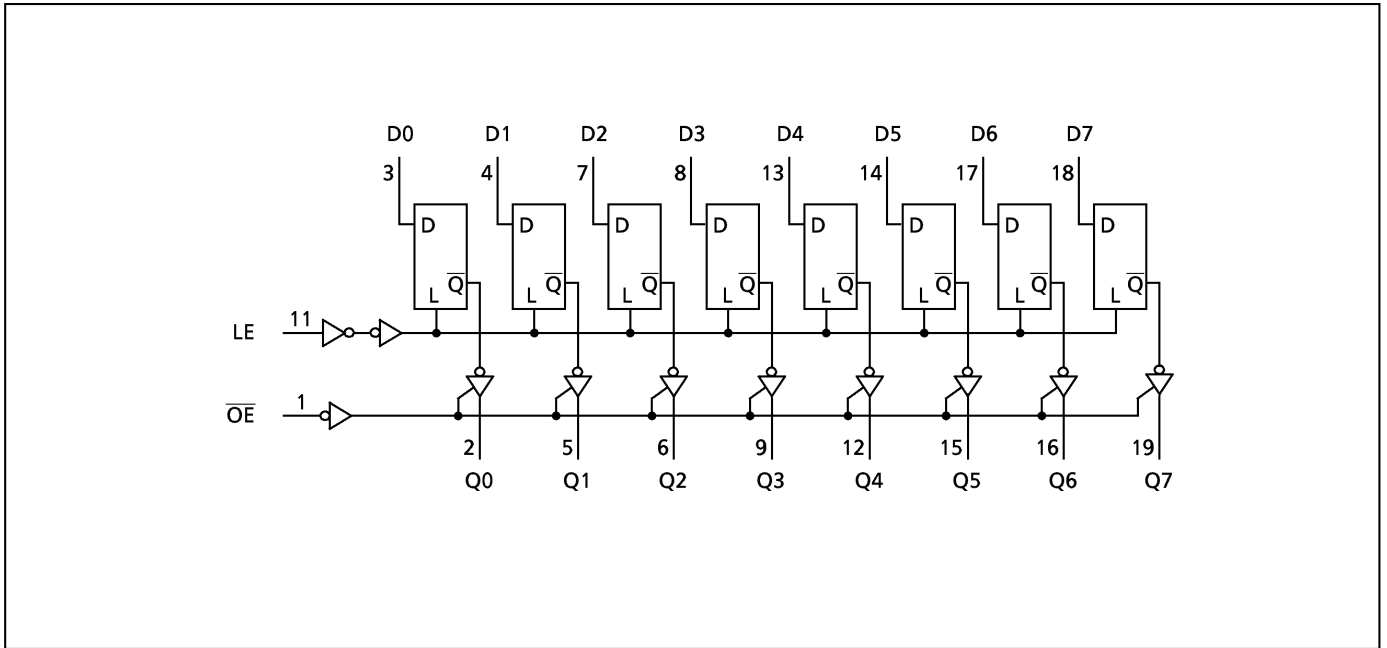
**PIN ASSIGNMENT**



**IEC LOGIC SYMBOL**



SYSTEM DIAGRAM



**ABSOLUTE MAXIMUM RATINGS**

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	$V_{CC}$	-0.5~7	V
DC Input Voltage	$V_{IN}$	-0.5~ $V_{CC}+0.5$	V
DC Output Voltage	$V_{OUT}$	-0.5~ $V_{CC}+0.5$	V
Input Diode Current	$I_{IK}$	± 20	mA
Output Diode Current	$I_{OK}$	± 20	mA
DC Output Current	$I_{OUT}$	± 35	mA
DC $V_{CC}$ /Ground Current	$I_{CC}$	± 75	mA
Power Dissipation	$P_D$	500 (DIP)* / 180 (SOP)	mW
Storage Temperature	$T_{stg}$	-65~150	°C

\*500mW in the range of  $T_a = -40^{\circ}\text{C} \sim 65^{\circ}\text{C}$ . From  $T_a = 65^{\circ}\text{C}$  to  $85^{\circ}\text{C}$  a derating factor of  $-10\text{mW}/^{\circ}\text{C}$  shall be applied until 300mW.

**RECOMMENDED OPERATING CONDITIONS**

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	$V_{CC}$	2~6	V
Input Voltage	$V_{IN}$	0~ $V_{CC}$	V
Output Voltage	$V_{OUT}$	0~ $V_{CC}$	V
Operating Temperature	$T_{opr}$	-40~85	°C
Input Rise and Fall Time	$t_r, t_f$	0~1000 ( $V_{CC} = 2.0\text{V}$ ) 0~500 ( $V_{CC} = 4.5\text{V}$ ) 0~400 ( $V_{CC} = 6.0\text{V}$ )	ns

**DC ELECTRICAL CHARACTERISTICS**

PARAMETER	SYMBOL	TEST CONDITION	$V_{CC}$ (V)	$T_a = 25^{\circ}\text{C}$			$T_a = -40 \sim 85^{\circ}\text{C}$		UNIT	
				MIN.	TYP.	MAX.	MIN.	MAX.		
High - Level Input Voltage	$V_{IH}$		2.0 4.5 6.0	1.50 3.15 4.20	— — —	— — —	1.50 3.15 4.20	— — —	V	
Low - Level Input Voltage	$V_{IL}$		2.0 4.5 6.0	— — —	— — —	0.50 1.35 1.80	— — —	0.50 1.35 1.80	— — —	V
High - Level Output Voltage	$V_{OH}$	$V_{IN} = V_{IH}$ or $V_{IL}$	$I_{OH} = -20\mu\text{A}$	2.0	1.9	2.0	—	1.9	—	V
				4.5	4.4	4.5	—	4.4	—	
			$I_{OH} = -6\text{ mA}$ $I_{OH} = -7.8\text{mA}$	4.5	4.18	4.31	—	4.13	—	V
				6.0	5.68	5.80	—	5.63	—	
Low - Level Output Voltage	$V_{OL}$	$V_{IN} = V_{IH}$ or $V_{IL}$	$I_{OL} = 20\mu\text{A}$	2.0	—	0.0	0.1	—	0.1	V
				4.5	—	0.0	0.1	—	0.1	
			$I_{OL} = 6\text{ mA}$ $I_{OL} = 7.8\text{mA}$	4.5	—	0.17	0.26	—	0.33	V
				6.0	—	0.18	0.26	—	0.33	
3 - State Output Off - State Current	$I_{OZ}$	$V_{IN} = V_{IH}$ or $V_{IL}$ $V_{OUT} = V_{CC}$ or GND	6.0	—	—	± 0.5	—	± 5.0	$\mu\text{A}$	
Input Leakage Current	$I_{IN}$	$V_{IN} = V_{CC}$ or GND	6.0	—	—	± 0.1	—	± 1.0		
Quiescent Supply Current	$I_{CC}$	$V_{IN} = V_{CC}$ or GND	6.0	—	—	4.0	—	40.0		

**TIMING REQUIREMENTS ( Input  $t_r = t_f = 6ns$  )**

PARAMETER	SYMBOL	TEST CONDITION	V <sub>CC</sub> (V)	Ta = 25°C		Ta = -40~85°C	UNIT
				TYP.	LIMIT	LIMIT	
Minimum Pulse Width (LE)	t <sub>w(H)</sub>		2.0	—	75	95	ns
			4.5	—	15	19	
			6.0	—	13	16	
Minimum Set-up Time (Dn)	t <sub>s</sub>		2.0	—	50	65	
			4.5	—	10	13	
			6.0	—	9	11	
Minimum Hold Time (Dn)	t <sub>h</sub>		2.0	—	5	5	
			4.5	—	5	5	
			6.0	—	5	5	

**AC ELECTRICAL CHARACTERISTICS ( Input  $t_r = t_f = 6ns$  )**

PARAMETER	SYMBOL	TEST CONDITION	CL (pF)	V <sub>CC</sub> (V)	Ta = 25°C			Ta = -40~85°C		UNIT						
					MIN.	TYP.	MAX.	MIN.	MAX.							
Output Transition Time	t <sub>TLH</sub> t <sub>THL</sub>		50	2.0	—	20	60	—	75	ns						
				4.5	—	6	12	—	15							
				6.0	—	5	10	—	13							
Propagation Delay Time (LE-Q)	t <sub>pLH</sub> t <sub>pHL</sub>		50	2.0	—	42	125	—	155							
				4.5	—	14	25	—	31							
				6.0	—	12	21	—	26							
	50	2.0	—	57	175	—	220	44	37							
											4.5	—	19	35	—	44
											6.0	—	16	30	—	37
Propagation Delay Time (D-Q)	t <sub>pLH</sub> t <sub>pHL</sub>		50	2.0	—	42	125	—	155							
				4.5	—	14	25	—	31							
				6.0	—	12	21	—	26							
	150	2.0	—	57	175	—	220	44	37							
										4.5	—	19	35	—	44	
										6.0	—	16	30	—	37	
Output Enable Time	t <sub>pZL</sub> t <sub>pZH</sub>	R <sub>L</sub> = 1kΩ	50	2.0	—	39	125	—	155							
				4.5	—	13	25	—	31							
				6.0	—	11	21	—	26							
	150	2.0	—	54	175	—	220	44	37							
										4.5	—	18	35	—	44	
										6.0	—	15	30	—	37	
Output Disable Time	t <sub>pLZ</sub> t <sub>pHZ</sub>	R <sub>L</sub> = 1kΩ	50	2.0	—	30	125	—	155							
				4.5	—	14	25	—	31							
				6.0	—	13	21	—	26							
Input Capacitance	C <sub>IN</sub>				—	5	10	—	10	pF						
Output Capacitance	C <sub>OUT</sub>				—	10	—	—	—							
Power Dissipation Capacitance	C <sub>PD</sub> (1)				—	38	—	—	—							

Note (1) C<sub>PD</sub> is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation :

$$I_{CC}(\text{opr}) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC} / 8 \text{ (per Latch)}$$

And the total C<sub>PD</sub> when n pcs. of Latch operate can be gained by the following equation :

$$C_{PD}(\text{total}) = 22 + 16 \cdot n$$

**DIP 20PIN PACKAGE DIMENSIONS (DIP20-P-300-2.54A)**

Unit in mm



**SOP 20PIN (200mil BODY) PACKAGE DIMENSIONS (SOP20-P-300-1.27)**

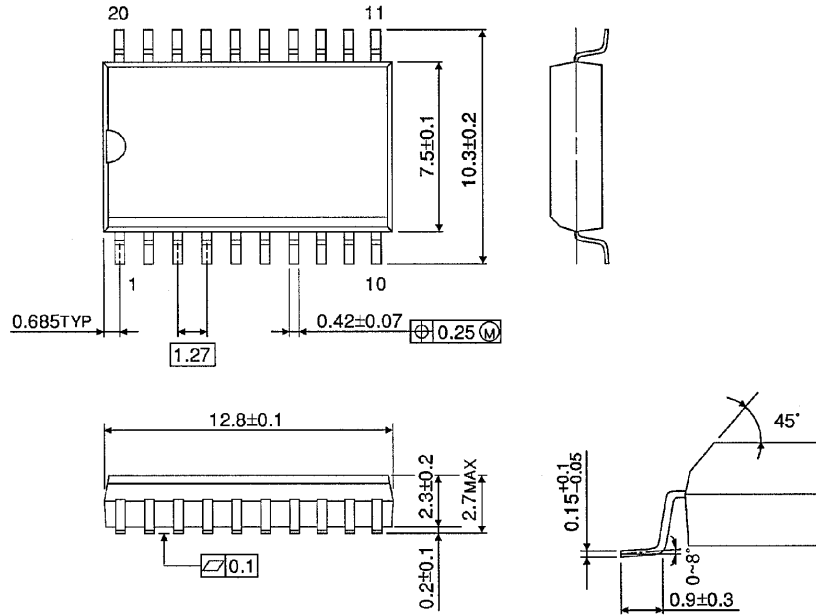
Unit in mm



**SOP 20PIN (300mil BODY) PACKAGE DIMENSIONS (SOL20-P-300-1.27)**

Unit in mm

(Note) This package is not available in Japan.



Weight : 0.46g (Typ.)

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