512K (32K x 16) OTP CMOS EPROM

Features

- **Fast Read Access Time - 45 ns**
- **Low Power CMOS Operation**
  - **100 µA max. Standby**
  - **30 mA max. Active at 5 MHz**
- **JEDEC Standard Packages**
  - **44-Lead PLCC**
  - **40-Lead TSOP (10mm x 14mm)**
- **5V ± 10% Power Supply**
- **High Reliability CMOS Technology**
  - **2000V ESD Protection**
  - **200 mA Latchup Immunity**
- **Rapid™ Programming Algorithm - 50 µs/word (typical)**
- **CMOS and TTL Compatible Inputs and Outputs**
- **Integrated Product Identification Code**
- **Commercial and Industrial Temperature Ranges**

Description

The AT27C516 is a low-power, high performance 524,288 bit one-time programmable read only memory (OTP EPROM) organized 32K by 16 bits. It requires only one 5V power supply in normal read mode operation. Any word can be accessed in less than 45 ns, eliminating the need for speed reducing WAIT states. The by-16 organization make this part ideal for high-performance 16 and 32 bit microprocessor systems.

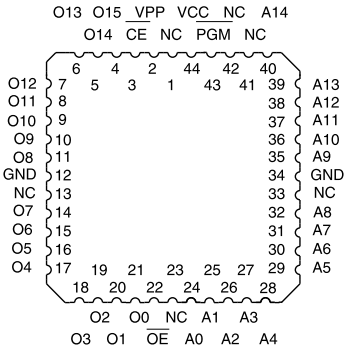
(continued)

Pin Configurations

Pin Name	Function
A0 - A14	Addresses
O0 - O15	Outputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{PGM}$	Program Strobe
NC	No Connect

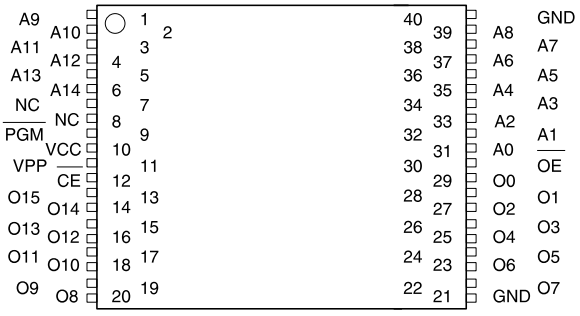
Note: Both GND pins must be connected.

PLCC Top View



Note: PLCC Package Pins 1 and 23 are DON'T CONNECT.

TSOP Top View
Type 1



0362C

Description (Continued)

In read mode, the AT27C516 typically consumes 15 mA. Standby mode supply current is typically less than 10 µA.

The AT27C516 is available in industry standard JEDEC-approved one-time programmable (OTP) plastic PLCC and TSOP packages. The device features two-line control ($\overline{CE}$, $\overline{OE}$) to eliminate bus contention in high-speed systems.

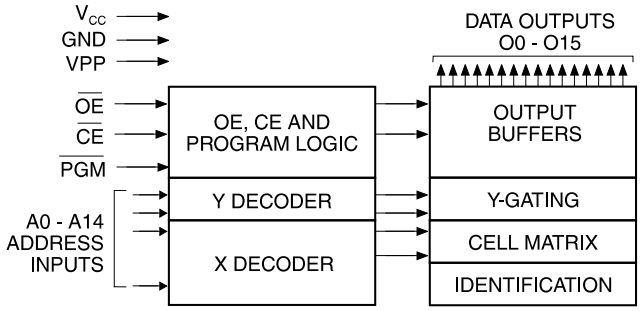
With 32K word storage capability, the AT27C516 allows firmware to be stored reliably and to be accessed by the system without the delays of mass storage media.

Atmel's 27C516 have additional features to ensure high quality and efficient production use. The Rapid™ Programming Algorithm reduces the time required to program the part and guarantees reliable programming. Programming time is typically only 50 µs/word. The Integrated Product Identification Code electronically identifies the device and manufacturer. This feature is used by industry standard programming equipment to select the proper programming algorithms and voltages.

System Considerations

Switching between active and standby conditions via the Chip Enable pin may produce transient voltage excursions. Unless accommodated by the system design, these transients may exceed data sheet limits, resulting in device non-conformance. At a minimum, a 0.1 µF high frequency, low inherent inductance, ceramic capacitor should be utilized for each device. This capacitor should be connected between the V_{CC} and Ground terminals of the device, as close to the device as possible. Additionally, to stabilize the supply voltage level on printed circuit boards with large EPROM arrays, a 4.7 µF bulk electrolytic capacitor should be utilized, again connected between the V_{CC} and Ground terminals. This capacitor should be positioned as close as possible to the point where the power supply is connected to the array.

Block Diagram



Absolute Maximum Ratings*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-2.0V to +7.0V (1)
Voltage on A9 with Respect to Ground	-2.0V to +14.0V (1)
V_{PP} Supply Voltage with Respect to Ground	-2.0V to +14.0V (1)

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note: 1. Minimum voltage is -0.6V dc which may undershoot to -2.0V for pulses of less than 20 ns. Maximum output pin voltage is V_{CC} + 0.75V dc which may overshoot to +7.0V for pulses of less than 20 ns.

Operating Modes

Mode \ Pin	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	Ai	V_{PP}	**Outputs**
Read	V_{IL}	V_{IL}	X (1)	Ai	X	D_{OUT}
Output Disable	X	V_{IH}	X	X	X	High Z
Standby	V_{IH}	X	X	X	X (5)	High Z
Rapid Program (2)	V_{IL}	V_{IH}	V_{IL}	Ai	V_{PP}	D_{IN}
PGM Verify	V_{IL}	V_{IL}	V_{IH}	Ai	V_{PP}	D_{OUT}
PGM Inhibit	V_{IH}	X	X	X	V_{PP}	High Z
Product Identification (4)	V_{IL}	V_{IL}	X	A9 = V_H (3) A0 = V_{IH} or V_{IL} A1 - A14 = V_{IL}	V_{CC}	Identification Code

Notes: 1. X can be V_{IL} or V_{IH}.
2. Refer to Programming characteristics.
3. V_H = 12.0 ± 0.5V.
4. Two identifier words may be selected. All Ai inputs are held low (V_{IL}), except A9 which is set to V_H and A0 which is toggled low (V_{IL}) to select the Manufacturer's Identification word and high (V_{IH}) to select the Device Code word.
5. Standby V_{CC} current (I_{SB}) is specified with V_{PP} = V_{CC}. V_{CC} > V_{PP} will cause a slight increase in I_{SB}.

DC and AC Operating Conditions for Read Operation

		AT27C516				
		-45	-55	-70	-85	-10
Operating Temperature (Case)	Com.	0°C - 70°C	0°C - 70°C	0°C - 70°C	0°C - 70°C	0°C - 70°C
	Ind.	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C
V_{CC} Power Supply		5V ± 10%	5V ± 10%	5V ± 10%	5V ± 10%	5V ± 10%

DC and Operating Characteristics for Read Operation

Symbol	Parameter	Condition	Min	Max	Units
I_{LI}	Input Load Current	V_{IN} = 0V to V_{CC}		±1	µA
I_{LO}	Output Leakage Current	V_{OUT} = 0V to V_{CC}		±5	µA
I_{PP1} (2)	V_{PP} (1) Read/Standby Current	V_{PP} = V_{CC}		10	µA
I_{SB}	V_{CC} (1) Standby Current	I_{SB1} (CMOS), $\overline{CE}$ = V_{CC} ± 0.3V		100	µA
		I_{SB2} (TTL), $\overline{CE}$ = 2.0 to V_{CC} + 0.5V		1	mA
I_{CC}	V_{CC} Active Current	f = 5 MHz, I_{OUT} = 0 mA, $\overline{CE}$ = V_{IL}		30	mA
V_{IL}	Input Low Voltage		-0.6	0.8	V
V_{IH}	Input High Voltage		2.0	V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = -400 µA	2.4		V

Notes: 1. V_{CC} must be applied simultaneously or before V_{PP}, and removed simultaneously or after V_{PP}.

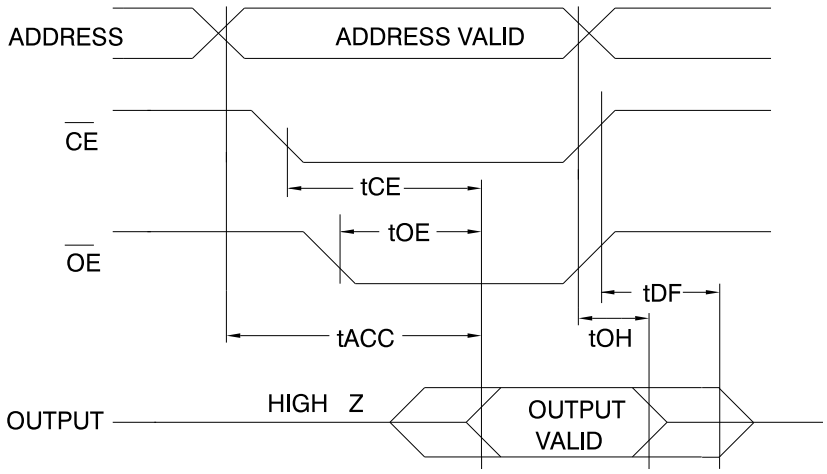
2. V_{PP} may be connected directly to V_{CC}, except during programming. The supply current would then be the sum of I_{CC} and I_{PP}.

AC Characteristics for Read Operation

			AT27C516										
			-45		-55		-70		-85		-10		
Symbol	Parameter	Condition	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Units
t_{ACC} (3)	Address to Output Delay	$\overline{CE}$ = $\overline{OE}$ = VIL		45		55		70		85		100	ns
t_{CE} (2)	$\overline{CE}$ to Output Delay	$\overline{OE}$ = V_{IL}		45		55		70		85		100	ns
t_{OE} (2, 3)	$\overline{OE}$ to Output Delay	$\overline{CE}$ = V_{IL}		20		25		25		30		30	ns
t_{DF} (4, 5)	$\overline{OE}$ or $\overline{CE}$ High to Output Float, whichever occurred first			20		25		25		30		30	ns
t_{OH}	Output Hold from Address, $\overline{CE}$ or $\overline{OE}$, whichever occurred first		7		7		7		0		0		ns

Notes: 2, 3, 4, 5. - see AC Waveforms for Read Operation.

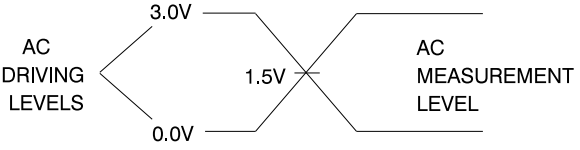
AC Waveforms for Read Operation (1)



Notes: 1. Timing measurement reference level is 1.5V for -45 and -55 devices. Input AC drive levels are V_{IL} = 0.0V and V_{IH} = 3.0V. Timing measurement reference levels for all other speed grades are V_{OL} = 0.8V and V_{OH} = 2.0V. Input AC drive levels are V_{IL} = 0.45V and V_{IH} = 2.4V.
2. $\overline{OE}$ may be delayed up to t_{CE} - t_{OE} after the falling edge of $\overline{CE}$ without impact on t_{CE} .
3. $\overline{OE}$ may be delayed up to t_{ACC} - t_{OE} after the address is valid without impact on t_{ACC} .
4. This parameter is only sampled and is not 100% tested.
5. Output float is defined as the point when data is no longer driven.

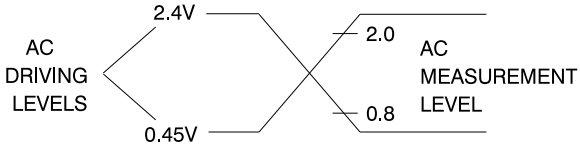
Input Test Waveforms and Measurement Levels

For -45, -55, and -70 Devices Only:



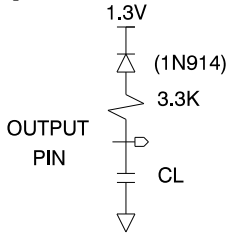
t_R, t_F < 5 ns (10% to 90%)

For -85 and -10 Devices Only:



t_R, t_F < 20 ns (10% to 90%)

Output Test Load



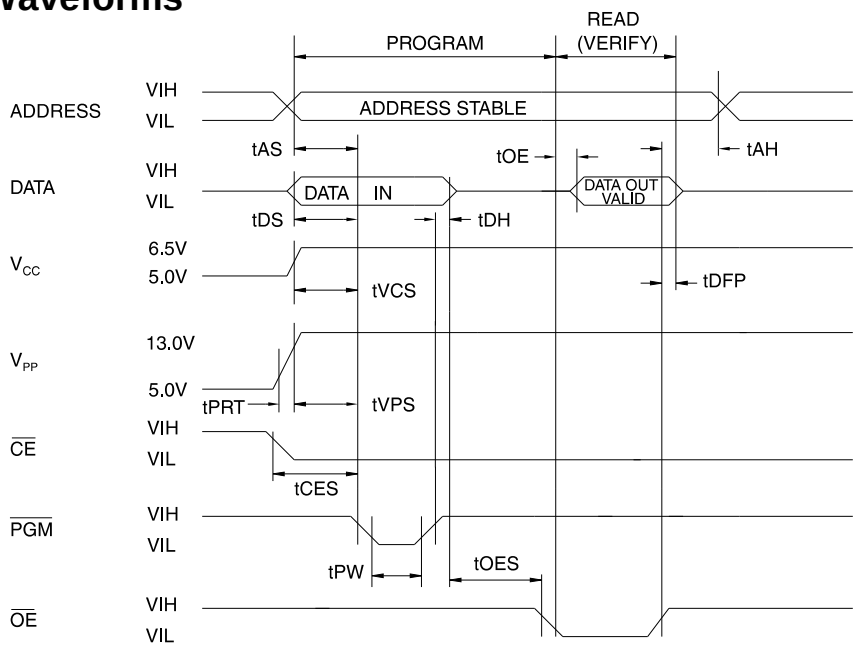
Note: CL = 100 pF including jig capacitance except -45, -55 and -70 devices, where CL = 30 pF.

Pin Capacitance (f = 1 MHz T = 25°C) (1)

	Typ	Max	Units	Conditions
C_{IN}	4	10	pF	V_{IN} = 0V
C_{OUT}	8	12	pF	V_{OUT} = 0V

Note: 1. Typical values for nominal supply voltage. This parameter is only sampled and is not 100% tested.

Programming Waveforms [1]



Notes: 1. The Input Timing Reference is 0.8V for V_{IL} and 2.0V for V_{IH}.
2. t_{OE} and t_{DFP} are characteristics of the device but must be accommodated by the programmer.
3. When programming the AT27C516 a 0.1 µF capacitor is required across V_{PP} and ground to suppress spurious voltage transients.

DC Programming Characteristics

T_A = 25 ± 5°C, V_{CC} = 6.5 ± 0.25V, V_{PP} = 13.0 ± 0.25V

Symbol	Parameter	Test Conditions	Limits Min	Limits Max	Units
I_{LI}	Input Load Current	$V_{IN} = V_{IL}, V_{IH}$		±10	µA
V_{IL}	Input Low Level		-0.6	0.8	V
V_{IH}	Input High Level		2.0	V_{CC} + 0.1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = -400 µA	2.4		V
I_{CC2}	V_{CC} Supply Current (Program and Verify)			50	mA
I_{PP2}	V_{PP} Supply Current	$\overline{CE} = \overline{PGM} = V_{IL}$		30	mA
V_{ID}	A9 Product Identification Voltage		11.5	12.5	V

AC Programming Characteristics

T_A = 25 ± 5°C, V_{CC} = 6.5 ± 0.25V, V_{PP} = 13.0 ± 0.25V

Symbol	Parameter	Test Conditions* (1)	Limit Min	Limit Max	Units
t_{AS}	Address Setup Time		2		µs
t_{CES}	$\overline{CE}$ Setup Time		2		µs
t_{OES}	$\overline{OE}$ Setup Time		2		µs
t_{DS}	Data Setup Time		2		µs
t_{AH}	Address Hold Time		0		µs
t_{DH}	Data Hold Time		2		µs
t_{DFP}	$\overline{OE}$ High to Output Float Delay (2)		0	130	ns
t_{VPS}	V_{PP} Setup Time		2		µs
t_{VCS}	V_{CC} Setup Time		2		µs
t_{PW}	$\overline{PGM}$ Program Pulse Width (3)		47.5	52.5	µs
t_{OE}	Data Valid from $\overline{OE}$			150	ns
t_{PRT}	V_{PP} Pulse Rise Time During Programming		50		ns

*AC Conditions of Test:

Input Rise and Fall Times (10% to 90%).....20 ns
Input Pulse Levels.....0.45V to 2.4V
Input Timing Reference Level.....0.8V to 2.0V
Output Timing Reference Level.....0.8V to 2.0V

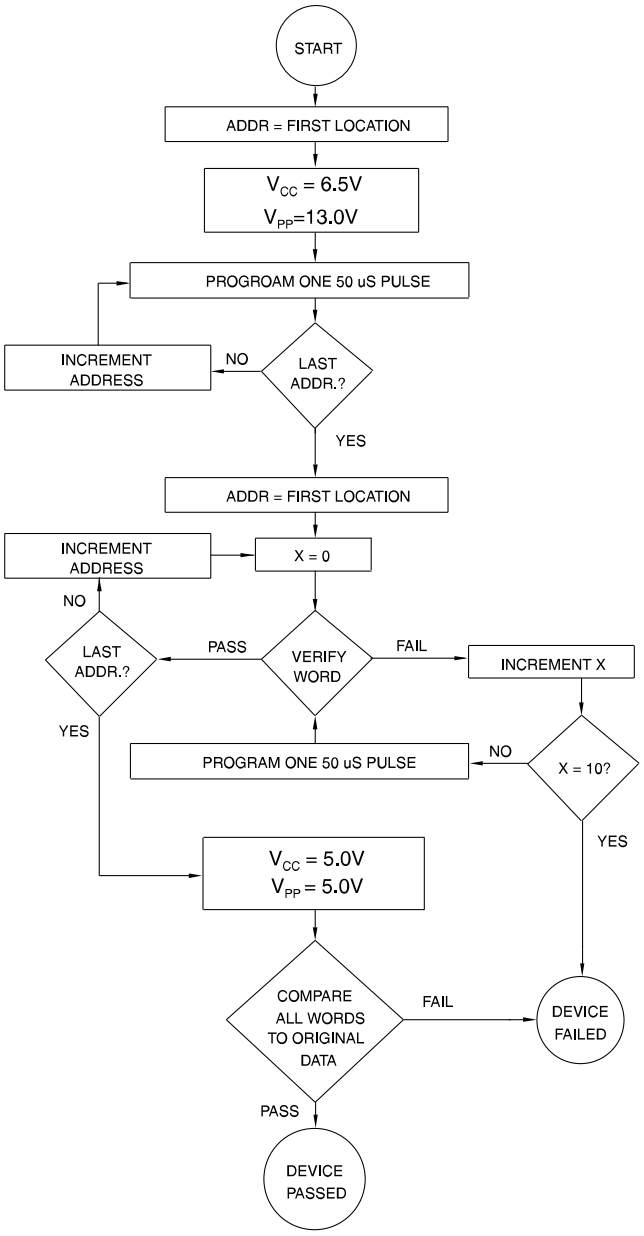
Notes: 1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. This parameter is only sampled and is not 100% tested. Output Float is defined as the point where data is no longer driven — see timing diagram.
3. Program Pulse width tolerance is 50 µsec ± 5%.

Atmel's 27C516 Integrated Product Identification Code

Codes	Pins A0	015-08	O7	O6	O5	O4	O3	O2	O1	O0	Hex Data
Manufacturer	0	0	0	0	0	1	1	1	1	0	001E
Device Type	1	0	1	1	1	1	0	0	1	0	00F2

Rapid Programming Algorithm

A 50 µs $\overline{PGM}$ pulse width is used to program. The address is set to the first location. V_{CC} is raised to 6.5V and V_{PP} is raised to 13.0V. Each address is first programmed with one 50 µs $\overline{PGM}$ pulse without verification. Then a verification / reprogramming loop is executed for each address. In the event a word fails to pass verification, up to 10 successive 50 µs pulses are applied with a verification after each pulse. If the word fails to verify after 10 pulses have been applied, the part is considered failed. After the word verifies properly, the next address is selected until all have been checked. V_{PP} is then lowered to 5.0V and V_{CC} to 5.0V. All words are read again and compared with the original data to determine if the device passes or fails.



Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
45	30	0.1	AT27C516-45JC AT27C516-45VC	44J 40V	Commercial (0°C to 70°C)
	30	0.1	AT27C516-45JI AT27C516-45VI	44J 40V	Industrial (-40°C to 85°C)
55	30	0.1	AT27C516-55JC AT27C516-55VC	44J 40V	Commercial (0°C to 70°C)
	30	0.1	AT27C516-55JI AT27C516-55VI	44J 40V	Industrial (-40°C to 85°C)
70	30	0.1	AT27C516-70JC AT27C516-70VC	44J 40V	Commercial (0°C to 70°C)
	30	0.1	AT27C516-70JI AT27C516-70VI	44J 40V	Industrial (-40°C to 85°C)
85	30	0.1	AT27C516-85JC AT27C516-85VC	44J 40V	Commercial (0°C to 70°C)
	30	0.1	AT27C516-85JI AT27C516-85VI	44J 40V	Industrial (-40°C to 85°C)
100	30	0.1	AT27C516-10JC AT27C516-10VC	44J 40V	Commercial (0°C to 70°C)
	30	0.1	AT27C516-10JI AT27C516-10VI	44J 40V	Industrial (-40°C to 85°C)

Package Type	
44J	44 Lead, Plastic J-Leaded Chip Carrier (PLCC)
40V	40 Lead, Plastic Thin Small Outline Package (TSOP) (10mm x 14mm)