Data Sheet November 1999 File Number 3120.3

Quad Monolithic SPST, CMOS Analog Switch

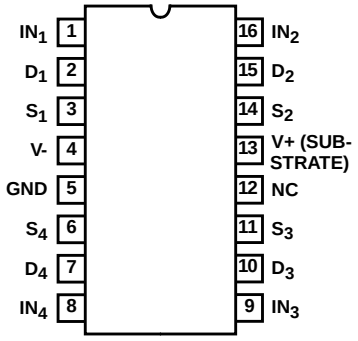
The DG308A quad monolithic SPST, CMOS switch is latch proof and is designed to block signals up to $30V_{P-P}$ when OFF. Featuring low ON resistance, low power consumption, and rail-to-rail analog signal range, this switch is ideally suited for high speed switching applications in communications, instrumentation and process control. The DG308A has single and dual supply capability. The input thresholds are CMOS compatible.

Ordering Information

PART NUMBER	TEMP. RANGE (^oC)	PACKAGE	PKG. NO.
DG308ACJ	0 to 70	16 Ld PDIP	E16.3
DG308ACY	0 to 70	16 Ld SOIC	M16.15

Pinout

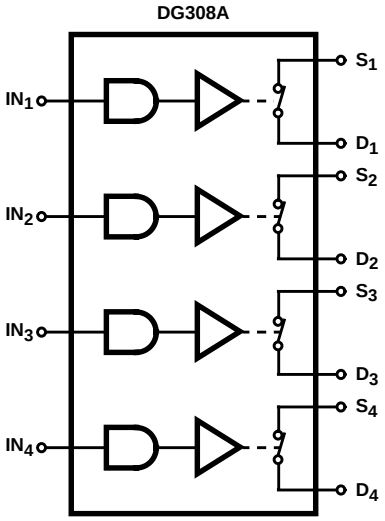
DG308A
(PDIP, SOIC)
TOP VIEW



Features

- Low Power Consumption
- CMOS Compatible
- ±15V Analog Signal Range
- Single or Dual Supply Capability
- Alternate Source

Functional Diagram



SWITCHES SHOWN FOR LOGIC "1" INPUT

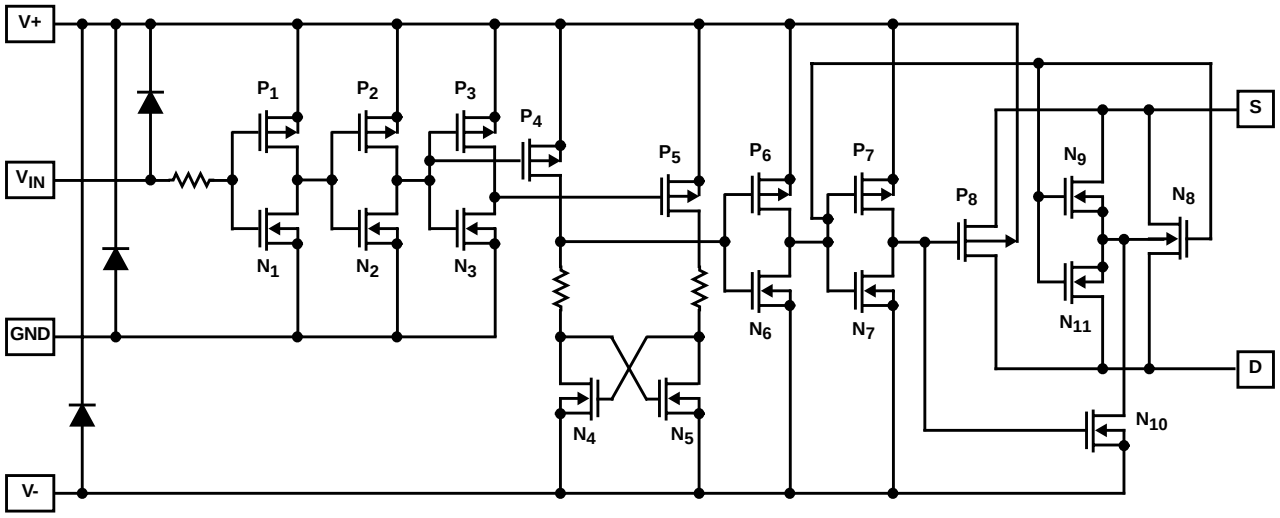
TRUTH TABLE

LOGIC	DG308A
0	OFF
1	ON

Logic "0" ≤3.5V, Logic "1" ≥ 11V at V+ = 15V.

Schematic Diagram (One Channel)

DG308A



Absolute Maximum Ratings

V+ to V- 44V
V- to Ground. 25V
Digital Inputs, V_S, V_D (Note 1). . . . . (V-) -2V to (V+) +2V
or 30mA, Whichever Comes First
Continuous Current, (Any Terminal Except S) 30mA
Continuous Current, (S or D) 20mA
Peak Current, S or D (Pulsed 1ms, 10% Duty Cycle Max) 70mA

Thermal Information

Thermal Resistance (Typical, Note 2)	θ_{JA} ($^oC/W$)
PDIP Package	90
SOIC Package	115

Maximum Junction Temperature . . . . . 150^oC
Maximum Storage Temperature Range. . . . . 65^oC to 150^oC
Maximum Lead Temperature (Soldering 10s) . . . . . 300^oC
(SOIC - Lead Tips Only)

Operating Conditions

Temperature Range
"C" Suffix . . . . . 0^oC to 70^oC

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. Signals on S_X, D_X, or IN_X exceeding V+ or V- will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
2. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications V+ = 15V, V- = -15V, GND = 0V, $T_A = 25^oC$

PARAMETER	TEST CONDITIONS		(NOTE 4) MIN	(NOTE 3) TYP	(NOTE 4) MAX	UNITS
DYNAMIC CHARACTERISTICS						
Turn-ON Time, t_{ON}	See Figure 1		-	130	200	ns
Turn-OFF Time, t_{OFF}	See Figure 1		-	90	150	ns
Charge Injection, Q	C_L = 1µF, R_S = 0, V_S = 0V		-	-10	-	pC
OFF Isolation, OIRR	V_{IN} = 0V, R_L = 75Ω, V_S = $2V_{P-P}$, f = 500kHz (Note 5)		-	78	-	dB
Source OFF Capacitance, $C_{S(OFF)}$	f = 140kHz	V_S = 0V V_{IN} = 0V	-	11	-	pF
Drain OFF Capacitance, $C_{D(OFF)}$		V_D = 0V V_{IN} = 0V	-	8	-	pF
Channel ON Capacitance, $C_{D(ON)} + C_{S(ON)}$		$V_S = V_D$ = 0V V_{IN} = 15V	-	27	-	pF
DIGITAL INPUT CHARACTERISTICS						
Input Current with Voltage High, I_{IH}	V_{IN} = 15V, Full Temperature Range		-	0.001	1	µA
Input Current with Voltage Low, I_{IL}	V_{IN} = 0V, Full Temperature Range		-1	-0.001	-	µA
ANALOG SWITCH CHARACTERISTICS						
Analog Signal Range, V_{ANALOG}			-15	-	15	V
Drain-Source ON Resistance, $r_{DS(ON)}$	V_{IN} = 11V	I_S = -1mA, V_D = +10V	-	60	100	Ω
		I_S = 1mA, V_D = -10V	-	60	100	Ω
Source OFF Leakage Current, $I_{S(OFF)}$	V_{IN} = 3.5V	V_S = 14V, V_D = -14V	-	0.1	5	nA
		V_S = -14V, V_D = 14V	-5	-0.1	-	nA
Drain OFF Leakage Current, $I_{D(OFF)}$		V_S = -14V, V_D = 14V	-	0.1	5	nA
		V_S = 14V, V_D = -14V	-5	-0.1	-	nA
Channel ON Leakage Current, $I_{D(ON)}$	V_{IN} = 11V	$V_D = V_S$ = 14V	-	0.1	5	nA
		$V_D = V_S$ = -14V	-5	-0.1	-	nA

Electrical Specifications V+ = 15V, V- = -15V, GND = 0V, $T_A = 25^oC$ **(Continued)**

PARAMETER	TEST CONDITIONS	(NOTE 4) MIN	(NOTE 3) TYP	(NOTE 4) MAX	UNITS
POWER SUPPLY CHARACTERISTICS					
Positive Supply Current, I+	All Channels ON or OFF V_{IN} = 0V or 15V	-	0.001	100	µA
Negative Supply Current, I-		-100	-0.001	-	µA

NOTES:

3. Typical values are for design aid only, not guaranteed and not subject to production testing.
4. The algebraic convention whereby the most negative value is a minimum, and the most positive is a maximum, is used in this data sheet.
5. OFF isolation = 20 Log V_D/V_S, where V_S = input to OFF switch, and V_D = output.

Test Circuit and Waveforms

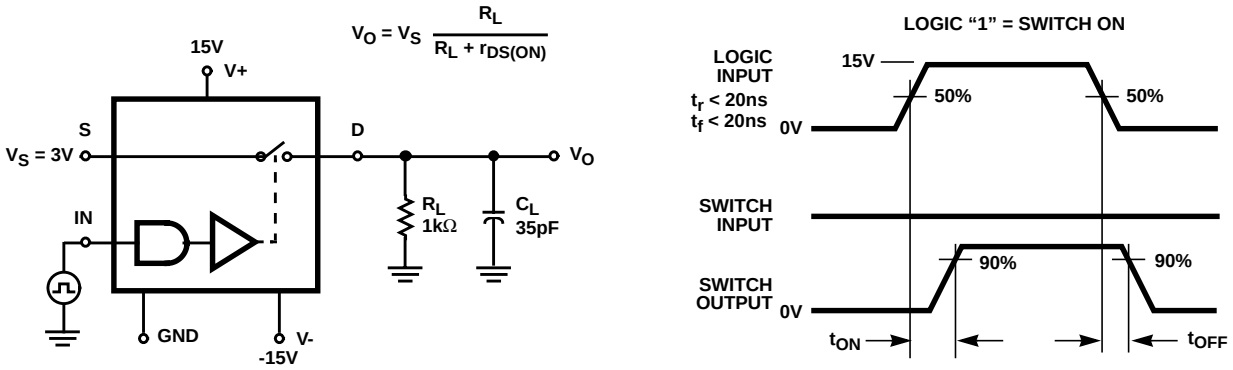


FIGURE 1. t_{ON} AND t_{OFF} TEST CIRCUIT AND MEASUREMENT POINTS

Die Characteristics

DIE DIMENSIONS:

2058µm x 2109µm

METALLIZATION:

Type: Al
Thickness: 10kÅ ±1kÅ

PASSIVATION:

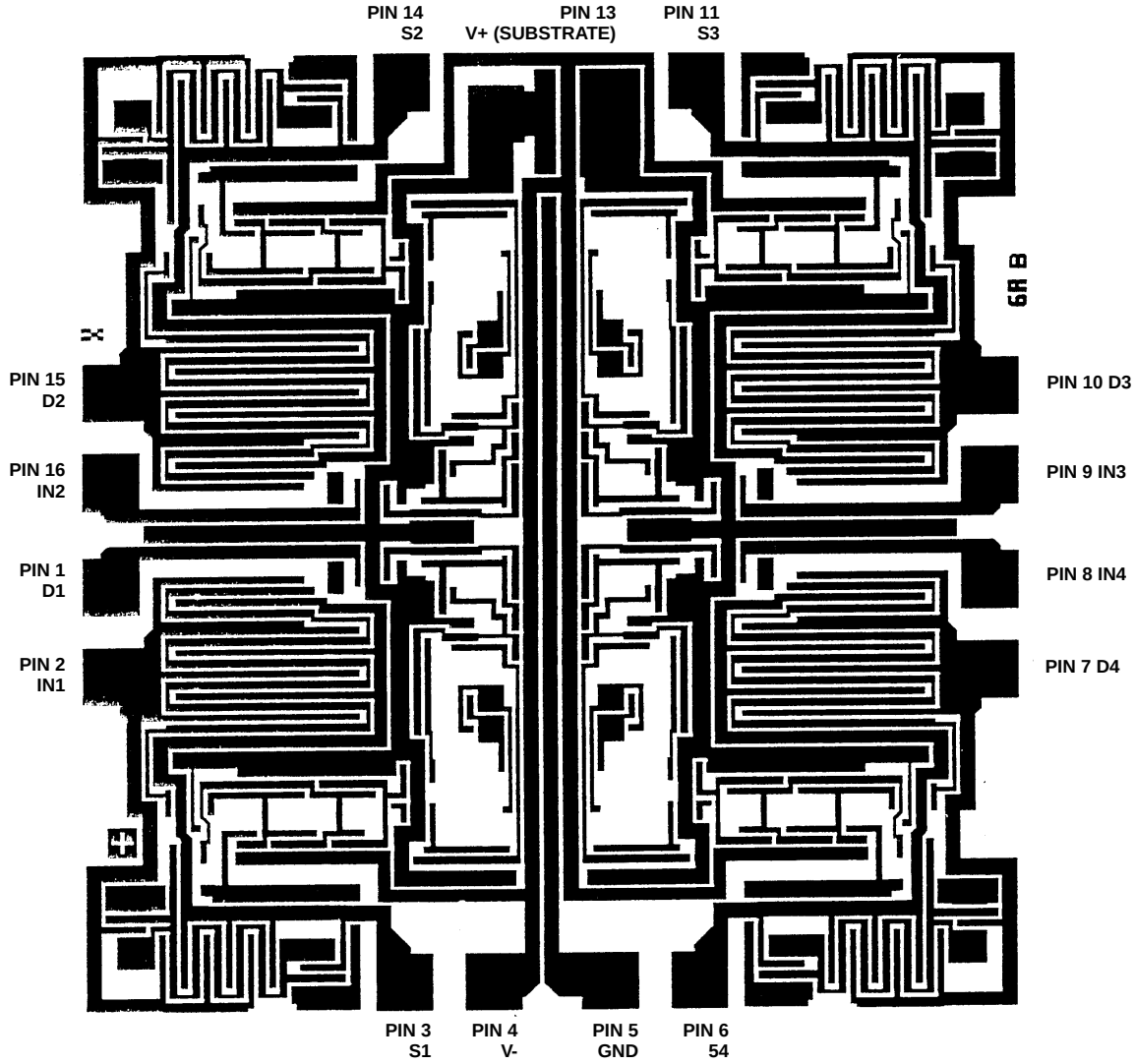
Type: PSG Over Nitride
PSG Thickness: 7kÅ ±1.4kÅ
Nitride Thickness:8kÅ ±1.2kÅ

WORST CASE CURRENT DENSITY:

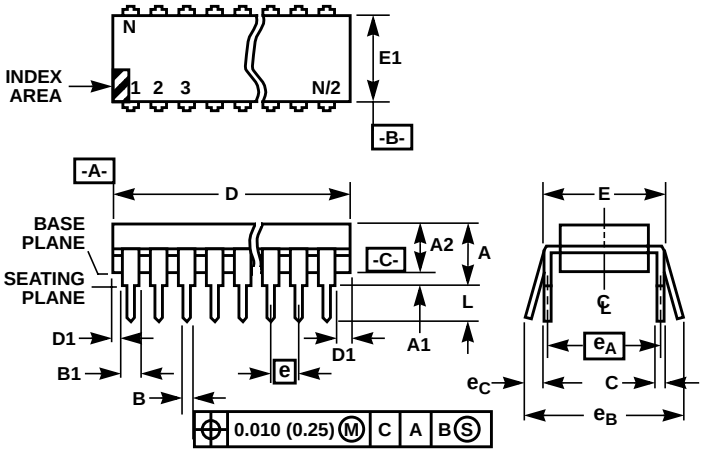
9.1×10^4 A/cm^2

Metallization Mask Layout

DG308A



Dual-In-Line Plastic Packages (PDIP)



NOTES:

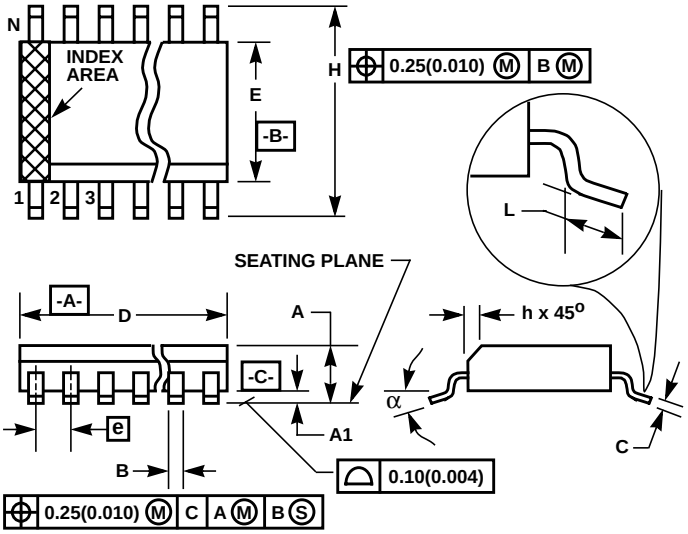
1. Controlling Dimensions: INCH. In case of conflict between English and Metric dimensions, the inch dimensions control.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication No. 95.
4. Dimensions A, A1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.
5. D, D1, and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
6. E and e_A are measured with the leads constrained to be perpendicular to datum -C-.
7. e_B and e_C are measured at the lead tips with the leads unconstrained. e_C must be zero or greater.
8. B1 maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25mm).
9. N is the maximum number of terminal positions.
10. Corner leads (1, N, N/2 and N/2 + 1) for E8.3, E16.3, E18.3, E28.3, E42.6 will have a B1 dimension of 0.030 - 0.045 inch (0.76 - 1.14mm).

E16.3 (JEDEC MS-001-BB ISSUE D)
16 LEAD DUAL-IN-LINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.210	-	5.33	4
A1	0.015	-	0.39	-	4
A2	0.115	0.195	2.93	4.95	-
B	0.014	0.022	0.356	0.558	-
B1	0.045	0.070	1.15	1.77	8, 10
C	0.008	0.014	0.204	0.355	-
D	0.735	0.775	18.66	19.68	5
D1	0.005	-	0.13	-	5
E	0.300	0.325	7.62	8.25	6
E1	0.240	0.280	6.10	7.11	5
e	0.100 BSC		2.54 BSC		-
e_A	0.300 BSC		7.62 BSC		6
e_B	-	0.430	-	10.92	7
L	0.115	0.150	2.93	3.81	4
N	16		16		9

Rev. 0 12/93

Small Outline Plastic Packages (SOIC)



NOTES:

1. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width “B”, as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

M16.15 (JEDEC MS-012-AC ISSUE C)
16 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0532	0.0688	1.35	1.75	-
A1	0.0040	0.0098	0.10	0.25	-
B	0.013	0.020	0.33	0.51	9
C	0.0075	0.0098	0.19	0.25	-
D	0.3859	0.3937	9.80	10.00	3
E	0.1497	0.1574	3.80	4.00	4
e	0.050 BSC		1.27 BSC		-
H	0.2284	0.2440	5.80	6.20	-
h	0.0099	0.0196	0.25	0.50	5
L	0.016	0.050	0.40	1.27	6
N	16		16		7
α	0^o	8^o	0^o	8^o	-

Rev. 0 12/93

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