



LC72321

Single-Chip Microcontroller with PLL and LCD Driver

Preliminary

Overview

The LC72321 is a single-chip microcontroller for use in electronic tuning applications. It includes on chip both LCD drivers and a PLL circuit that can operate at up to 150 MHz. It features a large-capacity ROM, a highly efficient instruction set, and powerful hardware.

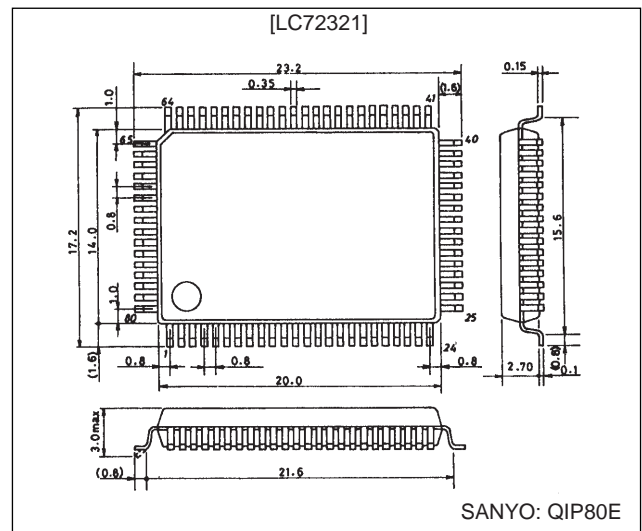
Functions

- Serial I/O
 - Built-in timer interrupts: 80 μ s, 1 ms, 2 ms and 5 ms
 - Stack: Eight levels
 - Beep control: Six beep tones (2.08, 2.25, 2.5, 3.0, 3.75, and 4.17 kHz)
 - Fast programmable divider
 - General-purpose counters: HCTR for frequency measurement and LCTR for frequency or period measurement
 - LCD driver for displays with up to 56 segments (1/2 duty, 1/2 bias)
 - Program memory (ROM): 16 bits \times 4095
 - Data memory (RAM): 4 bits \times 256
 - All instructions are single-word instructions
 - Cycle time: 2.67 μ s, 13.33 μ s, or 40.00 μ s (option)
 - Unlock FF: 0.55 μ s detection, 1.1 μ s detection
 - Timer FF: 1 ms, 5ms, 25ms, 125ms
 - Input ports*: One dedicated key input port and one high breakdown voltage port
 - Output ports*: Two dedicated key output ports, one high breakdown voltage open drain port
Two CMOS output ports (of which one can be switched to be used as LCD driver outputs)
Seven CMOS output ports (mask option switchable to use as LCD ports)
 - I/O ports*: One switchable between input and output in four-bit units and one switchable between input and output in one-bit units
- Note: * Each port consists of four bits
- Program runaway can be detected and a special address set. (Programmable watchdog timer)
 - Voltage detection type reset circuit
 - One 6-bit A/D converter
 - Two 8-bit D/A converters (PWM)
 - One external interrupt (The LC72321 provides an external interrupt, and internal interrupt and a serial I/O interrupt, one of which can be selected under program control.)
 - Hold mode for RAM backup
 - Sense FF for hot/cold startup determination
 - PLL: 4.5 to 5.5 V
 - CPU: 3.5 to 5.5 V
 - RAM: 1.3 to 5.5 V

Package Dimensions

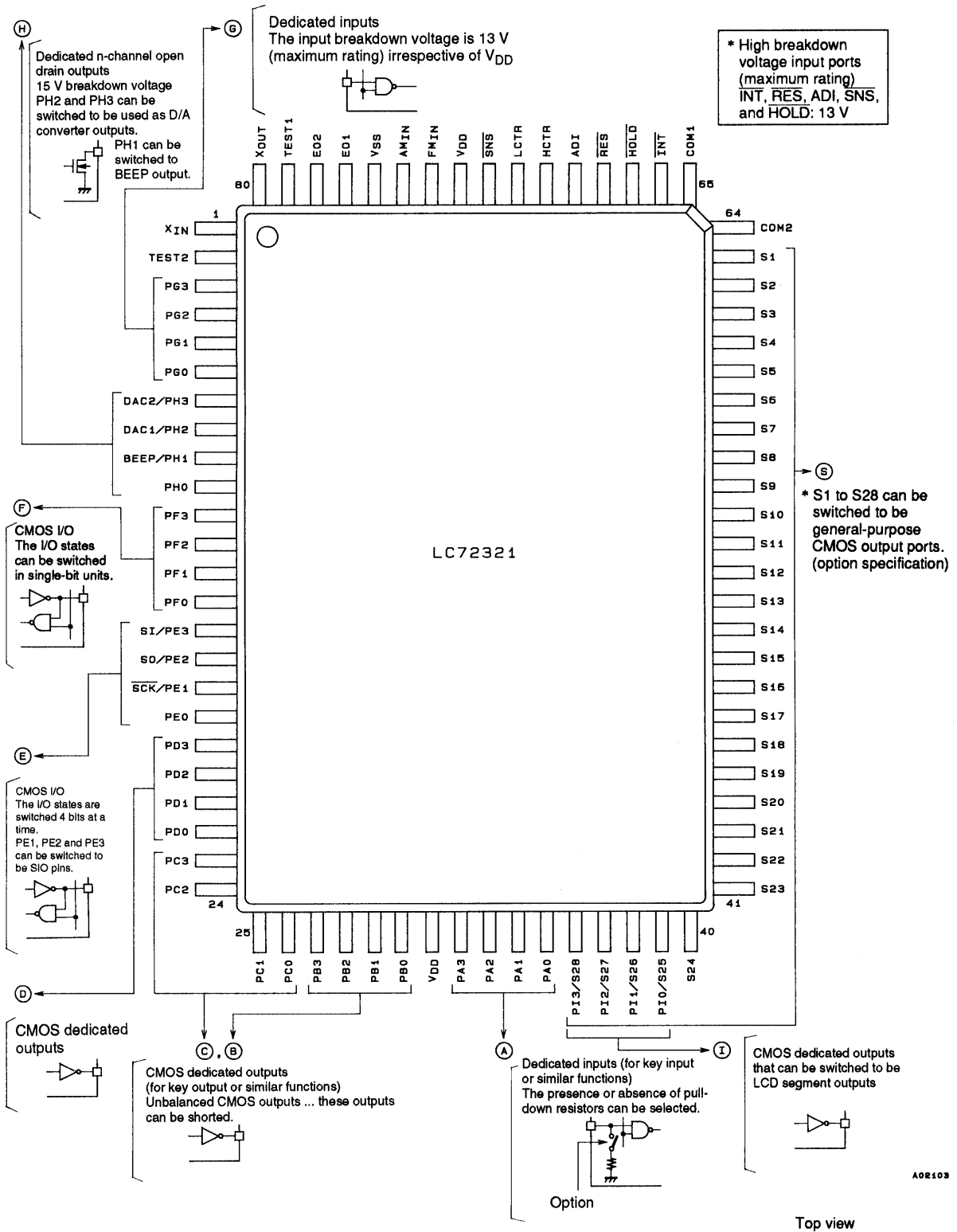
unit: mm

3174-QIP80E



LC72321

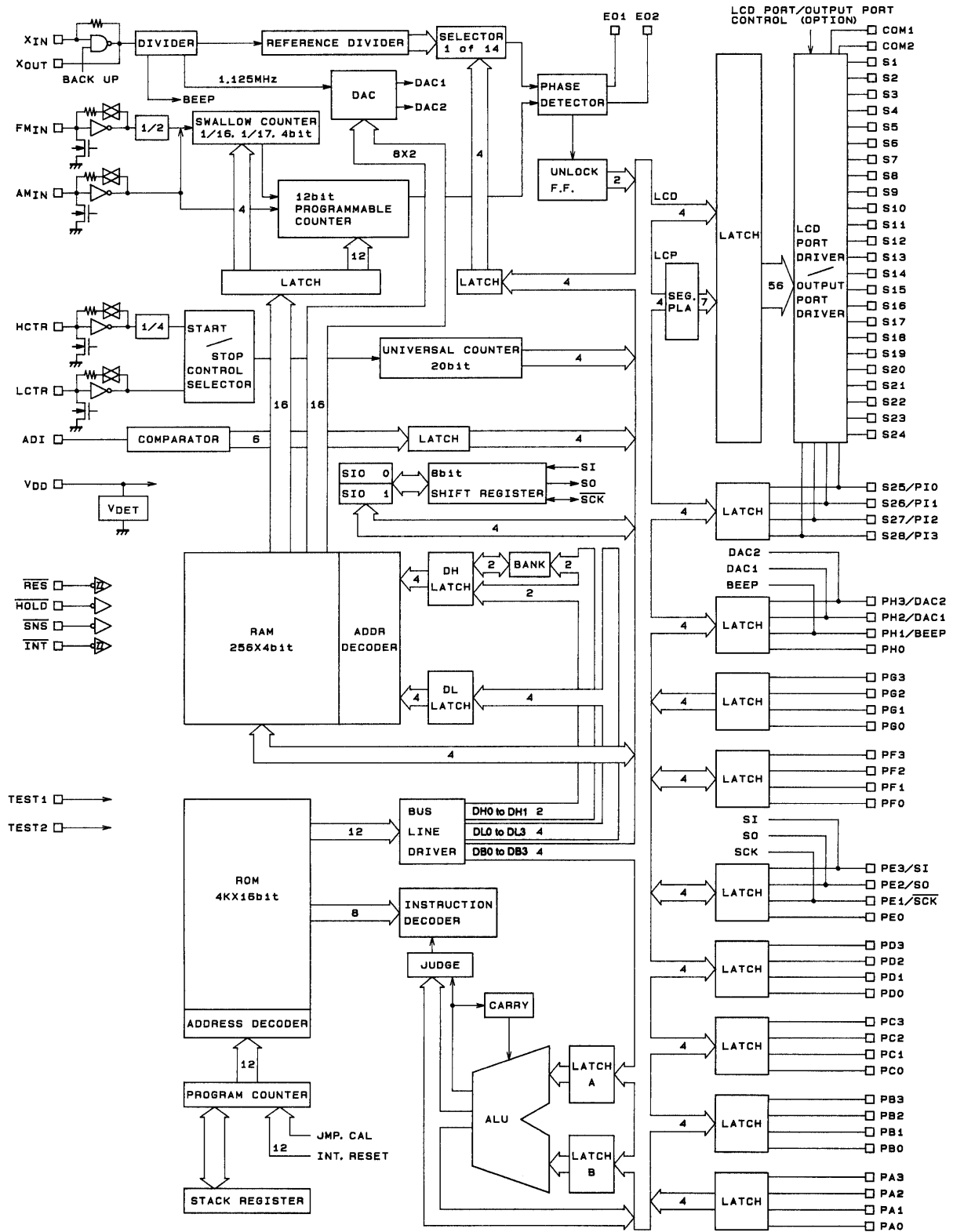
Pin Assignment



A0E103

LC72321

Block Diagram



A02104

Specifications

Absolute Maximum Ratings at $T_a = 25^\circ\text{C}$, $V_{SS} = 0\text{ V}$

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	$V_{DD\text{ max}}$		-0.3 to +6.5	V
Input voltage	V_{IN1}	HOLD, INT, RES, SNS, and the G port	-0.3 to +13	V
	V_{IN2}	Inputs other than V_{IN1}	-0.3 to $V_{DD} + 0.3$	V
Output voltage	V_{OUT1}	H port	-0.3 to +15	V
	V_{OUT2}	Outputs other than V_{OUT1}	-0.3 to $V_{DD} + 0.3$	V
Output current	I_{OUT1}	All D and H port pins	0 to 5	mA
	I_{OUT2}	All E and F port pins	0 to 3	mA
	I_{OUT3}	All B and C port pins	0 to 1	mA
	I_{OUT4}	S1 to S28 and all I port pins	0 to 1	mA
Allowable power dissipation	$Pd\text{ max}$	$T_a = -40\text{ to }+85^\circ\text{C}$	300*	mW
Operating temperature range	Topg		-40 to +85	$^\circ\text{C}$
Storage temperature range	Tstg		-45 to +125	$^\circ\text{C}$

Note: * Reference value

Allowable Operating Ranges at $T_a = -40\text{ to }+85^\circ\text{C}$, $V_{DD} = 3.5\text{ to }5.5\text{ V}$

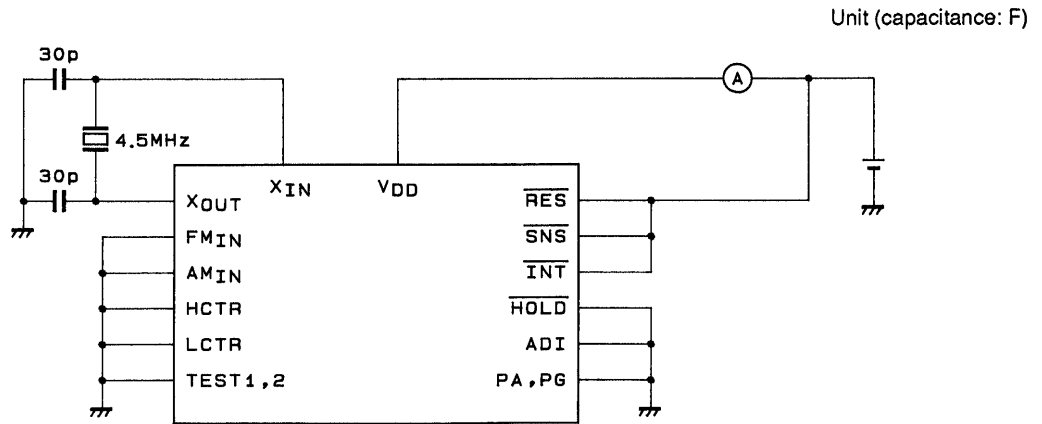
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Supply voltage	V_{DD1}	CPU and PLL operating	4.5		5.5	V
	V_{DD2}	CPU operating	3.5		5.5	V
	V_{DD3}	Memory retention voltage	1.3		5.5	V
Input high level voltage	V_{IH1}	G port	$0.7 V_{DD}$		8.0	V
	V_{IH2}	RES, INT, HOLD	$0.8 V_{DD}$		8.0	V
	V_{IH3}	SNS	2.5		8.0	V
	V_{IH4}	A port	$0.6 V_{DD}$		V_{DD}	V
	V_{IH5}	PE0, PE2, F port	$0.7 V_{DD}$		V_{DD}	V
	V_{IH6}	LCTR (period measurement), V_{DD1} , PE1, PE3	$0.8 V_{DD}$		V_{DD}	V
Input low level voltage	V_{IL1}	G port	0		$0.3 V_{DD}$	V
	V_{IL2}	RES, INT, PE1, PE3	0		$0.2 V_{DD}$	V
	V_{IL3}	SNS	0		1.3	V
	V_{IL4}	A port	0		$0.2 V_{DD}$	V
	V_{IL5}	PE0, PE2, F port	0		$0.3 V_{DD}$	V
	V_{IL6}	LCTR (period measurement), V_{DD1}	0		$0.2 V_{DD}$	V
	V_{IL7}	HOLD	0		$0.4 V_{DD}$	V
Input frequency	f_{IN1}	XIN	4.0	4.5	5.0	MHz
	f_{IN2}	FMIN, V_{IN2} , V_{DD1}	10		130	MHz
	f_{IN3}	FMIN, V_{IN3} , V_{DD1}	10		150	MHz
	f_{IN4}	AMIN (L), V_{IN4} , V_{DD1}	0.5		10	MHz
	f_{IN5}	AMIN (H), V_{IN5} , V_{DD1}	2.0		40	MHz
	f_{IN6}	HCTR, V_{IN6} , V_{DD1}	0.4		12	MHz
	f_{IN7}	LCTR (frequency), V_{IN7} , V_{DD1}	100		500	kHz
	f_{IN8}	LCTR (period), V_{IH6} , V_{IL6} , V_{DD1}	1		20×10^3	Hz
Input amplitude	V_{IN1}	XIN	0.50		1.5	Vrms
	V_{IN2}	FMIN	0.10		1.5	Vrms
	V_{IN3}	FMIN	0.15		1.5	Vrms
	$V_{IN4, 5}$	AMIN	0.10		1.5	Vrms
	$V_{IN6, 7}$	LCTR, HCTR	0.10		1.5	Vrms
Input voltage range	V_{IN8}	ADI	0		V_{DD}	V

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Electrical Characteristics for the Allowable Operating Ranges

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Hysteresis	V _H	LCTR (period), $\overline{\text{RES}}$, $\overline{\text{INT}}$, PE1, PE3	0.1 V _{DD}			V
Rejected pulse width	P _{REJ}	$\overline{\text{SNS}}$			50	μs
Power-down detection voltage	V _{DET}		2.7	3.0	3.3	V
Input high level current	I _{IH1}	$\overline{\text{INT}}$, $\overline{\text{HOLD}}$, $\overline{\text{RES}}$, $\overline{\text{ADI}}$, $\overline{\text{SNS}}$, and the G port: V _I = 5.5 V			3.0	μA
	I _{IH2}	A, E, and F ports: E and F ports with outputs off, A port with no R _{PD} , V _I = V _{DD}			3.0	μA
	I _{IH3}	XIN: V _I = V _{DD} = 5.0 V	2.0	5.0	15	μA
	I _{IH4}	FMIN, AMIN, HCTR, LCTR: V _I = V _{DD} = 5.0 V	4.0	10	30	μA
	I _{IH5}	A port: With an R _{PD} , V _I = V _{DD} = 5.0 V		50		μA
Input low level current	I _{IL1}	$\overline{\text{INT}}$, $\overline{\text{HOLD}}$, $\overline{\text{RES}}$, $\overline{\text{ADI}}$, $\overline{\text{SNS}}$, and the G port: V _I = V _{SS}			3.0	μA
	I _{IL2}	A, E, and F ports: E and F ports with outputs off, A port with no R _{PD} , V _I = V _{SS}			3.0	μA
	I _{IL3}	XIN: V _{IN} = V _{SS}	2.0	5.0	15	μA
	I _{IL4}	FMIN, AMIN, HCTR, LCTR: V _I = V _{SS}	4.0	10	30	μA
Input floating voltage	V _{IF}	A port: With an R _{PD}			0.05 V _{DD}	V
Pull-down resistance	R _{PD}	A port: With an R _{PD} , V _{DD} = 5.0 V	75	100	200	kΩ
Output high level off leakage current	I _{OFFH1}	EO1, EO2: V _O = V _{DD}		0.01	10	nA
	I _{OFFH2}	B, C, D, E, F, and I ports: V _O = V _{DD}			3.0	μA
	I _{OFFH3}	H port: V _O = 13 V			5.0	μA
Output low level off leakage current	I _{OFFL1}	EO1, EO2: V _O = V _{SS}		0.01	10	nA
	I _{OFFL2}	B, C, D, E, F, and I ports: V _O = V _{SS}			3.0	μA
Output high level voltage	V _{OH1}	B and C ports: I _O = 1 mA	V _{DD} - 2.0	V _{DD} - 1.0	V _{DD} - 0.5	V
	V _{OH2}	E and F ports: I _O = 1 mA	V _{DD} - 1.0			V
	V _{OH3}	EO1, EO2: I _O = 500 μA	V _{DD} - 1.0			V
	V _{OH4}	XOUT: I _O = 200 μA	V _{DD} - 1.0			V
	V _{OH5}	S1 to S28 and the I port: I _O = -0.1 mA	V _{DD} - 1.0			V
	V _{OH6}	D port: I _O = 5 mA	V _{DD} - 1.0			V
	V _{OH7}	COM1, COM2: I _O = 25 μA	V _{DD} - 0.75	V _{DD} - 0.5	V _{DD} - 0.3	V
Output low level voltage	V _{OL1}	B and C ports: I _O = 50 μA	0.5	1.0	2.0	V
	V _{OL2}	E and F ports: I _O = 1 mA			1.0	V
	V _{OL3}	EO1, EO2: I _O = 500 μA			1.0	V
	V _{OL4}	XOUT: I _O = 200 μA			1.0	V
	V _{OL5}	S1 to S28 and the I port: I _O = 0.1 mA			1.0	V
	V _{OL6}	D port: I _O = 5 mA			1.0	V
	V _{OL7}	COM1, COM2: I _O = 25 μA	0.3	0.5	0.75	V
	V _{OL8}	H port: I _O = 5 mA	(150 Ω) 0.75		(400 Ω) 2.0	V
Output middle level voltage	V _{M1}	COM1, COM2: V _{DD} = 5.0 V, I _O = 25 μA	2.0	2.5	3.0	V
A/D conversion error		ADI: V _{DD1}	-1/2		1/2	LSB
Current drain	I _{DD1}	V _{DD1} , f _{IN2} = 130 MHz		15	20	mA
	I _{DD2}	V _{DD1} , PLL stopped, CT = 2.67 μs (HOLD mode, Figure 1)		1.5		mA
	I _{DD3}	V _{DD1} , PLL stopped, CT = 13.33 μs (HOLD mode, Figure 1)		1.0		mA
	I _{DD4}	V _{DD1} , PLL stopped, CT = 40.00 μs (HOLD mode, Figure 1)		0.7		mA
	I _{DD5}	V _{DD} = 5.5 V, oscillator stopped, Ta = 25°C (BACKUP mode, Figure 2)			5	μA
	V _{DD} = 2.5 V, oscillator stopped, Ta = 25°C (BACKUP mode, Figure 2)			1	μA	

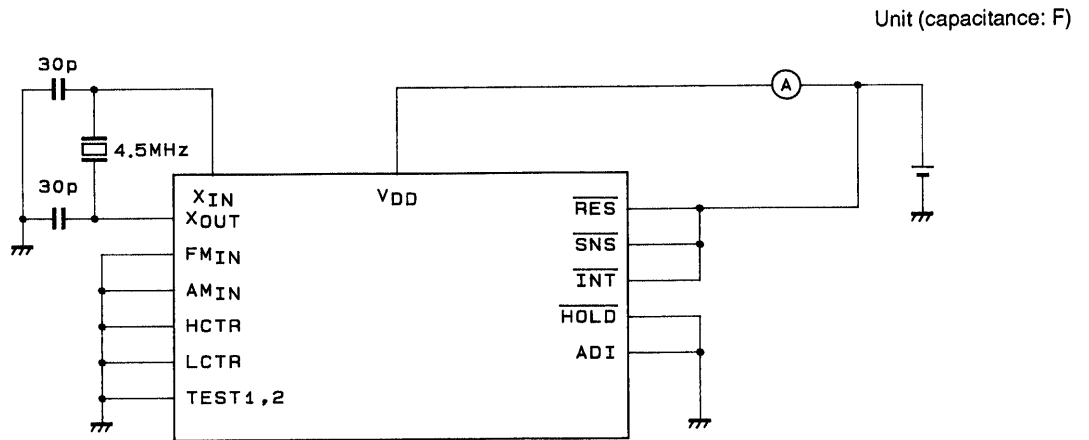
Test Circuits



Note: PB to PF, PH, and PI are all open. However, PE and PF are output selected.

A02105

Figure 1 I_{DD2} to I_{DD4} in HOLD Mode



Note: PA to PI, S1 to S4, COM1, and COM2 are all open.

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Figure 2 I_{DD5} in BACK UP Mode

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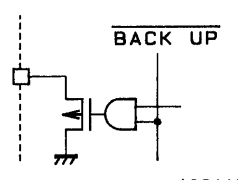
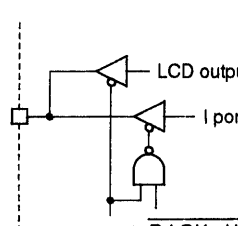
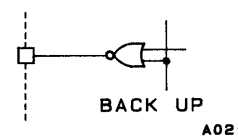
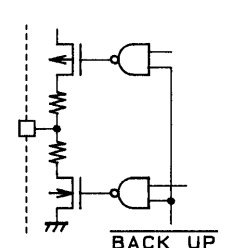
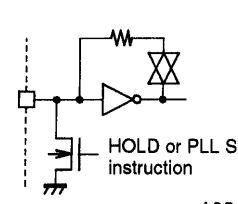
Pin Functions

Pin	Pin No.	Function	I/O	I/O circuit type
PA0 PA1 PA2 PA3	35 34 33 32	Low threshold type dedicated input port These pins can be used, for example, for key data acquisition. Built-in pull-down resistors can be specified as an option. This option is in 4-pin units, and cannot be specified for individual pins. Input through these pins is disabled in BACKUP mode.	Input	<p style="text-align: right;">A02107</p>
PB0 PB1 PB2 PB3 PC0 PC1 PC2 PC3	30 29 28 27 26 25 24 23	Dedicated output ports Since the output transistor impedances are unbalanced CMOS, these pins can be effectively used for functions such as key scan timing. These pins go to the output high impedance state in BACKUP mode. These pins go to the low level during a reset, i.e., when the \overline{RES} pin is low.	Output	<p style="text-align: right;">A02108</p>
PD0 PD1 PD2 PD3	22 21 20 19	Dedicated output ports These are normal CMOS outputs. These pins go to the output high impedance state in BACKUP mode. These pins go to the low level during a reset, i.e., when the \overline{RES} pin is low.		<p style="text-align: right;">A02109</p>
PE0 $\overline{PE1/SCK}$ PE2/SO PE3/SI	18 17 16 15	I/O port These pins are switched between input and output as follows. Once an input instruction (IN, TPT, or TPF) is executed, these pins latch in the input mode. Once an output instruction (OUT, SPB, or RPB) is executed, they latch in the output mode. Note that PE1, PE2 and PE3 are also used as the serial I/O port. These pins go to the input mode during a reset, i.e., when the \overline{RES} pin is low. In BACKUP mode these pins go to the input mode with input disabled.	I/O	<p>PE1, PE3</p> <p style="text-align: right;">A02109</p>
PF0 PF1 PF2 PF3	14 13 12 11	I/O port These pins are switched between input and output by the FPC instruction. The I/O states of this port can be specified for individual pins. These pins go to the input mode during a reset, i.e., when the \overline{RES} pin is low. In BACKUP mode these pins go to the input mode with input disabled.		<p>Others</p> <p style="text-align: right;">A02110</p>
PG0 PG1 PG2 PG3	6 5 4 3	Dedicated input port Input through these pins is disabled in BACKUP mode.	Input	<p style="text-align: right;">A02111</p>

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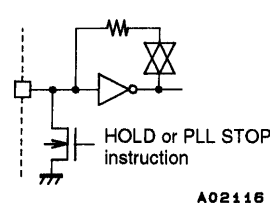
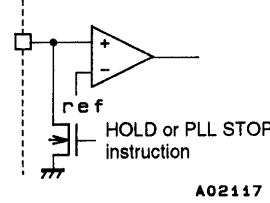
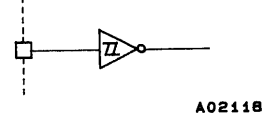
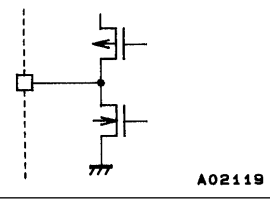
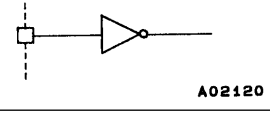
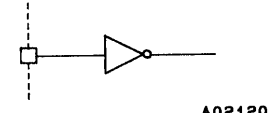
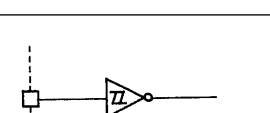
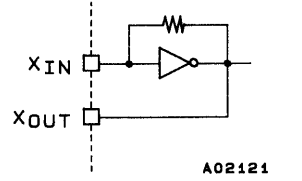
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Pin	Pin No.	Function	I/O	I/O circuit type
PH0 PH1/BEEP PH2/DAC1 PH3/DAC2	10 9 8 7	Dedicated output port Since these pins are high breakdown voltage n-channel transistor open-drain outputs, they can be effectively used for functions such as band power supply switching. Note that PH1 is also used as the BEEP output and that PH2 and PH3 are also used as the DAC1 and DAC2 outputs. These ports go to the high impedance state during a reset, i.e., when the RES pin is low, and in BACKUP mode.	Output	 A02112
PI0/S25 PI1/S26 PI2/S27 PI3/S28	39 38 37 36	Dedicated output port While these pins have a CMOS output circuit structure, they can be switched to function as LCD drivers. Their function is switched by the SS and RS instructions. These pins cannot be switched individually. The LCD driver function is selected and a segment off signal is output when power is first applied or when \overline{RES} is low. These pins are held at the low level in BACKUP mode. Note that when the general-purpose port use option is specified, these pins output the contents of IPORT when LPC is 1, and the contents of the general-purpose output port LATCH when LPC is 0.	Output	 A02113
S1 to S24	63 to 40	LCD driver segment outputs A frame frequency of 100 Hz and a 1/2 duty, 1/2 bias drive type are used. A segment off signal is output when power is first applied or when RES is low. These pins are held at the low level in BACKUP mode. The use of these pins as general-purpose output ports can be specified as an option.	Output	 A02114
COM1 COM2	65 64	LCD driver common outputs A 1/2 duty, 1/2 bias drive type is used. The output when power is first applied or when \overline{RES} is low is identical to the normal operating mode output. These pins are held at the low level in BACKUP mode.	Output	 A02115
FMIN	74	FM VCO (local oscillator) input The input must be capacitor-coupled. The input frequency range is from 10 to 130 MHz.	Input	 A02116
AMIN	75	AM VCO (local oscillator) input The band supported by this pin can be selected using the PLL instruction. High (2 to 40 MHz) → SW Low (0.5 to 10 MHz) → LW and MW		

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Pin	Pin No.	Function	I/O	I/O circuit type
HCTR	70	Universal counter input The input should be capacitor-coupled. The input frequency range is from 0.4 to 12 MHz. This input can be effectively used for FM IF or AM IF counting.	Input	 <p style="text-align: right;">A02116</p>
LCTR	71	Universal counter input The input should be capacitor-coupled for input frequencies in the range 100 to 150 kHz. Capacitor coupling is not required for input frequencies from 1 Hz to 20 kHz. This input can be effectively used for AM IF counting. This pin can also be used as a normal input port.		
ADI	69	A/D converter input A 1.28 ms period is required for a 6-bit sequential comparison conversion. The full scale input is $((63/96) \cdot V_{DD})$ for a data value of 3FH.	Input	 <p style="text-align: right;">A02117</p>
$\overline{\text{INT}}$	66	External interrupt request input An interrupt is generated when the INTEN flag is set (by an SS instruction) and a falling edge is input. This pin can also be used as a normal input port.	Input	 <p style="text-align: right;">A02118</p>
EO1 EO2	77 78	Reference frequency and programmable divisor phase comparison error outputs Charge pump circuits are built in. EO1 and EO2 are the same.	Output	 <p style="text-align: right;">A02119</p>
$\overline{\text{SNS}}$	72	Input pin used to determine if a power outage has occurred in BACKUP mode This pin can also be used as a normal input port.	Input	 <p style="text-align: right;">A02120</p>
$\overline{\text{HOLD}}$	67	Input pin used to force the LC72322 to HOLD mode The LC72322 goes to $\overline{\text{HOLD}}$ mode when the HOLDEN flag is set (by an SS instruction) and the HOLD input goes low. A high breakdown voltage circuit is used so that this input can be used in conjunction with the normal power switch.	Input	 <p style="text-align: right;">A02120</p>
$\overline{\text{RES}}$	68	System reset input This signal should be held low for 75 ms after power is first applied to effect a power-up reset. The reset starts when a low level has been input for at least six reference clock cycles.	Input	 <p style="text-align: right;">A02118</p>
XIN XOUT	1 80	Crystal oscillator connections (4.5 MHz) A feedback resistor is built in.	Input Output	 <p style="text-align: right;">A02121</p>
TEST1 TEST2	2 79	LSI test pins. These pins must be connected to V_{SS} .	—	
V_{DD} V_{SS}	31, 73 76	Power supply	—	

LC72321 Instruction Table

Abbreviations:

ADDR: Program memory address [12 bits]

b: Borrow

B: Bank number [2 bits]

C: Carry

DH: Data memory address high (row address) [2 bits]

DL: Data memory address low (column address) [4 bits]

I: Immediate data [4 bits]

M: Data memory address

N: Bit position [4 bits]

Pn: Port number [4 bits]

r: General register (one of the locations 00 to 0FH in bank 0)

Rn: Register number [4 bits]

(): Contents of register or memory

()N: Contents of bit N of register or memory

Instruction group	Mnemonic	Operand		Function	Operation	Machine code											
		1st	2nd			D15	14	13	12	11	10	9	8	7	6	5	4
Addition instructions	AD	r	M	Add M to r	$r \leftarrow (r) + (M)$	0	1	0	0	0	0	DH	DL	Rn			
	ADS	r	M	Add M to r, then skip if carry	$r \leftarrow (r) + (M)$ skip if carry	0	1	0	0	0	1	DH	DL	Rn			
	AC	r	M	Add M to r with carry	$r \leftarrow (r) + (M) + C$	0	1	0	0	1	0	DH	DL	Rn			
	ACS	r	M	Add M to r with carry, then skip if carry	$r \leftarrow (r) + (M) + C$ skip if carry	0	1	0	1	0	0	DH	DL	Rn			
	AI	M	I	Add I to M	$M \leftarrow (M) + I$	0	1	0	1	0	0	DH	DL	I			
	AIS	M	I	Add I to M, then skip if carry	$M \leftarrow (M) + I$ skip if carry	0	1	0	1	0	1	DH	DL	I			
	AIC	M	I	Add I to M with carry	$M \leftarrow (M) + I + C$	0	1	0	1	1	0	DH	DL	I			
	AICS	M	I	Add I to M with carry, then skip if carry	$M \leftarrow (M) + I + C$ skip if carry	0	1	0	1	1	1	DH	DL	I			
Subtraction instructions	SU	r	M	Subtract M from r	$r \leftarrow (r) - (M)$	0	1	1	0	0	0	DH	DL	Rn			
	SUS	r	M	Subtract M from r, then skip if borrow	$r \leftarrow (r) - (M)$ skip if borrow	0	1	1	0	0	1	DH	DL	Rn			
	SB	r	M	Subtract M from r with borrow	$r \leftarrow (r) - (M) - b$	0	1	1	0	1	0	DH	DL	Rn			
	SBS	r	M	Subtract M from r with borrow, then skip if borrow	$r \leftarrow (r) - (M) - b$ skip if borrow	0	1	1	0	0	0	DH	DL	Rn			
	SI	M	I	Subtract I from M	$M \leftarrow (M) - I$	0	1	1	1	0	0	DH	DL	I			
	SIS	M	I	Subtract I from M, then skip if borrow	$M \leftarrow (M) - I$ skip if borrow	0	1	1	1	0	1	DH	DL	I			
	SIB	M	I	Subtract I from M with borrow	$M \leftarrow (M) - I - b$	0	1	1	1	1	0	DH	DL	I			
	SIBS	M	I	Subtract I from M with borrow, then skip if borrow	$M \leftarrow (M) - I - b$ skip if borrow	0	1	0	1	1	1	DH	DL	I			
Comparison instructions	SEQ	r	M	Skip if r equals M	$r - M$ skip if zero	0	0	0	0	0	1	DH	DL	Rn			
	SGE	r	M	Skip if r is greater than or equal to M	$r - M$ skip if not borrow $(r) \geq (M)$	0	0	0	0	1	1	DH	DL	Rn			
	SEQL	M	I	Skip if M equal to I	$M - I$ skip if zero	0	0	1	1	0	1	DH	DL	I			
	SGEL	M	I	Skip if M is greater than or equal to I	$M - I$ skip if not borrow $(M) \geq I$	0	0	1	1	1	1	DH	DL	I			

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Instruction group	Mnemonic	Operand		Function	Operation	Machine code															
		1st	2nd			D15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	D0
Logical operation instructions	AND	M	I	AND I with M	$M \leftarrow (M) \wedge I$	0	0	1	1	0	0	DH	DL	I							
	OR	M	I	OR I with M	$M \leftarrow (M) \vee I$	0	0	1	1	1	0	DH	DL	I							
	EXL	r	M	Exclusive OR M with r	$r \leftarrow (r) \oplus (M)$	0	0	1	0	0	0	DH	DL	Rn							
Transfer instructions	LD	r	M	Load M to r	$r \leftarrow (M)$	1	0	0	0	0	0	DH	DL	Rn							
	ST	M	r	Store r to M	$M \leftarrow (r)$	1	0	0	0	0	1	DH	DL	Rn							
	MVRD	r	M	Move M to destination M referring to r in the same row	$[DH, Rn] \leftarrow (M)$	1	0	0	0	1	0	DH	DL	Rn							
	MVRS	M	r	Move source M referring to r to M in the same row	$M \leftarrow [DH, Rn]$	1	0	0	0	1	1	DH	DL	Rn							
	MVSR	M1	M2	Move M to M in the same row	$[DH, DL1] \leftarrow [DH, DL2]$	1	0	0	1	0	0	DH	DL1	DL2							
	MVI	M	I	Move I to M	$M \leftarrow I$	1	0	0	1	0	1	DH	DL	I							
	PLL	M	r	Load M to PLL registers	$PLL\ r \leftarrow PLL\ DATA$	1	0	0	1	1	0	DH	DL	Rn							
Bit test instructions	TMT	M	N	Test M bits, then skip if all bits specified are true	if $M(N) = \text{all } 1s$, then skip	1	0	1	0	0	1	DH	DL	N							
	TMF	M	N	Test M bits, then skip if all bits specified are false	if $M(N) = \text{all } 0s$, then skip	1	0	1	0	1	1	DH	DL	N							
Jump and subroutine call instructions	JMP	ADDR		Jump to the address	$PC \leftarrow ADDR$	1	0	1	1	ADDR (12 bits)											
	CAL	ADDR		Call subroutine	$Stack \leftarrow (PC) + 1$	1	1	0	0	ADDR (12 bits)											
	RT			Return from subroutine	$PC \leftarrow Stack$	1	1	0	1	0	1	0	0	0	0	0	0	0	0	0	0
	RTI			Return from interrupt	$PC \leftarrow Stack$	1	1	0	1	0	1	0	1	0	0	0	0	0	0	0	0
F/F test instructions	TTM	N		Test timer F/F then skip if it has not been set	if timer $F/F = 0$, then skip	1	1	0	1	0	1	1	0	0	0	0	0	N			
	TUL	N		Test unlock F/F then skip if it has not been set	if $UL\ F/F = 0$, then skip	1	1	0	1	0	1	1	1	0	0	0	0	N			
Status register instructions	SS	N		Set status register	(Status register 1) $N \leftarrow 1$	1	1	0	1	1	1	0	0	0	0	0	0	N			
	RS	N		Reset status register	(Status register 1) $N \leftarrow 0$	1	1	0	1	1	1	0	1	0	0	0	0	N			
	TST	N		Test status register true	if (Status register 2) $N = \text{all } 1s$, then skip	1	1	0	1	1	1	1	0	0	0	0	0	N			
	TSF	N		Test status register false	if (Status register 2) $N = \text{all } 0s$, then skip	1	1	0	1	1	1	1	1	0	0	0	0	N			
Bank switching instructions	BANK	B		Select bank	$BANK \leftarrow B$	1	1	0	1	0	0	B	0	0	0	0	0	0	0	0	

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Instruction group	Mnemonic	Operand		Function	Operation	Machine code															
		1st	2nd			D15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	D0
I/O instructions group	LCD	M	I	Output segment pattern to LCD digit direct	LCD (DIGIT) ← M	1	1	1	0	0	0	DH	DL	DIGIT							
	LCP	M	I	Output segment pattern to LCD digit through PLA	LCD (DIGIT) ← PLA ← M	1	1	1	0	0	1	DH	DL	DIGIT							
	IN	M	P	Input port data to M	M ← (Port (P))	1	1	1	0	1	0	DH	DL	P							
	OUT	M	P	Output contents of M to port	(Port (P)) ← M	1	1	1	0	1	1	DH	DL	P							
	SPB	P	N	Set port bits	(Port (P)) N ← 1	1	1	1	1	0	0	0	0	P	N						
	RPB	P	N	Reset port bits	(Port (P)) N ← 0	1	1	1	1	0	1	0	1	P	N						
	TPT	P	N	Test port bits, then skip if all bits specified are true	if (Port (P)) N = all 1s, then skip	1	1	1	1	1	0	1	0	P	N						
TPF	P	N	Test port bits, then skip if all bits specified are false	if (Port (P)) N = all 0s, then skip	1	1	1	1	1	1	1	1	P	N							
Universal counter instructions	UCS	I		Set I to UCCW1	UCCW1 ← I	0	0	0	0	0	0	0	1	0	0	0	0	I			
	UCC	I		Set I to UCCW2	UCCW2 ← I	0	0	0	0	0	0	1	1	0	0	0	0	I			
Other instructions	FPC	N		F port I/O control	FPC latch ← N	0	0	0	1	0	0	0	0	0	0	0	0	N			
	CKSTP			Clock stop	Stop clock if HOLD = 0	0	0	0	1	0	0	0	1	0	0	0	0	0	0	0	0
	DAC	I		Load M to D/A registers	DAreg ← DAC DATA	0	0	0	0	0	0	1	0	0	0	0	0	I			
	SIO	I1	I2	Serial I/O control	SIOW ← I1, I2	0	0	0	1	0	0	1	1	I1	I2						
	SIOL	M	I	Load SIOreg to M	M ← SIOreg	0	0	0	1	1	0	DH	DL	I							
	SIOS	M	I	Store M to SIOreg	SIOreg ← M	0	0	0	1	0	1	DH	DL	I							
	BEEP	I		Beep control	BEEPreg ← I	0	0	0	1	0	0	1	0	0	0	0	0	I			
NOP			No operation		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	

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