Ordering number: EN4359A

CMOS LSI

SANYO No. 4359A

LC74721, LC74721M

On-screen Video Display Controllers for NTSC or PAL-M

Overview

The LC74721 and LC74721M are CMOS, video display controllers for superimposing text and low-level graphics onto an NTSC or PAL-M compatible television receiver. Up to 240, 8 × 8-pixel characters can be displayed under microprocessor control on a 24-character by 10-line display.

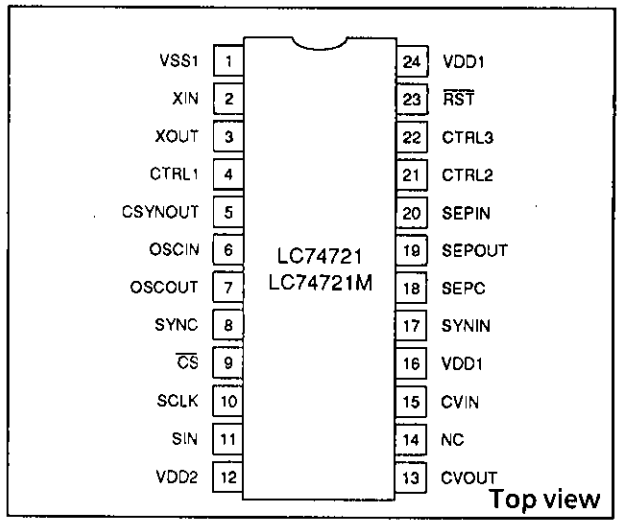
The LC74721 and LC74721M feature selectable pixel width and height, and 64 vertical and 64 horizontal display start positions. It also features a flashing enable bit for each character position.

The LC74721 and LC74721M operate from a 5 V supply. The LC74721 is available in 24-pin DIPs, and the LC74721M, in 24-pin MFPs.

Features

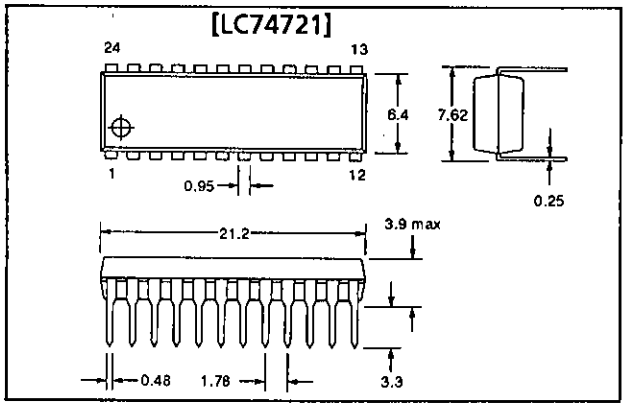
- Complete text and graphics video overlay circuitry
- 64-character internal character generator ROM
- 8 × 8-pixel characters
- Three pixel widths and three pixel heights
- Selectable background color
- Built-in synchronization check and separation circuitry
- Approximately 0.5 or 1 s period character flashing option
- NTSC or PAL-M format compatibility
- 8-bit serial input format
- 5 V supply
- 24-pin plastic DIP (300 mil) and 24-pin plastic MFP (375 mil)

Pin Assignment

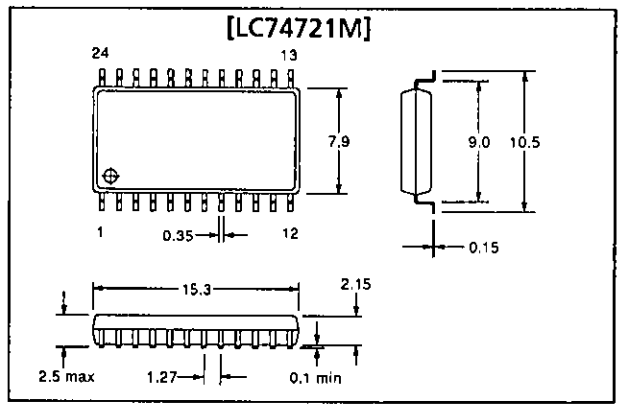


Package Dimensions

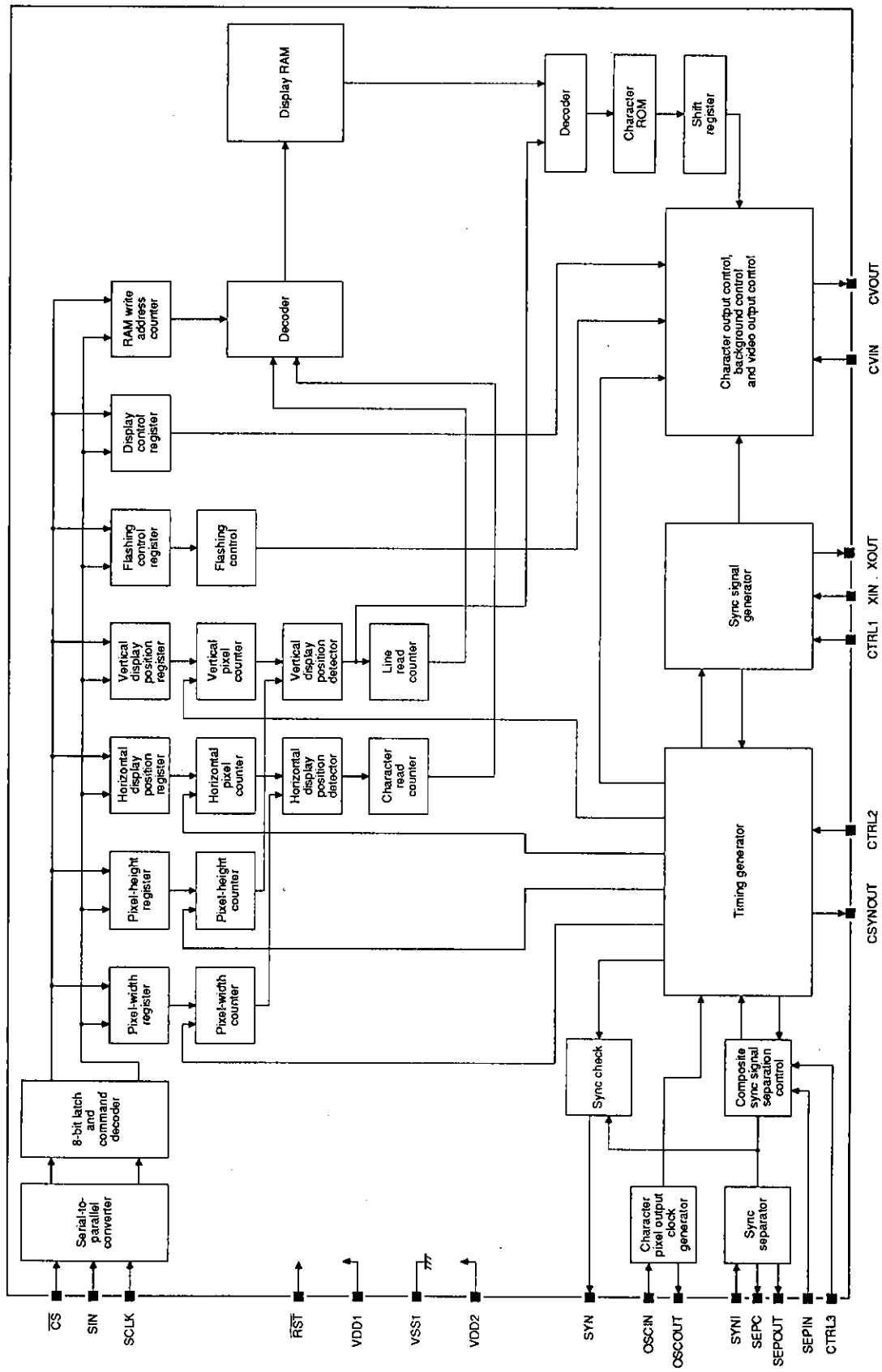
3067-DIP24S



3045B-MFP24



Block Diagram



Pin Functions

Number	Name	Function
1	VSS1	Ground
2	XIN	Internal sync signal crystal oscillator capacitor connections or external clock input ($2f_{SC}$ or $4f_{SC}$)
3	XOUT	
4	CTRL1	Clock input mode select. HIGH for external clock input mode, and LOW for crystal oscillator mode
5	CSYNOUT	Composite synchronization signal output. During reset ($\overline{RST}$ LOW), crystal oscillator clock is output. No output for internal reset command
6	OSCIN	LC oscillator input. LC circuit for pixel clock generation character output
7	OSCOUT	LC oscillator output. LC circuit for pixel clock generation character output
8	SYNC	External synchronization signal check output. During reset ($\overline{RST}$ LOW), pixel clock is output. No output for internal reset command
9	$\overline{CS}$	Serial data input enable when LOW, with pull-up resistance
10	SCLK	Clock input for serial data input, with pull-up resistance
11	SIN	Serial data input, with pull-up resistance
12	VDD2	Power supply for composite video image signal level modulation (for analog system)
13	CVOUT	Composite video image signal output
14	NC	No connection
15	CVIN	Composite video image signal input
16	VDD1	5 V power supply for digital system
17	SYNCIN	Synchronization separation circuit input. If internal sync separation circuit is not used, use SYNCIN to input an external horizontal or composite synchronization signal.
18	SEPC	Synchronization separation circuit modulator capacitor connection. Leave open if not used.
19	SEPOUT	Composite synchronization separation circuit output. Outputs SYNCIN signal if internal sync separation is not used.
20	SEPIN	Vertical synchronization signal input. Tie to VDD1 if not used.
21	CTRL2	NTSC/PAL-M sync signal generation method select input. LOW for NTSC
22	CTRL3	SEPIN input control. $\overline{VSYNC}$ input signal when LOW
23	$\overline{RST}$	System reset input, with pull-up resistance
24	VDD1	5 V power supply for digital system

Specifications

Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit
Supply voltage range	V_{DD1}, V_{DD2}	V_{SS} – 0.3 to V_{SS} + 7.0	V
Input voltage range	V_I	V_{SS} – 0.3 to V_{DD} + 0.3	V
Output voltage range	V_O	V_{SS} – 0.3 to V_{DD} + 0.3	V
Power dissipation (T_a = 25 °C)	P_D	350	mW
Operating temperature range	Topr	–30 to +70	°C
Storage temperature range	T_{stg}	–40 to +125	°C

Recommended Operating Conditions

T_a = 25 °C

Parameter	Symbol	Ratings	Unit
Logic supply voltage	V_{DD1}	5.0	V
Analog supply voltage	V_{DD2}	5.0	V
Logic supply voltage range	V_{DD1}	4.5 to 5.5	V
Analog supply voltage range	V_{DD2}	4.5 to ($1.27V_{DD1}$)	V

Electrical Characteristics

V_{DD1} = 5 V, T_a = −30 to +70 °C unless otherwise noted

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
VDD1 logic supply current	I_{DD1}	All outputs open, 7.159 MHz crystal oscillator, 8 MHz LC oscillator	–	–	15	mA
VDD2 analog supply current	I_{DD2}	V_{DD2} = 5 V	–	–	20	mA
CVIN input leakage current	I_{L1}		–	–	1	μA
CVOUT output leakage current	I_{L2}		–	–	1	μA
CTRL1, CTRL2, CTRL3 and OSCIN LOW-level input current	I_{IL}	$V_I = V_{SS1}$	−1.0	–	–	μA
$\overline{RST}$, $\overline{CS}$, SIN, SCLK, CTRL1, SEPIN, CTRL2 and CTRL3 HIGH-level input current	I_{IH}	$V_I = V_{DD1}$	–	–	1.0	μA
$\overline{RST}$, $\overline{CS}$, SIN and SCLK LOW-level input voltage	V_{IL1}		V_{SS} − 0.3	–	$0.2V_{DD1}$	V
CTRL1, CTRL2, CTRL3 and SEPIN LOW-level input voltage	V_{IL2}		V_{SS} − 0.3	–	$0.3V_{DD1}$	V
$\overline{RST}$, $\overline{CS}$, SIN and SCLK HIGH-level input voltage	V_{IH1}		$0.8V_{DD1}$	–	V_{DD1} + 0.3	V
CTRL1, CTRL2, CTRL3 and SEPIN HIGH-level input voltage	V_{IH2}		$0.7V_{DD1}$	–	V_{DD1} + 0.3	V
CVIN composite video input voltage	V_{I1}	Measured peak to peak	–	2.0	–	V_{p-p}
SYNCIN composite video input voltage	V_{I2}	Measured peak to peak	–	2.0	2.5	V_{p-p}
XIN input voltage	V_{I3}	External clock input, f_{IN} = $2f_{SC}$ or $4f_{SC}$	0.20	–	5.0	V_{p-p}
CSYNOUT, SYNC and SEPOUT LOW-level output voltage	V_{OL1}	V_{DD1} = 4.5 V, I_{OL} = 1.0 mA	–	–	1.0	V
CSYNOUT, SYNC and SEPOUT HIGH-level output voltage	V_{OH1}	V_{DD1} = 4.5 V, I_{OH} = −1.0 mA	3.5	–	–	V
CVOUT sync voltage	V_{SN}	See note 1.	0.70	0.82	0.94	V
		See note 2.	0.87	0.99	1.11	V
CVOUT pedestal voltage	V_{PD}	See note 1.	1.27	1.39	1.51	V
		See note 2.	1.44	1.56	1.68	V
CVOUT LOW-level color burst voltage	V_{CBL}	See note 1.	0.98	1.10	1.22	V
		See note 2.	1.15	1.27	1.39	V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
CVOUT HIGH-level color burst voltage	V_{CBH}	See note 1.	1.58	1.70	1.82	V
		See note 2.	1.74	1.86	1.98	V
CVOUT LOW-level background color voltage	V_{RSL}	See note 1.	1.42	1.54	1.66	V
		See note 2.	1.59	1.71	1.83	V
CVOUT HIGH-level background color voltage	V_{RSH}	See note 1.	1.94	2.06	2.18	V
		See note 2.	2.11	2.23	2.35	V
CVOUT border voltage	V_{BK}	See note 1.	1.50	1.62	1.74	V
		See note 2.	1.68	1.80	1.92	V
CVOUT character voltage	V_{CHA}	See note 1.	2.61	2.73	2.85	V
		See note 2.	2.80	2.92	3.04	V
$\overline{RST}$, $\overline{CS}$, SIN and SCLK pull-up resistance	R_{pu}	Depends on optional settings at pins	25	50	90	kΩ
XIN and XOUT oscillator frequency	f_{OSC1}	NTSC ($2f_{sc}$)	–	7.159	–	MHz
		NTSC ($4f_{sc}$)	–	14.318	–	MHz
		PAL-M ($4f_{sc}$)	–	14.302	–	MHz
OSCIN and OSCOUT oscillator frequency	f_{OSC2}	LC oscillator	5	–	10	MHz

Notes

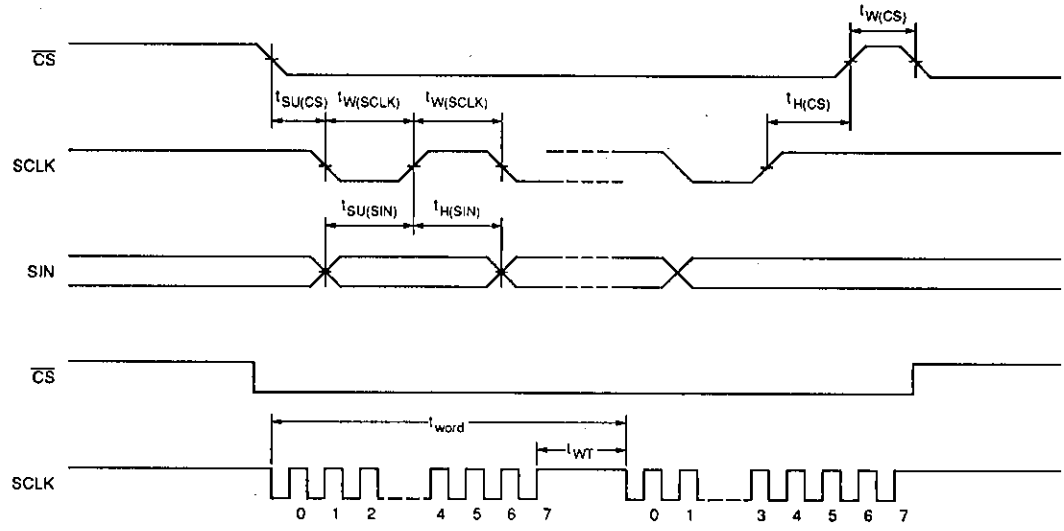
1. CV_{OUT} at $V_{DD1} = V_{DD2} = 5$ V, 0.8 V sync level
2. CV_{OUT} at $V_{DD1} = V_{DD2} = 5$ V, 1.0 V sync level

Timing Characteristics

$V_{DD1} = 5 \pm 0.5$ V, $T_a = -30$ to $+75$ °C

Parameter	Symbol	Ratings			Unit
		min	typ	max	
SCLK input pulsewidth	$t_{W(SCLK)}$	200	–	–	ns
$\overline{CS}$ HIGH-level input pulsewidth	$t_{W(CS)}$	1	–	–	µs
$\overline{CS}$ input setup time	$t_{SU(CS)}$	200	–	–	ns
SIN data input setup time	$t_{SU(SIN)}$	200	–	–	ns
$\overline{CS}$ input hold time	$t_{H(CS)}$	2	–	–	µs
SIN data input hold time	$t_{H(SIN)}$	200	–	–	ns
8-bit data word write time	t_{WORD}	4.2	–	–	µs
RAM data write time	t_{WT}	1	–	–	µs

Serial data input timing



Display Control Features And Characteristics

Display Control Command Structure

The display control commands, COMMAND0 to COMMAND5, are shifted in 8-bit serial units. The first byte of a command consists of an identification code and data. The second byte consists of data only. Once the command identification code in byte 1 has been written, it is saved until the next time the first byte is written. If COMMAND1 is written, the display character write mode begins and the first byte does not change. When $\overline{CS}$ is HIGH, COMMAND0 is set.

Display Control Command Data

Command	First byte								Second byte							
	Command code				Data or register storing data				Data or register storing data							
	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
COMMAND0 Display memory (VRAM) write address setting command	1	0	0	0	V3	V2	V1	V0	0	0	0	H4	H3	H2	H1	H0
COMMAND1 Display character data write command	1	0	0	1	0	0	0	0	at	0	C5	C4	C3	C2	C1	C0
COMMAND2 Vertical display position and character size setting command	1	0	1	0	VS21	VS20	VS11	VS10	0	FS	VP5	VP4	VP3	VP2	VP1	VP0
COMMAND3 Horizontal display position and character size setting command	1	0	1	1	HS21	HS20	HS11	HS10	0	LC	HP5	HP4	HP3	HP2	HP1	HP0
COMMAND4 Display control setting command	1	1	0	0	TST MOD	CB	OSC STP	SYS RST	0	0	NON	EG	BK1	BK0	RV	DSP ON
COMMAND5 Synchronization signal control setting command	1	1	0	1	PH1	PH0	BCL	INT	0	RN2	RN1	RN0	SN3	SN2	SN1	SN0

COMMAND0: Display Memory Write Address Setting Command

COMMAND0: first byte

DA0 to DA7	Register name	Register Contents		Remarks
		Status	Function	
0	V0	0	Display memory address 0 to 9H	
		1		
1	V1	0		
		1		
2	V2	0		
		1		
3	V3	0		
		1		
4	–	0	COMMAND0 identification code	
5	–	0		
6	–	0		
7	–	1		

COMMAND0: second byte

DA0 to DA7	Register name	Register Contents		Remarks
		Status	Function	
0	H0	0	Display memory address 0 to 17H	
		1		
1	H1	0		
		1		
2	H2	0		
		1		
3	H3	0		
		1		
4	H4	0		
		1		
5	–	0		
6	–	0		
7	–	0	Second byte identification bit	

Note

On system reset with $\overline{RST}$, the status of all registers is set to 0.

COMMAND1: Display Character Data Write Command

COMMAND1: first byte

DA0 to DA7	Register name	Register Contents		Remarks
		Status	Function	
0	–	0		
1	–	0		
2	–	0		
3	–	0		
4	–	1	COMMAND1 identification code	After command is input, display character data write mode is set until $\overline{CS}$ is set HIGH.
5	–	0		
6	–	0		
7	–	1		

COMMAND1: second byte

DA0 to DA7	Register name	Register Contents		Remarks
		Status	Function	
0	C0	0	Character code 0 to 3FH	
		1		
1	C1	0		
		1		
2	C2	0		
		1		
3	C3	0		
		1		
4	C4	0		
		1		
5	C5	0		
		1		
6	–	0		
7	at	0	Character attribute OFF	
		1	Character attribute ON	

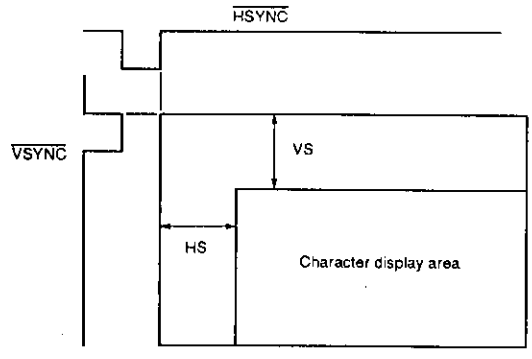
Note
On system reset with $\overline{RST}$, the status of all registers is set to 0.

COMMAND2: Vertical Display Position and Character Size Setting Command

COMMAND2: first byte

DA0 to DA7	Register name	Register Contents		Remarks
		Status	Function	
0	VS10	0	VS11 / VS10 / Height: 0 / 0 / 1H/pixel; 0 / 1 / 2H/pixel; 1 / 0 / 3H/pixel; 1 / 1 / 1H/pixel	First row vertical character size
		1		
1	VS11	0		
		1		
2	VS20	0	VS21 / VS20 / Height: 0 / 0 / 1H/pixel; 0 / 1 / 2H/pixel; 1 / 0 / 3H/pixel; 1 / 1 / 1H/pixel	Second row vertical character size
		1		
3	VS21	0		
		1		
4	–	0	COMMAND2 identification code	
5	–	1		
6	–	0		
7	–	1		

COMMAND2: second byte

DA0 to DA7	Register name	Register Contents		Remarks
		Status	Function	
0	VP0	0	Initial vertical coordinate position determined by $VS = H \times \left(2 \sum_{n=0}^{5} 2^n \, VPn\right)$ where H is the horizontal synchronization pulse period. 	The initial vertical coordinate position is set in 6 bits, VP0 to VP5, where the lsb, VP0, corresponds to 2H.
		1		
1	VP1	0		
		1		
2	VP2	0		
		1		
3	VP3	0		
		1		
4	VP4	0		
		1		
5	VP5	0		
		1		
6	FS	0	$2f_{SC}$ crystal oscillator frequency	
		1	$4f_{SC}$ crystal oscillator frequency	
7	–	0	Second byte identification bit	

Note

On system reset with $\overline{RST}$, the status of all registers is set to 0.

COMMAND3: Horizontal Display Position and Character Size Setting Command

COMMAND3: first byte

<table>
<tr><th rowspan="2">DA0 to DA7</th><th rowspan="2">Register name</th><th colspan="2">Register Contents</th><th rowspan="2">Remarks</th></tr>
<tr><th>Status</th><th>Function</th></tr>
<tr><td rowspan="2">0</td><td rowspan="2">HS10</td><td>0</td><td rowspan="5"><table><tr><th>HS11</th><th>HS10</th><th>Width</th></tr><tr><td>0</td><td>0</td><td>1Tc/pixel</td></tr><tr><td>0</td><td>1</td><td>2Tc/pixel</td></tr><tr><td>1</td><td>0</td><td>3Tc/pixel</td></tr><tr><td>1</td><td>1</td><td>1Tc/pixel</td></tr></table></td><td rowspan="3">First row horizontal character size</td></tr>
<tr><td>1</td></tr>
<tr><td rowspan="2">1</td><td rowspan="2">HS11</td><td>0</td></tr>
<tr><td>1</td></tr>
<tr><td rowspan="2">2</td><td rowspan="2">HS20</td><td>0</td><td rowspan="5"><table><tr><th>HS21</th><th>HS20</th><th>Width</th></tr><tr><td>0</td><td>0</td><td>1Tc/pixel</td></tr><tr><td>0</td><td>1</td><td>2Tc/pixel</td></tr><tr><td>1</td><td>0</td><td>3Tc/pixel</td></tr><tr><td>1</td><td>1</td><td>1Tc/pixel</td></tr></table></td><td rowspan="3">Second row horizontal character size</td></tr>
<tr><td>1</td></tr>
<tr><td rowspan="2">3</td><td rowspan="2">HS21</td><td>0</td></tr>
<tr><td>1</td></tr>
<tr><td>4</td><td>–</td><td>1</td><td rowspan="4">COMMAND3 identification code</td><td rowspan="4"></td></tr>
<tr><td>5</td><td>–</td><td>1</td></tr>
<tr><td>6</td><td>–</td><td>0</td></tr>
<tr><td>7</td><td>–</td><td>1</td></tr>
</table>

COMMAND3: second byte

<table>
<tr><th rowspan="2">DA0 to DA7</th><th rowspan="2">Register name</th><th colspan="2">Register Contents</th><th rowspan="2">Remarks</th></tr>
<tr><th>Status</th><th>Function</th></tr>
<tr><td rowspan="2">0</td><td rowspan="2">HP0</td><td>0</td><td rowspan="10">The initial horizontal coordinate position is given by
$HS = T_C \times \left(2 \sum_{n=0}^{5} 2^n HPn\right)$
where T_c is the OSCIN and OSCOUT operation mode oscillation period.</td><td rowspan="10">The initial horizontal coordinate position is set in 6 bits, HP0 to HP5, where the lsb, HP0, corresponds to 2Tc.</td></tr>
<tr><td>1</td></tr>
<tr><td rowspan="2">1</td><td rowspan="2">HP1</td><td>0</td></tr>
<tr><td>1</td></tr>
<tr><td rowspan="2">2</td><td rowspan="2">HP2</td><td>0</td></tr>
<tr><td>1</td></tr>
<tr><td rowspan="2">3</td><td rowspan="2">HP3</td><td>0</td></tr>
<tr><td>1</td></tr>
<tr><td rowspan="2">4</td><td rowspan="2">HP4</td><td>0</td></tr>
<tr><td>1</td></tr>
<tr><td rowspan="2">5</td><td rowspan="2">HP5</td><td>0</td></tr>
<tr><td>1</td></tr>
<tr><td rowspan="2">6</td><td rowspan="2">LC</td><td>0</td><td>LC oscillator dot clock</td><td rowspan="2">Selects the dot clock used for the character display transverse direction</td></tr>
<tr><td>1</td><td>Crystal oscillator dot clock</td></tr>
<tr><td>7</td><td>–</td><td>0</td><td>Second byte identification bit</td><td></td></tr>
</table>

Note

On system reset with $\overline{RST}$, the status of all registers is set to 0.

COMMAND 4: Display Control Setting Command

COMMAND4: first byte

DA0 to DA7	Register name	Register Contents		Remarks
		Status	Function	
0	SYSRST	0		A system reset also occurs when $\overline{CS}$ goes LOW.
		1	Resets all registers and turns the display OFF	
1	OSCSTP	0	Crystal and LC oscillator stop disable	External sync mode character display
		1	Crystal and LC oscillator circuitry stop enable	
2	CB	0	Color burst signal is output.	When BCL is HIGH only.
		1	Color burst signal is not output.	
3	TSTMOD	0	Normal operating mode	Test mode should not be selected during normal operation.
		1	Test mode	
4	–	0	COMMAND4 identification code	
5	–	0		
6	–	1		
7	–	1		

COMMAND4: second byte

DA0 to DA7	Register name	Register Contents		Remarks
		Status	Function	
0	DSPON	0	Character display OFF	
		1	Character display ON	
1	RV	0	Inverse characters OFF	
		1	Inverse characters ON	
2	BK0	0	Blinking OFF	When blinking inverse characters, characters alternate between normal and inverse.
		1	Blinking ON	
3	BK1	0	Blinking period 0.5 s	Selects blinking period.
		1	Blinking period 1.0 s	
4	EG	0	Border OFF	Interlaced/non-interlaced switching
		1	Border ON	
5	NON	0	Interlaced scanning, 262.5 H/field	
		1	Non-interlaced scanning, 263 H/field	
6	–	0		
7	–	0	Second byte identification bit	

Note
On system reset with $\overline{RST}$, the status of all registers is set to 0.

COMMAND5: Synchronization Signal Control Setting Command

COMMAND5: first byte

DA0 to DA7	Register name	Register Contents		Remarks
		Status	Function	
0	INT	0	External synchronization	Switches between external and internal synchronization
		1	Internal synchronization	
1	BCL	0	Background color available	Only available with internal synchronization
		1	Background color not available (background level only set)	
2	PH0	0	PH1 = 0, PH0 = 0: Background color's phase π/2 PH1 = 0, PH0 = 1: Background color's phase π PH1 = 1, PH0 = 0: Background color's phase 3π/2 PH1 = 1, PH0 = 1: Background color's phase In phase	Phase selection. In PAL-M mode, there is only one background color (blue-black). Otherwise, there are 4 types.
		1		
3	PH1	0		
		1		
4	–	1	COMMAND5 identification code	
5	–	0		
6	–	1		
7	–	1		

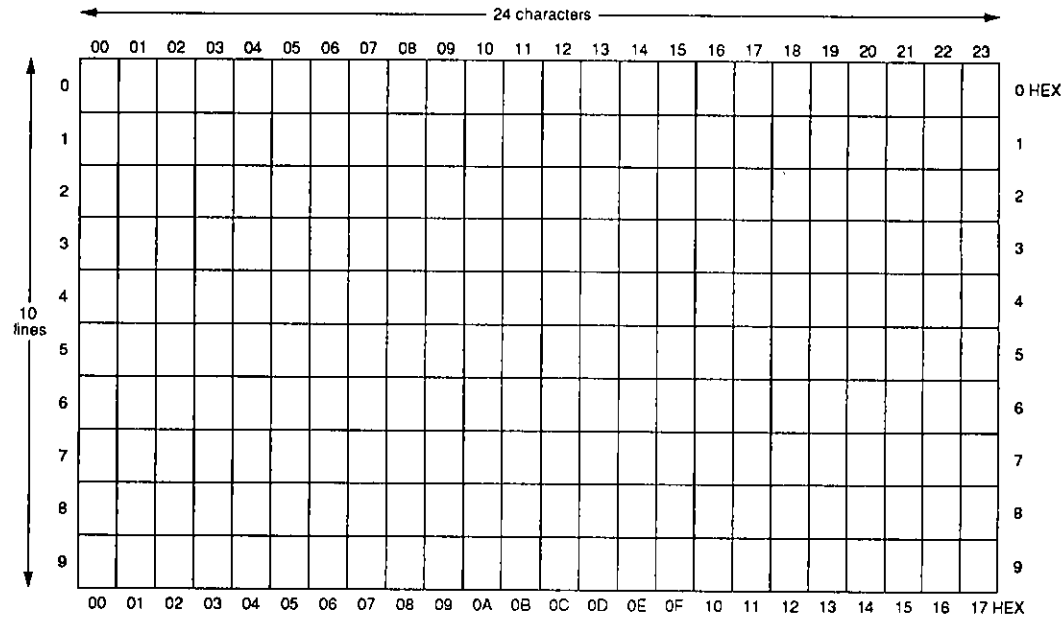
COMMAND5: second byte

DA0 to DA7	Register name	Register Contents		Remarks
		Status	Function	
0	SN0	0	SN3 SN2 SN1 SN0 Detection frequency 0 0 0 0 No detection 0 0 0 1 32 times 0 0 1 0 64 times 0 1 0 0 128 times 1 0 0 0 256 times	External sync signal detection control Determines when the signal goes from ON to OFF. Selects the sampling period, in units of the horizontal sync signal cycle (1 H), for which the sync continues and cannot be detected.
		1		
1	SN1	0		
		1		
2	SN2	0		
		1		
3	SN3	0		
		1		
4	RN0	0	RN2 RN1 RN0 Detection frequency 0 0 0 0 times 0 0 1 4 times 0 1 0 8 times 1 0 0 16 times	External sync signal detection control Determines when the signal goes from OFF to ON. Selects the sampling period, in units of the horizontal sync signal cycle (1 H), for which the sync continues and can be detected.
		1		
5	RN1	0		
		1		
6	RN2	0		
		1		
7	–	0	Second byte identification bit	

Note
On system reset with $\overline{RST}$, the status of all registers is set to 0.

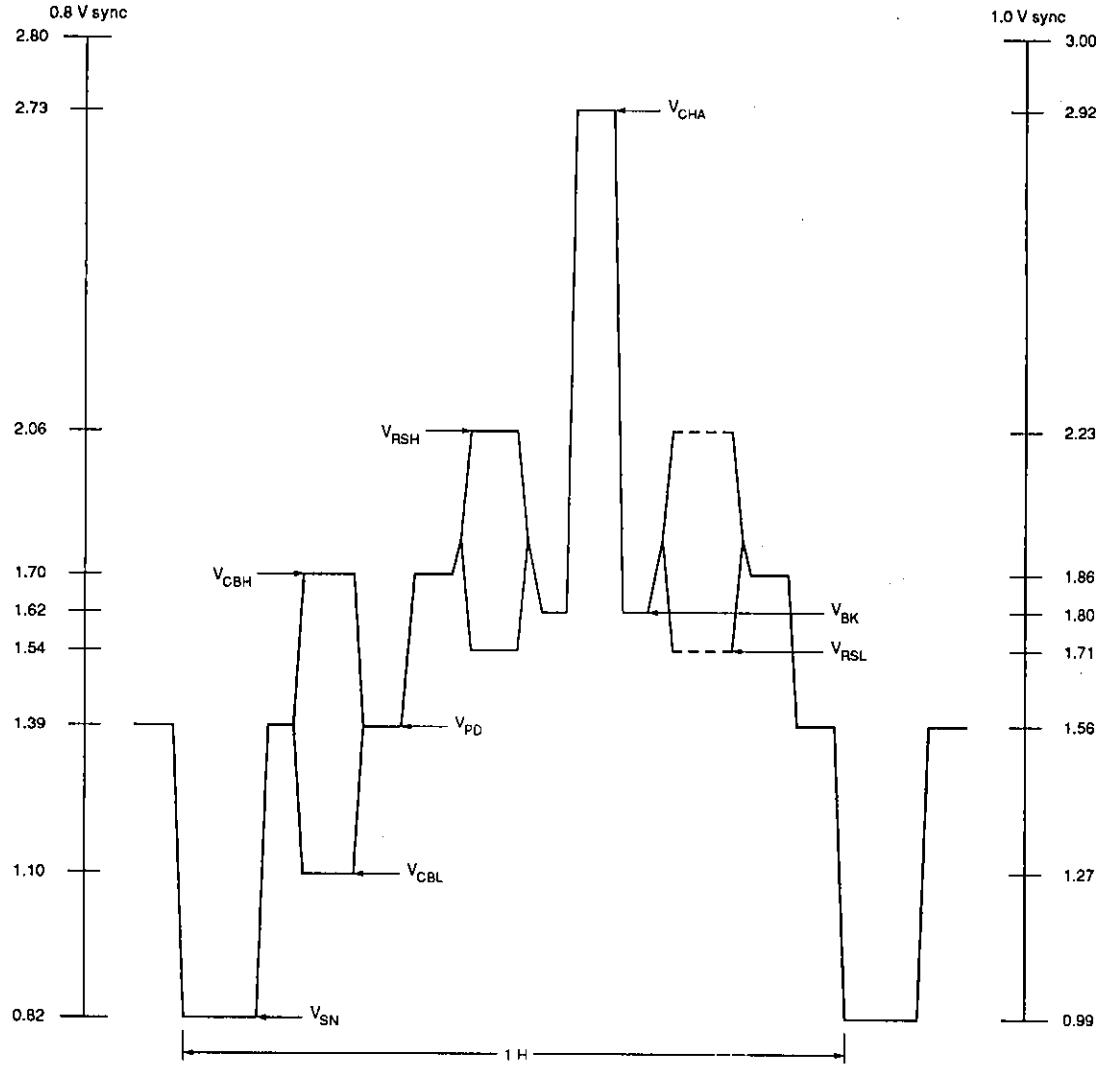
Display Configuration

The display is 24 characters by 10 rows large. Up to 240 characters can be displayed, unless the character size is expanded. The display memory address is set as a row address in the range 0 to 9 and a column address in the range 0 to 23.



Composite Video Output

CVOUT output waveform (V_{DD2} = 5.00 V)



Output voltage level	Symbol	Output voltage at 0.8 V sync (V)	Output voltage at 1.0 V sync (V)
Character	V_{CHA}	2.73	2.92
HIGH-level background color	V_{RSH}	2.06	2.23
HIGH-level color burst	V_{CBH}	1.70	1.86
LOW-level background color	V_{RSL}	1.54	1.71
Border	V_{BK}	1.62	1.80
Pedestal	V_{PD}	1.39	1.56
LOW-level color burst	V_{CBL}	1.10	1.27
Sync	V_{SN}	0.82	0.99

Note

V_{DD2} = 5.00 V