

SPC11A

12KB Sound Controller

Preliminary

JUL. 09, 2001

Version 0.1

Table of Contents

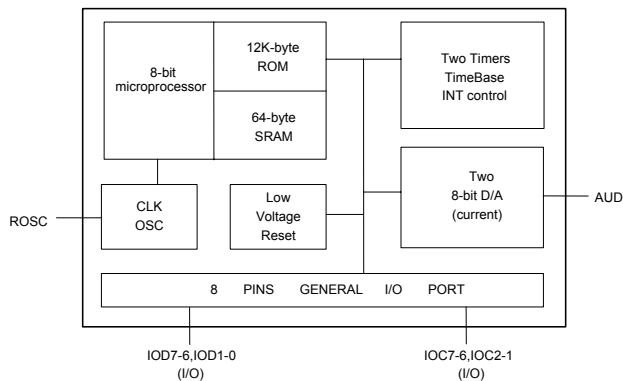
	<u>PAGE</u>
1. GENERAL DESCRIPTION	3
2. BLOCK DIAGRAM	3
3. FEATURES	3
4. APPLICATION FIELD	3
5. SIGNAL DESCRIPTIONS*	4
6. FUNCTIONAL DESCRIPTIONS	5
6.1. CPU	5
6.2. ROM AREA	5
6.3. RAM AREA.....	5
6.4. MAP OF MEMORY AND I/Os	5
6.5. I/O PORT CONFIGURATION*	5
6.6. POWER SAVING MODE	5
6.7. LOW VOLTAGE RESET	6
6.8. TIMER/COUNTER	6
6.9. SPEECH AND MELODY	7
7. ELECTRICAL SPECIFICATIONS	8
7.1. ABSOLUTE MAXIMUM RATINGS	8
7.2. AC CHARACTERISTICS (T _A = 25°C)	8
7.3. DC CHARACTERISTICS (VDD = 3.0V, T _A = 25°C)	8
7.4. DC CHARACTERISTICS (VDD = 5.0V, T _A = 25°C)	8
8. APPLICATION CIRCUITS	9
8.1. APPLICATION CIRCUIT	9
8.2. CURRENT MODE DAC SPEAKER DRIVER	10
9. PACKAGE/PAD LOCATIONS	11
9.1. PAD ASSIGNMENT	11
9.2. ORDERING INFORMATION	11
9.3. PAD LOCATIONS	12
10. DISCLAIMER	13
11. REVISION HISTORY	14

12KB SOUND CONTROLLER

1. GENERAL DESCRIPTION

The SPC11A, a two-channel speech/melody synthesizer, equips an 8-bit CMOS microprocessor with 69 instructions, 12K-byte ROM for speech and melody data (speech compressed by a 4-bit ADPCM with approx. three seconds speech duration @ 6.0KHz sampling rate) and 64-byte working SRAM. Other primary features include two Timer/Counters, 8 Software Selectable I/Os, and one 8-bit current D/A output. In audio processing, melody and speech can be mixed into one output. It operates at a wide voltage range of 2.4V - 5.5V with a Low Voltage Reset function that automatically resets CPU when operating voltage is less than 1.3V/2.7V. Plus, a Clock Stop mode is built in for power savings. The unique power saving mode saves the RAM contents, but freezes the oscillator to stop executing other functions. The maximum CPU frequency can run up to 6.0MHz and the instruction cycle is two clock cycles (min.) ~ six clock cycles (max.). The SPC11A loads, not only the latest technology, but also the full commitment and technical support of Sunplus.

2. BLOCK DIAGRAM



3. FEATURES

- 8-bit microprocessor
- 12K-byte ROM for program and audio data
- 64-byte working SRAM
- Software-based audio processing
- Wide operating voltage: 2.4V - 5.5V @ 4.0MHz
3.6V - 5.5V @ 6.0MHz
- Supports ROSC only
- Max. CPU clock: 4.0MHz @ 3.0V, 6.0MHz @ 5.0V
- Standby mode (Clock Stop mode) for power savings.
Max. 2 μ A @ 5.0V
- 500ns instruction cycle time @ 4.0MHz CPU clock
- Eight general I/Os
- Two 12-bit timer/counters
- Six INT sources
- Key wake-up function
- Approx. 3-sec speech @ 6.0KHz sampling rate with ADPCM
- One D/A output
- Low Voltage Reset

4. APPLICATION FIELD

- Intelligent education toys
Ex. Pattern to voice (animal, car, color, etc.)
Spelling (English or Chinese)
Math
- Advanced toy controller
- General speech synthesizer
- Industrial controller

5. SIGNAL DESCRIPTIONS*

Mnemonic	PIN No.	Type	Description
VDD	9	I	Power input
VSS	10	I	Ground
ROSC	11	I	ROSC Resistor input (Resistor must be connected to VDD)
RESET	13	I	RESET
TEST	12	I	TEST MODE
AUD	14	O	AUDIO OUTPUT
IOC1	8	I/O	Port C is a 4-bit bi-directional programmable Input / Output port with Pull-high or Open-drain option. In input mode, Port C can be in either Pure or Pull-high states. In output mode, Port C can be a Buffer or Open-drain NMOS type (sink current). IOC1: EXT INT IN IOC2: EXT COUNT IN **See note 1 and 2 below.
IOC2	7	I/O	
IOC6	6	I/O	
IOC7	5	I/O	
IOD0	1	I/O	Port D is a 4-bit bi-directional programmable Input / Output port with Pull-low or Open-drain option. In input mode, Port D can be either Pure or Pull-low states. In output mode, Port D can be either Buffer or Open-drain PMOS type (send current). (Key change, Wake up I/O) **See note 1 and 2 below.
IOD1	2	I/O	
IOD6	3	I/O	
IOD7	4	I/O	

* Refer to SPC Programming Guide for more information.

**Note: 1.) Two input states can be specified: Pure Input, Pull-High or Pull Low.

2.) Three output states can be specified: Buffer output, Open Drain PMOS output (send), or Open Drain NMOS output (sink).

6. FUNCTIONAL DESCRIPTIONS

6.1. CPU

The microprocessor in SPC11A is a high performance 8-bit processor equipped Accumulator, Program Counter, X Register, Stack pointer and Processor Status Register (the same as the 6502 instruction structure). The maximum CPU speed of 6.0MHz is capable of bringing you the cleaner speech, pleasant music as well as achieving the best performance.

6.2. ROM Area

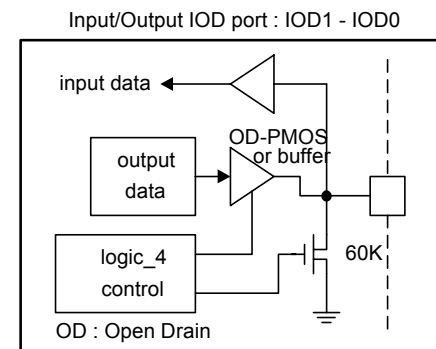
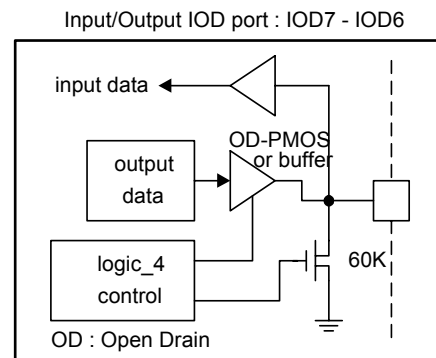
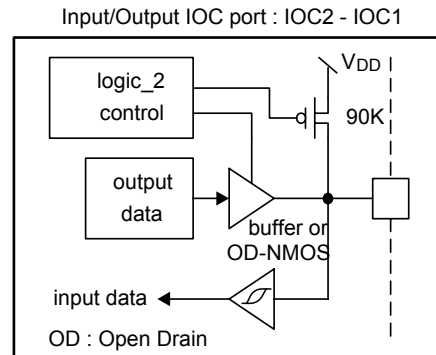
The ROM area in SPC11A is 12K-byte that can be used for program as well as data.

6.3. RAM Area

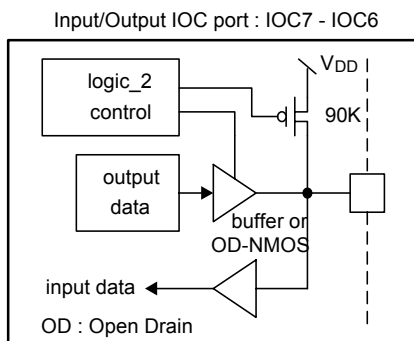
The total RAM size is 64-bytes (including Stack) starting from address \$C0 through \$FF.

6.4. Map of Memory and I/Os

*I/O PORT:	*MEMORY MAP (From ROM view)
- PORT IOC \$0004	\$0000
IOD \$0005	Hardware register, I/Os
- I/O CONFIG \$0000	\$00C0
\$0001	USER RAM and STACK
*NMI SOURCE:	\$0100
- INTA (from TIMER A)	UNUSED
	\$0400
*INT SOURCE:	SUNPLUS TEST PROGRAM
- INTA (from TIMER A)	\$0600
- INTB (from TIMER B)	USER'S PROGRAM & DATA AREA
- CPU CLK / 1024	\$2FFF
- CPU CLK / 8192	DUMMY AREA
- CPU CLK / 65536	\$7C00
- EXT INT	USER'S PROGRAM & DATA AREA
	\$7FFF



6.5. I/O Port Configuration*



Note: * Values are for VDD = 5.0V test conditions only.

6.6. Power Saving Mode

The SPC11A includes a power saving mode (Standby mode) for those applications that require very low standby current. To enter standby mode, the Wake-Up Register must be enabled and then stop the CPU clock by writing the STOP CLOCK Register to enter standby mode. In such mode, RAM and I/Os will remain in their previous states until being awoken. Port IOD(7, 6, 1, 0) is the only wake-up source in the SPC11A. After the SPC11A is awoken, the internal CPU will go to the RESET State ($T_w \geq 65536 \times T_1$) and continue to execute program. Wakeup Reset will not affect RAM nor I/Os (FIG.1).

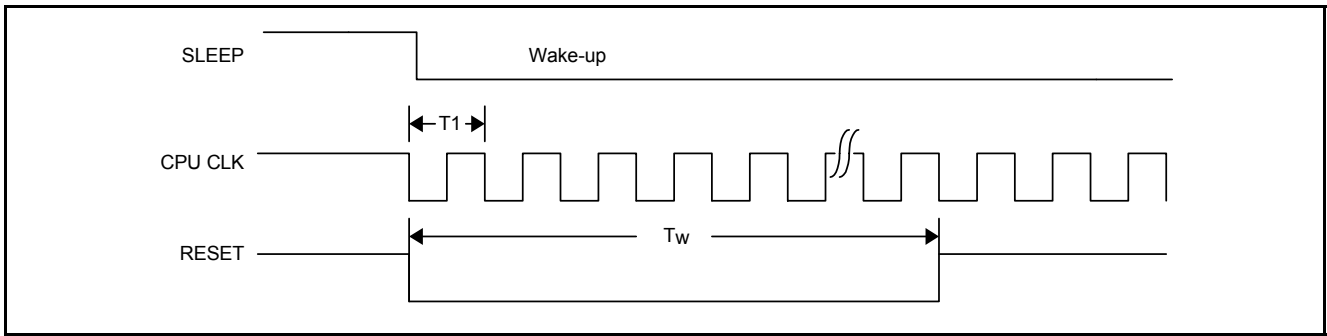


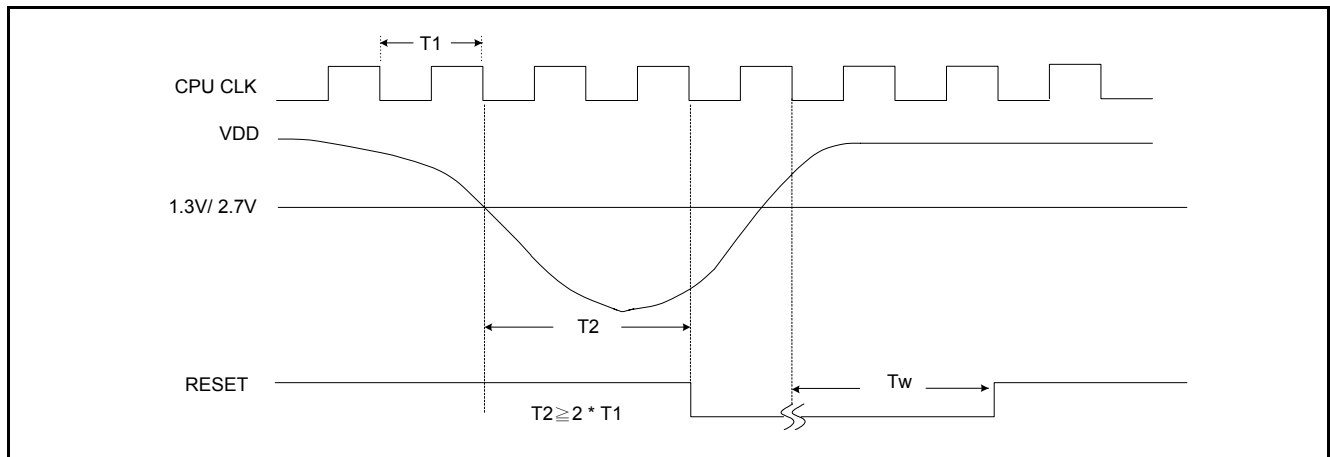
FIG. 1

$$T1 = 1 / (F_{CPU}), Tw \geq 65536 \times T1$$

6.7. Low Voltage Reset

The SPC11A has a Low Voltage Reset (LVR) function. In general, the CPU becomes unstable and malfunctions when the power voltage drops below certain operating voltage. With the unique

design of Low Voltage Reset in SPC11A, it is able to reset all functions to the initial operational (stable) state if the VDD power-supply voltage drops below 1.3V or 2.7V (FIG.2).



(The LVR function is the same as Power ON Reset or External Reset.)

FIG. 2

6.8. Timer/Counter

The SPC11A has two 12-bit timer/counters, TMA and TMB respectively. TMA can be specified as a timer or a counter, but TMB can only be used as a timer. In the timer mode, TMA and TMB are re-loaded up-counters. When timer rollovers from \$0FFF to \$0000, the carry (overflow) signal will make the user's preset value to be loaded into timer automatically and up-count again. At the same time, the carry signal will generate an INT

signal if the corresponding bit is enabled in the INT ENABLE Register. Suppose TMA is specified as a counter, users can reset it by loading #0 into the counter. After the counter has been activated, the value in the counter can also be read at the same time. The read instruction will not affect the value of the counter nor reset it.

Clock source of Timer/Counter can be selected as follows:

Timer/Counter		Clock Source
TMA	12-BIT TIMER	CPU CLOCK (T) or T/4
	12-BIT COUNTER	T/64, T/8192, T/65536 or EXT CLK
TMB	12-BIT TIMER	T or T/4
MODE SELECT REGISTER		TMA only, select timer or counter
TIMER CLOCK SELECTOR		Select T or T/4

6.9. Speech and Melody

Since the SPC11A provides a large ROM and wide range of CPU operating speeds, it is the most suitable device for speech and melody synthesis.

In speech synthesis, the SPC11A can use NMI for accurate sampling frequency. The user can store the speech data in ROM and play it back with realistic sound quality. Several algorithms are recommended for high fidelity and compression of sound: PCM, LOG PCM, and ADPCM.

In melody synthesis, the SPC11A provides a dual tone mode to obtain melodious music. After selecting the dual tone mode, the user only needs to program either TMA or TMB, or both TMA and TMB to generate expected frequency for each channel. The hardware will toggle the tone wave automatically without entering into an interrupt service routine. The user can create musical instruments or sound effects by simply controlling the envelope of tone output.

7. ELECTRICAL SPECIFICATIONS

7.1. Absolute Maximum Ratings

Characteristics	Symbol	Ratings
DC Supply Voltage	V_+	< 7.0V
Input Voltage Range	V_{IN}	-0.5V to $V_+ + 0.5V$
Operating Temperature	T_A	0°C to +60°C
Storage Temperature	T_{STO}	-50°C to +150°C

Note: Stresses beyond those given in the Absolute Maximum Rating table may cause operational errors or damage to the device. For normal operational conditions see AC/DC Electrical Characteristics.

7.2. AC Characteristics ($T_A = 25^\circ\text{C}$)

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
OSC Frequency	F_{OSC2}	-	2.0	4.0	MHz	VDD = 2.4V - 3.6V, for 2-battery
		-	4.0	6.0	MHz	VDD = 3.6V - 5.5V, for 3-battery

7.3. DC Characteristics (VDD = 3.0V, $T_A = 25^\circ\text{C}$)

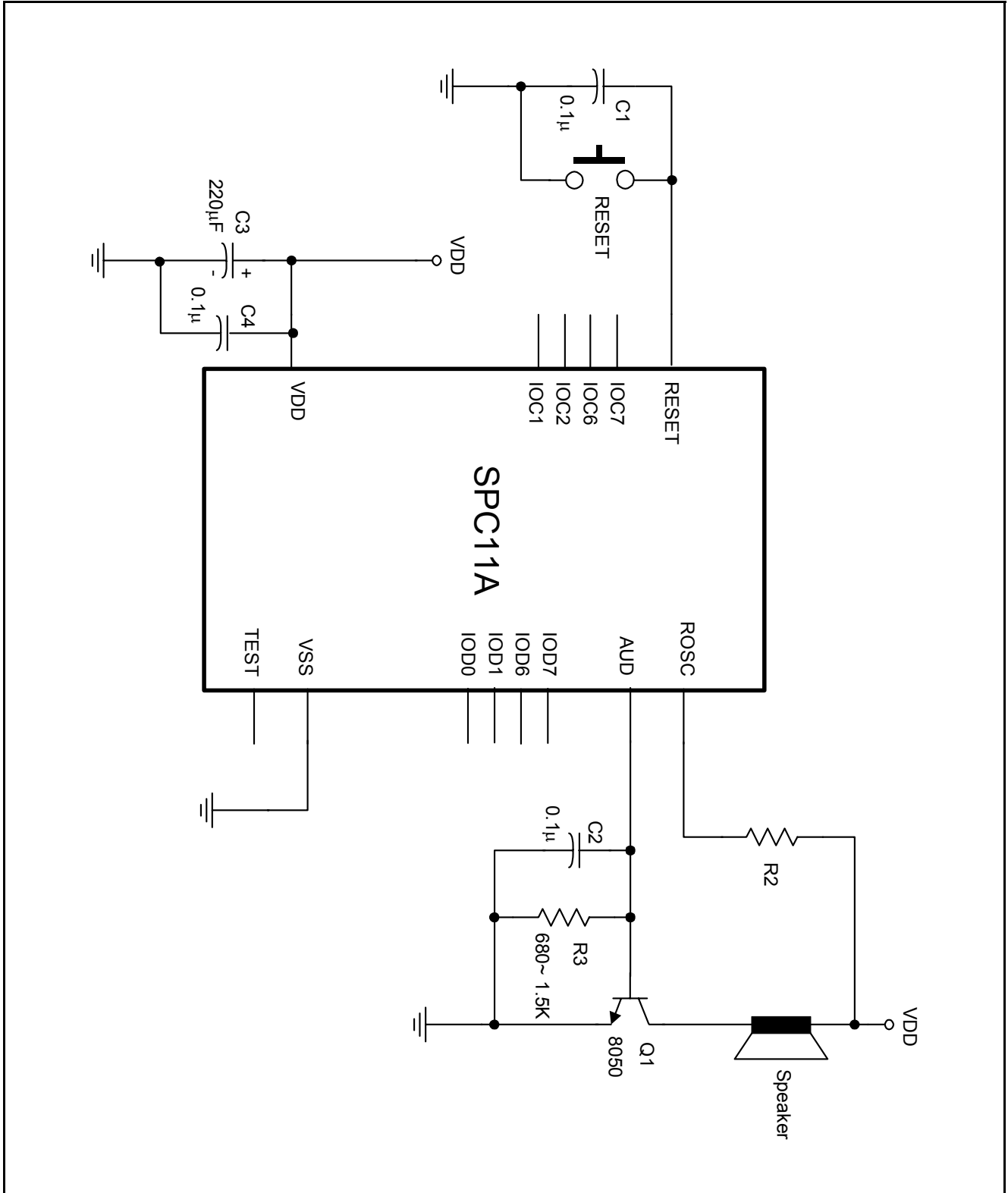
Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
Operating Voltage	VDD	2.4	-	3.6	V	For 2-battery
Operating Current	I_{OP}	-	1.5	2.0	mA	$F_{CPU} = 3.0\text{MHz}$ @ 3.0V, no load
Standby Current	I_{STBY}	-	-	2.0	μA	VDD = 3.0V
Audio output current	I_{AUD}	-	-1.5	-	mA	VDD = 3.0V, one-channel
Input High Level	V_{IH}	2.0	-	-	V	VDD = 3.0V
Input High Level (IOC2-1)	V_{IH}	1.6	-	-	V	VDD = 3.0V
Input Low Level	V_{IL}	-	-	0.8	V	VDD = 3.0V
Input Low Level (IOC2-1)	V_{IL}	-	-	1.1	V	VDD = 3.0V
Output High I (IOC, IOD)	I_{OH}	-1.0	-	-	mA	VDD = 3.0V, $V_{OH} = 2.0V$
Output Sink I (IOC, IOD)	I_{OL}	2.0	-	-	mA	VDD = 3.0V, $V_{OL} = 0.8V$
Input Resistor (IOD)	R_{IN}	-	100	-	Kohm	Pull Low, VDD = 3.0V, $V_{IN} = VDD$

7.4. DC Characteristics (VDD = 5.0V, $T_A = 25^\circ\text{C}$)

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
Operating Voltage	VDD	3.6	-	5.5	V	For 3-battery
Operating Current	I_{OP}	-	4.0	5.0	mA	$F_{CPU} = 4.0\text{MHz}$ @ 5.0V, no load
Standby Current	I_{STBY}	-	-	2.0	μA	VDD = 5.0V
Audio output current	I_{AUD}	-	-3.0	-	mA	VDD = 5.0V, one-channel
Input High Level	V_{IH}	3.0	-	-	V	VDD = 5.0V
Input High Level (IOC2-1)	V_{IH}	2.0	-	-	V	VDD = 5.0V
Input Low Level	V_{IL}	-	-	0.8	V	VDD = 5.0V
Input Low Level (IOC2-1)	V_{IL}	-	-	1.6	V	VDD = 5.0V
Output High I (IOC, IOD)	I_{OH}	-1.0	-	-	mA	VDD = 5.0V, $V_{OH} = 4.2V$
Output Sink I (IOC, IOD)	I_{OL}	4.0	-	-	mA	VDD = 5.0V, $V_{OL} = 0.8V$
Input Resistor (IOD)	R_{IN}	-	60	-	Kohm	Pull Low, VDD = 5.0V, $V_{IN} = VDD$

8. APPLICATION CIRCUITS

8.1. Application Circuit



8.2. Current Mode DAC Speaker Driver

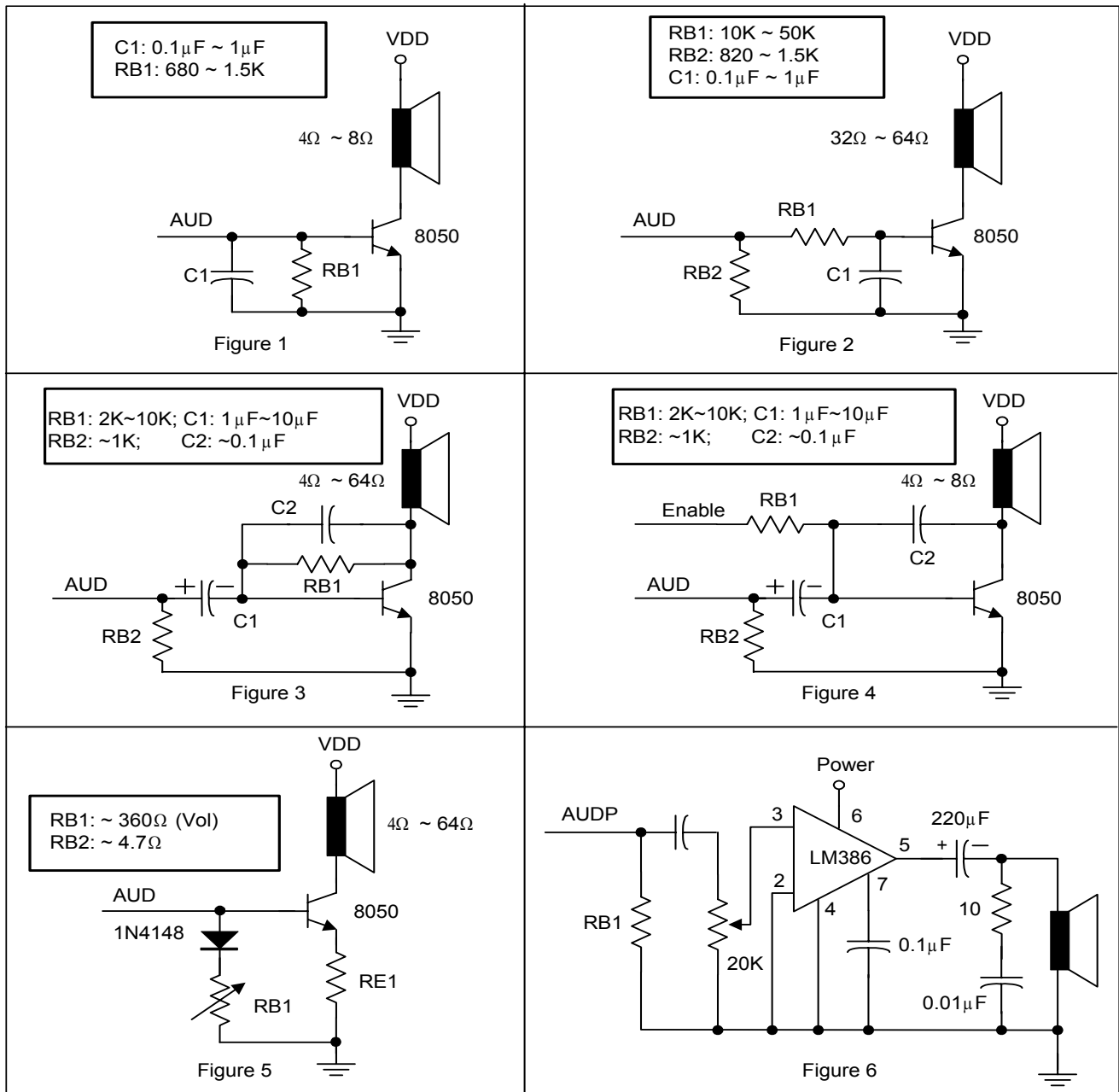


Figure 1: The simplest CKT uses with low impedance speaker. It has high operation current, but low cost.

Figure 2: It is the same as Figure 1 but a high impedance speaker is used.

Figure 3: The CKT contains a low pass filter. It is capable of providing higher speech quality, but it takes higher operation current.

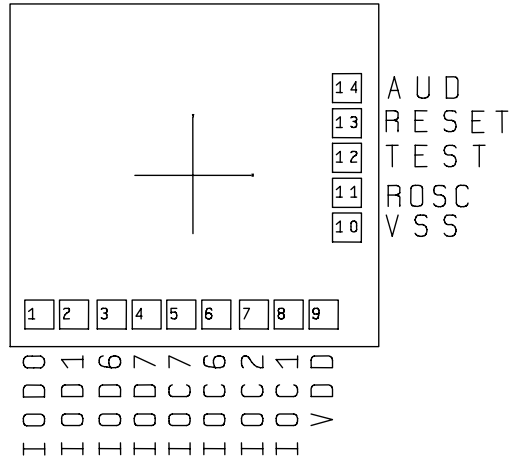
Figure 4: Improved version of Figure 3. The standby current can be controlled by the enable pin.

Figure 5: The current mirror mode. It is able to control the volume. In addition, it is more stable and has lower operation current than Figure 1-3.

Figure 6: High quality, low operation current CKT, but more expensive.

9. PACKAGE/PAD LOCATIONS

9.1. PAD Assignment



Chip Size: 1370 μ m x 1280 μ m

This IC substrate should be connected to VSS

Note1: Chip size included scribe line.

Note2: The 0.1 μ F capacitor between VDD and VSS should be placed to IC as close as possible.

9.2. Ordering Information

Product Number	Package Type
SPC11A-nnnnV-C	Chip form

Note1: Code number (nnnnV) is assigned for customer.

Note2: Code number (nnnn = 0000 - 9999); version (A = A - Z).

9.3. PAD Locations

PAD No.	PAD Name	X	Y
1	IOD0	-535	-479
2	IOD1	-411	-479
3	IOD6	-287	-479
4	IOD7	-163	-479
5	IOC7	-42	-479
6	IOC6	80	-479
7	IOC2	201	-479
8	IOC1	323	-479
9	VDD	443	-479
10	VSS	522	-182
11	ROSC	522	-62
12	TEST	522	58
13	RESET	523	178
14	AUD	522	298

10. DISCLAIMER

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11. REVISION HISTORY

Date	Revision #	Description	Page
JUL. 09, 2001	0.1	Original	14