SPF MIR3 02

Plastic Fiber Optic Receiver including Bigfoot™ IC for MOST®

Preliminary Data Sheet

The data sheet of the 4-pin MOST Optical Receiver (MIR3 02) has to be taken as preliminary. Samples which are delivered before the qualification and the production release are engineering samples.

Features

Excellent solution for converting high speed data from Plastic Optical Fiber (POF) to digital output.

- High speed receiver up to 50 MBaud (25Mbit/s net data rate)
- TTL Data Output (Light to Logic Function)
- Network activity sensing during ZeroPower Mode (I_{CC}<10µA)
- BUS Activity Status Output
- Good 650nm sensitivity for working in a low attenuation range of PMMA Fiber
- Low cost

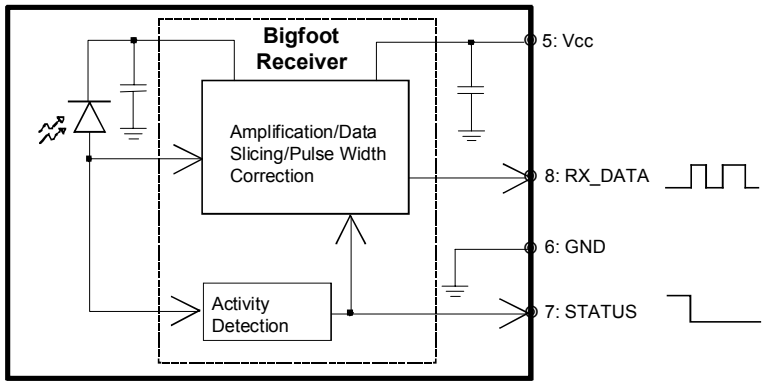
Applications

- Optical Receiver for MOST Systems

Description

The 4-pin MOST Optical Receiver (MIR3 02) is a highly integrated CMOS IC (Bigfoot™) combined with a high speed PIN - diode designed to receive up to 25Mbit/s optical data which is bi-phase coded at up to 50Mbaud and convert this optical data to a TTL compatible data stream.
This high performance, low cost, CMOS receiver consists of a low noise transimpedance amplifier and comparator in the data path. A timer circuit puts the part into a low power mode if optical data is not received for 10µs (typ.). During the low power mode, the PIN diode is still being observed and if activity is detected, Bigfoot will resume full power operation within 3.5ms (typ.).
A STATUS-pin indicates if modulated light is received (Light on -> STATUS = low). With the STATUS-pin the power supply of the whole MOST device can be switched ON.

SPF MIR3 02



Actual design status:

Bigfoot IC Revision	package type	Optical Sensitivity	device marking	Data sheet is valid since
J	CAI	-24.5 dBm	date code, MIR3 02	2-Dec-02

Maximum Ratings

Parameter	Symbol	Min	Max	Unit
Storage Temperature Range	T_{STG}	-40	100	°C
Junction Temperature	T_J	-40	100	°C
Soldering Temperature (>2.5 mm from case bottom t≤5s)	T_S	-	235	°C
Power Dissipation	P_{TOT}	-	300	mW
Power Supply Voltage	V_{CCMax}	-0.5	6.0	V
DC Current To Any Pin Except Power	$I_{I/OMax}$	-	±10	mA

Recommended Operating Conditions

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V_{CC}	4.75	5.25	V
Operating Temperature Range	T_A	-40	85	°C

All the data in this specification refers to the operating conditions above, unless otherwise stated.

Optical Signal Characteristics (22.5 MBit MOST Data)

Parameter	Symbol	Min	Typ	Max	Unit
Maximum Photosensitivity Wavelength (T_A=25°C)	λ_{Smax}	-	850	-	nm
Photosensitivity Spectral Range (T_A=25°C) (S ≥ 10% S_{max})	λ	400	-	1100	nm
Optical Sensitivity *1) *2) *3)	S	-24.5	-	-	dBm
Optical overload *1) *2) *3)	P_{max}	-2	-	-	dBm
Optical receivable power for low power mode *1)	P_{OFF}	-	-	-40	dBm

*1) Optical power data are average values when using a MOST optical transmitter with λ_{peak} of 650 nm typical and measured at the end of a plastic optical fiber with metal insert.

*2) It is proposed to use the OptoLyzer4MOST, MOST Optical Network Analyzer, described in: http://www.oasis.de (with MOST Data @44.1KHz FS) or Standard BER Measuring Equipment running with 45 MBaud (BER≤ 10^{-9} with 2^7-1 word length).

*3) The values are determined by locking a OS8104 in Slave-mode to the signal.

DC Characteristics

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
Supply Voltage		V_{CC}	4.75	5.0	5.25	V
Low Level Output Voltage	I_{OL} = 2.4mA	V_{OL}	-	-	0.4	V
High Level Output Voltage	I_{OH} = 2.4mA	V_{OH}	V_{CC}-1.0	-	-	V
Supply Current	Full power mode Low power mode	I_{CC}	-	18.5 5	22 10	mA µA

AC Electrical Characteristics

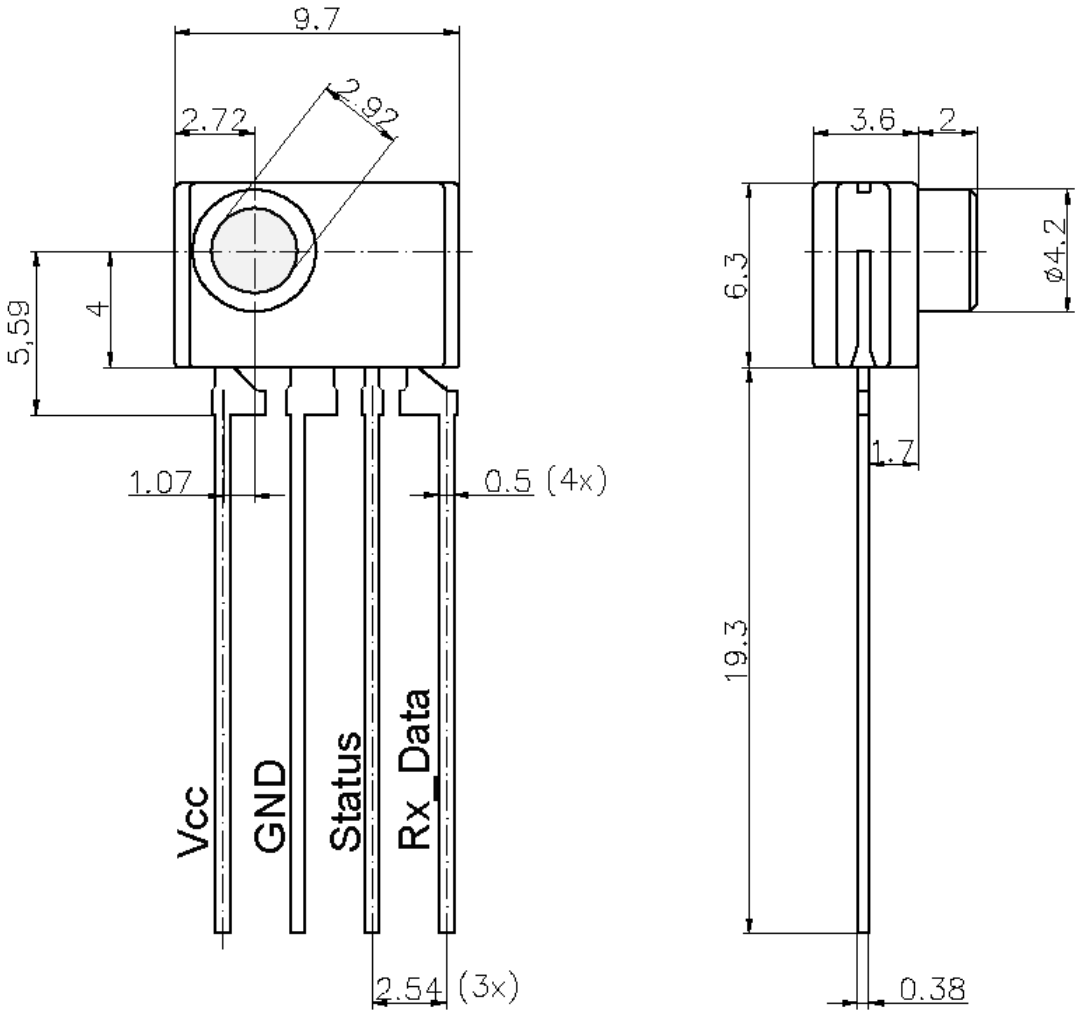
Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
Power Supply Rejection Ratio	25 MHz Power Supply Noise	PSRR	-	30	-	dB
Output Rise Time	C_L=10pF *1)	t_r	-	7.5	9	ns
Output Fall Time	C_L=10pF *1)	t_f	-	6	7	ns
Output Pulse Width Variation *2)	MOST Data 44.1 kHz FS (-2...-24.5dBm)	t_{PWV}	15.5	-	32.8	ns
Output Average Pulse Width Distortion *2)	MOST Data 44.1 kHz FS (-2...-24.5dBm)	t_{APWD}	0	-	8	ns
Power-up time at detection of rising V_{CC}	When part first powers up	t_{PUO}	-	3.5	17	ms
Power-up time from low power mode *3)		t_{PU}	-	2.5	12	ms
Low Power mode timer delay	Time from detection of inactivity to low power mode	T_{LPM}	-	10	22	µs

*1) With C_L = 25pF, the rise/ fall increases to about 12 ns. Therefore, keep the distance from Bigfoot to the MOST – chip as short as possible for keeping C_L low.

*2) MOST Data 44.1KHz FS corresponds to a 45 MBaud data stream.
Since the Bigfoot transmitter is used as optical source, this is the link PWV/APWD which appears from node to node. Optical power data are average values when using a MOST optical transmitter with λ_{peak} of 650 nm typical and measured at the end of a plastic optical fiber with metal insert.

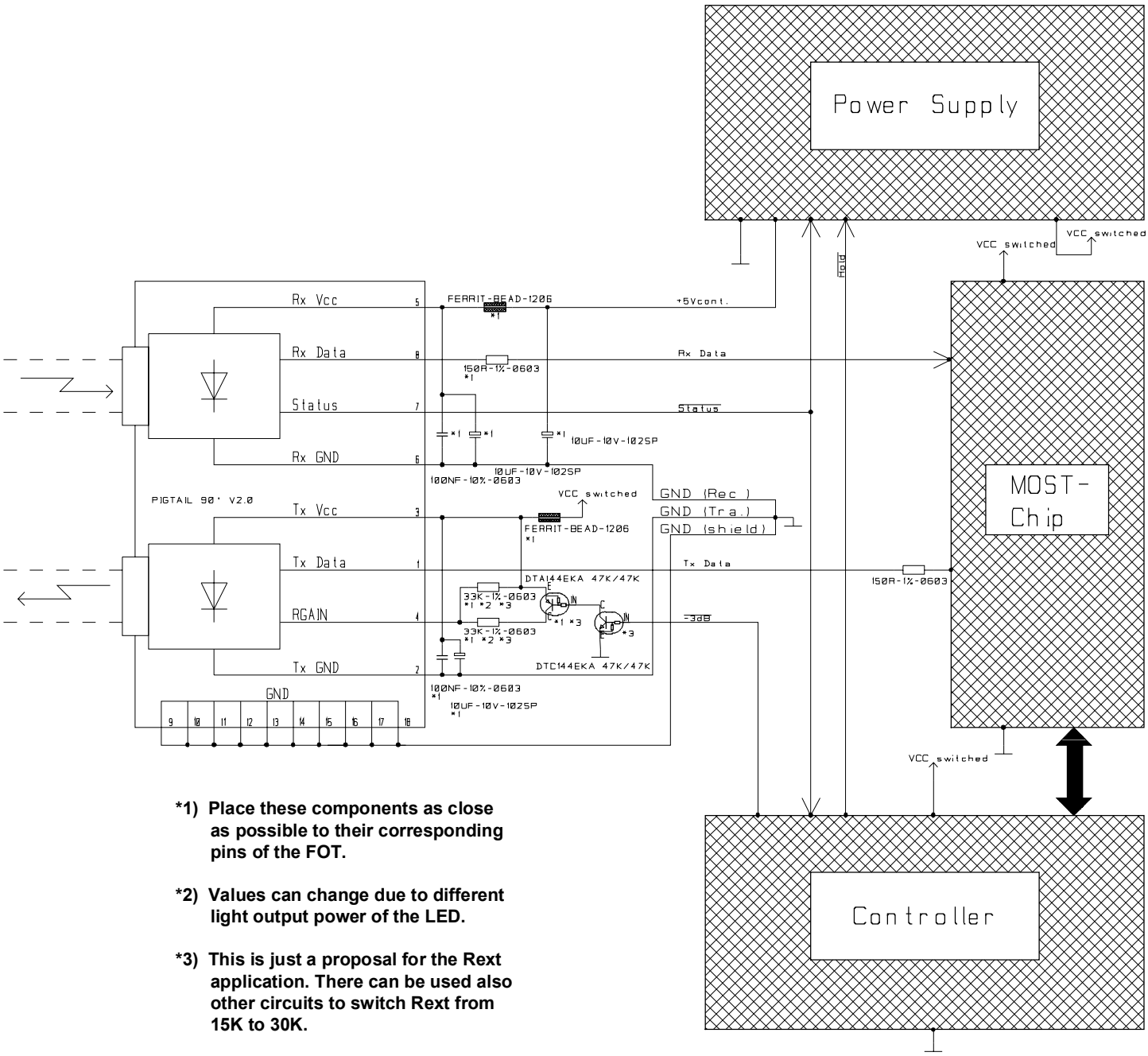
*3) Any receiving circuitry receiving data from RX_DATA must be powered within 50ms after /STATUS gets active. There must be a protective resistor of 50Ohm (minimum) between RX_DATA and the receiving circuitry. A typical value for this resistor is 150Ohm.

Mechanical Design MIR3 02: CAI package (cavity as interface)



Lot number, production week, component type are given on CAI backside by laser marking (for details see marking specification).

Application Circuit:



***1) Place these components as close as possible to their corresponding pins of the FOT.**

***2) Values can change due to different light output power of the LED.**

***3) This is just a proposal for the Rext application. There can be used also other circuits to switch Rext from 15K to 30K.**

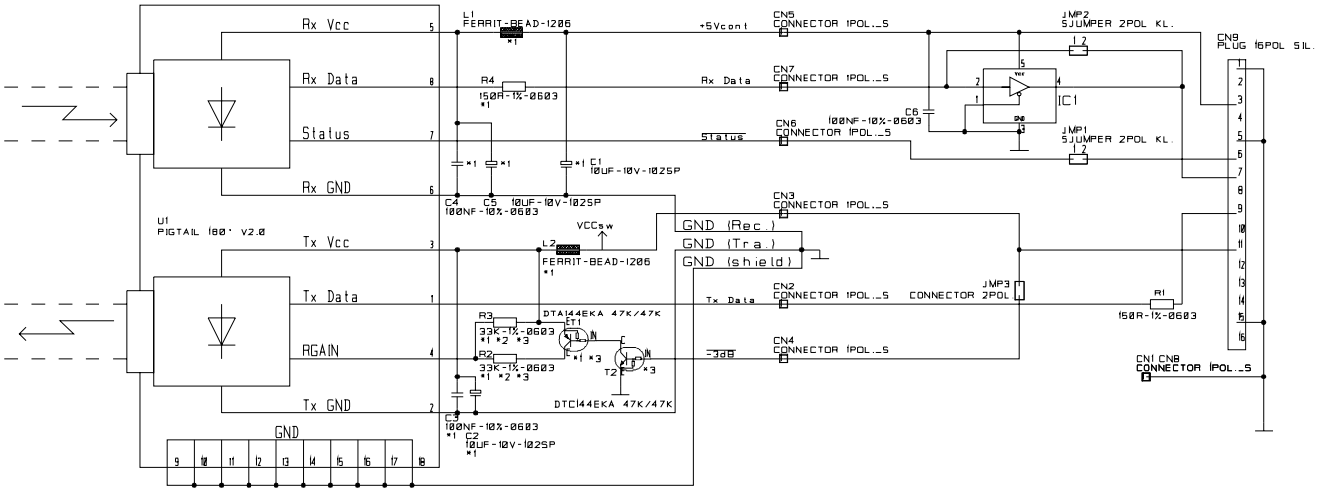
Design & Layout rules:

- The 100nF bypass capacitors of the FOTs must be located as close as possible between the pins V_{CC} and GND of the FOTs. Use ceramic caps and tantalum caps with low ESR.
- Also the inductor/ ferrite bead (receiver) and the -3dB - control circuit (transmitter) must be placed as close as possible to the FOTs. We prefer ferrite beads (e.g. type 74279214 Würth Elektronik) since the D.C. resistance is very low. In case other inductors are used, the D.C. resistance should be less than 3Ohm.
- For EMC, a ferrite bead should be connected to the power supply, close to the transmitter and the receiver. Do not use only one ferrite bead together for receiver and transmitter!

- For the ground connection a ground plane is recommended (Y-structure). That means the ground planes of the transmitter, the receiver and the shielding must be separated. The three ground planes should be connected together behind the bypass capacitors (refer to the PCB design below). This ground signal should be connected directly to the ground plane of the MOST controller (e.g. OS8104) and the power supply on the top layer and/or bottom layer and ground layer as it is indicated in the example below.
- If a multi layer design is used the ground layer must have the same ground separation like shown for the top layer!
- A serial resistor in the Rx/ Tx data line will also reduce EMC - problems. For Rx the resistor must be placed near the receiver - for Tx the resistor must be placed near the MOST controller chip. The value depends on the distance between the FOTs and the MOST chip (< 5cm) and can be within a range up to 150R. Higher values for the resistors will increase jitter and can therefore cause locking problems of the MOST PLL!
- The Rx/ Tx signals should not be routed in parallel over a long distance, but may be embedded with ground copper, if possible.
- The GND pin and the pin of R_{ext} (15K - resistor) of the transmitter are used for heat dissipation. Therefore there should be a good connection to the PCB → no isolation gaps! Both pins should dip into a copper area (see layout example below).

Layout example:

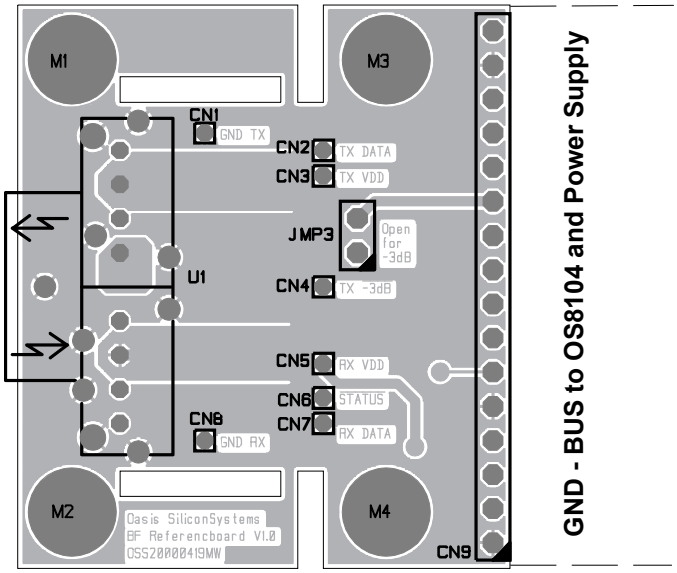
The reference board from OASIS Silicon Systems follows the requirements above. The schematic is very similar to the example above, but does not include the connection to the power supply, the OS8104 or the micro controller.



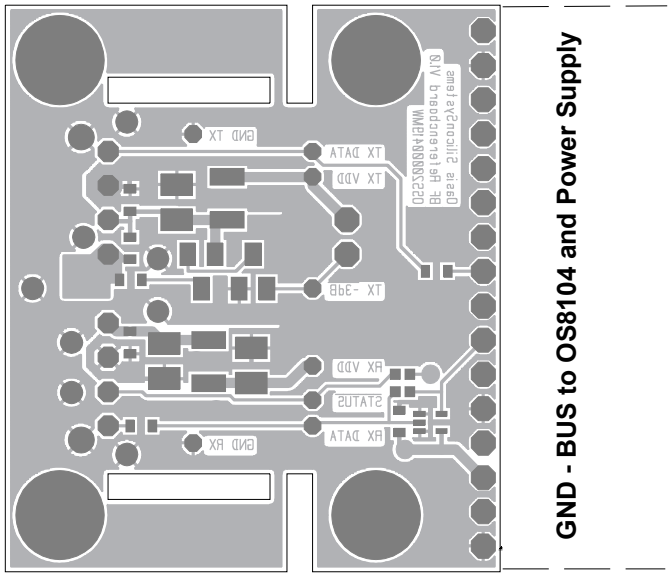
The examples below for top- and bottom layer is the layout of the reference design board and shows how the layout around the optical receiver and transmitter should look like.
It is strongly recommended to follow these examples in your design to get best performance!

Note:
The buffer circuit (IC1), the connectors and jumpers in the middle to the right section of the schematic are only for being used together with the reference board, and will not be necessary for your hardware design.

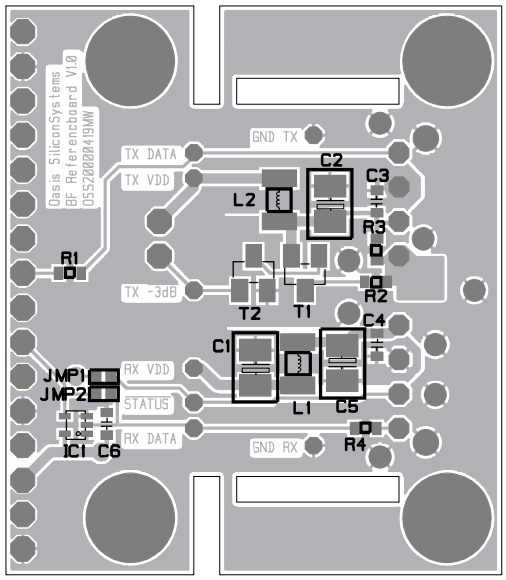
Top Layer with 180° version of the pigtail:



Bottom Layer (seen from the top side of the PCB):



Bottom Layer: Bottom side / positions



Other items:

- The shown circuit for the –3dB attenuation is just a proposal. Also any other circuit which can double the value of R_{ext} is permitted.

- **Due to the fact that the optical average level jumps if the power control signal (/-3dB) is toggled, LOCK/ coding – errors can occur at the subsequent device for a short time.** This is not very critical, since it occurs only in diagnosis mode. After a time of 10ms, the device should lock again if the optical attenuation between the devices is not too high.

- The Rx and Tx signals can be measured by using standard probes (>1M/<10pF). However, if the signal quality is very bad, and the LOCK signal of the MOST chip is flaky, connecting a passive probe to the Rx signal can cause the MOST chip to lock better or worse to the signal. This is due to the capacitance of the analog probe which is usually in the range of 8..12pF, which shifts the phase and PWD of the signal. In this case an active probe with a capacitance of less than 1pF is recommended.

- The reference test board which corresponds to the layout examples above, is available at the Oasis SiliconSystems AG.

History of Design and Specification Status of MOST Receiver:

Data Sheet Status	Bigfoot IC Revision	device marking	comments, cause of change, important differences to last Status
2-Dec-02	J	date code, MIR3 02	New release

Notes: