

# Z90219/213/212/211/218

# Z8<sup>®</sup> DIGITAL TELEVISION CONTROLLERS

#### **FEATURES**

Device	ROM (KB)	RAM* (Bytes)	I/O Lines	Voltage Range
Z90211	16 (OTP)	237	20	4.5V to 5.5V
Z90218	8	237	20	4.5V to 5.5V
Z90212	12	237	20	4.5V to 5.5V
Z90213	16	237	20	4.5V to 5.5V
Z90219	32 (ext.)	237	N/A	4.5V to 5.5V

Note: OTP and Z9021x products under development

Z8-Based CMOS Microcontroller for Consumer Television, Cable Box, and Satellite Receiver Applications.

- 42-Pin SDIP Package
- Z8<sup>®</sup> Microcontroller Core at 6 MHz
- Mask ROM sizes Available in 8, 12 and 16 Kbytes
- Eleven Pulse Width Modulators

#### ■ On-Chip Infrared (IR) Capture Registers

- Four Channel 3-bit Analog-to-Digital Converter
- Twenty General Purpose I/O Pins
- I<sup>2</sup>C Serial Communication Port)

#### On Screen Display (OSD) Section

- Supports Displays up to 10 rows by 24 Columns with 256 Characters
- Character Cell Resolution of 14 Pixels by 18 Scan lines
- Variable Inter-row Spacing from 0-15 Horizontal Scan Lines
- Foreground and Background Colors Fully Programmable by Character

#### **GENERAL DESCRIPTION**

The Z9021x Digital Television Controller (DTC) family is Zilog's latest and most powerful Z8-based DTC product offering. These parts feature larger system RAM and ROM options, together with a host of new features including a new color palette system, flexible inter-row spacing, higher character cell resolution, background mesh effect, dedicated I.R. capture registers, on-chip Analog-to-Digital conversion, and a hardware Master mode I<sup>2</sup>C interface. The familiar Z8 core in combination with these advanced features makes the Z9021x family an ideal choice for low to midrange televisions in both PAL and NTSC markets.

The Z9021x family consists of two basic device types; Z9020x and Z9021x. The only difference between the two types is the presence of a hardware I<sup>2</sup>C serial communication port and half-tone OSD circuitry on the Z9021x family. Of course I<sup>2</sup>C communication is supported on the Z9020x family in software with the dedication of any two I/O pins to the task.

The Z9021x family takes full advantage of the Z8's expanded register file space to offer greater flexibility in On Screen Display creation.

#### **BLOCK DIAGRAM**

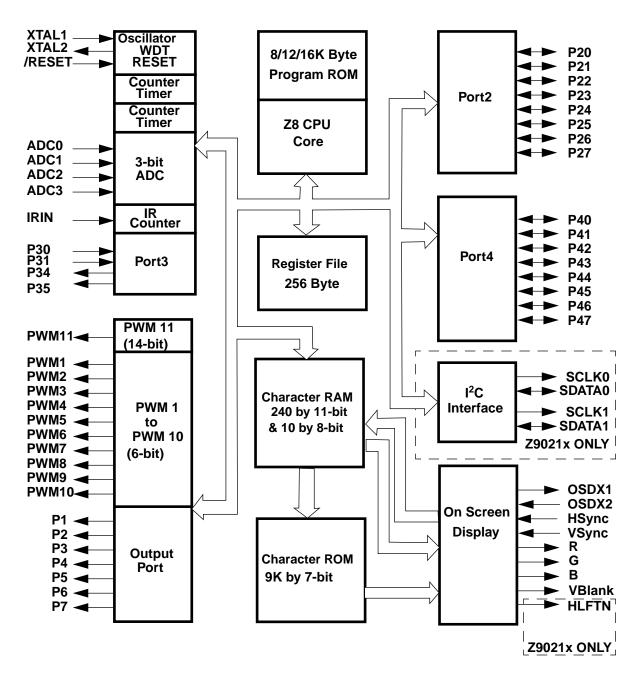
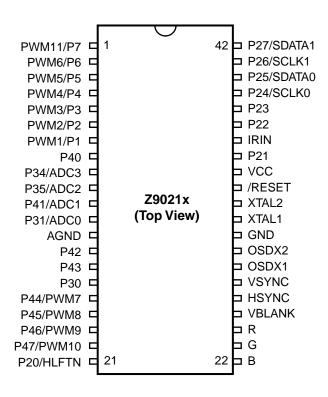


Figure 1. Functional Block Diagram

#### PIN IDENTIFICATION



# PIN IDENTIFICATION

Table 1. Z9021x 42L SDIP Package

Pin Function	Pin Number	I/O/PWR	Reset State	Name
+5 Volts	34	PWR	PWR	VCC
0 Volts	30,13	PWR	PWR	GND,AGND
Infra Red remote capture inpu	ıt 36	I	1	IRIN
14-bit Pulse Width Modulator output	1	0	0	PWM11
6-bit Pulse Width Modulator output	20,19,18,17,2,3,4, 5,6,7	0	0	PWM[10:1]
Fixed output ports	7,6,5,4,3,2,1	0	0	P[1:7]
Bit programmable Input/Output ports	42,41,40,39,38,37 35,21	, I/O	I	P2[7:0]
Half tone output	21	0	I	HLFTN
I <sup>2</sup> C Data	40,42	I/O	I	SDATA0,1
I <sup>2</sup> C Clock	39,41	0	I	SCLK0,1
Fixed output ports	10,9	0	0	P3[5:4]
Fixed input ports	12,16	I	1	P3[1:0]
Bit programmable Input/Output ports	20,19,18,17,15,14 11,8	, I/O	I	P4[7:0]
Crystal oscillator input	31	1	1	XTAL1
Crystal oscillator output	32	0	0	XTAL2
Dot clock oscillator input	28	1	1	OSDX1
Dot clock oscillator output	29	0	0	OSDX2
Horizontal Sync	26	I	1	HSYNC
Vertical Sync	27	I	I	VSYNC
Video blank	25	0	0	VBLANK
Video R,G,B	24,23,22	0	0	R,G,B
3-bit Analog to Digital converter input	9,10,11,12	Al	I	ADC[3:0]
Device reset	33		1	/RESET

#### **ABSOLUTE MAXIMUM RATINGS**

Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; operation of the device at any condition above those indicated in the operational sec-

tions of these specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability

Table 2.

Symbol	<b>Parameters</b>	Min	Max	Units	Notes
V <sub>cc</sub>	Power Supply Voltage	-0.3	+7	V	
V <sub>i</sub>	Input Voltage	-0.3	V <sub>cc</sub> +0.3	V	
$V_{o}$	Output Voltage	-0.3	V <sub>cc</sub> +0.3	V	
l <sub>oh</sub>	Output Current High		-10	mA	per pin
I <sub>oh</sub>	Output Current High		-100	mA	per device
I <sub>ol</sub>	Output Current Low		20	mA	per pin
I <sub>ol</sub>	Output Current Low		200	mA	per device
T <sub>a</sub>	Operating Temperature	0	70	°C	
T <sub>STG</sub>	Operating Temperature	-55	150	°C	

# **DC CHARACTERISTICS**

 $T_A = 0^{\circ}\text{C} \text{ to } + 70^{\circ}\text{C}; V_{CC} = +4.5\text{V to } +5.5\text{V}; F_{OSC} = 6\text{MHz}$ 

Table 3.

Symbol	Parameter	Min	Typical	Max	Units	Conditions
V <sub>cc</sub>	Power Supply Voltage	4.75	5.00	5.25	V	
$\overline{V_{ih}}$	Input Voltage High	0.7V <sub>cc</sub>	3.0	V <sub>cc</sub>	V	
$V_{il}$	Input Voltage Low	0	1.48	0.2V <sub>cc</sub>	V	
V <sub>ihc</sub>	Input XTAL/Osc in High	0.8V <sub>cc</sub>	3.2	V <sub>cc</sub>	V	
V <sub>ilc</sub>	Input XTAL/Osc In Low		0.98	0.07V <sub>cc</sub>	V	
V <sub>oh</sub>	Output Voltage High	V <sub>cc</sub> -0.4	4.75		V	I <sub>oh</sub> =-0.75mA
V <sub>ol</sub>	Output Voltage Low		0.16	0.4	V	I <sub>ol</sub> =1.00mA
$\overline{V_{hy}}$	Schmitt Hysteresis	0.1V <sub>cc</sub>	0.8		V	
I <sub>ir</sub>	Reset Input Current		-46	-80	uA	V <sub>ri</sub> =0V
l <sub>il</sub>	Input Leakage	-3.0	0.01	3.0	uA	0V,V <sub>cc</sub>
I <sub>ol</sub>	Tri-State Leakage	-3.0	0.02	3.0	uA	0V,V <sub>cc</sub>
$\overline{I_{cc}}$	Supply Current		13.2	20	mA	All inputs at rail;outputs floating
I <sub>cc1</sub>	Sleep Mode Current		3.2	6	mA	All inputs at rail;outputs floating
I <sub>cc2</sub>	Stop Mode Curren	t	0.1	10	uA	All inputs at rail;outputs floating

**Note:** Typical values measured at 25°C. Minimum and Maximum values given from 0°C to 70°C.

# **AC CHARACTERISTICS**

Table 4.

Symbol	Parameter	Min	Max	Unit
T <sub>p</sub> C	Input clock period	166	1000	ns
$T_rC, T_fC$	Clock input raise and fall		25	ns
T <sub>w</sub> C	Input clock width	35		ns
$T_wT_{in}L$	Timer input low width	70		ns
$T_wT_{in}H$	Timer input high width	3T <sub>p</sub> C		
$T_pT_{in}$	Timer input period	8T <sub>p</sub> C		
$T_rT_{in}, T_rT_{in}$	Timer input raise and fall		100	ns
T <sub>w</sub> IL	Int request input low	70		ns
T <sub>w</sub> IH	Int request input high	3T <sub>p</sub> C		
T <sub>d</sub> POR	Power-On reset delay	25	100	ms
T <sub>d</sub> LVIRES	Low voltage detect to internal RESET condition	200		ns
T <sub>w</sub> RES	Reset minimum width	5T <sub>p</sub> C		
$T_dH_sOI$	H <sub>sync</sub> start to V <sub>osc</sub> stop	2T <sub>p</sub> V	3T <sub>p</sub> V	
T <sub>d</sub> H <sub>s</sub> Oh	H <sub>sync</sub> start to V <sub>osc</sub> start		1T <sub>p</sub> V	
	$T_{r}C, T_{f}C$ $T_{w}C$ $T_{w}T_{in}L$ $T_{p}T_{in}$ $T_{r}T_{in}, T_{r}T_{in}$ $T_{w}IL$ $T_{w}IH$ $T_{d}POR$ $T_{d}LVIRES$ $T_{d}H_{s}OI$	$\begin{array}{cccc} T_rC, T_fC & Clock input raise and fall \\ T_wC & Input clock width \\ T_wT_{in}L & Timer input low width \\ T_pT_{in}H & Timer input high width \\ T_pT_{in} & Timer input period \\ T_rT_{in}, T_rT_{in} & Timer input raise and fall \\ T_wIL & Int request input low \\ T_wIH & Int request input high \\ T_dPOR & Power-On reset delay \\ T_dLVIRES & Low voltage detect to internal RESET condition \\ T_wRES & Reset minimum width \\ T_dH_sOI & H_{sync} start to V_{osc} stop \\ \end{array}$	$\begin{array}{cccccccccccccccccccccccccccccccccccc$	$\begin{array}{cccccccccccccccccccccccccccccccccccc$

# **AC TIMING DIAGRAMS**

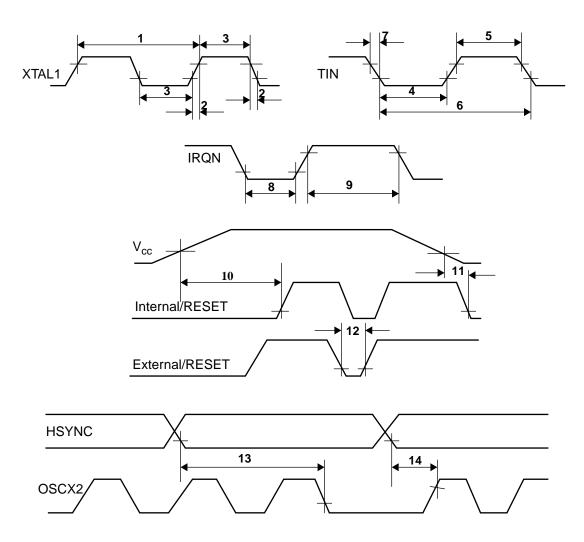


Figure 2. Timing Diagram

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