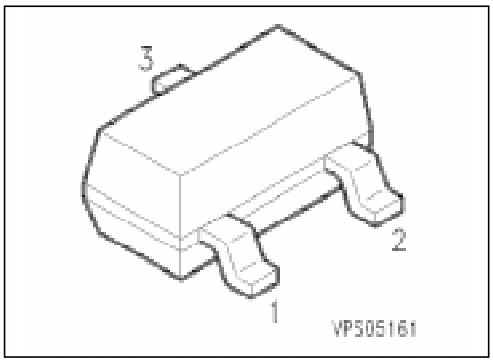
SIEMENS

PNP Silicon Darlington Transistors

SMBTA 63
SMBTA 64

- High collector current
- High DC current gain



Type	Marking	Ordering Code (tape and reel)	Pin Configuration 1	2	3	Package[1]
SMBTA 63 SMBTA 64	s2U s2V	Q68000-A2625 Q68000-A2485	B	E	C	SOT-23

Maximum Ratings

Parameter	Symbol	Values SMBTA 63	SMBTA 64	Unit
Collector-emitter voltage	V_{CE0}	30	30	V
Collector-base voltage	V_{CB0}	30	30	
Emitter-base voltage	V_{EB0}	10	10	
Collector current	I_C	500		mA
Peak collector current	I_{CM}	800		
Base current	I_B	100		
Peak base current	I_{BM}	200		
Total power dissipation, $T_S = 81$ °C	P_{tot}	360		mW
Junction temperature	T_j	150		°C
Storage temperature range	T_{stg}	– 65 … + 150		

Thermal Resistance

Junction - ambient[2]	$R_{th\ JA}$	≤ 280	K/W
Junction - soldering point	$R_{th\ JS}$	≤ 210	

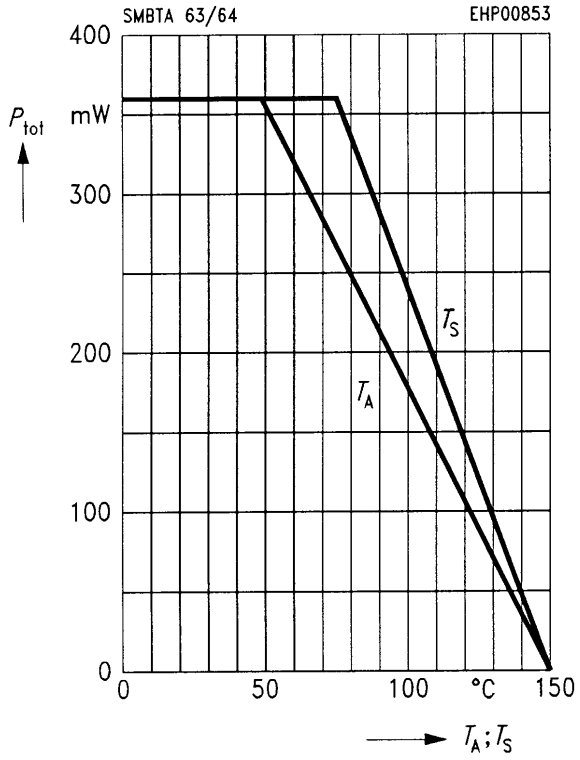
1) For detailed information see chapter Package Outlines.
2) Package mounted on epoxy pcb 40 mm × 40 mm × 1.5 mm/6 cm² Cu.

Electrical Characteristics
at T_A = 25 °C, unless otherwise specified.

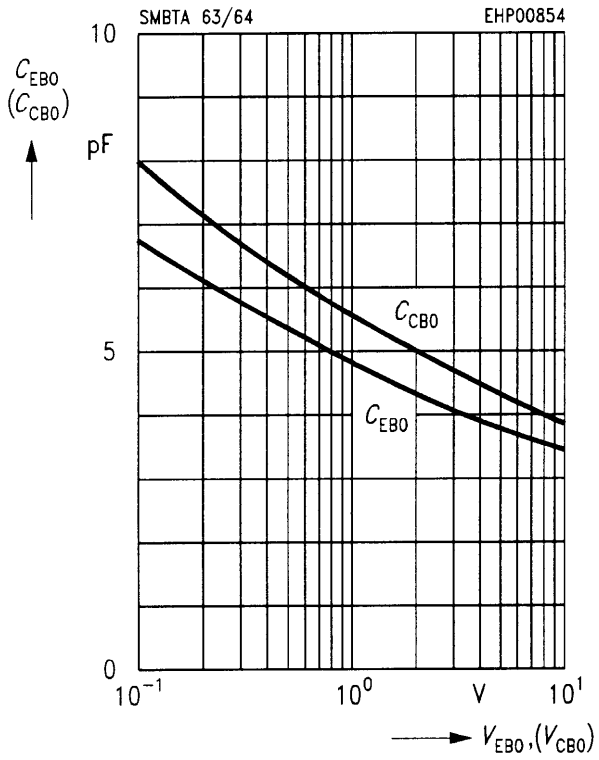
Parameter	Symbol	Values			Unit
		min.	typ.	max.	
DC characteristics					
Collector-emitter breakdown voltage I_C = 10 µA	$V_{(BR)CE0}$	30	–	–	V
Collector-base breakdown voltage I_C = 10 µA	$V_{(BR)CB0}$	30	–	–	
Emitter-base breakdown voltage I_E = 10 µA	$V_{(BR)EB0}$	10	–	–	
Collector-base cutoff current V_{CB} = 30 V	I_{CB0}	–	–	100	nA
Emitter cutoff current V_{EB} = 10 V	I_{EB0}	–	–	100	
DC current gain[1)] I_C = 10 mA, V_{CE} = 5 V SMBTA 63 SMBTA 64 I_C = 100 mA, V_{CE} = 5 V SMBTA 63 SMBTA 64	h_{FE}	 5000 10000 10000 20000	 – – – –	 – – – –	–
Collector-emitter saturation voltage[1)] I_C = 100 mA, I_B = 0.1 mA	V_{CEsat}	–	–	1.5	V
Base-emitter saturation voltage[1)] I_C = 100 mA, I_B = 0.1 mA	V_{BEsat}	–	–	2	
AC characteristics					
Transition frequency I_C = 50 mA, V_{CE} = 5 V, f = 20 MHz	f_T	125	–	–	MHz

1) Pulse test conditions: $t \leq 300$ µs, $D = 2$ %.

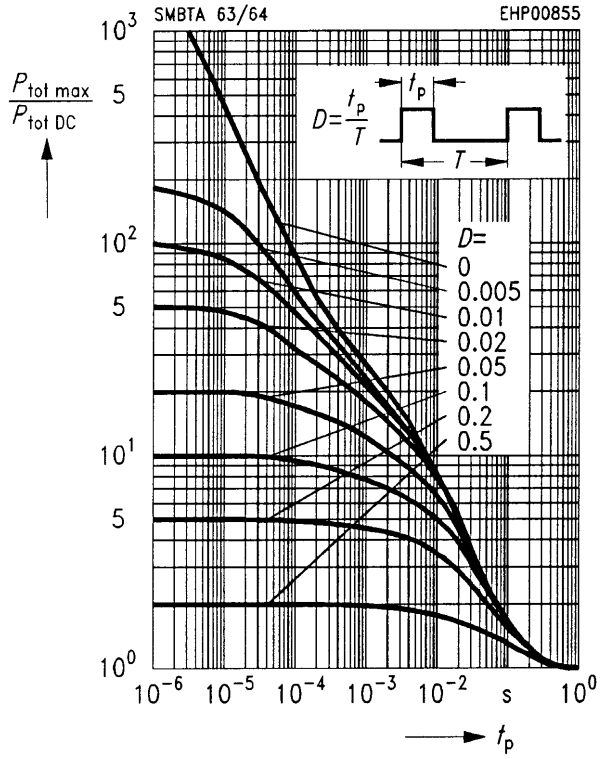
Total power dissipation $P_{tot} = f(T_A^*; T_S)$
* Package mounted on epoxy



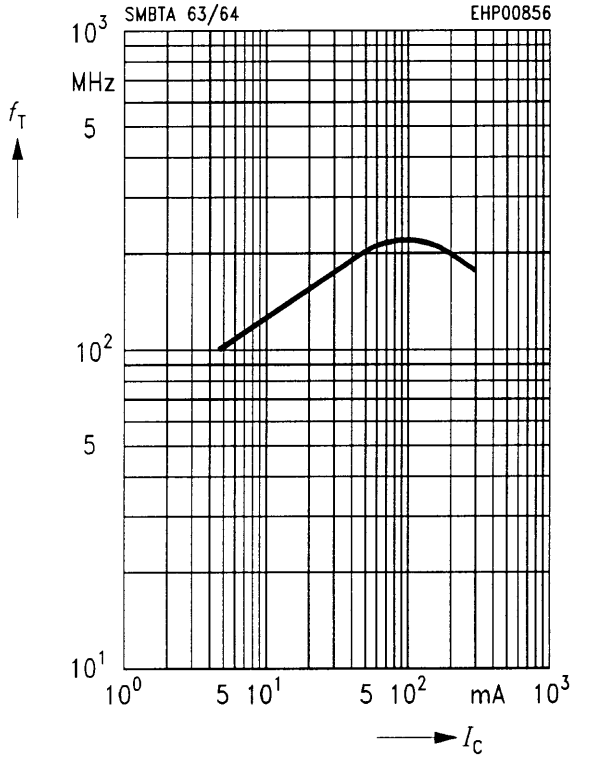
Collector-base capacitance $C_{CB0} = f(V_{CB0})$
Emitter-base capacitance $C_{EB0} = f(V_{EB0})$
f = 1 MHz



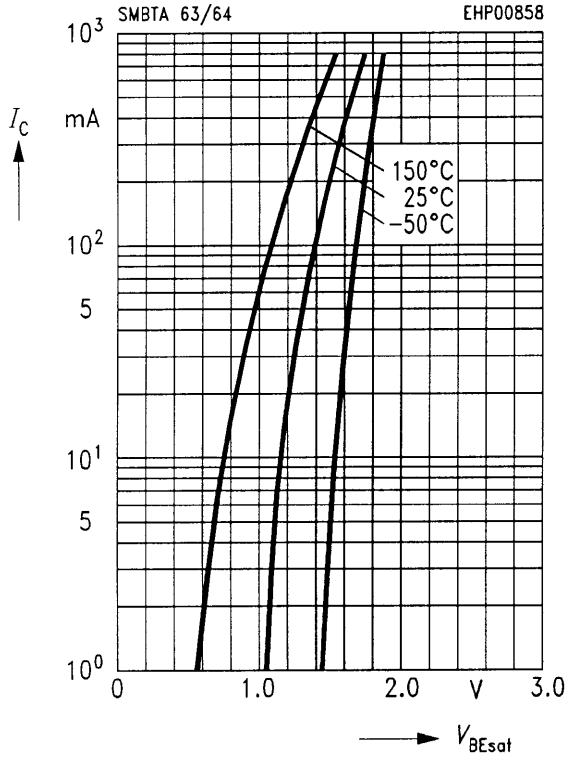
Permissible pulse load $P_{tot\,max}/P_{tot\,DC} = f(t_p)$



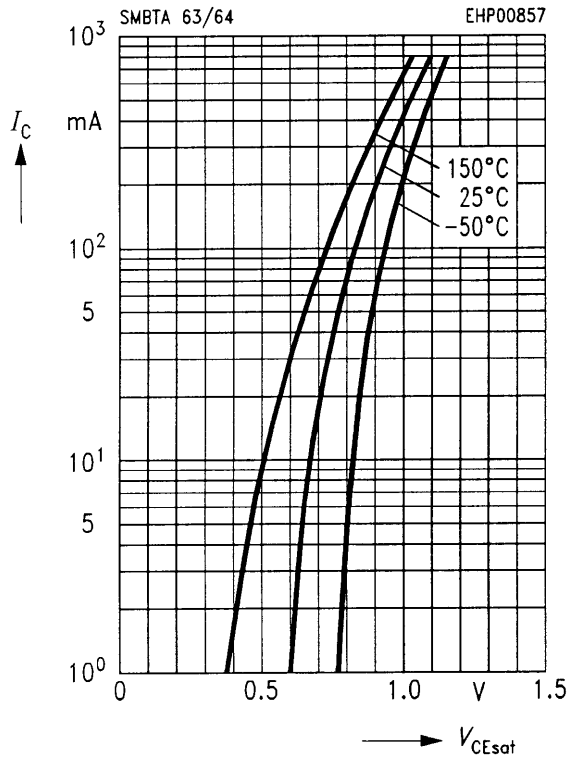
Transition frequency $f_T = f(I_C)$
V_{CE} = 5 V



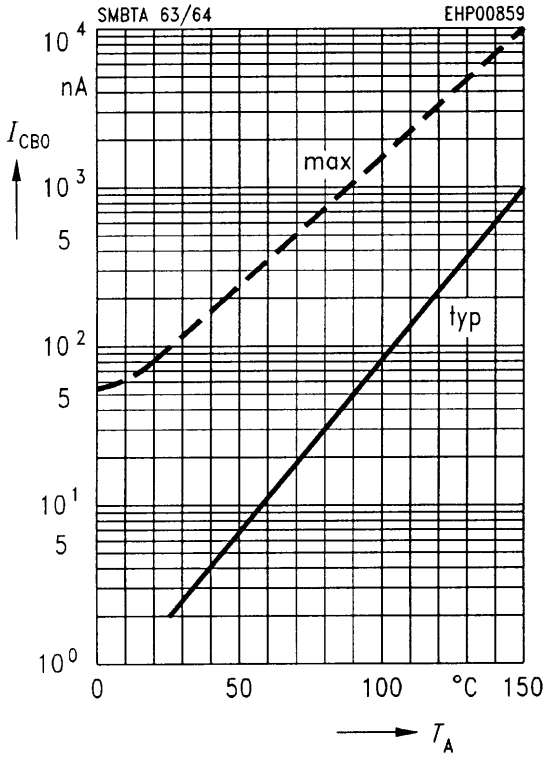
Base-emitter saturation voltage
$I_C = f(V_{BE\,sat})$, $h_{FE} = 1000$



Collector-emitter saturation voltage
$I_C = f(V_{CE\,sat})$, $h_{FE} = 1000$



Collector cutoff current $I_{CB0} = f(T_A)$
$V_{CB} = V_{CE\,max}$



DC current gain $h_{FE} = f(I_C)$
$V_{CE} = 5$ V