Features

- **Two Independent PN (Pseudo-Random Noise) Generators**
- **Programmable R7 (128) to R13 (8,192) PN Sequence Lengths**
- **Programmable Tau-Dither Amplitude**
- **Programmable PN Phase Adjustment to 1/16 Chip**
- **Correlation Acquisition Interface**
- **Programming Register Control**
- **Microcontroller Compatible Bus Interface**
- **Patent-Pending Frequency Diversity**
- **Low Speed Link Data Path for Supervisory and Setup Functions**

Spread-Spectrum Signal Processor Integrated Circuit

Preliminary

Description

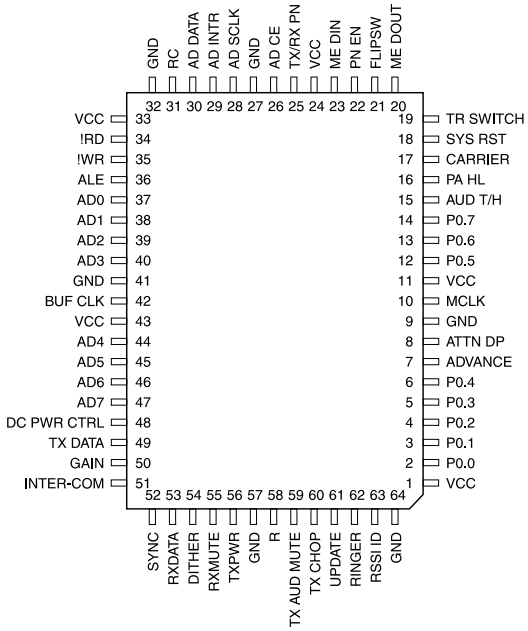
The AT48802 Spread-Spectrum Signal Processor (SSSP) chip from Atmel handles all PN code generation, synchronization, and handshaking required for either station (handset or base station) of a time division duplex direct sequence spread-spectrum cordless telephone. The AT48802 supports RF spreading and despreading for the best rejection of interference. In conjunction with a single-chip microcontroller, the circuit performs the following functions:

- Generates a pseudo-random sequence for spreading the transmitted signal.
- Generates a pseudo-random sequence for despreading in the receiver.
- Generates a sliding phase PN for acquiring synchronization with an incoming signal.
- Controls receive signal strength measurement timing for correlation peak detection.
- Operates a tau-dither tracking loop, with adaptive threshold, to maintain synchronization with the incoming signal.
- Controls transmit keying antenna switching for time-division duplexing.

(continued)

Pin Configuration

64 Lead PQFP



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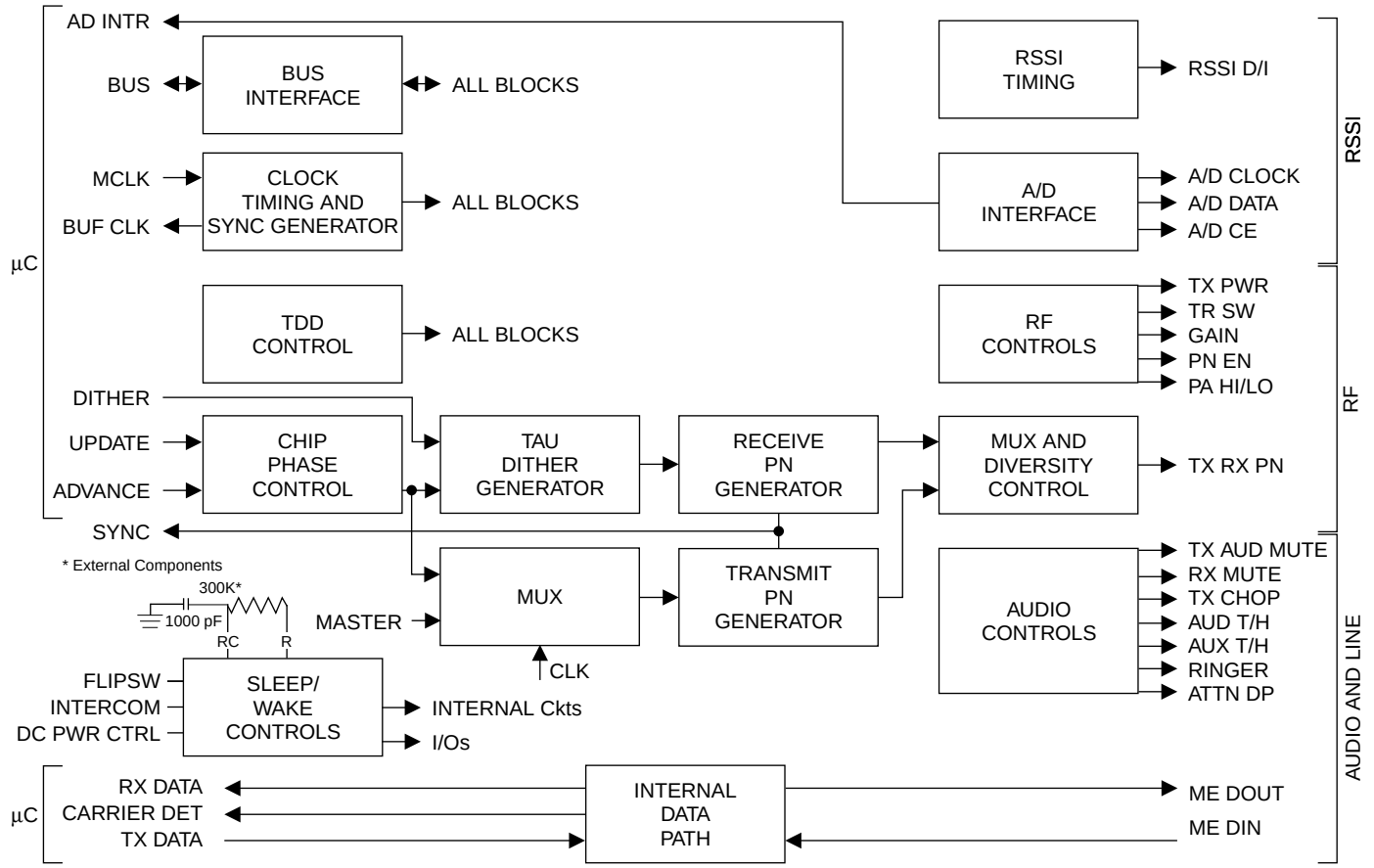
Description (Continued)

- Controls receive audio or data sampling time and duration.
- Controls wake-up and sleep functionality for remote battery operated handset.

The AT48802 unique spread-spectrum architecture capitalizes on the benefits of long range, signal-to-noise improvements, multi-path protection, and privacy. This design employs proven analog FM modulation to achieve the lowest possible system cost yet the highest processing gain and sound quality. The chip is a fully static design.

Block Diagram



Pin Description

Name	Pin#	I/O/T	Description
AD CE	26	O	Chip enable for external A/D converter, true = low.
AD DATA	30	I	8 bit serial input for external A/D.
AD INTR	29	O	Interrupt to controller to read A/D data, true = high.
AD SCLK	28	O	Clock for A/D converter.
ADVANCE	7	I	Advance or retard the chip phase. High = advance.
AD0	37	I/T	General purpose bi-directional port for microcontroller interface.
AD1	38	I/T	General purpose bi-directional port for microcontroller interface.
AD2	39	I/T	General purpose bi-directional port for microcontroller interface.
AD3	40	I/T	General purpose bi-directional port for microcontroller interface.
AD4	44	I/T	General purpose bi-directional port for microcontroller interface.
AD5	45	I/T	General purpose bi-directional port for microcontroller interface.
AD6	46	I/T	General purpose bi-directional port for microcontroller interface.
AD7	47	I/T	General purpose bi-directional port for microcontroller interface.
ALE	36	I	Address Latch Enable for port AD. Down edge latches.
ATTN DP	8	O	Can drive dial pulse relay or other function.
AUD T/H	15	O	Driver for audio track and hold.
BUF CLK	42	O	Replica of MCLK high speed clock input, for driving microcontroller clock input.
CARRIER	17	O	Internal data path, high = carrier present.
DC PWR CTRL	48	O	Can control a V_{CC} switch to turn on and off the other circuits.
DITHER	54	O	Indicates whether the tau-dither state is retarded or not retarded. High = retarded.
FLIPSW	21	I	A programmable transition on this pin will cause the chip to wake-up.
GAIN	50	O	May be used to control RF receive gain.
GND	9 27 32 41 57 64	I	DC power return = 0 Volts
INTERCOM	51	I	A programmable transition on this pin will cause the chip to wake-up.
MCLK	10	I	High speed clock input to chip.
ME DIN	23	I	Internal data path input from RF module.
ME DOUT	20	O	Internal data output to RF module.
P0.0	2	O	General purpose output port.
P0.1	3	O	General purpose output port.
P0.2	4	O	General purpose output port.

(continued)

Pin Description (Continued)

Name	Pin#	I/O/T	Description
P0.3	5	O	General purpose output port.
P0.4	6	O	General purpose output port.
P0.5	12	O	General purpose output port.
P0.6	13	O	General purpose output port.
P0.7	14	O	General purpose output port.
PA HL	16	O	May be used to control a switch which controls the RF transmit power.
PN EN	22	T	For controlling whether the RF module runs on spread-spectrum or narrowband.
R	58	O	Low speed clock oscillator for sleep control.
RC	31	I	Low speed clock oscillator for sleep control.
!RD	34	I	Read strobe input for port AD, low = true.
RINGER	62	O	Ring control output.
RSSI ID	63	O	RSSI integrate/dump control.
RX DATA	53	O	Internal data path output to microcontroller.
RX MUTE	55	O	Mute receive audio.
SYNC	52	T	PN epoch sync for receive, transmit or both.
SYS RST	18	I	Not a user control. Hold high always.
TR SWITCH	19	O	Controls state of RF module transmit/receive switch.
TX CHOP	60	O	Controls switch to disconnect audio from RF module modulation input during receive part of TDD.
TX DATA	49	I	Internal data path input from microcontroller.
TX AUD MUTE	59	O	For disconnecting transmit audio when data must be transmitted.
TX PWR	56	O	Turns on RF module transmit power during transmit part of TDD, and off during receive part of TDD.
TX/RX PN	25	T	Pseudo-noise sequence to RF module.
UPDATE	61	I	Causes chip phase control to step the phase. Used in conjunction with ADVANCE pin 7.
V_{CC}	1 11 24 33 43		DC power input = +V_{CC} Volts.
!WR	35	I	Write strobe for Port AD. Low = true.

Time Division Duplex Architecture

The AT48802 processor supports a Time Division Duplex (TDD) mode of operation where the transceiver transmits information during one time period and receives during an alternating time period. This architecture has the benefit of optimizing the frequency channel utilization as the transmit and receive frequencies can be equal to or close to one another, without spreading at two frequencies that are wide apart. The chip generates all TDD signals, (including those signals that account for time delays through the RF transceiver) that are necessary to implement a full-duplex voice communication system. All internal timing is derived from a master external clock. The chip is fully static and can work at any clock frequency less than 20 MHz. In all the following discussions the clock rate is assumed to be 15.360 MHz which is available from the companion RF module.

The 15.360 MHz master clock is internally divided down to a 7.5 kHz TDD rate, alternating between transmit cycle and receive cycle. That is, the transmit and receive cycles last for 66.67µs.

Sleep Mode and Battery Functionality

In most battery applications it is necessary to power down one end of the communication link except when a call is to be made. The sleep mode circuits of the AT48802 control this function.

The sleep mode circuits consist of a timer which runs from a low frequency (4 kHz) RC oscillator and a set of latches to interact with the rest of the chip which runs from the high frequency clock input. The sleep mode circuits also can also disable and protect the I/O's of the high frequency circuits. The protected mode is such that the outputs are three-stated and the input is floating. In addition, the sleep control section has a DC power control output which can be used to shutdown external circuits V_{CC}.

The chip should always be connected to V_{CC} in order for the sleep mode to be usable; the sleep mode circuits are alive and running as long as V_{CC} is applied, however their power drain is extremely small.

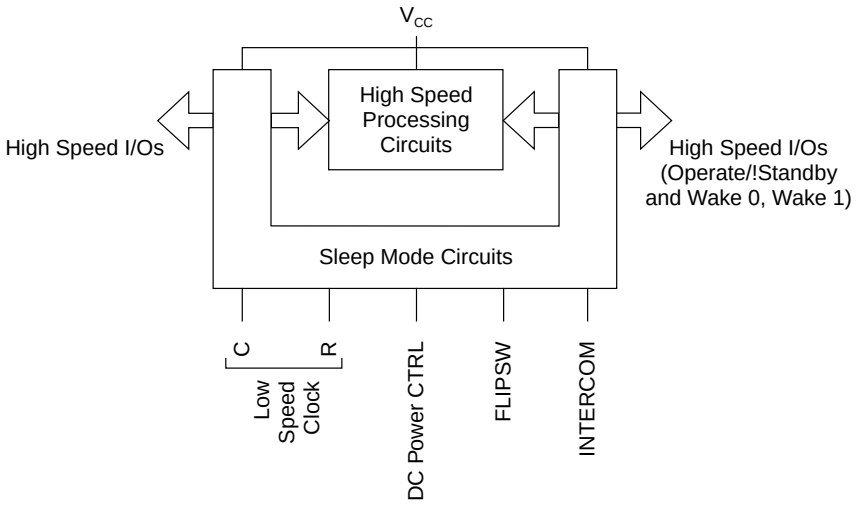
The sleep circuits will wake-up the chip, and other circuits if desired, in any one of three ways.

1. Time-out from the 4 kHz Oscillator will happen about 2 seconds (one half cycle of divided by 214) after going to sleep. Then the remote set could, for example, briefly listen for an incoming call using narrowband reception (which has little or no acquisition time), and listen for a predetermined tone with a very narrowband filter. For different wake-up periods the value of the C can be changed.
2. If the INTERCOM input is activated. The edge sense is programmable at R6 b7.
3. If the FLIPSW input is activated. The edge sense is programmable at R11 b7.

When the chip wakes up it stores information about the reason for wake-up in the I/O Registers at R14 b0-2 so the microprocessor can respond in a suitable way. The edge sense for FLIPSW and INTERCOM are programmed at R14 b4-5. (Note: Throughout this document "Rx by" means Register x bit y; x is hexadecimal.)

Once the chip is awake, only the microprocessor can put it back into sleep mode. It does this through the bus port at R0 b7. The OPERATE bit must be set before the command to STANDBY can be recognized. If the chip is awake and the user activates the INTERCOM or FLIPSW inputs, then the microprocessor can sense these actions at R14 b4-5.

Figure 1. Sleep Mode Arrangement



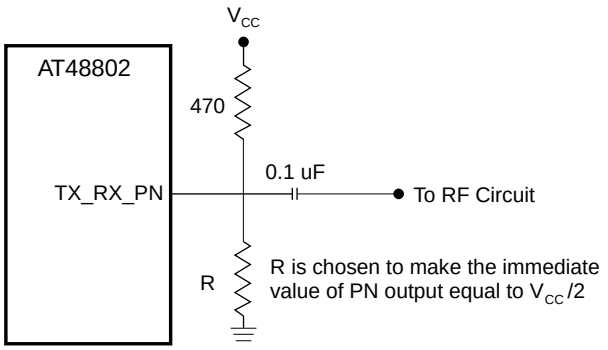
PN Code Generation

The AT48802 contains two independently programmable pseudo-random noise (PN) generators. One is used for transmit and the other is for receive. They are 13-stage linear feedback shift registers clocked at f(master clock) / 16, or the “chip rate”, normally 960 kHz (based on a 15.36 MHz master clock). Each can be programmed to operate with lengths of 7 to 13-stages PN (8,192 bit code sequence length). These lengths are actually linear maximal lengths plus one to simplify the internal circuitry. The long code length has the benefit of having many different maximal-length codes available for co-location operation in similar spread-spectrum equipment with minimum mutual interference, thus allowing efficient use of frequency channels. For example, there are over 600 maximal-length sequences available for R13 PN, and over 300 for R11 PN. Each maximal-length code can be considered a unique user channel.

The “Mask” bit in each PN register controls the counter sequence by setting feedback tap weights to either 0 or 1. The Transmit PN Generator (Tx PN) output and the Receive PN Generator (Rx PN) output are time division multiplexed precisely by the 50% duty-cycle TX PWR signal. That is, during the transmit cycle, only the Tx PN codes are outputted at the TX/RX PN pin. Conversely during the receive cycle, only the Rx PN codes are outputted. There is no prohibition against using the same code for transmit and receive. The shift register taps are set at R2 b0-4 and R1 b0-7 for receive, and R4 b0-4 and R3 b0-7 for transmit.

For definition purposes the end of the link which is initiating the link is the MASTER, and the end which is responding is the SLAVE. This means, e.g., for a cordless phone, if you are calling out then the handset becomes the MASTER and the base station is the SLAVE. If someone is calling you, then the base station is the MASTER (because it is initiating the radio link) and the handset is the SLAVE. This function is set at R0 b6.

Figure 2. PN Coupling for Spectral Control



If the chip is the MASTER, then the transmit PN generator is clocked from the clock generator and the receive PN generator is clocked from the chip phase control (through the tau-dither generator). If the chip is the SLAVE, then both PN generators are clocked from the chip phase control. Therefore the MASTER transmit has independent timing and the SLAVE locks both PN generators, via the chip phase control, to the receive signal. Finally, the MASTER receive PN uses the chip phase control to lock to its received signal from the SLAVE. In this way one can see the outline of an acquisition process.

The AT48802 PN spectral control feature enables the radio frequency transmit spectrum to easily meet the FCC requirement that out-of-band energy in a 100 kHz bandwidth be at least 20dB below in-band maximum energy in the same bandwidth. By this means one can achieve more spreading and more widely spaced frequency channels with less output filtering and still meet the requirements. The TX RX PN output is three-stated for one MCLK (master clock, the 15.36 MHz input) at each transition. By means of external pull resistors, this makes the PN voltage waveform rest at $V_{CC}/2$ for 60 ns on every transition. The objective is that the RF transmit power should go to zero during these periods. This introduces a spectral notch at 7.5 MHz on each side of center. If this waveform is faithfully preserved by the spreading mixer and subsequent amplifiers then the RF transmit spectrum will have nulls near ±7.5 MHz. This reduces the normal PN lobes which might otherwise exceed allowed amplitude. A particular application may or may not need this feature; for example, if only one frequency channel is being used, and it is in the center of the band, then depending on the output filter one may not have this problem. In such a case a simple lowpass filter may be used from the PN generator output to the RF module PN input.

A force-load function is provided for initializing the PN generator to ensure the transmit and receive PN generator coefficients can be loaded into the counters without locking up during the first-time loading after a power up cycle. This is common among multiple feedback PN counters. The force-load bit can be set by a logic 1 to the FLOAD bit in the control register (Register 0, bit 1).

The Transmit PN and the Receive PN counters can be synchronized by asserting a logic 1 to the PN RESET bit in the control register (Register 0, bit 0). The PN OUT function at R0 b5 turns on the PN when set.

Frequency Diversity Improves Signal-to-Noise Ratio

Built into the AT48802 is an exclusive frequency diversity function, which enhances protection from PN noise due to imperfect correlation. The chip encodes the PN code sequence such that when spread, the information is modulated and transmitted redundantly in two side lobes. That is, the redundant information is contained in two main lobes with a null at the carrier instead of the classical single lobe spreading spectra. The spreading bandwidth also doubles, effectively doubling the spreading chip rate. This has the benefit of increased processing gain and greatly reducing the residual PN noise near the carrier after correlation. The frequency diversity can be user enabled by setting the BW (Band-Width) bit high in the PN register (Register 2, bit 7 for Receive PN, and Register 4, bit 7 for Transmit PN). The transmit and receive PN generators are set independently.

Chip Phase and Tau-Dither Control

The chip phase control circuit enables the user to step the chip phase in either direction by amounts from 1/16 to 8/16 chip per update. The size of the step is set in R5 b0-2, the step direction is controlled by the ADVANCE line, and the command to do a step is by pulsing the UPDATE line. The maximum allowed update rate is MCLOCK/32.

The tau-dither circuit is used to assist in the tracking a correlation peak. This is done as follows. When the locally generated receive PN is a good match to the incoming signal at RF, then the RF signal is accurately despread and the signal energy is gathered into a narrow spectral region around the carrier. If a narrow IF filter is used to filter this signal, then when the chip phase match to the incoming signal is good then the most possible power will get through the narrow IF filter; when the chip phase is advanced or retarded from the best place, then the signal power in a narrow band will fall. The tau-dither circuits, when activated, step the PN chip phase back and forth by a settable amount at a rate of TDD/2. If one looks at the RF module RSSI (receive signal strength indicator) by using the A/D converter interface, then when the PN phase is, on the average, optimum then the alternating output of RSSI will show small variation at a rate of TDD/2. If the peak is not centered, then the RSSI variation at TDD/2 measured through the A/D converter interface, will become larger because one phase of tau-dither will produce less RSSI than the other. Now one can track the peak by using the microprocessor to close this control loop which has as an input to the RSSI variation at TDD/2 measured through the A/D converter interface and has output using the UPDATE and ADVANCE controls. The control loop should null the TDD/2 signal.

The available tau-dither amounts are 1/16 chip peak-to-peak, to 15/16 chip peak-to-peak, set at R5 b3-5. Dither on/off is controlled via R0 b4 (track = high = dither on). The tau-dither phase is actually only a retard or no retard with respect to the chip phase when tau-dither is off, this is a detail which the control system designer may need.

If the tau-dither amplitude is changed it will not take affect until the receive PN code is reloaded. The DITHER output of the chip tells the microprocessor whether the dither phase is retarded (High) or not retarded. High is retarded.

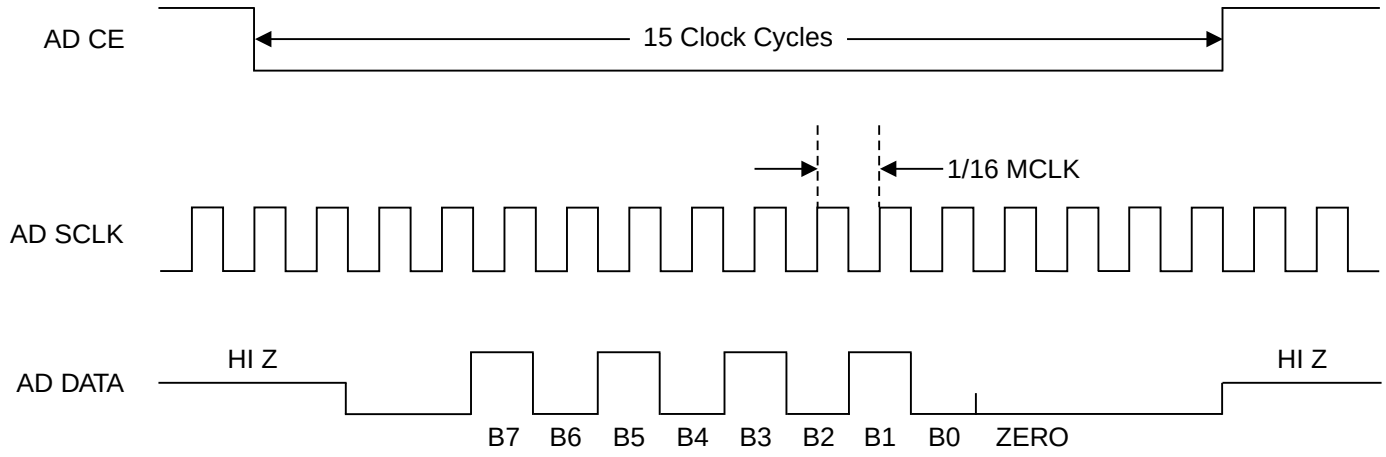
RSSI Interface

The purpose of this circuitry is to provide an interface to a serial A/D converter and an integrate/dump filter, if desired. The interface is synchronized to TDD. The data from the A/D converter is converted to parallel and loaded to the register at R8 b0-7. The RSSI function provides an integrated/dump command output with timing completely adjustable throughout the TDD cycle and also completely adjustable for pulse width, except the hardware will not allow the timing of RSSI ID to conflict with the A/D converter command. This allows optimum filtering of the RSSI signal if desired. The adjustable timing is necessary to allow for different RF designs with different amounts of delay in the IF filter. The sense of the RSSI ID output, that is, which way is integrate and which way is dump, is controlled via RC b6-7

RSSI ID timing is set via RC b0-5 for delay and RD b0-5 for pulse width. The smallest step is MCLK/32 = 2 us for a 15.36 MHz clock. The 5 bits allow adjustment over a range of TDD/2. In order to get the other half TDD cycle, one must invert the RSSI ID bits at RC b6-7, which will invert the waveform.

Figure 3 shows the A/D converter timing for a converter such as the Linear Technology LTC 1196 National Semiconductor ADC0831 or similar.

Figure 3. A/D Converter Acquisition Timing Diagram



RF Controls

AD SCLK is always present. When AD CE is high then the A/D converter is in the low power mode. Sampling and conversion begins on the next negative clock edge after AD CE goes low. For AD CE = 15 cycles wide, conversion is guaranteed to be completed and still allow time to output 8 data bits before the AD CE goes high again.

TX PWR

The Transmit Power control is synchronous with the TDD cycle so that the transmit power can turn on and off as needed. Its sense is settable through R6 b1-2, or it can be set always in one state for simplex applications.

TR SW

The Transmit Receive Switch function is intended to control an antenna transmit-receive switch. Its timing is synchronous with TDD and the sense is settable through R9 b4-5, or can be set always in one state for simplex applications.

Gain

Intended to control the LNA V_{CC} or current to two different states in order to provide a receive path attenuator to keep the RSSI level in best range for chip lock loop function. The timing is synchronous with TDD or can be set always in one state, via R9 b2-3.

PN EN

The PN Enable function is intended to allow the RF module to be set to either spread-spectrum or narrow band transmission and reception. Narrowband mode is useful for a telephone handset to very quickly wake-up and determine if it is being signaled by the base, because the more lengthy spread-spectrum acquisition process is avoided when no signal is present, thus making the battery standby time long. If a narrowband signal is present then a spread-spectrum acquisition may be done to fully establish the link. The PN EN function is controlled by R2 b5-6 to be either low, high, or three-state high impedance.

PA HI/LO

Power Amp High Low is an output to control the power amp V_{CC} in the RF module so that in narrowband mode the transmit power can be held below 1mW to meet FCC requirements. This is controlled through R6 b0.

Audio and Line Controls

TX AUD MUTE and RX MUTE

Transmit Audio Mute and Receive Mute are intended to allow the user audio to be turned off as needed to prevent the other end from hearing undesired signals or noise during acquisition, or any other time. They are set via R0 b2-3.

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Audio and Line Controls (Continued)

TX CHOP

Transmit Chop is timed with TDD and can turn off the audio used to modulate transmit RF during the receive period. If the RF module has a single synthesizer then this function is needed to prevent a large sidetone due to receive RF local oscillator modulation. R13 b0-1 control this function to be high, low, TDD or inverse TDD.

AUD T/H and AUX T/H

Both Audio Track/Hold and Auxiliary Track/Hold have the same, independently settable function. If this chip is used in a high rate TDD system with analog audio modulation then it is necessary to track and hold the receive audio since it is only present half the time at the TDD rate of 7.5 kHz. AUD T/H provides a fully adjustable TDD rate pulse to do this. The pulse width and pulse timing are fully adjustable over the range of 1 TDD cycle in increments of 1/64 of a TDD cycle, i.e., 2.1us steps, for a 15.36 MHz clock. The delay and pulse width are programmable via RE b0-5 and RF b0-5 (R10 b0-5 and RF b0-5 for AUX T/H). These register settings provide TDD/2 adjustability, and rest of the range is provided by RE b6-7 (or R10 b6-7 for AUX T/H) which can invert the output, or cause it to be always high or always low.

Ringer and ATTN DP

Ringer is controlled by R4 b5-6 and can be output always high, always low, three-state and 1875 Hz tone to drive a speaker or piezo transducer. Attenuator Dial Pulse is available to drive a relay when needed for pulse dialing. In the handset of a telephone there is no relay (it is in the base) so this output could be used to turn on/off an audio attenuator.

Microprocessor Bi-Directional Bus Interface

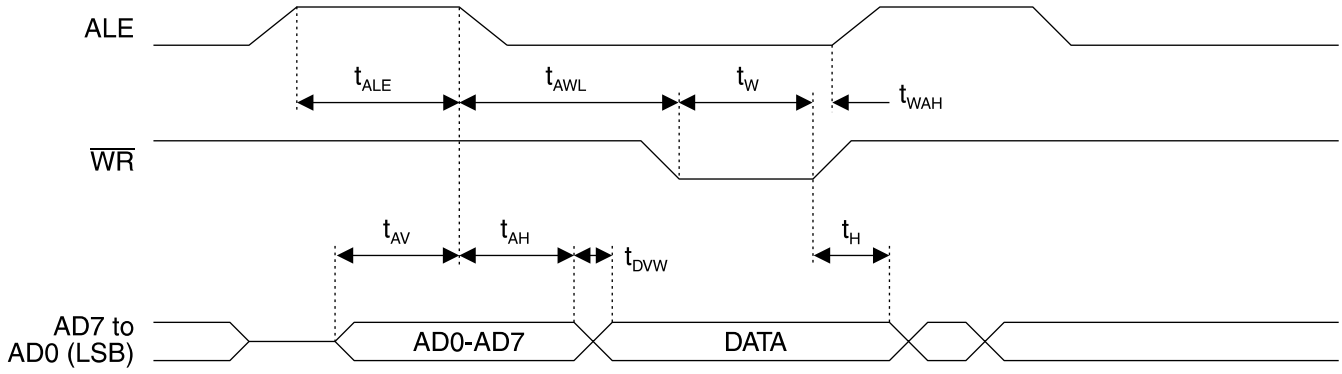
Most control functions, including most Spread-Spectrum controls, PN registers, RF Controls, and telephone controls are loadable into a set of control registers via an 8 bit data bus. This 8 bit bi-directional address / data bus, AD7 - AD0 (LSB), is compatible with the 80C51 / 80C52 family of microcontroller. Register data can be read back via the same data bus. Twenty-one control registers (HEX 00 to HEX 14) are provided for complete implementation of cordless phone or wireless communication systems. Register 8 and Register 14 are read only. Do not write to R14 b7.

The microcontroller may run using the same 15.36 MHz master clock that the ASIC uses. However that is not absolutely necessary. In any case, it must be rated to operate to at least 16 MHz frequency.

Data Bus Write Cycle Timing

The bus multiplexes address information as well as data. Address decoding is internally provided. The register address is directly mapped to the low-order address bits. That is, register 0 has the address code of HEX 00, while register A has the address code of HEX 0A. During a WRITE cycle, the address is latched into the address decoder by the falling edge of the ALE signal. Data from the microprocessor must be valid when the $\overline{WR}$ signal goes from a low-to-high state. Figure 4 shows the WRITE cycle timing.

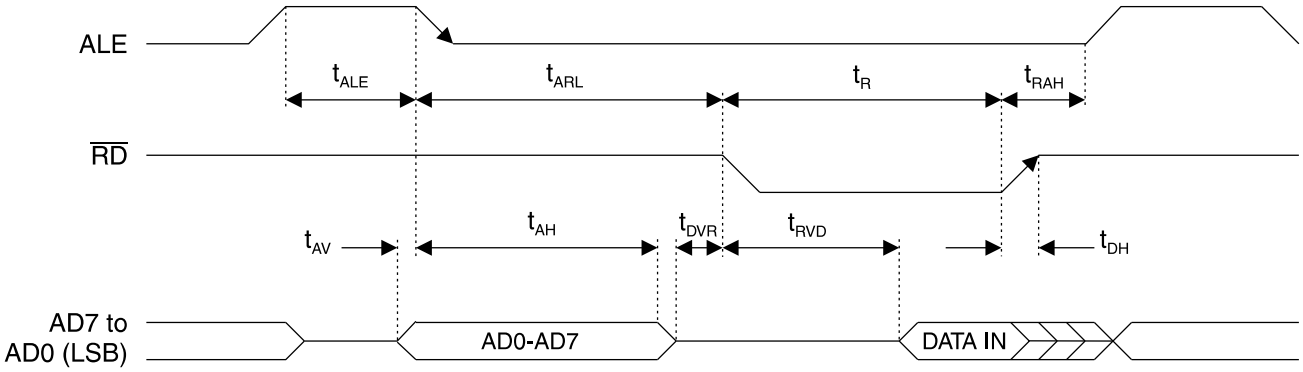
Figure 4. Write Cycle Timing Diagram



Data Bus Read Cycle Timing

The READ cycle's multiplexed addressing scheme is the same as the WRITE cycle. Address mapping is also similarly made to the lower-order address bits. That is, register 0 has an address code of HEX 00, while register A has an address code of HEX 0A. Data will be valid on the data bus and $\overline{RD}$ signal latches data as it goes from a low to a high state. The timing is shown in Figure 5 below.

Figure 5. Read Cycle Timing Diagram



Internal Data Path

The AT48802 has a 234 bits per second synchronous full duplex internal data path. This uses in-band signaling by Manchester coded BPSK modulating an 1875 Hz carrier, so voice must be disabled when data is on. This path is intended for call setup and control functions.

To transmit data, R6 b6 (TDE transmit data enable) must be set. The data presented to the TX DATA pin 49 will be transmitted out of the ME DOUT pin 20. The input data must be synchronized, and this can be achieved by using the DITHER pin 54 as a clock. When transmission is complete the TDE bit should be reset.

To receive data, R6 b5 (RDE receive data enable) must be set. The CARRIER output pin 17 will indicate when valid data is available. The ME DATA IN pin 23 must be presented with a digital signal; an analog signal would have to be sent through a comparator with the correct amount of hysteresis first. The RX DATA pin 53 has the received data on it for use by the microcontroller. When reception is complete then R6 b5 should be reset.

The data receiver has fully adjustable internal timing to accommodate the delays of various RF designs.

TDD Rate

R9 b7, when set low, causes the TDD rate to be normal 7500 Hz. When set high, the TDD rate is 1875 Hz. This mode can cause the transmit signal to be 1875 Hz square wave AM. This is useful when the handset must wake-up and detect whether it is being signaled in a very short time. If the PN is turned off then the receive microcontroller can be setup as a very narrow 1875 Hz filter and detector to decide very quickly if the base is signaling the handset. If not, it may go back to sleep.

When in 1875 Hz TDD mode, delays and pulse widths of RSSI, AUD T/H, AUX T/H and internal data path timing do not change, and still work in normal specified manner, so this mode is only for very specialized use.

Port 0

Port 0 is a general purpose register output port of the AT48802. It is suitable for various housekeeping functions of a telephone such as making LED indicators turn on, driving a DTMF generator, keypad sensor, etc. This port is accessed through R7 b0-7 and its outputs appear on pins 2 through 6 and 12 through 14 of the chip.

Test Aids

Sync Output

The SYNC pin 52 can be used to observe the timing of TX PN epoch and/or RX PN epoch. The functionality is controlled by R9 b0-1. The pulse indicates when the generators start their PN codes, which are called the epochs. When a chip phase lock is achieved, the syncs are almost coincident.

Alternate Port 0

General purpose output port 0 bits 0-3 can be programmed in normal operation by writing to register 7. Alternate usage of these bits for engineering test purposes is enabled and disabled by first writing the desired configuration to register 13 (decimal 19). Note that in each case, a zero bit in register 13 enables the standard configuration for the ASIC port 0 outputs.

Table 1. Port bit 0.0 alternate usage:

P0.0		Test Selector P0.0 Function
Reg 0x13	bits [3:2]	
0	0	Follows P0.0 (Reg 7 bit 0) normal operation
0	1	Data path demodulator, receive clock
1	0	Data path demodulator, receive local oscillator
1	1	Data path demodulator, dump signal (bit synchronized integrate and dump processing)

The alternate uses of port 0.0 all deal with timing signals associated with the phase shift keyed data path operation. These signals are used for correctly setting the timing delays associated with hardware dependent delays in the RF and audio data circuitry. Applications using the WLI reference design are not required to adjust the timing settings (register 12 contents).

Table 2. Port bit 0.1 alternate usage:

P0.1		Test Selector P0.1 Function
Reg 0x13	bits [5:4]	
0	0	Follows P0.1 (Reg 7 bit 1) normal operation
0	1	Data path demodulator, phase shift keyed output
1	0	Data path demodulator, integrator's LSB
1	1	Data path demodulator, carrier detector output

The alternate uses of port 0.1 all deal with timing signals associated with the phase shift keyed data path operation. These signals are used for correctly setting the timing delays associated with hardware dependent delays in the RF and audio data circuitry. Applications using the WLI reference design are not required to adjust the timing settings (register 12 contents).

Table 3. Port bit 0.2 alternate usage:

P0.2	Test Selector P0.2 Function
Reg 0x13 bit [6]	
0	Follows P0.2 (Reg 7 bit 2) normal operation
1	Receive PN Sync Pulse

The alternate use of port 0.2 allows the receive PN generator synchronization pulse to be probed. Note that an external pin on the ASIC is also dedicated to this function, and can be controlled by register 9 bits 0 and 1.

Table 4. Port bit 0.3 alternate usage:

P0.3	Test Selector P0.3 Function
Reg 0x13 bit [7]	
0	Follows P0.3 (Reg 7 bit 3) normal operation
1	Transmit PN Sync

The alternate use of port 0.3 allows the transmit PN generator synchronization pulse to be probed. Note that an external pin on the ASIC is also dedicated to this function, and can be controlled by register 9 bits 0 and 1.

Register Structure

Address/Usage	7	6	5	4	3	2	1	0
0x00 General Operation	Operate !Standby	Master !Slave	PN OUT	Track/ !Acquire	TX audio mute	RX audio mute	Force Load	RE-SYNC
0x01 RX Polynomial	RX-P8	RX-P7	RX-P6	RX-P5	RX-P4	RX-P3	RX-P2	RX-P1
0x02 RX Polynomial	RX-BW	PN EN 1	PN EN 0	RX-P13	RX-P12	RX-P11	RX-P10	RX-P9
0x03 TX Polynomial	TX-P8	TX-P7	TX-P6	TX-P5	TX-P4	TX-P3	TX-P2	TX-P1
0x04 TX Polynomial	TX-BW	Ring Function 1	Ring Function 0	TX-P13	TX-P12	TX-P11	TX-P10	TX-P9
0x05 ACQ and Track Control	PH1	PH0	TD2	TD1	TD0	N2	N1	N0
0x06 TX PWR / DPATH / Ring	Flip Switch Polarity (Wakeup)	TDE	RDE	RDP	Ring Attn Dial Pulse	TX PWR 1	TX PWR 0	PA HI/LO
0x07 General Purpose Port	P0.7	P0.6	P0.5	P0.4	P0.3	P0.2	P0.1	P0.0
0x08 RSSI A/D	A/D bit 7	A/D bit 6	A/D bit 5	A/D bit 4	A/D bit 3	A/D bit 2	A/D bit 1	A/D bit 0
0x09 Gain / TDD Rate / Syncs	TDD Rate Select 1875/!7500	Soft Reset	TR SW 1	TR SW 0	GAIN 1	GAIN 0	Sync Mode (Bin/Tri)	Sync Select TX/!RX

(continued)

Register Structure (Continued)

Address/Usage	7	6	5	4	3	2	1	0
0x0A TX PN Mask	TX PN Mask bit 12	TX PN Mask bit 11	TX PN Mask bit 10	TX PN Mask bit 9	TX PN Mask bit 8	TX PN Mask bit 7	TX PN Mask bit 6	TX PN Mask bit 5
0x0B RX PN Mask	RX PN Mask bit 12	RX PN Mask bit 11	RX PN Mask bit 10	RX PN Mask bit 9	RX PN Mask bit 8	RX PN Mask bit 7	RX PN Mask bit 6	RX PN Mask bit 5
0x0C RSSI Delay	RSSI ID 1	RSSI ID 0	TD5	TD4	TD3	TD2	TD1	TD0
0x0D RSSI Width				TW4	TW3	TW2	TW1	TW0
0x0E AUD T/H Delay	AUD T/H 1	AUD T/H 0	TD5	TD4	TD3	TD2	TD1	TD0
0x0F AUD T/H Width				TW4	TW3	TW2	TW1	TW0
0x10 AUX T/H Delay	AUX T/H 1	AUX T/H 0	TD5	TD4	TD3	TD2	TD1	TD0
0x11 AUX T/H Width	Intercom Polarity (Wakeup)	P0.7 mux 0 = Reg 7 1 = Aux T/H		TW4	TW3	TW2	TW1	TW0
0x12 Data Path Delays	DPATH DUMP 3	DPATH DUMP 2	DPATH DUMP 1	DPATH LO1	DPATH LO0	DPATH CLK2	DPATH CLK1	DPATH CLK0
0x13 Bit Functions	P0.3 OPT TXPN Sync	P0.2 OPT RX PN Sync	P0.1 OPT1 (dpath)	P0.1 OPT0 (dpath)	P0.0 OPT1 (dpath)	P0.0 OPT0 (dpath)	TX CHOP 1	TX CHOP 0
0x14 Sleep Mode / Wake	Test Mode		Sense Intercom Input Line	Sense Flip Switch Input Line		Wake Intercom sw latch	WAKE Flip sw latch	Wake Timer time-out latch

Register Functions

Function	Register	Bit #	Description
RESYNC	0	0	0 = Normal PN counter operation. 1 = Re-synchronizes RX PN and TX PN generators to the same counting state.
Force Load	0	1	0 = No action. 1 = Forces an immediate loading of the TX PN polynomial from the transmit polynomial register into the PN generator and the RX PN polynomial from the receive polynomial register into the RX PN generator.
RX Audio Mute	0	2	0 = Sets a logic 0 to the RX MUTE pin 55. 1 = Sets a logic 1 to the RX MUTE pin 55.
TX Audio Mute	0	3	0 = Sets a logic 0 to the TX MUTE pin 59. 1 = Sets a logic 1 to the TX MUTE pin 59.
Track !Acquire	0	4	0 = tau-dither on. 1 = tau-dither off.
PN OUT	0	5	0 = TX RX PN pin 25 is disabled and always low. 1 = TX RX PN pin 25 is enabled and toggles.
Master !Slave	0	6	0 = Sets the unit to Slave mode of operation (Unit receiving a link setup request). 1 = Master mode operation (Unit originating a link setup request).
Operate !Standby	0	7	See section 2.2
RX-P1 through RX-P8	1	0-7	Low-order receive PN polynomial (shift register tap weights). P1 is LSB.
RX-P9 through RX-P13	2	0-4	High-order receive PN polynomial (shift register tap weights). P13 is MSB.
PN EN	2	5-6	PN EN 0 / PN EN 1 / PN EN pin 22 0 / 0 / 0 0 / 1 / Three-state 1 / 0 / Three-state 1 / 1 / 1
RX-BW	2	7	0 = Disables receive diversity mode. 1 = Enables receive diversity mode.
TX-P1 through TX-P8	3	0-7	Low-order transmit PN polynomial. P1 is LSB.
TX-P9 through TX-P13	4	0-4	High-order transmit PN polynomial. P13 is MSB.
Ring Func 0 Ring Func 1	4	5-6	Ring F0 / Ring F1 / Ringer pin 62 0 / 0 / 0 0 / 1 / Three-state 1 / 0 / 1875 Hz 1 / 1 / 1

(continued)

Register Functions (Continued)

Function	Register	Bit #	Description
TX-BW	4	7	0 = Disables transmit diversity mode. 1 = Enables transmit diversity mode.
N0, N1, N2 (N0 = LSB)	5	0-2	Chip Phase Control Step Size. N2, N1, N0 — Step Size 000 — 1/16 Chip 001 — 2/16 Chip 010 — 3/16 Chip 011 — 4/16 Chip 100 — 5/16 Chip 101 — 6/16 Chip 110 — 7/16 Chip 111 — 8/16 Chip
TD0, TD1, TD2 (TD0 = LSB)	5	3-5	Tau-Dither Amplitude. TD2, TD1, TD0 — Peak-to-Peak Amplitude 000 — 1/16 Chip 001 — 3/16 Chip 010 — 5/16 Chip 011 — 7/16 Chip 100 — 9/16 Chip 101 — 11/16 Chip 110 — 13/16 Chip 111 — 15/16 Chip Note: To load a new tau-dither value, it must be followed by the loading of a Receiver PN code to latch in the new Tau-Dither.
PH0, PH1	5	6, 7	Selects one of 4 phases of the R11 sync (from the Master's Tx PN generator) with which to reset the Master's receive PN Generator when attempting to acquire code lock with the Slave unit. This is useful in acquisition when transitioning from R11 to R13 which is four times as long. This specialized function is used in the Atmel acquisition software.
PA HI/LO	6	0	0 = PA HI/LO pin 16 low. 1 = PA HI/LO pin 16 high. Intended for control of RF transmit power to a lower level in narrowband mode.

(continued)

Register Functions (Continued)

Function	Register	Bit #	Description
TX PWR 0 TX PWR 1	6	1-2	Turn RF transmitter on or off. TX PWR 0 / TX PWR 1 / TX PWR pin 56 0 / 0 / 0 0 / 1 / TDD 1 / 0 / !TDD 1 / 1 / 1
Ring Attn or Dial Pulse	6	3	For attenuating the ring amplitude as heard in the handset, or for controlling an off hook/pulse dial relay in the base station of a telephone. Useful in handset when there is no separate ring transducer from the speaker. 1 sets 1, 0 sets 0 at pin 8.
RDP	6	4	Receive data polarity. Inverts or does not invert receive data in the internal data path.
RDE TDE	5	5-6	Receive and transmit data enable. 0 = disable, 1 = enable input pins 49 and 53.
Flip Switch Polarity	6	7	Wakeup edge sense polarity for input pin 21 0 = down edge, 1 = up edge sensing.
Port 0	7	0-7	Controls general purpose output port at pins 2-6 and 12-14. Non-inverting.
RSSI AD	8	0-7	Read only, contains the data from the A to D converter gathered serially from pins 26, 28, 30. Non-inverting. Bit 0 = LSB.
Sync Select Sync Mode	9	0-1	These bits control how transmit and receive epoch sync pulses appear on pin 52. Select / Mode / Sync pin 52 0 / 0 / Trinary, rec up, xmt down 0 / 1 / Binary, rec up 1 / 0 / Trinary, xmt up, rec down 1 / 1 / Binary, xmt up
Gain 0, 1	9	2-3	Intended to control two receive gain states in the RF module. Gain 0 / Gain 1 / Gain pin 50 0 / 0 / 0 0 / 1 / TDD 1 / 0 / !TDD 1 / 1 / 1

(continued)

Register Functions (Continued)

Function	Register	Bit #	Description
TR SW 0, 1	9	4-5	Intended to control the transmit-receive switch in the RF module. TR SW 0 / TR SW 1 / TR SWITCH pin 19 0 / 0 / 0 0 / 1 / TDD 1 / 0 / !TDD 1 / 1 / 1
Soft Reset	9	6	Not a user control.
TDD Rate Select	9	7	See Section 2.11, 1 = 1875 Hz, 0 = 7500 Hz.
TX PN Mask RX PN Mask	A B	0-7 0-7	These set the length of the PN code. Function is the same for transmit and receive. Shift Register Size / Code Length / Mask R13 / 8192 / FF R12 / 4096 / 7F R11 / 2048 / 3F R10 / 1024 / 1F R9 / 512 / 0F R8 / 256 / 07 R7 / 128 / 03 R6 / 64 / 01
RSSI Delay	C	0-5	RSSI ID pin 63 delay with respect to internal TDD positive edge. 1 LSB = 2.1 µs or 32MCLK. Bit 0 = LSB. Range is TDD/2. The range is increased to TDD by inverting the signal using RSSI I/D bits 6 and 7 (see below).
RSSI ID 0-1	C	6-7	Used in conjunction with RSSI Delay. RSSI ID / RSSI ID / RSSI ID pin 63 0 / 0 / 0 0 / 1 / TDD, delayed 1 / 0 / !TDD, delayed 1 / 1 / 1 Intended to be used with an integrate and dump filter; See Section 2.6.
RSSI Width	D	0-4	Used in conjunction with RSSI Delay. 1 LSB = 2.1µs or 32MCLK. Bit 0 = LSB.
AUD TH Delay AUD TH 0-1 AUD TH Width	E E F	0-5 6-7 0-4	Same functionality as RSSI above except applies to the AUD TH signal at pin 15. See section 2.8.3.

(continued)

Register Functions (Continued)

Function	Register	Bit #	Description
AUX TH Delay AUX TH 0-1 AUX TH Width	10 10 11	0-5 6-7 0-4	Same functionality as RSSI above except applies to the AUX TH signal at pin 14 if so selected by Register 11 bit 6 (see below). See section 2.8.3. Pin 14 is dual use.
Port 0 bit 7 Mux	11	6	Controls a multiplexed output pin 14. 0 selects register 7 bit 6 non-inverted. 1 selects AUX TH function, see above.
Intercom Polarity	11	7	Wakeup edge sense polarity for input pin 51. 0 = down edge, 1 = up edge sensing.
Data Path Delays	12	0-7	These bits set the delays in the various sub-functions of the internal data path receiver. This allows any arbitrary time delay in the RF module design and still optimally detect data.
TX CHOP 0, 1	13	0-1	Intended to control an audio switch which disconnects audio from the RF module modulation input during the receive part of TDD. Pin 60. TX CHOP 0 / TX CHOP 1 / TX CHOP pin 60 0 / 0 / 0 0 / 1 / TDD 1 / 0 / !TDD 1 / 1 / 1
P0.0 OPT 0, 1	13	2-3	Allows internal data path signals to be observed at pin 2 for engineering purposes, to assist in setting the data path delays. P0.0 OPT1 / P0.0 OPT0 / Port 0.0 muxed function 0 / 0 / Register 7 bit 0 0 / 1 / RX_CLK (me_din_smp) 1 / 0 / Rx_LO (delay_div512) 1 / 1 / Dump
P0.1 OPT 0, 1	13	4-5	Equivalent function to Port 0 bit 0 above, except for Port 0 bit 1, pin 3. P0.1 OPT1 / P0.1 OPT0 / Port 0.1 muxed function 0 / 0 / Register 7 bit 1 0 / 1 / Demod, PSK Demod O/P 1 / 0 / Demod, Integrator's LSB 1 / 1 / Demod, Carrier Detector

(continued)

Register Functions (Continued)

Function	Register	Bit #	Description
P0.2 OPT	13	6	0 selects register 7 bit 2 to output at pin 4. 1 selects RX PN Sync to output at pin 4.
P0.3 OPT	13	7	0 selects register 7 bit 3 to output at pin 5. 1 selects TX PN Sync to output at pin 5.
Wake latches	14	0-2	Allows the microcontroller to see why the unit came awake, to allow proper response. Wake 0 / Wake 1 / Wake 2 / Wakeup Cause 0 / 0 / 0 / power on reset 0 / 0 / 1 / timer 0 / 1 / 0 / FLIPSW 0 / 1 / 1 / timer and FLIPSW 1 / 0 / 0 / INTERCOM 1 / 0 / 1 / timer and INTERCOM 1 / 1 / 0 / FLIPSW and INTERCOM 1 / 1 / 1 / Everything WAKE bits are cleared (set to 0) upon entering the sleep mode. See section 2.2.
Sense FLIPSW	14	4	Direct sense of FLIPSW input pin 21. For example, when the handset is already awake and the user wants to hang up and start a new call, then the microcontroller could sense this by scanning this bit. Not latched.
Sense INTERCOM	14	5	Direct sense of INTERCOM pin 51. For example, when the handset is already awake and the user wants to hang up and start an intercom call, then the microcontroller could sense this by scanning this bit. Not latched.
Test Mode	14	7	Not a user function.

Absolute Maximum Ratings*

Lead Temperature	300°C
Storage Temperature	-55°C to +125°C
V_{CC}, Supply Voltage	-0.3V to +7.0V
Input Pin Voltage	-0.3V to V_{CC} + 0.3V
Input Pin Current	-10 mA to +10 mA

*NOTICE: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Operating Characteristics

Parameter	Conditions	Min	Max	Units
V_{CC}, Supply Voltage		4	6	Volts
I_{DD}, Supply Current	V_{CC} = 5.0V, MCLK = 15.36 MHz Standby Mode		TBD TBD	mA µA
Ambient Temperature		0	70	°C

DC Electrical Characteristics (1)

Unless Otherwise Specified, V_{CC} = +5V, 0°C ≤ T_A ≤ 70°C

Parameter	Min	Max	Units
CMOS Input Specifications			
V_{IL}, Low Level Input Voltage		0.3 V_{CC}	Volts
V_{IH}, High level Input Voltage	0.7 V_{CC}		Volts
I_{IL}, Low Level Input Current		-1.0	µA
I_{IH}, High Level Input Current		1.0	µA
CMOS Output Specifications			
V_{OL}, Low Level Output Voltage		0.4	Volts
V_{OH}, High Level Output Voltage	3.5		Volts
Output Current			
Pins 15, 17, 19, 20, 26, 28, 29, 50, 53, 54, 55, 56, 58, 59, 60, 63		2	mA
Pins 16, 22, 37, 38, 39, 40, 44, 45, 46, 47, 52, 62		4	mA
Pins 2, 3, 4, 5, 6, 12, 13, 14, 42		8	mA
Pin 48		16	mA
Pins 8, 25		24	mA

Note: 1. Sleep Mode
The following pins are functional and active during sleep mode: all V_{CC} and GND; 18, 21, 31, 48, 51, 58. All other inputs are protected so that regardless of source voltage, within normal 0 to V_{CC} limits, and impedance, including floating, no static current larger than normal static current will be drawn from the power supply. All other outputs are three-stated by a special internal control line from the sleep mode control circuits.

AC Electrical Characteristics

$0°C \le T_A \le +70°C$, $4.0V \le V_{CC} \le 6.0$
$T_{CLK} = 1/f_{MCLK}$

Parameter	Min	Max	Units
t_{ALE}, ALE High Pulse Width	50		ns
t_{AV}, Address Valid to ALE Low	10		ns
t_{AH}, Address Hold After ALE Low	10		ns
t_{AWL}, ALE Low to WR Low	20		ns
t_W, WR Pulse Width	2 T_{CLK}		sec
t_R, RD Pulse Width	2 T_{CLK}		sec
t_{DVW}, Data Valid to WR Transition	0		ns
t_{DVR}, Data Valid to RD Transition		10	ns
t_H, Data Hold After WR	10		ns
t_{WAH}, WR High to ALE High	10		ns
t_{RAH}, RD High to ALE High	10		ns
t_{RVD}, RD to Valid Data	0	T_{CLK}	sec
t_{DH}, Data Hold After RD	0	T_{CLK}	sec
t_{ARL}, ALE Low to RD Low	20		ns

Figure 6. Write Cycle Timing Diagram

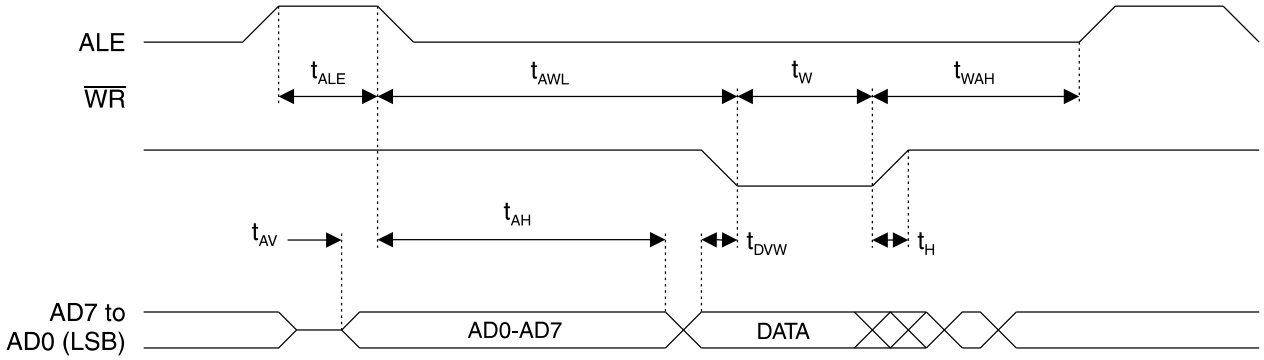
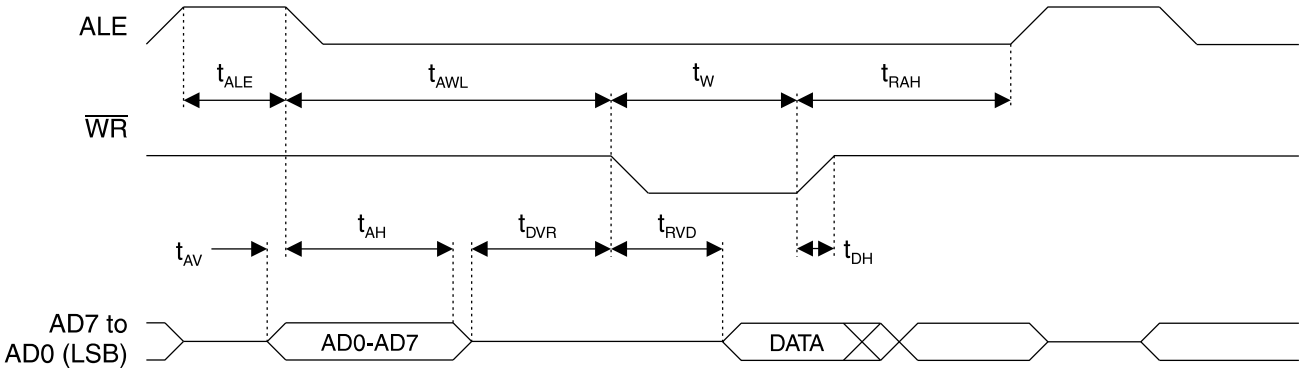


Figure 7. Read Cycle Timing Diagram



Ordering Information

Speed (MHz)	Power Supply	Ordering Code	Package	Operation Range
16	5V ± 20%	AT48802-16QC	64Q	Commercial (0°C to 70°C)
		AT48802-16QI	64Q	Industrial (-40°C to 85°C)

Package Type	
64Q	64 Lead, Plastic Gull Wing Quad Flatpack (PQFP)