PHP/PHB/PHD108NQ03LT

TrenchMOS™ logic level FET

Rev. 02 — 11 September 2002 **Product data**

1. Product profile

1.1 Description

N-channel enhancement mode field-effect transistor in a plastic package using TrenchMOS™ technology.

Product availability:

PHP108NQ03LT in SOT78 (TO-220AB)
PHB108NQ03LT in SOT404 (D^2-PAK)
PHD108NQ03LT in SOT428 (D-PAK).

1.2 Features

- Logic level compatible
- Very low on-state resistance

1.3 Applications

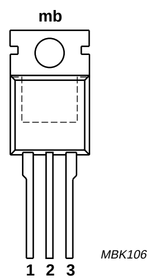
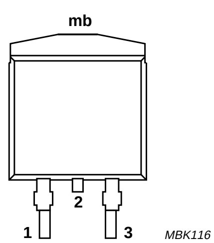
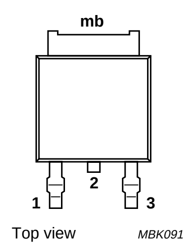
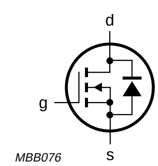
- DC to DC converters
- Switched mode power supplies

1.4 Quick reference data

- V_{DS} = 25 V
- I_D = 75 A
- P_{tot} = 180 W
- $R_{DSon} \leq 6$ mΩ

2. Pinning information

Table 1: Pinning - SOT78, SOT404, SOT428, simplified outline and symbol

Pin	Description	Simplified outline			Symbol
1	gate (g)	 SOT78 (TO-220AB)	 SOT404 (D^2-PAK)	 SOT428 (D-PAK)	
2	drain (d) [1]				
3	source (s)				
mb	mounting base, connected to drain (d)				

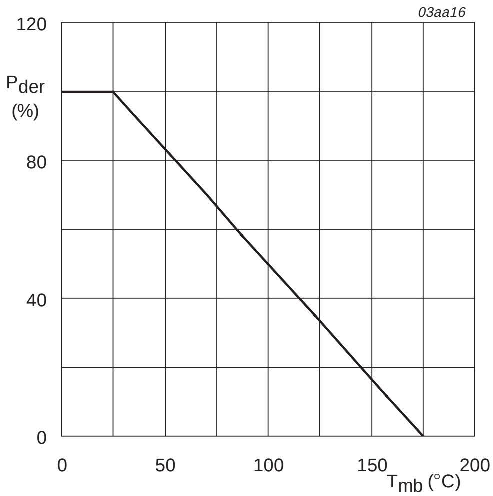
[1] It is not possible to make connection to pin 2 of the SOT404 or SOT428 packages.

3. Limiting values

Table 2: Limiting values

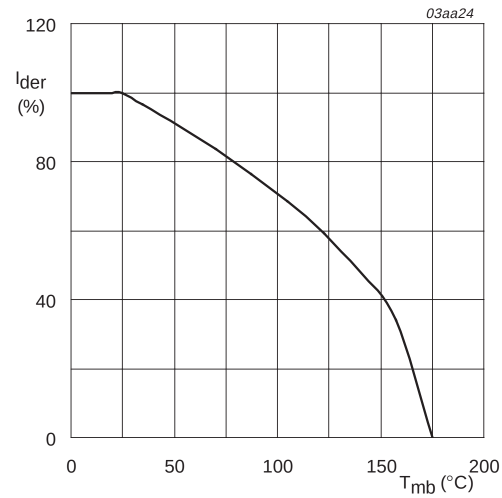
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage (DC)	25 °C ≤ T_j ≤ 175 °C	-	25	V
V_{DGR}	drain-gate voltage (DC)	25 °C ≤ T_j ≤ 175 °C; R_{GS} = 20 kΩ	-	25	V
I_D	drain current (DC)	T_{mb} = 25 °C; V_{GS} = 5 V; Figure 2 and 3	-	75	A
		T_{mb} = 100 °C; V_{GS} = 5 V; Figure 2 and 3	-	60	A
V_{GS}	gate-source voltage		-	±20	V
I_{DM}	peak drain current	T_{mb} = 25 °C; pulsed; t_p ≤ 10 µs; Figure 3	-	108	A
P_{tot}	total power dissipation	T_{mb} = 25 °C; Figure 1	-	180	W
T_{stg}	storage temperature		–55	+175	°C
T_j	junction temperature		–55	+175	°C
Source-drain diode					
I_S	source (diode forward) current (DC)	T_{mb} = 25 °C	-	75	A
I_{SM}	peak source (diode forward) current	T_{mb} = 25 °C; pulsed; t_p ≤ 10 µs	-	108	A
Avalanche ruggedness					
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	unclamped inductive load; I_D = 43 A; t_p = 0.25 ms; V_{DD} ≤ 15 V; R_{GS} = 50 Ω; V_{GS} = 10 V; starting T_j = 25 °C	-	180	mJ



$$P_{der} = \frac{P_{tot}}{P_{tot(25^\circ C)}} \times 100\%$$

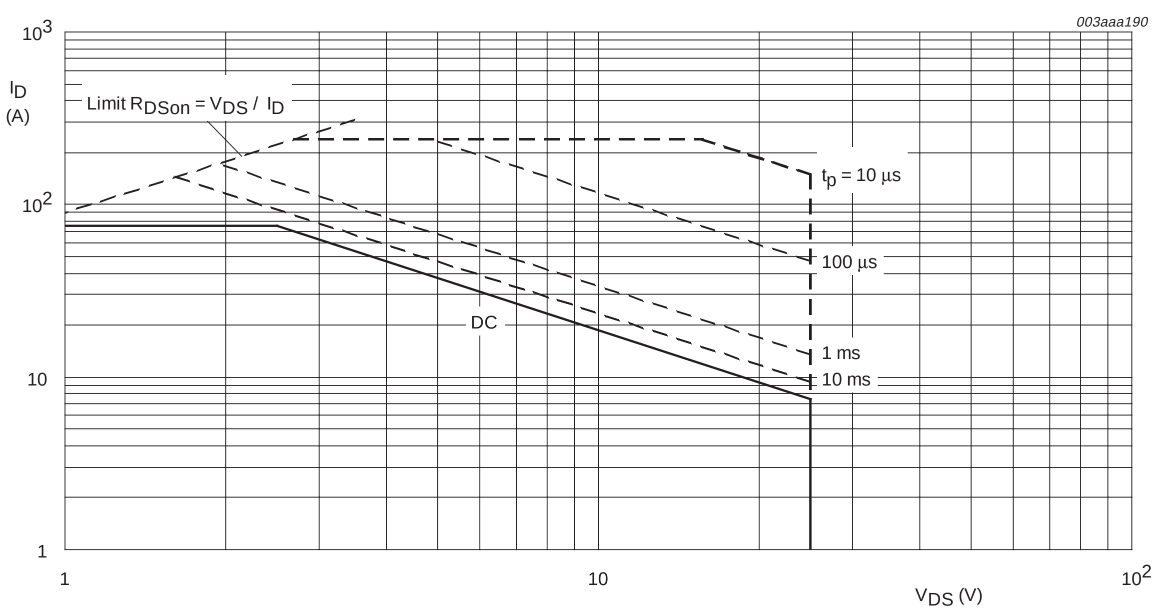
Fig 1. Normalized total power dissipation as a function of mounting base temperature.



$V_{GS} \geq 5$ V

$$I_{der} = \frac{I_D}{I_{D(25^\circ C)}} \times 100\%$$

Fig 2. Normalized continuous drain current as a function of mounting base temperature.



T_{mb} = 25 °C; I_{DM} is single pulse

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage.

4. Thermal characteristics

Table 3: Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Figure 4	-	-	0.8	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient					
	SOT78	vertical in still air	-	60	-	K/W
	SOT428	SOT428 minimum footprint; mounted on a PCB	-	75	-	K/W
	SOT404 and SOT428	SOT404 minimum footprint; mounted on a PCB	-	50	-	K/W

4.1 Transient thermal impedance

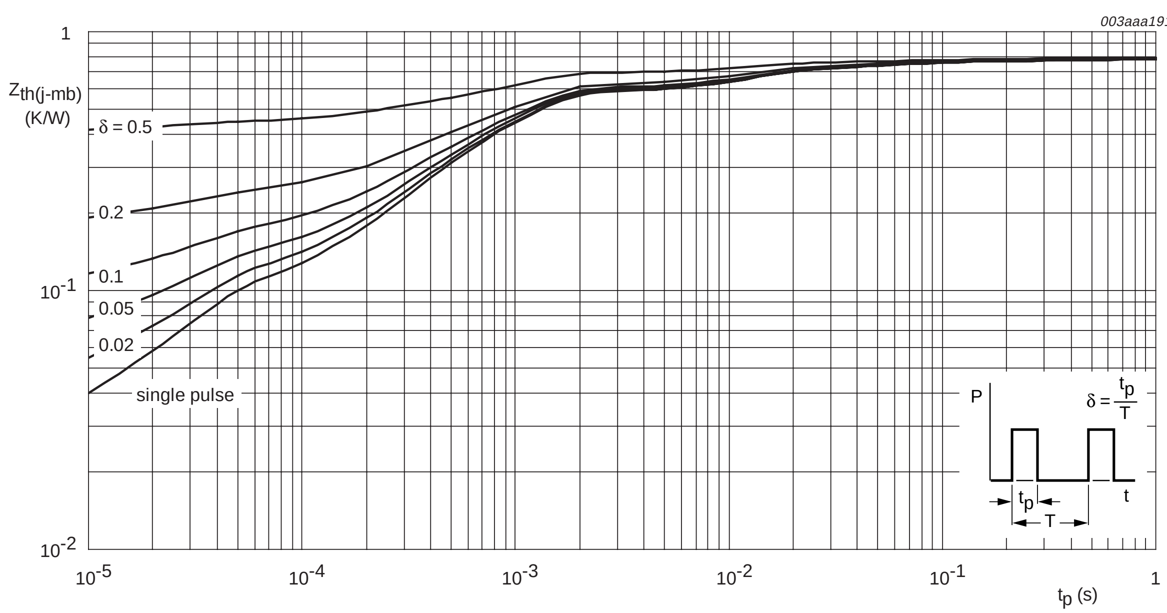


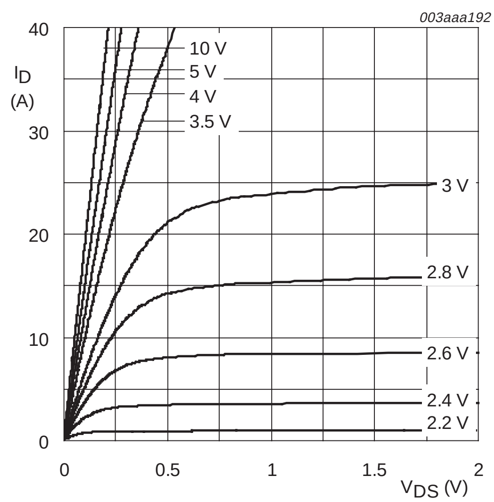
Fig 4. Transient thermal impedance from junction to mounting base as a function of pulse duration.

5. Characteristics

Table 4: Characteristics

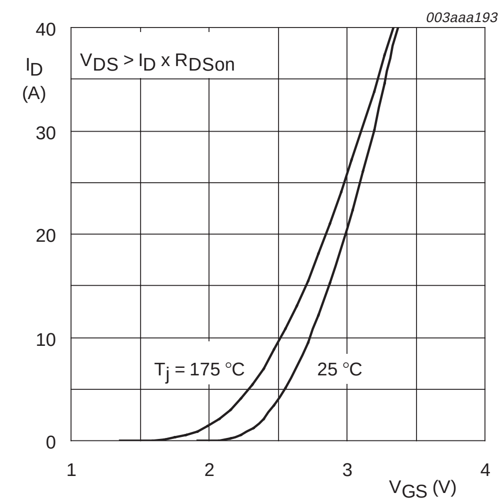
T_j = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 250 µA; V_{GS} = 0 V				
		T_j = 25 °C	25	-	-	V
		T_j = –55 °C	22	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA; V_{DS} = V_{GS}; Figure 9	1	-	2	V
I_{DSS}	drain-source leakage current	V_{DS} = 25 V; V_{GS} = 0 V				
		T_j = 25 °C	-	0.05	1	µA
		T_j = 175 °C	-	-	500	µA
I_{GSS}	gate-source leakage current	V_{GS} = ±10 V; V_{DS} = 0 V	-	0.02	100	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = 5 V; I_D = 25 A; Figure 7 and 8				
		T_j = 25 °C	-	6.2	7.5	mΩ
		T_j = 175 °C	-	10	14	mΩ
		V_{GS} = 10 V; I_D = 25 A	-	5.1	6.0	mΩ
Dynamic characteristics						
$Q_{g(tot)}$	total gate charge	I_D = 40 A; V_{DD} = 15 V; V_{GS} = 5 V; Figure 13	-	23	-	nC
Q_{gs}	gate-source charge		-	8.4	-	nC
Q_{gd}	gate-drain (Miller) charge		-	7.3	9.9	nC
C_{iss}	input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz; Figure 11	-	1990	-	pF
C_{oss}	output capacitance		-	580	-	pF
C_{rss}	reverse transfer capacitance		-	230	-	pF
$t_{d(on)}$	turn-on delay time	V_{DD} = 15 V; R_D = 0.6 Ω; V_{GS} = 5 V; R_G = 10 Ω	-	24	-	ns
t_r	rise time		-	102	-	ns
$t_{d(off)}$	turn-off delay time		-	53	-	ns
t_f	fall time		-	54	-	ns
Source-drain diode						
V_{SD}	source-drain (diode forward) voltage	I_S = 25 A; V_{GS} = 0 V; Figure 12	-	0.9	1.2	V
t_{rr}	reverse recovery time	I_S = 20 A; dI_S/dt = –100 A/µs; V_{GS} = 0 V; V_{DS} = 25 V	-	34	-	ns
Q_r	recovered charge		-	27	-	nC



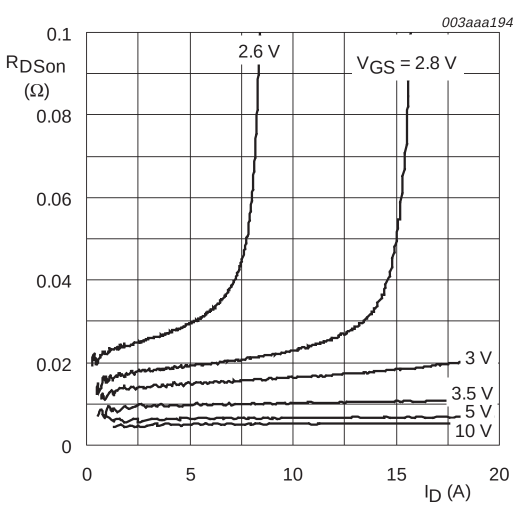
T_j = 25 °C

Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values.



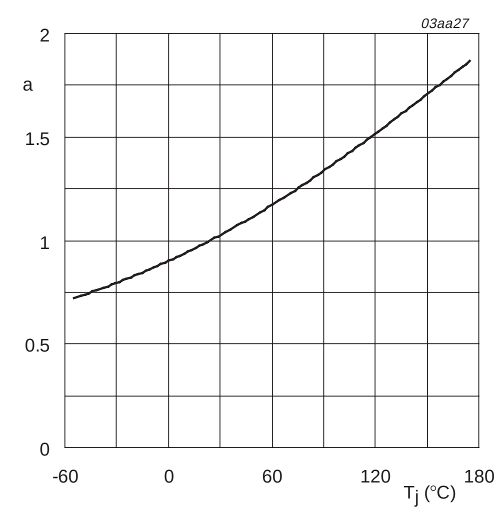
T_j = 25 °C and 175 °C; $V_{DS} > I_D \times R_{DSon}$

Fig 6. Transfer characteristics: drain current as a function of gate-source voltage; typical values.



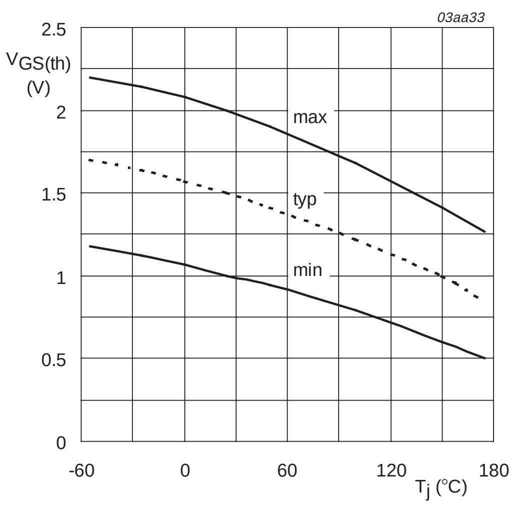
T_j = 25 °C

Fig 7. Drain-source on-state resistance as a function of drain current; typical values.



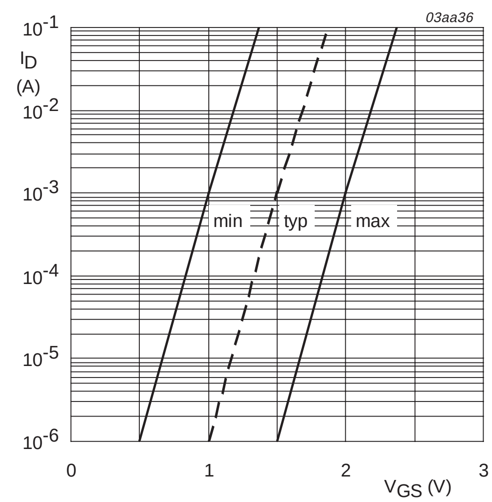
$$a = \frac{R_{DSon}}{R_{DSon(25°C)}}$$

Fig 8. Normalized drain source on-state resistance factor as a function of junction temperature.



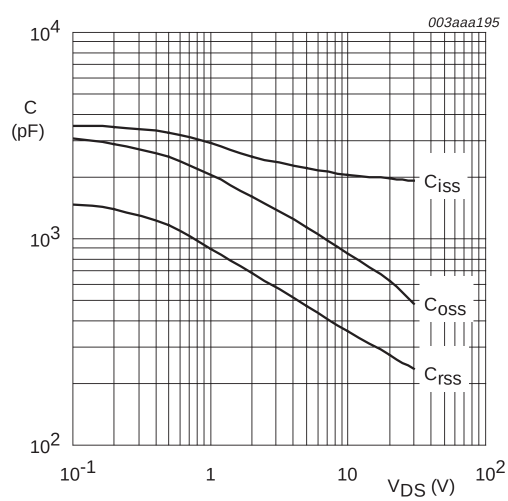
I_D = 1 mA; $V_{DS} = V_{GS}$

Fig 9. Gate-source threshold voltage as a function of junction temperature.



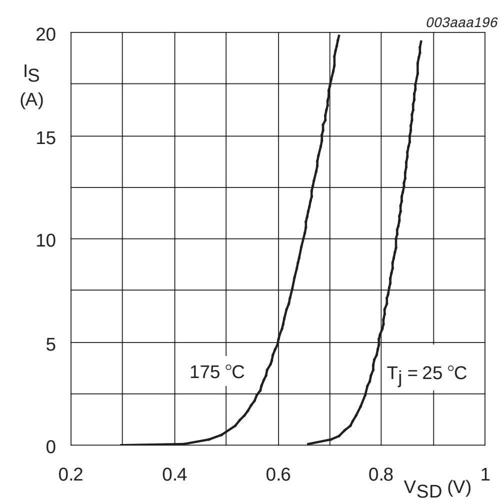
T_j = 25 °C; V_{DS} = 5 V

Fig 10. Sub-threshold drain current as a function of gate-source voltage.



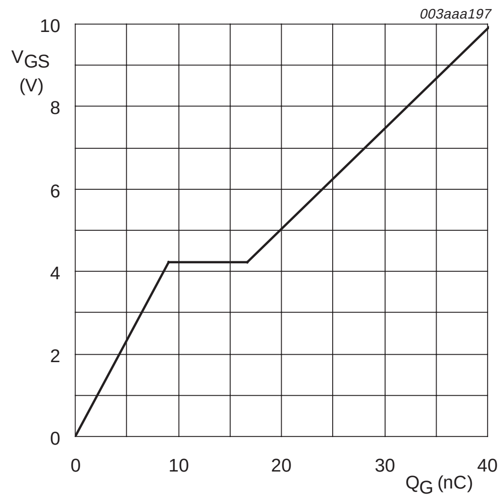
V_{GS} = 0 V; f = 1 MHz

Fig 11. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values.



T_j = 25 °C and 175 °C; V_{GS} = 0 V

Fig 12. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values.

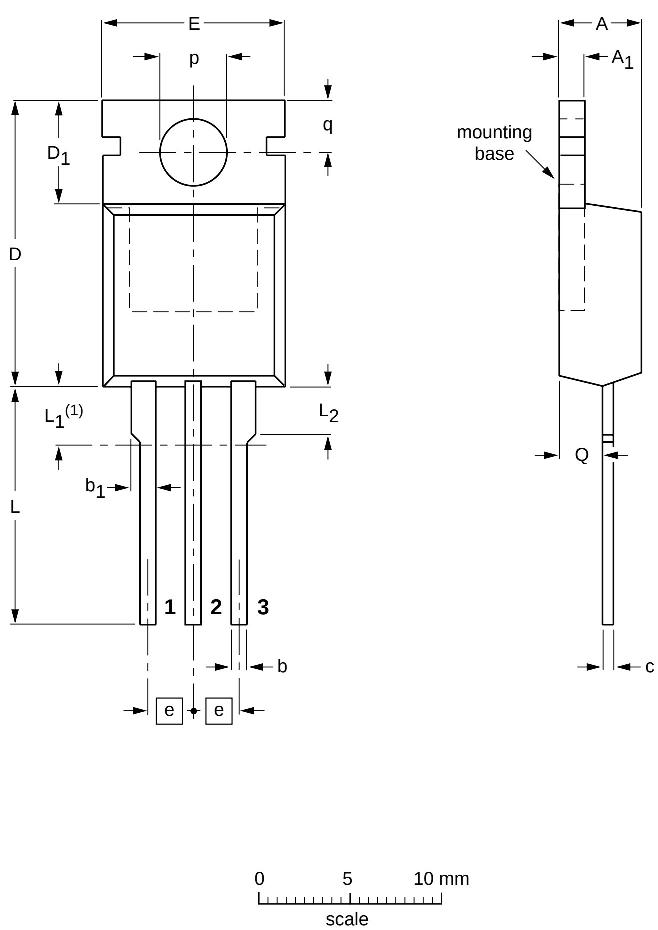


I_D = 40 A; V_{DD} = 15 V

Fig 13. Gate-source voltage as a function of gate charge; typical values.

6. Package outline

Plastic single-ended package; heatsink mounted; 1 mounting hole; 3-lead TO-220AB **SOT78**



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1	b	b_1	c	D	D_1	E	e	L	L_1(1)	L_2 max.	p	q	Q
mm	4.5 4.1	1.39 1.27	0.9 0.7	1.3 1.0	0.7 0.4	15.8 15.2	6.4 5.9	10.3 9.7	2.54	15.0 13.5	3.30 2.79	3.0	3.8 3.6	3.0 2.7	2.6 2.2

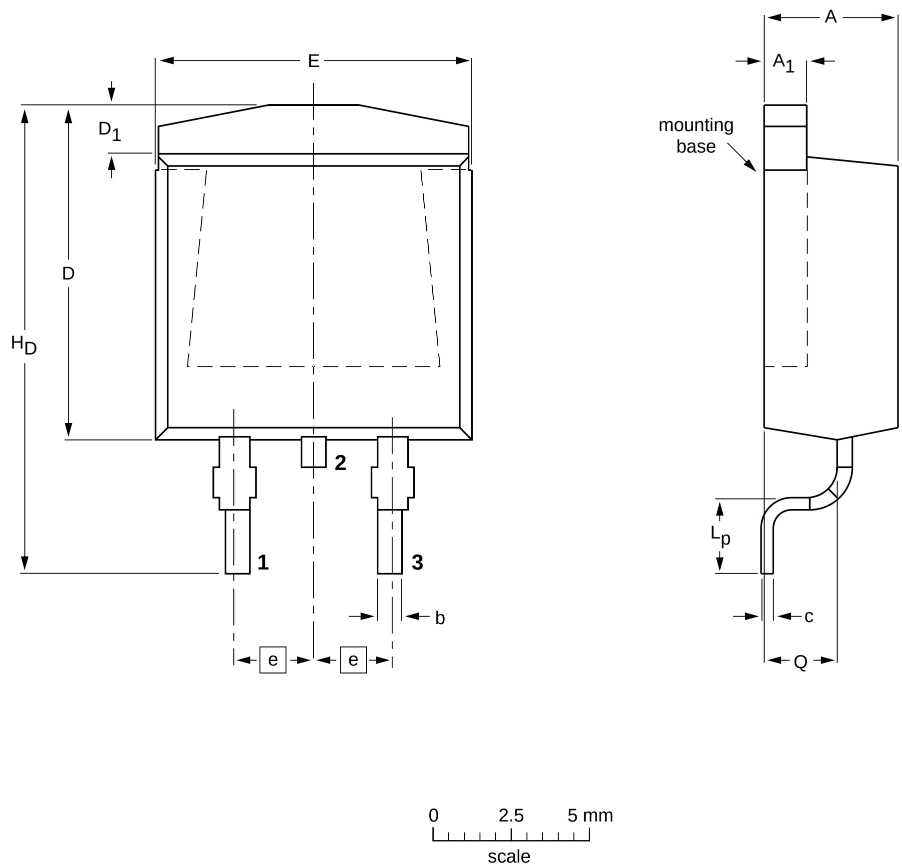
Note

1. Terminals in this zone are not tinned.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT78		3-lead TO-220AB	SC-46			~~00-09-07~~ 01-02-16

Fig 14. SOT78 (TO-220AB).

Plastic single-ended surface mounted package (Philips version of D2-PAK); 3 leads (one lead cropped) **SOT404**



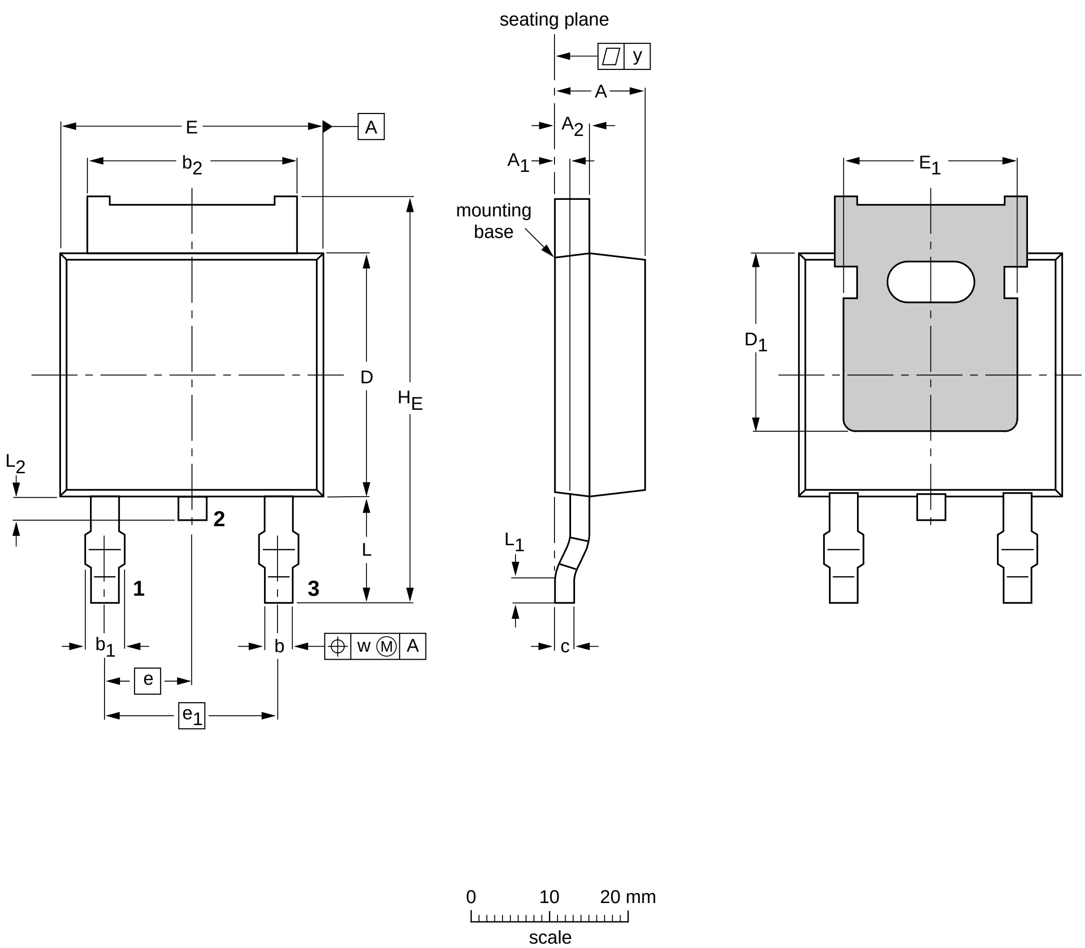
DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1	b	c	D max.	D_1	E	e	L_p	H_D	Q
mm	4.50 4.10	1.40 1.27	0.85 0.60	0.64 0.46	11	1.60 1.20	10.30 9.70	2.54	2.90 2.10	15.80 14.80	2.60 2.20

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT404						~~99-06-25~~ 01-02-12

Fig 15. SOT404 (D2-PAK).

Plastic single-ended surface mounted package (Philips version of D-PAK); 3 leads (one lead cropped) **SOT428**



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1(1)	A_2	b	b_1	b_2	c	D	D_1 min.	E	E_1	e	e_1	H_E	L	L_1 min.	L_2	w	y max.
mm	2.38 2.22	0.65 0.45	0.93 0.73	0.89 0.71	1.1 0.9	5.46 5.26	0.4 0.2	6.22 5.98	4.0	6.73 6.47	4.81 4.45	2.285	4.57	10.4 9.6	2.95 2.55	0.5	0.9 0.5	0.2	0.2

Note

1. Measured from heatsink back to lead.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT428		TO-252	SC-63			~~99-09-13~~ 01-12-11

Fig 16. SOT428 (D-PAK).

7. Revision history

Table 5: Revision history

Rev	Date	CPCN	Description
02	20020911	-	**Product data; second version; supersedes version of 18 December 2001.** Section 3 “Limiting values” Addition of $E_{DS(AL)S}$. Graphs updated to latest standard.
01	20011218	-	**Product data; initial version**

8. Data sheet status

Data sheet status[1]	Product status[2]	Definition
Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Changes will be communicated according to the Customer Product/Process Change Notification (CPCN) procedure SNW-SQ-650A.

[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

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For sales office addresses, send e-mail to: **sales.addresses@www.semiconductors.philips.com**.

Fax: +31 40 27 24825

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