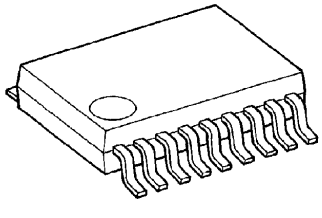
TENTATIVE TOSHIBA BIPOLAR DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

TD62382AFN

8 LOW INPUT ACTIVE DARLINGTON SINK DRIVER

The TD62382AFN is non-inverting transistor array which is comprised of eight Low saturation output stages and PNP input stages.
This device is low level input active driver and is suitable for operation with TTL, 5V CMOS and 5V Microprocessor which have sink current output drivers.
Applications include relay, hammer, lamp and LED display drivers.



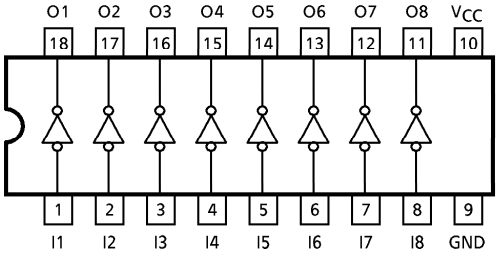
SSOP18-P-225-0.65

Weight : 0.09g (Typ.)

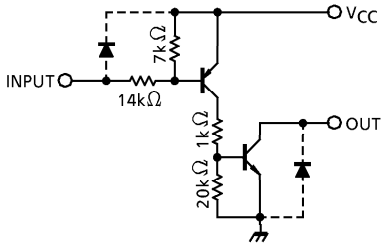
FEATURES

- Low Saturation Output : 0.23V (MAX.) @ Iout = 40mA (MAX.)
- Package Type : SSOP18 pin
- Output Rating : 50V (MIN.) / 50mA (MAX.)
- Low Level Active Input
- Input Compatible with TTL and 5V CMOS
- Standard Supply Voltage

PIN CONNECTION (TOP VIEW)



SCHEMATICS (EACH DRIVER)



(Note) The input and output parasitic diodes cannot be used as clamp diodes.

961001EBA2

MAXIMUM RATINGS (Ta = 25°C)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	V_{CC}	−0.5~7.0	V
Output Sustaining Voltage	$V_{CE\ (SUS)}$	−0.5~50	V
Output Current	I_{OUT}	50	mA / ch
Input Voltage	V_{IN}	−22~V_{CC} + 0.5	V
Input Current	I_{IN}	10	mA
Power Dissipation	P_D *	0.96	W
Operating Temperature	T_{opr}	−40~85	°C
Storage Temperature	T_{stg}	−55~150	°C

* On Glass Epoxy PCB (50 × 50 × 1.6mm Cu 40%)

RECOMMENDED OPERATING CONDITIONS (Ta = −40~85°C)

CHARACTERISTIC		SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Supply Voltage		V_{CC}		4.5	5.0	5.5	V
Output Sustaining Voltage		$V_{CE\ (SUS)}$		0	—	50	V
Output Current		I_{OUT}	DC 1 Circuit	0	—	40	mA / ch
			8 Circuits	0	—	40	
Input Voltage		V_{IN}		−20	—	V_{CC}	V
	Output On	$V_{IN\ (ON)}$		−20	—	V_{CC} − 3.5	
	Output Off	$V_{IN\ (OFF)}$		V_{CC} − 0.3	—	V_{CC} + 0.5	
Power Dissipation		P_D *		—	—	0.4	W

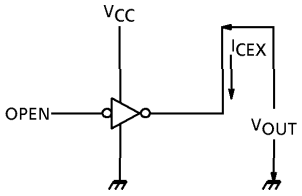
* On Glass Epoxy PCB (50 × 50 × 1.6mm Cu 40%)

ELECTRICAL CHARACTERISTICS (Ta = 25°C)

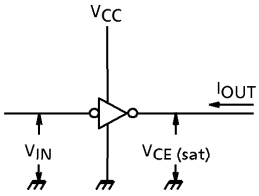
CHARACTERISTIC		SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Leakage Current		I_{CEX}	1	V_{CC} = 5.5V, I_{IN} = 0 V_{OUT} = 35V, Ta = 75°C	—	—	100	μA
Output Saturation Voltage		$V_{CE\ (sat)}$	2	V_{CC} = 4.5V, V_{IN} = 0.8V I_{OUT} = 40mA	—	—	0.23	V
Input Current	Output On	$I_{IN\ (ON)}$	3	V_{CC} = 5.5V, V_{IN} = 0.4V	—	−0.32	−0.45	mA
				V_{CC} = 5.5V, V_{IN} = −20V	—	—	−2.6	
	Output Off	$I_{IN\ (OFF)}$	4		—	—	−40	μA
Input Voltage (Output On)		$V_{IN\ (ON)}$	5		−20	—	V_{CC} − 3.5	V
Supply Current	Output On	$I_{CC\ (ON)}$	6	V_{CC} = 5.5V, V_{IN} = 0V	—	—	6	mA / ch
	Output Off	$I_{CC\ (OFF)}$		V_{CC} = V_{IN} = 5.5V, Ta = 75°C	—	—	100	μA
Turn-On Delay		t_{ON}	7	V_{CC} = 5V, V_{OUT} = 50V, R_L = 1kΩ	—	0.1	—	μs
Turn-Off Delay		t_{OFF}		C_L = 15pF, V_{OUT} = 50V, R_L = 1kΩ	—	3.0	—	

TEST CIRCUIT

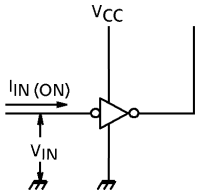
1. I_{CEX}



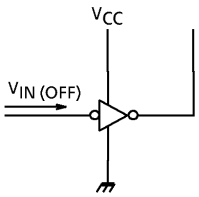
2. $V_{CE\ (sat)}$



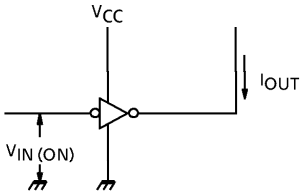
3. $I_{IN\ (ON)}$



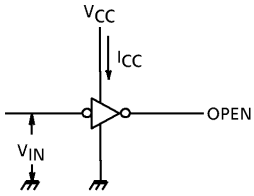
4. $I_{IN\ (OFF)}$



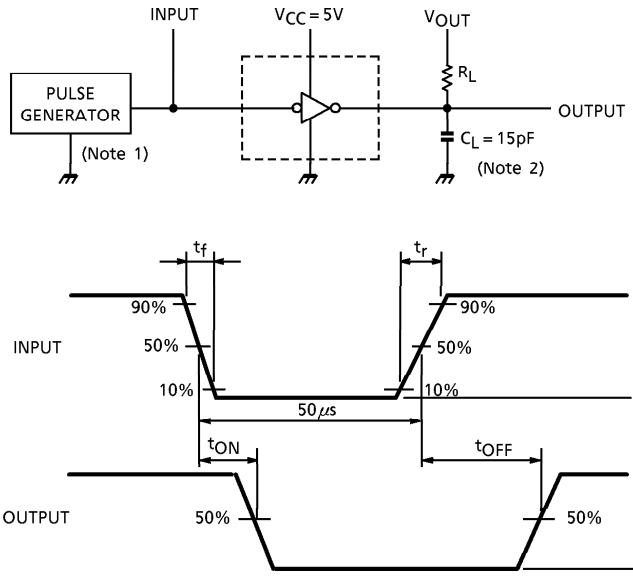
5. $V_{IN\ (ON)}$



6. I_{CC}



7. t_{ON}, t_{OFF}



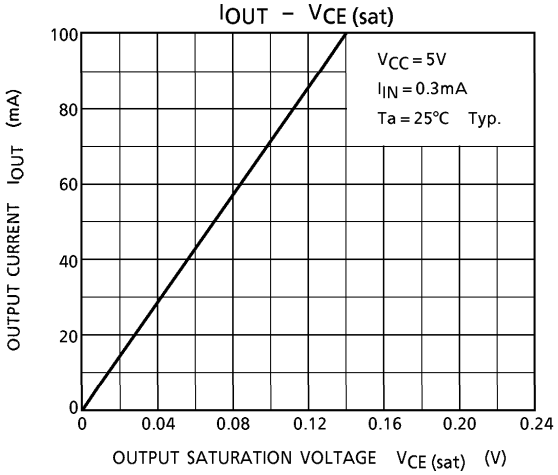
(Note 1) Pulse Width 50μs, Duty Cycle 10%
Output Impedance 50Ω, $t_r \leqq$ 10ns, $t_f \leqq$ 5ns

(Note 2) CL includes probe and jig capacitance.

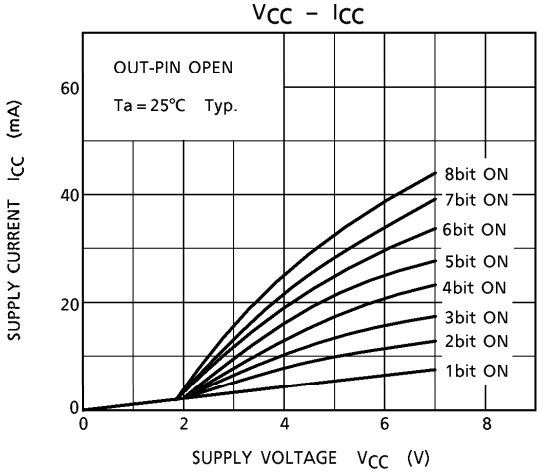
PRECAUTIONS for USING

Utmost care is necessary in the design of the output line, V_{CC} and GND line since IC may be destroyed due to short-circuit between outputs, air contamination fault, or fault by improper grounding.

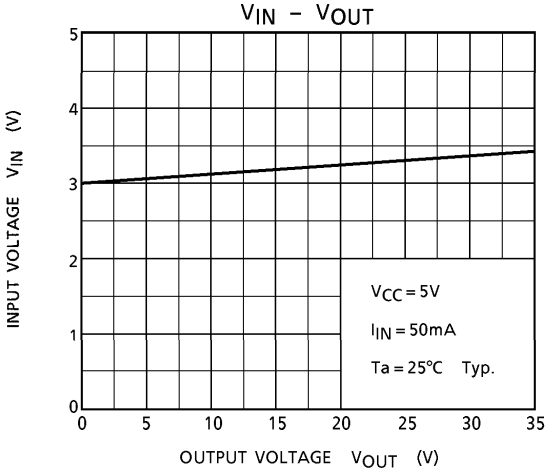
I_{OUT} – $V_{CE\ (sat)}$



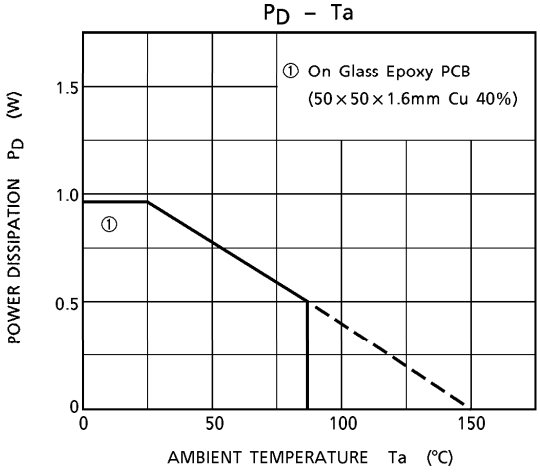
V_{CC} – I_{CC}



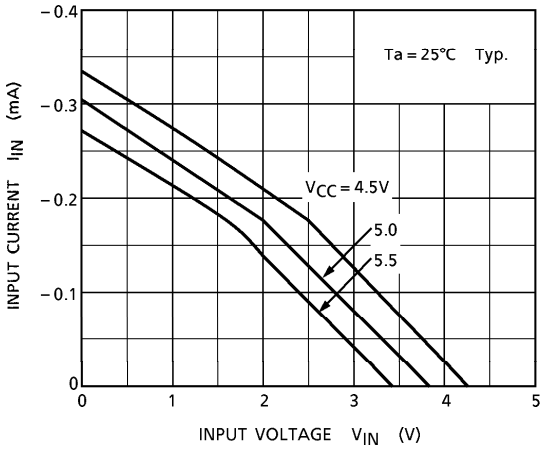
V_{IN} – V_{OUT}



P_D – Ta

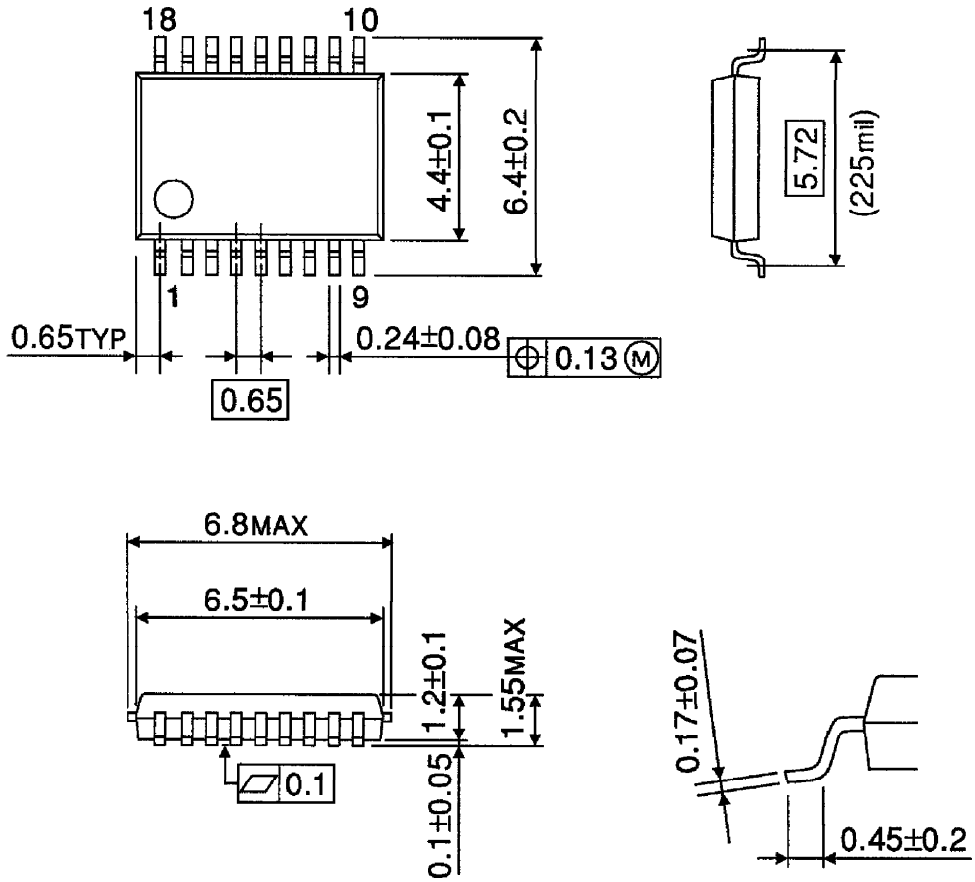


I_{IN} – V_{IN}



OUTLINE DRAWING

SSOP18-P-225-0.65 Unit : mm



Weight : 0.09g (Typ.)