



## Input Loading/Fan-Out

Pin Names	Description	HIGH/LOW	
		U.L. HIGH/LOW	Input $I_{IH}/I_{IL}$ Output $I_{OH}/I_{OL}$
A <sub>0</sub> –A <sub>7</sub>	Data Inputs/ Data Outputs	1.0/1.0 150/40	20 $\mu$ A/–0.6 mA –3 mA/24 mA
B <sub>0</sub> –B <sub>7</sub>	Data Inputs/ Data Outputs	1.0/1.0 600/106.6	20 $\mu$ A/–0.6 mA –12 mA/64 mA
APAR	A Bus Parity Input/Output	1.0/1.0 150/40	20 $\mu$ A/–0.6 mA –3 mA/24 mA
BPAR	B Bus Parity Input/Output	1.0/1.0 600/106.6	20 $\mu$ A/–0.6 mA –12 mA/64 mA
ODD/ $\overline{\text{EVEN}}$	Parity Select Input	1.0/1.0	20 $\mu$ A/–0.6 mA
$\overline{\text{GBA}}$ , $\overline{\text{GAB}}$	Output Enable Inputs	1.0/1.0	20 $\mu$ A/–0.6 mA
$\overline{\text{SEL}}$	Mode Select Input	1.0/1.0	20 $\mu$ A/–0.6 mA
LEA, LEB	Latch Enable Inputs	1.0/1.0	20 $\mu$ A/–0.6 mA
$\overline{\text{ERRA}}$ , $\overline{\text{ERRB}}$	Error Signal Outputs	50/33.3	–1 mA/20 mA

## Pin Descriptions

Pin Names	Description
A <sub>0</sub> –A <sub>7</sub>	A Bus Data Inputs/Data Outputs
B <sub>0</sub> –B <sub>7</sub>	B Bus Data Inputs/Data Outputs
APAR, BPAR	A and B Bus Parity Inputs
ODD/ $\overline{\text{EVEN}}$	ODD/ $\overline{\text{EVEN}}$ Parity Select, Active LOW for EVEN Parity
$\overline{\text{GBA}}$ , $\overline{\text{GAB}}$	Output Enables for A or B Bus, Active LOW
$\overline{\text{SEL}}$	Select Pin for Feed-Through or Generate Mode, LOW for Generate Mode
LEA, LEB	Latch Enables for A and B Latches, HIGH for Transparent Mode
$\overline{\text{ERRA}}$ , $\overline{\text{ERRB}}$	Error Signals for Checking Generated Parity with Parity In, LOW if Error Occurs

## Functional Description

The 74F899 has three principal modes of operation which are outlined below. These modes apply to both the A-to-B and B-to-A directions.

- Bus A (B) communicates to Bus B (A), parity is generated and passed on to the B (A) Bus as BPAR (APAR). If LEB (LEA) is HIGH and the Mode Select ( $\overline{\text{SEL}}$ ) is LOW, the parity generated from B[0:7] (A[0:7]) can be checked and monitored by  $\overline{\text{ERRB}}$  ( $\overline{\text{ERRA}}$ ).
- Bus A (B) communicates to Bus B (A) in a feed-through mode if  $\overline{\text{SEL}}$  is HIGH. Parity is still generated and checked as  $\overline{\text{ERRA}}$  and  $\overline{\text{ERRB}}$  in the feed-through mode (can be used as an interrupt to signal a data/parity bit error to the CPU).
- Independent Latch Enables (LEA and LEB) allow other permutations of generating/checking (see Function Table).

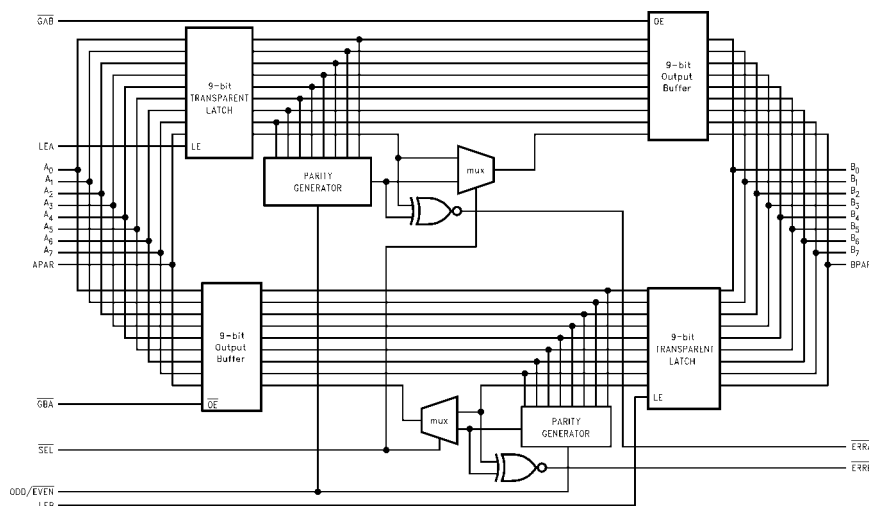
**Function Table**

Inputs					Operation
$\overline{\text{GAB}}$	$\overline{\text{GBA}}$	$\overline{\text{SEL}}$	LEA	LEB	
H	H	X	X	X	Busses A and B are 3-STATE.
H	L	L	L	H	Generates parity from B[0:7] based on $O/\overline{E}$ (Note 1). Generated parity $\rightarrow$ APAR. Generated parity checked against BPAR and output as $\overline{\text{ERRB}}$ .
H	L	L	H	H	Generates parity from B[0:7] based on $O/\overline{E}$ . Generated parity $\rightarrow$ APAR. Generated parity checked against BPAR and output as $\overline{\text{ERRB}}$ . Generated parity also fed back through the A latch for generate/check as $\overline{\text{ERRA}}$ .
H	L	L	X	L	Generates parity from B latch data based on $O/\overline{E}$ . Generated parity $\rightarrow$ APAR. Generated parity checked against latched BPAR and output as $\overline{\text{ERRB}}$ .
H	L	H	X	H	BPAR/B[0:7] $\rightarrow$ APAR/A[0:7] Feed-through mode. Generated parity checked against BPAR and output as $\overline{\text{ERRB}}$ .
H	L	H	H	H	BPAR/B[0:7] $\rightarrow$ APAR/A[0:7] Feed-through mode. Generated parity checked against BPAR and output as $\overline{\text{ERRB}}$ . Generated parity also fed back through the A latch for generate/check as $\overline{\text{ERRA}}$ .
L	H	L	H	L	Generates parity for A[0:7] based on $O/\overline{E}$ . Generated parity $\rightarrow$ BPAR. Generated parity checked against APAR and output as $\overline{\text{ERRA}}$ .
L	H	L	H	H	Generates parity from A[0:7] based on $O/\overline{E}$ . Generated parity $\rightarrow$ BPAR. Generated parity checked against APAR and output as $\overline{\text{ERRA}}$ . Generated parity also fed back through the B latch for generate/check as $\overline{\text{ERRB}}$ .
L	H	L	L	X	Generates parity from A latch data based on $O/\overline{E}$ . Generated parity $\rightarrow$ BPAR. Generated parity checked against latched APAR and output as $\overline{\text{ERRA}}$ .
L	H	H	H	L	APAR/A[0:7] $\rightarrow$ BPAR/B[0:7] Feed-through mode. Generated parity checked against APAR and output as $\overline{\text{ERRA}}$ .
L	H	H	H	H	APAR/A[0:7] $\rightarrow$ BPAR/B[0:7] Feed-through mode. Generated parity checked against APAR and output as $\overline{\text{ERRA}}$ . Generated parity also fed back through the B latch for generate/check as $\overline{\text{ERRB}}$ .

H = HIGH Voltage Level      L = LOW Voltage Level      X = Immaterial

**Note 1:**  $O/\overline{E}$  = ODD/EVEN

**Functional Block Diagram**



**Absolute Maximum Ratings** (Note 2)

Storage Temperature	-65°C to +150°C
Ambient Temperature under Bias	-55°C to +125°C
Junction Temperature under Bias	-55°C to +150°C
V <sub>CC</sub> Pin Potential to Ground Pin	-0.5V to +7.0V
Input Voltage (Note 3)	-0.5V to +7.0V
Input Current (Note 3)	-30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V <sub>CC</sub> = 0V)	
Standard Output	-0.5V to V <sub>CC</sub>
3-STATE Output	-0.5V to +5.5V
Current Applied to Output in LOW State (Max)	Twice the Rated I <sub>OL</sub> (mA)
ESD Last Passing Voltage (Min)	4000V

**Recommended Operating Conditions**

Free Air Ambient Temperature	0°C to +70°C
Supply Voltage	+4.5V to +5.5V

**Note 2:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 3:** Either voltage limit or current limit is sufficient to protect inputs.

**DC Electrical Characteristics**

Symbol	Parameter	Min	Typ	Max	Units	V <sub>CC</sub>	Conditions
V <sub>IH</sub>	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V <sub>IL</sub>	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V <sub>CD</sub>	Input Clamp Diode Voltage			-1.2	V	Min	I <sub>IN</sub> = -18 mA
V <sub>OH</sub>	Output HIGH Voltage	10% V <sub>CC</sub>	2.5		V		I <sub>OH</sub> = -1 mA
		10% V <sub>CC</sub>	2.4				I <sub>OH</sub> = -3 mA
		10% V <sub>CC</sub>	2.0				I <sub>OH</sub> = -15 mA (B <sub>n</sub> , B <sub>PAR</sub> )
		5% V <sub>CC</sub>	2.7				I <sub>OH</sub> = -1 mA
		5% V <sub>CC</sub>	2.7				I <sub>OH</sub> = -3 mA
V <sub>OL</sub>	Output LOW Voltage	10% V <sub>CC</sub>		0.5	V		I <sub>OL</sub> = 20 mA (A <sub>n</sub> , APAR, <u>ERRA</u> , <u>ERRB</u> )
		5% V <sub>CC</sub>		0.55			I <sub>OL</sub> = 24 mA (A <sub>n</sub> , APAR, <u>ERRA</u> , <u>ERRB</u> )
		10% V <sub>CC</sub>		0.55			I <sub>OL</sub> = 64 mA (B <sub>n</sub> , B <sub>PAR</sub> )
V <sub>TH</sub>	Input Threshold Voltage		1.45		V		±0.1V, Sweep Edge Rate must be > 1V/50 ns
V <sub>OLV</sub>	Negative Ground Bounce Voltage		1.0		V		Observed on "quiet" output during simultaneous switching of remaining outputs
V <sub>OLP</sub>	Positive Ground Bounce Voltage		1.0		V		Observed on "quiet" output during simultaneous switching of remaining outputs
I <sub>IL</sub>	Input Low Current			-0.6	mA	Max	V <sub>IN</sub> = 0.5V
I <sub>IH</sub>	Input HIGH Current			5.0	μA	Max	V <sub>IN</sub> = 2.7V
I <sub>BVI</sub>	Input HIGH Current Breakdown Test			7.0	μA	Max	V <sub>IN</sub> = 7.0V ( <u>ODD/EVEN</u> , <u>GAB</u> , <u>GAB</u> , <u>SEL</u> , <u>LEA</u> , <u>LEB</u> )
I <sub>BVIT</sub>	Input HIGH Current Breakdown (I/O)			0.5	mA	Max	V <sub>IN</sub> = 5.5V (A <sub>n</sub> , B <sub>n</sub> , A <sub>PAR</sub> , B <sub>PAR</sub> )
I <sub>CEX</sub>	Output HIGH Leakage Current			50	μA	Max	V <sub>OUT</sub> = V <sub>CC</sub>
V <sub>ID</sub>	Input Leakage Test	4.75			V	0.0	I <sub>ID</sub> = 1.9 μA All Other Pins Grounded
I <sub>OD</sub>	Output Leakage Circuit Current			3.75	μA	0.0	V <sub>IOD</sub> = 150 mV All Other Pins Grounded
I <sub>IL</sub>	Input Low Current			-0.6	mA	Max	V <sub>IN</sub> = 0.5V
I <sub>IH+</sub> I <sub>OZH</sub>	Output Leakage Current			70	μA	Max	V <sub>I/O</sub> = 2.7V (A <sub>n</sub> , B <sub>n</sub> , APAR, BPAR)

DC Electrical Characteristics (Continued)								
Symbol	Parameter	Min	Typ	Max	Units	V <sub>CC</sub>	Conditions	
I <sub>IL+</sub> I <sub>OZL</sub>	Output Leakage Current			-650	μA	Max	V <sub>I/O</sub> = 0.5V (A <sub>n</sub> , B <sub>n</sub> , APAR, BPAR)	
I <sub>OS</sub>	Output Short-Circuit Current	-60		-150	mA	Max	V <sub>OUT</sub> = 0V (A <sub>n</sub> , APAR, $\overline{\text{ERRA}}$ , $\overline{\text{ERRB}}$ )	
		-100		-225		Max	V <sub>OUT</sub> = 0V (B <sub>n</sub> , BPAR)	
I <sub>ZZ</sub>	Bus Drainage Test			500	μA	0.0V	V <sub>OUT</sub> = 5.25V	
I <sub>CCH</sub>	Power Supply Current		132	155	mA	Max	V <sub>O</sub> = HIGH	
I <sub>CCL</sub>	Power Supply Current		178	210	mA	Max	V <sub>O</sub> = LOW, GAB = LOW, GBA = HIGH, V <sub>IL</sub> = LOW	
I <sub>CCZ</sub>	Power Supply Current		160	190	mA	Max	V <sub>O</sub> = HIGH Z	
AC Electrical Characteristics								
Symbol	Parameter	T <sub>A</sub> = +25°C V <sub>CC</sub> = +5.0V C <sub>L</sub> = 50 pF			T <sub>A</sub> = 0°C to +70°C V <sub>CC</sub> = +5.0V C <sub>L</sub> = 50 pF		Units	Figure Number
		Min	Typ	Max	Min	Max		
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay A <sub>n</sub> , APAR to B <sub>n</sub> , BPAR	4.0	7.5	13.0	4.0	14.0	ns	Figure 1
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay A <sub>n</sub> , B <sub>n</sub> to BPAR, APAR	7.5	12.0	17.0	7.5	18.0		
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay A <sub>n</sub> , B <sub>n</sub> to $\overline{\text{ERRA}}$ , $\overline{\text{ERRB}}$	7.5	12.0	17.0	7.5	18.0	ns	Figure 3
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay ODD/EVEN to $\overline{\text{ERRA}}$ , $\overline{\text{ERRB}}$	4.5	7.5	11.0	4.5	12.0		
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay ODD/EVEN to APAR, BPAR	4.5	7.5	11.5	4.5	12.5	ns	Figure 5
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay APAR, BPAR to $\overline{\text{ERRA}}$ , $\overline{\text{ERRB}}$	5.5	9.0	13.0	5.5	14.0		
t <sub>PLH</sub> t <sub>PHL</sub>	LEA/LEB to $\overline{\text{ERRA}}$ / $\overline{\text{ERRB}}$	9.5	13.0	17.5	7.5	18.0	ns	Figure 7
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay SEL to APAR, BPAR	3.0	6.0	10.0	3.0	11.0		
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay LEB to A <sub>n</sub> , APAR	3.5	7.0	10.0	3.5	11.0	ns	Figure 11
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay LEA to B <sub>n</sub> , BPAR	3.5	6.5	10.0	3.5	11.0		
t <sub>PZH</sub> t <sub>PZL</sub>	Output Enable Time $\overline{\text{GBA}}$ or $\overline{\text{GAB}}$ to A <sub>n</sub> , APAR or B <sub>n</sub> , BPAR	1.0	4.5	10.0	1.0	11.0	ns	Figure 8, Figure 9
t <sub>PHZ</sub> t <sub>PLZ</sub>	Output Disable Time $\overline{\text{GBA}}$ or $\overline{\text{GAB}}$ to A <sub>n</sub> , APAR or B <sub>n</sub> , BPAR	1.0	4.0	7.0	1.0	8.0		
t <sub>S</sub> (H)	Setup Time, HIGH or LOW	5.0	1.6		5.0		ns	Figure 12, Figure 13
t <sub>S</sub> (L)	A <sub>n</sub> , B <sub>n</sub> to LEA, LEB	5.0	1.8		5.0			
t <sub>H</sub> (H)	Hold Time, HIGH or LOW	0	-1.7		0		ns	Figure 12, Figure 13
t <sub>H</sub> (L)	A <sub>n</sub> , B <sub>n</sub> to LEA, LEB	0	-1.5		0			
t <sub>W</sub>	Pulse Width for LEA, LEB	6.0	2.0		6.0		ns	Figure 14

AC Path

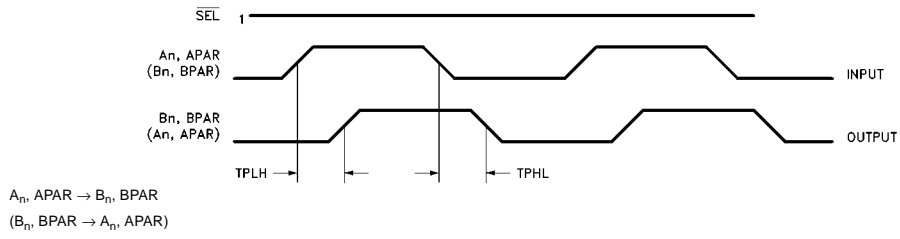


FIGURE 1.

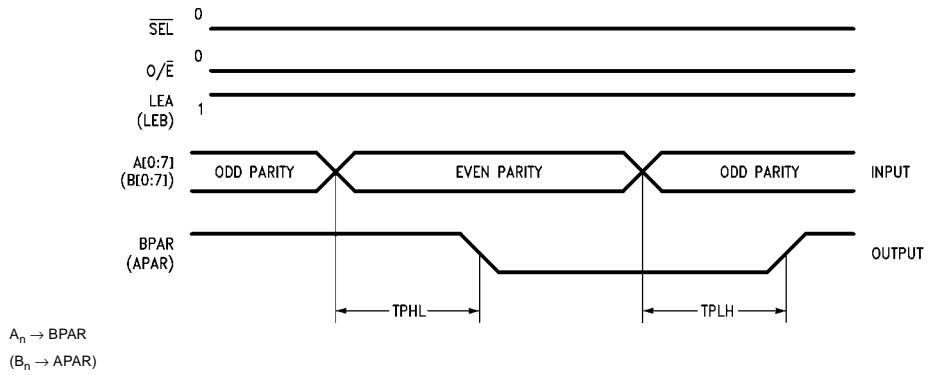


FIGURE 2.

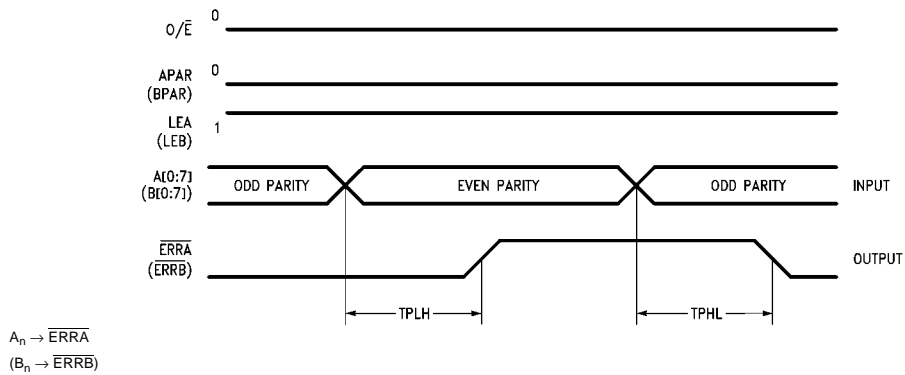


FIGURE 3.

AC Path (Continued)

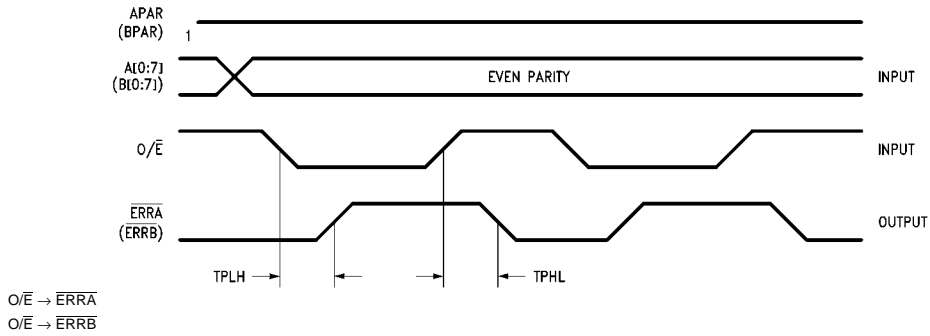


FIGURE 4.

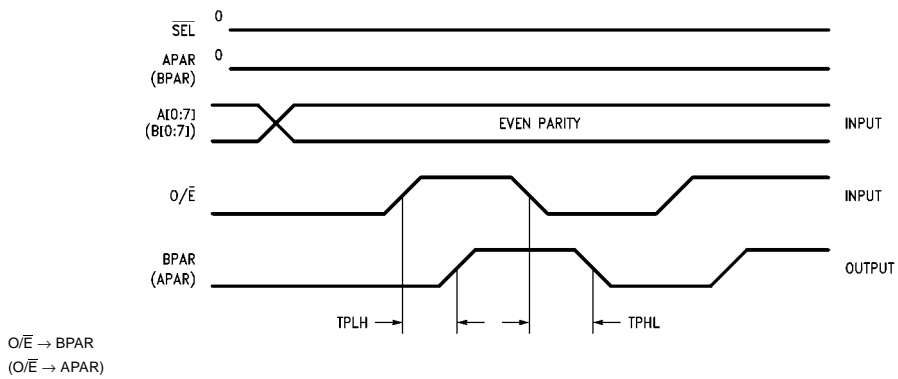


FIGURE 5.

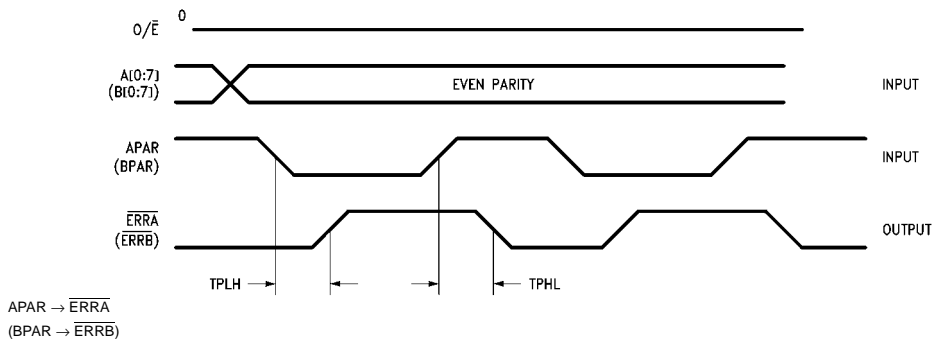


FIGURE 6.

**AC Path** (Continued)

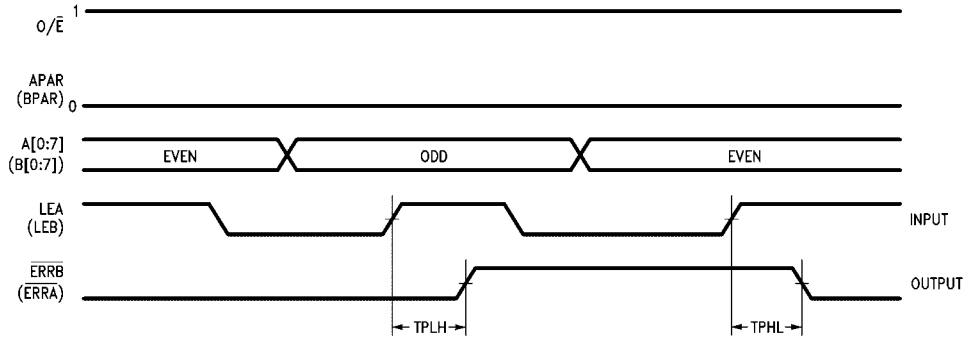


FIGURE 7.

ZH, HZ

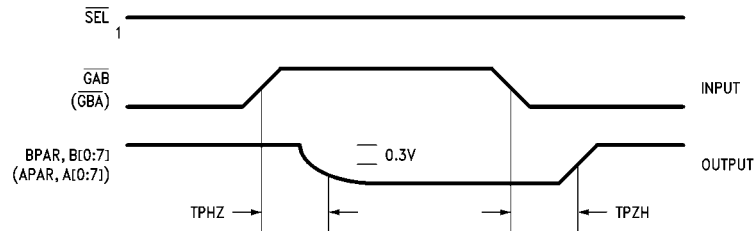


FIGURE 8.

ZL, LZ

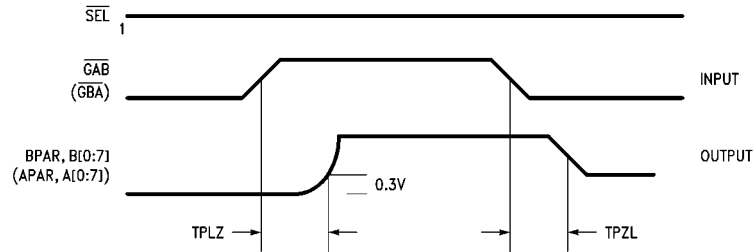
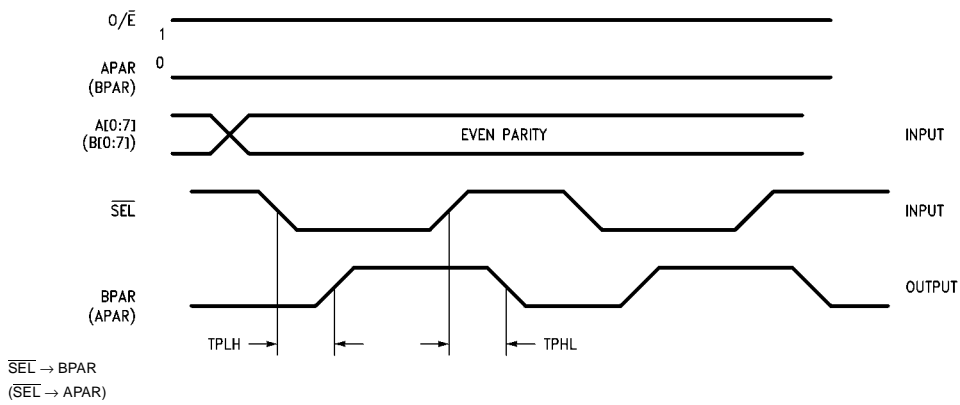


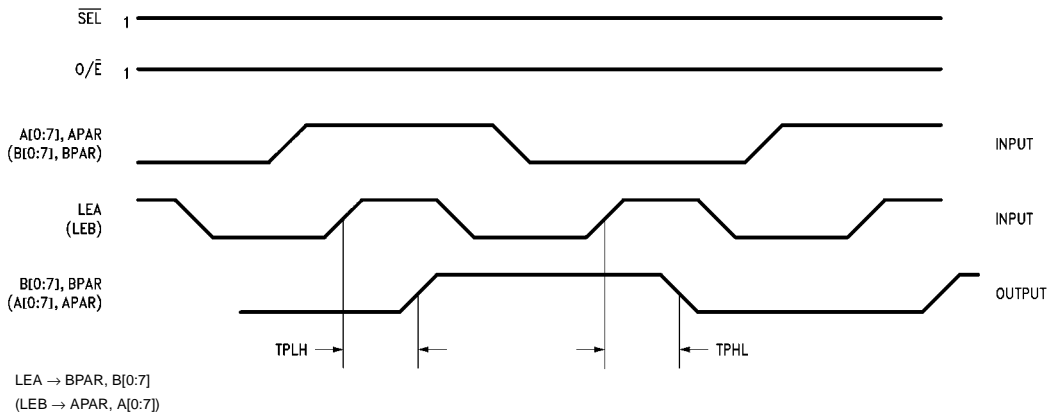
FIGURE 9.



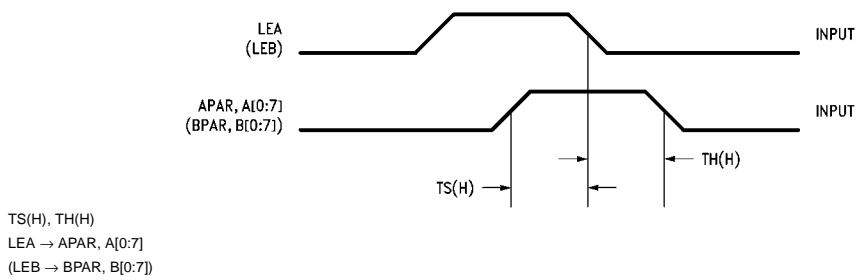
**AC Path** (Continued)



**FIGURE 10.**



**FIGURE 11.**



**FIGURE 12.**

**AC Path** (Continued)

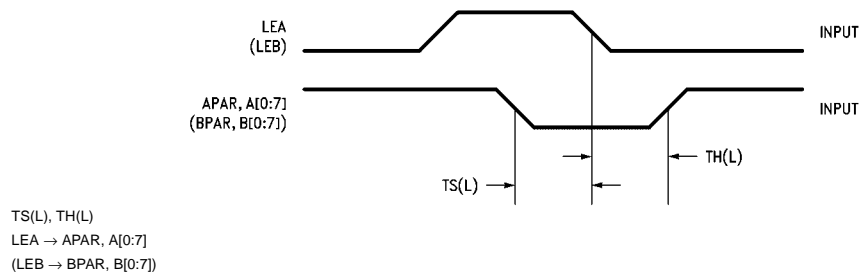


FIGURE 13.

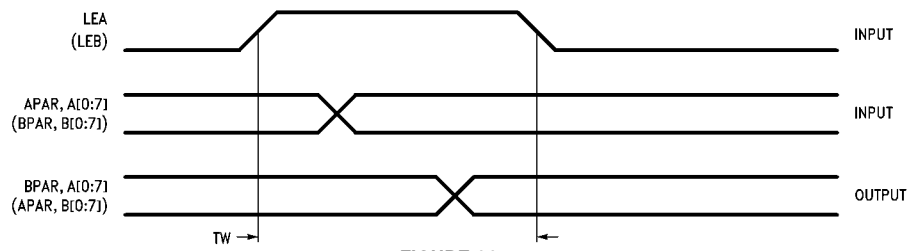
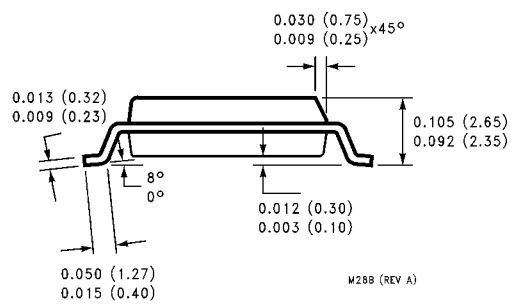
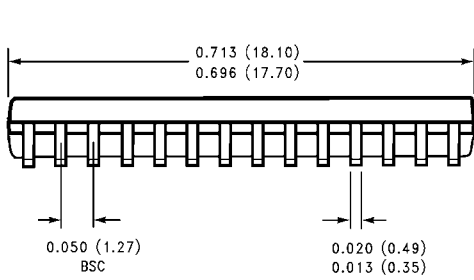
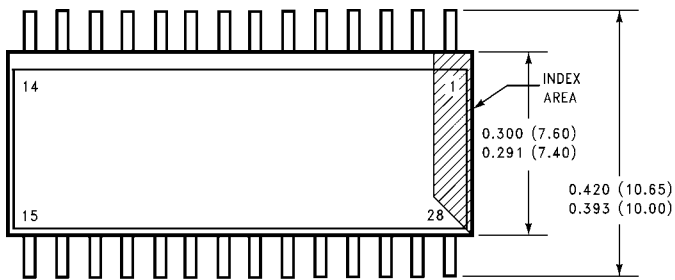


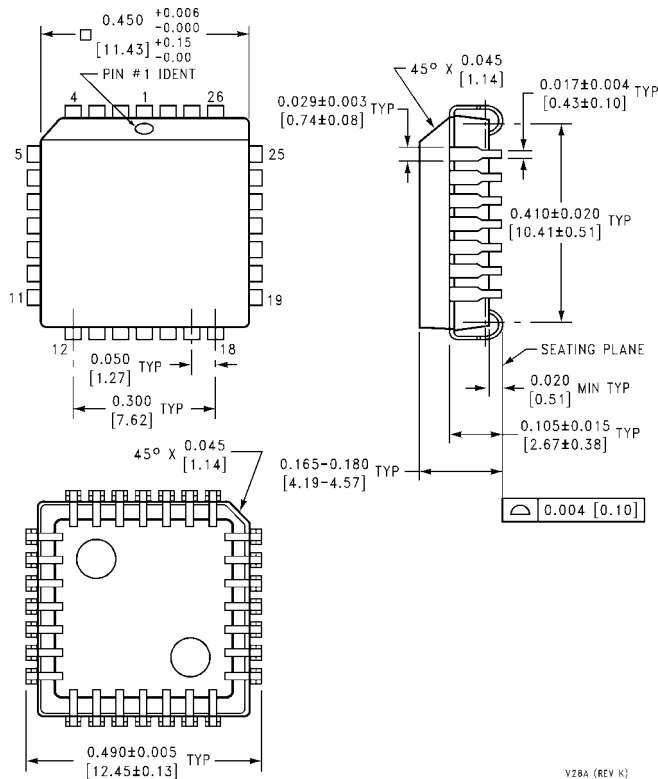
FIGURE 14.

**Physical Dimensions** inches (millimeters) unless otherwise noted



**28-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide  
Package Number M28B**

**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



**28-Lead Plastic Lead Chip Carrier (PLCC), JEDEC MO-047, 0.450 Square Package Number V28A**

V28A (REV K)

Fairchild does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied and Fairchild reserves the right at any time without notice to change said circuitry and specifications.

**LIFE SUPPORT POLICY**

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

[www.fairchildsemi.com](http://www.fairchildsemi.com)