

### SWITCHING

### P-CHANNEL MOS FET

### INDUSTRIAL USE

#### DESCRIPTION

This product is P-Channel MOS Field Effect Transistor designed for power management applications of notebook computers and Li-ion battery protection circuit.

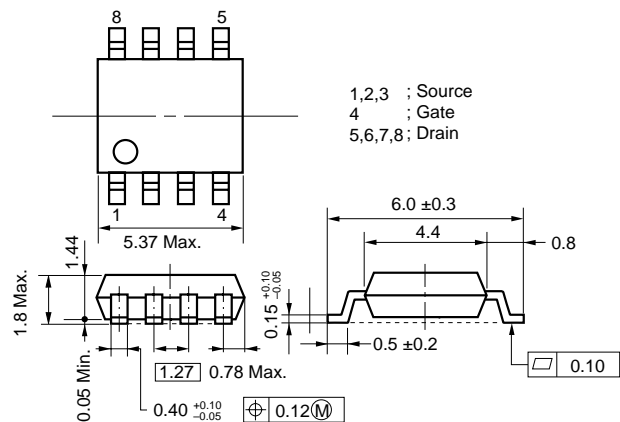
#### FEATURES

- Low on-resistance  
 $R_{DS(on)1} = 8.5 \text{ m}\Omega \text{ TYP. (} V_{GS} = -10 \text{ V, } I_D = -6.0 \text{ A)}$   
 $R_{DS(on)2} = 11.0 \text{ m}\Omega \text{ TYP. (} V_{GS} = -4.5 \text{ V, } I_D = -6.0 \text{ A)}$   
 $R_{DS(on)3} = 12.0 \text{ m}\Omega \text{ TYP. (} V_{GS} = -4.0 \text{ V, } I_D = -6.0 \text{ A)}$
- Low  $C_{iss}$  :  $C_{iss} = 3800 \text{ pF TYP.}$
- Built-in G-S protection diode
- Small and surface mount package (Power SOP8)

#### ORDERING INFORMATION

PART NUMBER	PACKAGE
$\mu$ PA1715G	Power SOP8

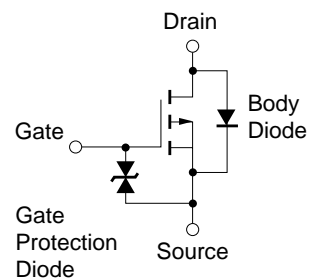
#### PACKAGE DRAWING (Unit : mm)



#### ABSOLUTE MAXIMUM RATINGS ( $T_A = 25^\circ\text{C}$ , All terminals are connected.)

Drain to Source Voltage ( $V_{GS} = 0 \text{ V}$ )	$V_{DSS}$	-30	V
Gate to Source Voltage ( $V_{DS} = 0 \text{ V}$ )	$V_{GSS}$	$\mp 20$	V
Drain Current (DC)	$I_{D(DC)}$	$\mp 11$	A
Drain Current (pulse) <sup>Note1</sup>	$I_{D(pulse)}$	$\mp 44$	A
Total Power Dissipation ( $T_A = 25^\circ\text{C}$ ) <sup>Note2</sup>	$P_T$	2.0	W
Channel Temperature	$T_{ch}$	150	$^\circ\text{C}$
Storage Temperature	$T_{stg}$	-55 to +150	$^\circ\text{C}$

#### EQUIVALENT CIRCUIT



**Notes 1.**  $PW \leq 10 \mu\text{s}$ , Duty Cycle  $\leq 1 \%$

**2.** Mounted on ceramic substrate of  $1200 \text{ mm}^2 \times 0.7 \text{ mm}$

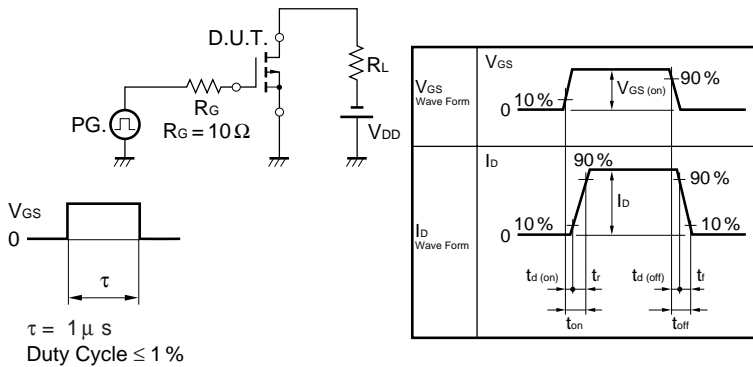
**Remark** The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

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 Not all devices/types available in every country. Please check with local NEC representative for availability and additional information.

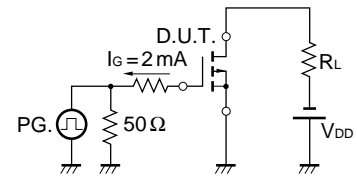
**ELECTRICAL CHARACTERISTICS (T<sub>A</sub> = 25 °C, All terminals are connected.)**

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Drain to Source On-state Resistance	R <sub>DS(on)1</sub>	V <sub>GS</sub> = -10 V, I <sub>D</sub> = -6.0 A		8.5	11.5	mΩ
	R <sub>DS(on)2</sub>	V <sub>GS</sub> = -4.5 V, I <sub>D</sub> = -6.0 A		11	16	mΩ
	R <sub>DS(on)3</sub>	V <sub>GS</sub> = -4.0 V, I <sub>D</sub> = -6.0 A		12	17.5	mΩ
Gate to Source Cut-off Voltage	V <sub>GS(off)</sub>	V <sub>DS</sub> = -10 V, I <sub>D</sub> = -1 mA	-1.0	-1.6	-2.5	V
Forward Transfer Admittance	y <sub>fs</sub>	V <sub>DS</sub> = -10 V, I <sub>D</sub> = -6.0 A	10	23		S
Drain Leakage Current	I <sub>DSS</sub>	V <sub>DS</sub> = -30 V, V <sub>GS</sub> = 0 V			-1	μA
Gate to Source Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> = ±20 V, V <sub>DS</sub> = 0 V			±10	μA
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> = -10 V		3800		pF
Output Capacitance	C <sub>oss</sub>	V <sub>GS</sub> = 0 V		1200		pF
Reverse Transfer Capacitance	C <sub>rss</sub>	f = 1 MHz		500		pF
Turn-on Delay Time	t <sub>d(on)</sub>	I <sub>D</sub> = -6.0 A		40		ns
Rise Time	t <sub>r</sub>	V <sub>GS(on)</sub> = -10 V		240		ns
Turn-off Delay Time	t <sub>d(off)</sub>	V <sub>DD</sub> = -15 V		230		ns
Fall Time	t <sub>f</sub>	R <sub>G</sub> = 10 Ω		160		ns
Total Gate Charge	Q <sub>G</sub>	I <sub>D</sub> = -11 A		70		nC
Gate to Source Charge	Q <sub>GS</sub>	V <sub>DD</sub> = -24 V		9		nC
Gate to Drain Charge	Q <sub>GD</sub>	V <sub>GS</sub> = -10 V		17		nC
Body Diode Forward Voltage	V <sub>F(S-D)</sub>	I <sub>F</sub> = 11 A, V <sub>GS</sub> = 0 V		0.8		V
Reverse Recovery Time	t <sub>rr</sub>	I <sub>F</sub> = 11 A, V <sub>GS</sub> = 0 V		53		ns
Reverse Recovery Charge	Q <sub>rr</sub>	di/dt = 100 A/μs		57		nC

**TEST CIRCUIT 1 SWITCHING TIME**

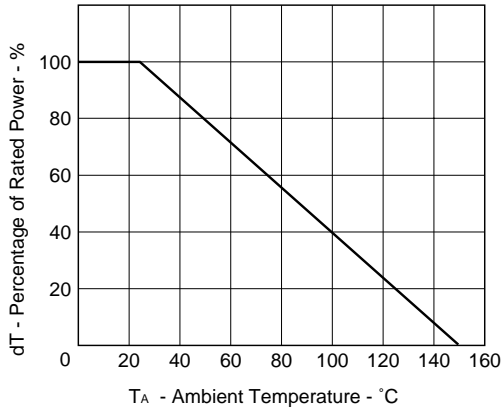


**TEST CIRCUIT 2 GATE CHARGE**

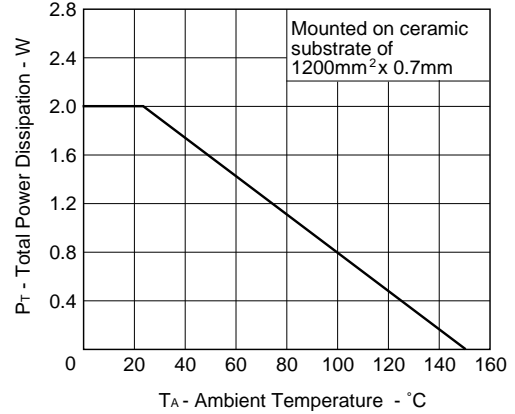


TYPICAL CHARACTERISTICS ( $T_A = 25^\circ\text{C}$ )

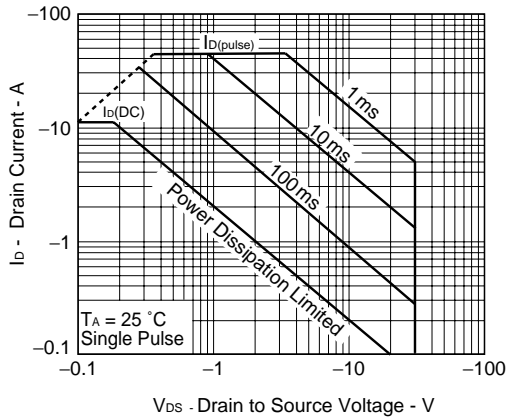
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE

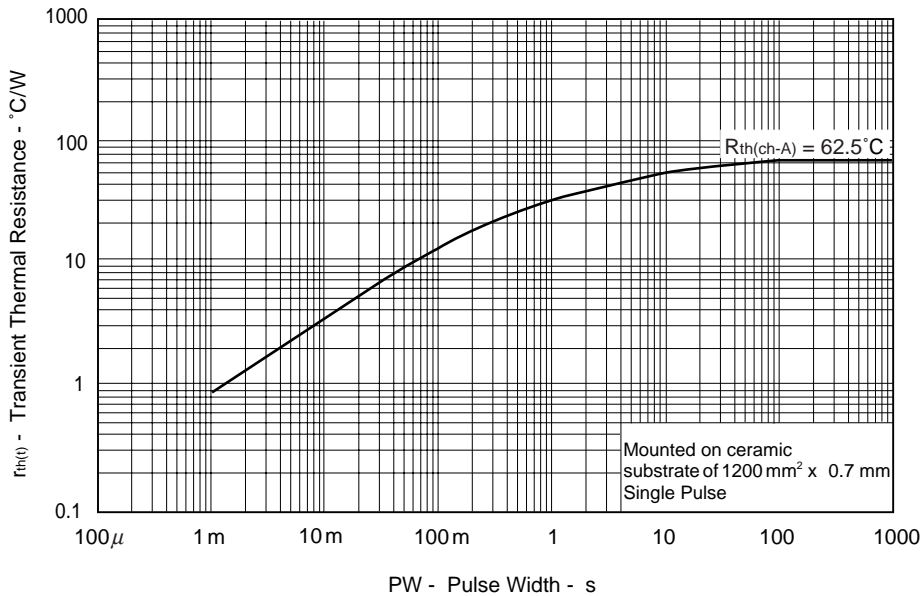


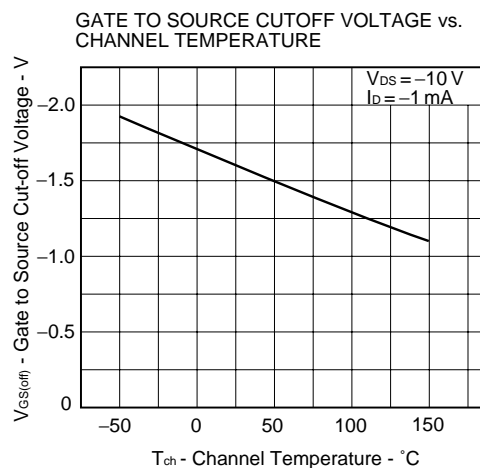
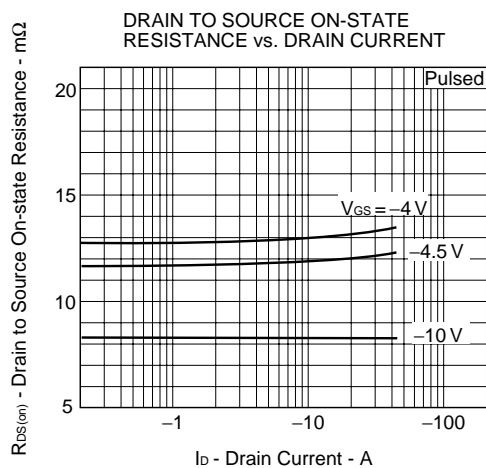
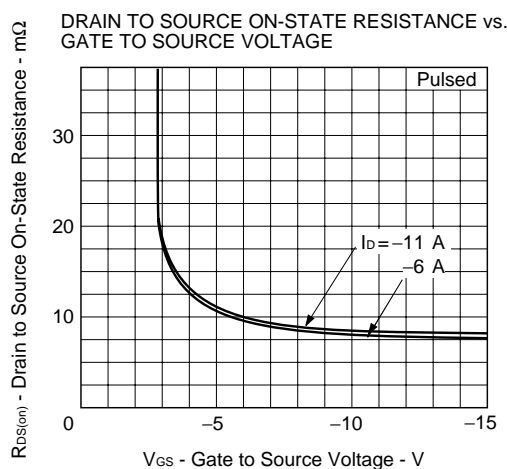
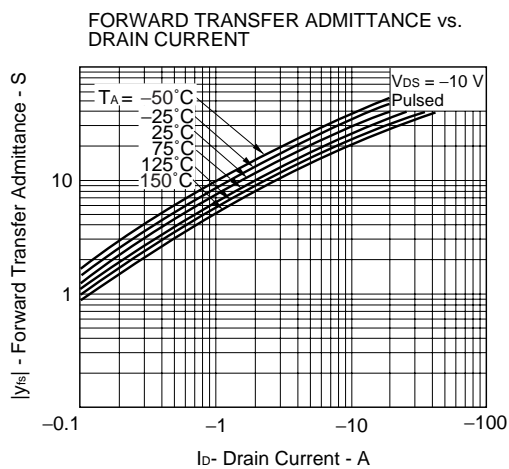
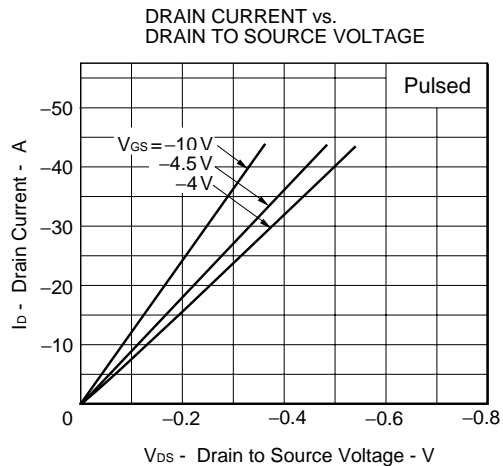
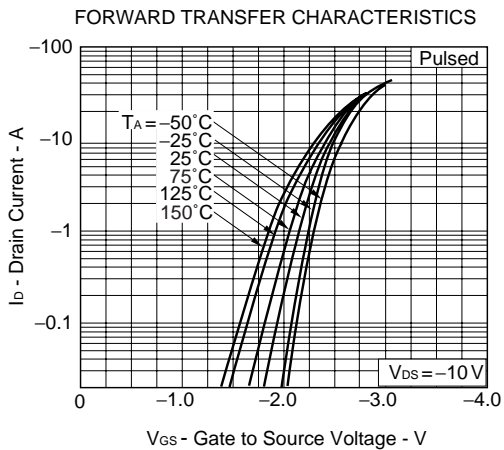
FORWARD BIAS SAFE OPERATING AREA



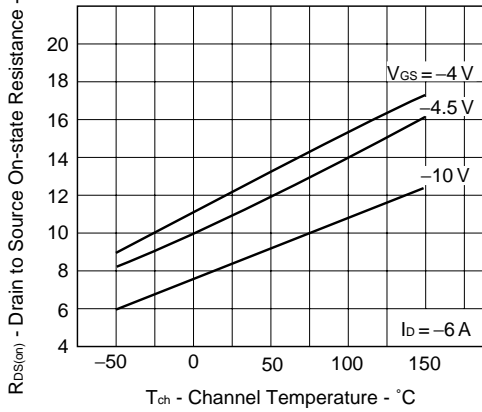
**Remark** Mounted on ceramic substrate of  $1200\text{ mm}^2 \times 0.7\text{ mm}$

TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH

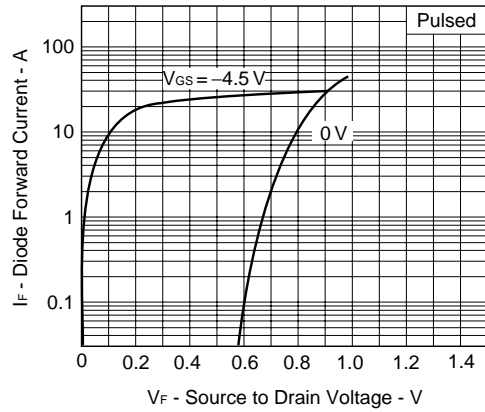




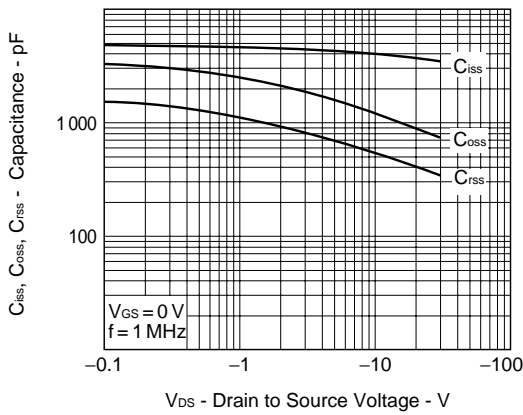
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



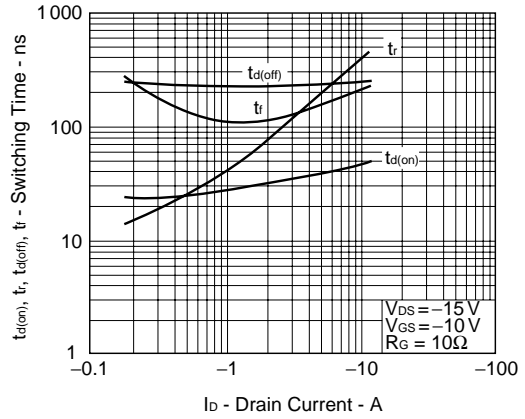
SOURCE TO DRAIN DIODE FORWARD VOLTAGE



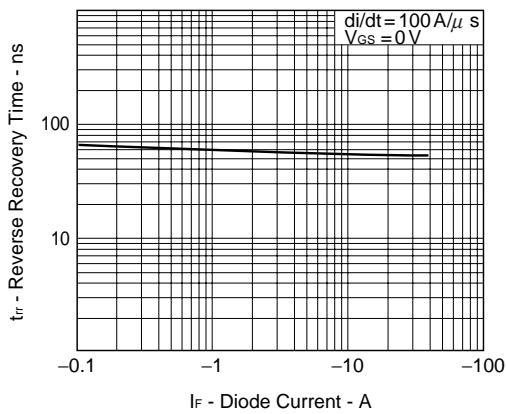
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



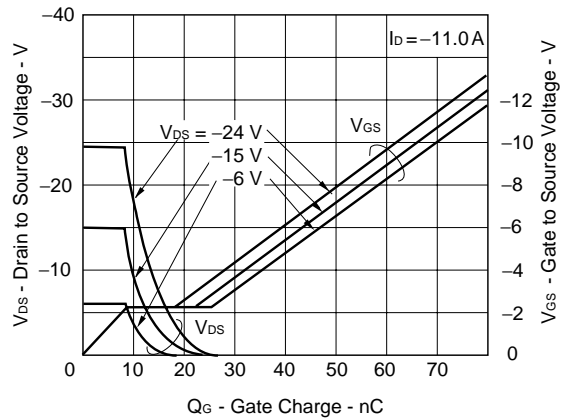
SWITCHING CHARACTERISTICS



REVERSE RECOVERY TIME vs. DIODE CURRENT



DYNAMIC INPUT/OUTPUT CHARACTERISTICS



[MEMO]

[MEMO]

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