Integrated Circuit Systems, Inc.

ICS93712

Advance Information

2 DIMM DDR Fanout Buffer

Recommended Application:

DDR fan out buffer for VIA PRO 266 DDR chipset

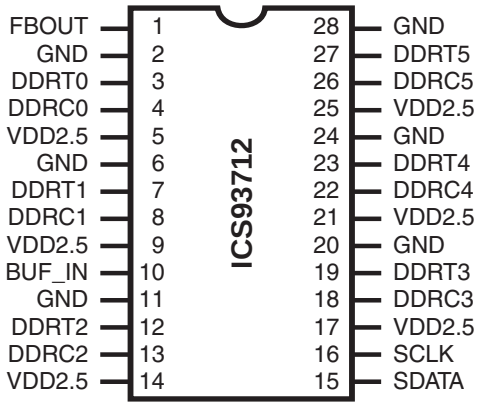
Product Description/Features:

- Low skew, fanout buffer
- 1 to 6 differential clock distribution
- I^2C for functional and output control
- Feedback pin for input to output synchronization
- Supports up to 2 DDR DIMMs
- Frequency support for up to 400MHz DDR, SDRAMs
- CMOS level control signal input

Switching Characteristics:

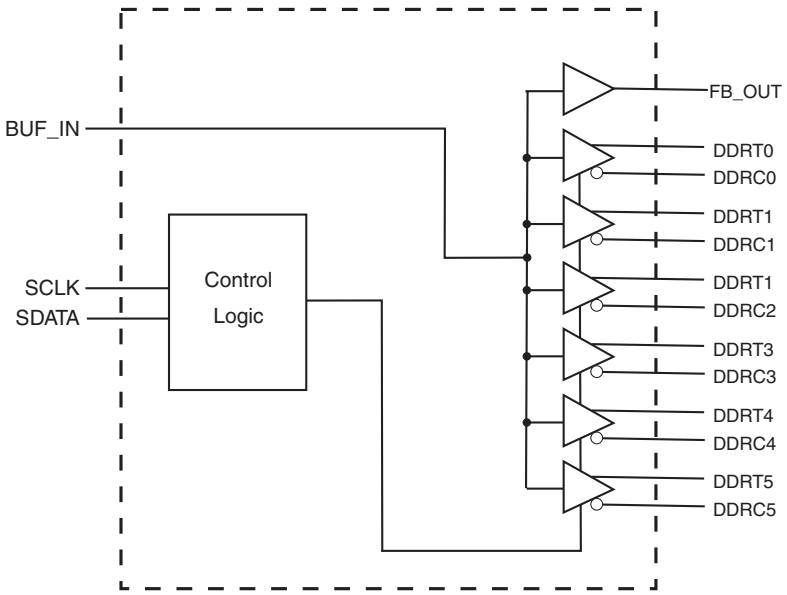
- OUTPUT - OUTPUT skew: <100ps
- Output Rise and Fall Time for DDR outputs: 650ps - 950ps
- DUTY CYCLE: 47% - 53%
- Pulse Skew: <100ps

Pin Configuration



28-Pin SSOP

Block Diagram



Pin Descriptions

PIN NUMBER	PIN NAME	TYPE	DESCRIPTION
1	FB_OUT	OUT	Feedback output, dedicated for external feedback
5, 9, 14, 17, 21, 25	VDD2.5	PWR	2.5V voltage supply
2, 6, 11, 20, 24, 28	GND	PWR	Ground
27, 23, 19, 12, 7, 3	DDRT (5:0)	OUT	"True" Clock of differential pair outputs.
26, 22, 18, 13, 8, 4	DDRC (5:0)	OUT	"Complementory" clocks of differential pair outputs.
10	BUF_IN	IN	Single ended buffer input
15	SDATA	I/O	Data pin for I^2C circuitry 5V tolerant
16	SCLK	IN	Clock input of I^2C input, 5V tolerant input

Byte 1: Reserved Register
(1= enable, 0 = disable)

BIT	PIN#	PWD	DESCRIPTION
Bit 7	-	1	Reserved
Bit 6	-	1	Reserved
Bit 5	-	1	Reserved
Bit 4	-	1	Reserved
Bit 3	-	1	Reserved
Bit 2	-	1	Reserved
Bit 1	-	1	Reserved
Bit 0	-	1	Reserved

Byte 2: Reserved Register
(1= enable, 0 = disable)

BIT	PIN#	PWD	DESCRIPTION
Bit 7	-	1	Reserved
Bit 6	-	1	Reserved
Bit 5	-	1	Reserved
Bit 4	-	1	Reserved
Bit 3	-	1	Reserved
Bit 2	-	1	Reserved
Bit 1	-	1	Reserved
Bit 0	-	1	Reserved

Byte 3: Reserved Register
(1= enable, 0 = disable)

BIT	PIN#	PWD	DESCRIPTION
Bit 7	-	1	Reserved
Bit 6	-	1	Reserved
Bit 5	-	1	Reserved
Bit 4	-	1	Reserved
Bit 3	-	1	Reserved
Bit 2	-	1	Reserved
Bit 1	-	1	Reserved
Bit 0	-	1	Reserved

Byte 4: Reserved Register
(1= enable, 0 = disable)

BIT	PIN#	PWD	DESCRIPTION
Bit 7	-	1	Reserved
Bit 6	-	1	Reserved
Bit 5	-	1	Reserved
Bit 4	-	1	Reserved
Bit 3	-	1	Reserved
Bit 2	-	1	Reserved
Bit 1	-	1	Reserved
Bit 0	-	1	Reserved

Byte 5: Reserved Register
(1= enable, 0 = disable)

BIT	PIN#	PWD	DESCRIPTION
Bit 7	-	1	Reserved
Bit 6	-	1	Reserved
Bit 5	-	1	Reserved
Bit 4	-	1	Reserved
Bit 3	-	1	Reserved
Bit 2	-	1	Reserved
Bit 1	-	1	Reserved
Bit 0	-	1	Reserved

Byte 6: Output Control
(1= enable, 0 = disable)

BIT	PIN#	PWD	DESCRIPTION
Bit 7	-	1	(Reserved)
Bit 6	-	0	(Reserved)
Bit 5	-	0	(Reserved)
Bit 4	-	0	(Reserved)
Bit 3	-	1	(Reserved)*
Bit 2	27, 26	1	DDRT5, DDRC5
Bit 1	23, 22	1	DDRT4, DDRC4
Bit 0	19, 18	1	DDRT3, DDRC3

Byte 7: Output Control
(1= enable, 0 = disable)

BIT	PIN#	PWD	DESCRIPTION
Bit 7	-	1	Reserved*
Bit 6	-	1	Reserved*
Bit 5	-	1	Reserved*
Bit 4	12, 13	1	DDRT2 DDRC2
Bit 3	-	1	Reserved*
Bit 2	7, 8	1	DDRT1 DDRC1
Bit 1	-	1	Reserved*
Bit 0	3, 4	1	DDRT0, DDRC0

Note:
* For lower power consumption, these bits should be driven to 0.

Switching Characteristics

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS
Maximum Operating Frequency			66		200	MHz
Input clock duty cycle	d_{tin}		40		60	%
Output to Output Skew	T_{skew}				100	ps
Pulse skew	T_{skewp}				100	ps
Duty cycle	D_C[2]	66MHz to 100MHz	48		52	%
		101MHz to 167MHz	47		53	%
Rise Time, Fall Time	tr, tf	Load = 120Ω/16pF	650		950	ps

Notes:
1. Refers to transition on noninverting output.
2. While the pulse skew is almost constant over frequency, the duty cycle error increases at higher frequencies. This is due to the formula: duty cycle=t_{wH}/t_c, were the cycle (t_c) decreases as the frequency goes up.

Absolute Maximum Ratings

Supply Voltage (VDD) . . . . . -0.5V to 3.6V
Logic Inputs . . . . . GND –0.5 V to V_{DD} +0.5 V
Ambient Operating Temperature . . . . . 0°C to +85°C
Storage Temperature . . . . . –65°C to +150°C

Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only and functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Electrical Characteristics - Input/Supply/Common Output Parameters

T_A = 0 - 85C; Supply Voltage VDD = 2.5 V +/- 0.2V (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input High Current	I_{IH}	VI = VDD or GND				µA
Input Low Current	I_{IL}	VI = VDD or GND				µA
Operating Supply Current	$I_{DD2.5}$	CL = 0pf				mA
	I_{DDPD}	CL = 0pf			100	µA
Output High Current	I_{OH}	VDD = 2.3V, V_{OUT} = 1V	-18			mA
Output Low Current	I_{OL}	VDD = 2.3V, V_{OUT} = 1.2V	26			mA
High-level output voltage	V_{OH}	VDD = min to max, IOH = -1 mA				V
		VDD = 2.3V, IOH = -12 mA				V
Low-level output voltage	V_{OL}	VDD = min to max I_{OL}=1 mA			0.1	
		VDD = 2.3V IOH=12 mA			0.6	V
Input Capacitance[1]	C_{IN}	VI = GND or VDD		2		pF

[1]Guaranteed by design, not 100% tested in production.

Recommended Operating Condition

T_A = 0 - 85C; Supply Voltage AVDD, VDD = 2.5 V +/- 0.2V (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Power Supply Voltage	V_{DD}		2.3	2.5	2.7	V
Input High Voltage	V_{IH}	OE input				V
Input Low Voltage	V_{IL}	OE input				V
Input voltage level	V_{IN}					V
Output differential-pair crossing voltage	V_{OC}					V

[1]Guaranteed by design, not 100% tested in production.

General I^2C serial interface information

The information in this section assumes familiarity with I^2C programming.
For more information, contact ICS for an I^2C programming application note.

How to Write:

- Controller (host) sends a start bit.
- Controller (host) sends the write address $D2_{(H)}$
- ICS clock will ***acknowledge***
- Controller (host) sends a dummy command code
- ICS clock will ***acknowledge***
- Controller (host) sends a dummy byte count
- ICS clock will ***acknowledge***
- Controller (host) starts sending first byte (Byte 0) through byte 6
- ICS clock will ***acknowledge*** each byte ***one at a time***.
- Controller (host) sends a Stop bit

How to Write:	
Controller (Host)	**ICS (Slave/Receiver)**
Start Bit	
Address $D2_{(H)}$	
	ACK
Dummy Command Code	
	ACK
Dummy Byte Count	
	ACK
Byte 0	
	ACK
Byte 1	
	ACK
Byte 2	
	ACK
Byte 3	
	ACK
Byte 4	
	ACK
Byte 5	
	ACK
Byte 6	
	ACK
Byte 7	
	ACK
Stop Bit	

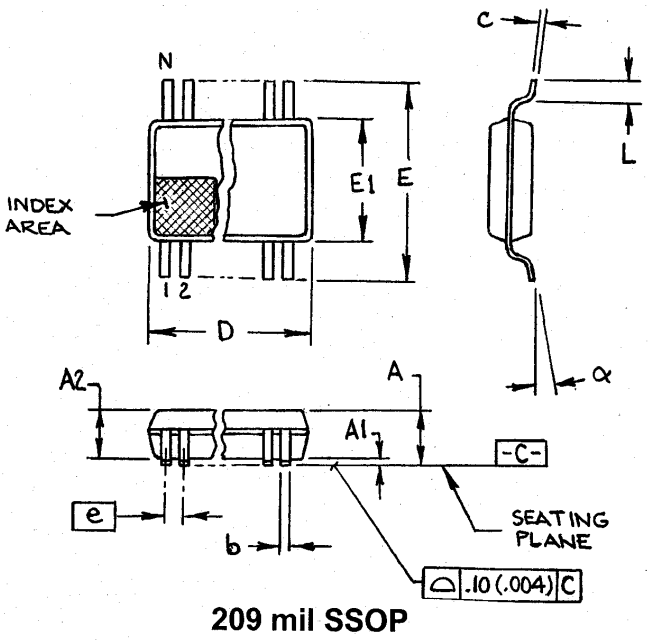
How to Read:

- Controller (host) will send start bit.
- Controller (host) sends the read address $D3_{(H)}$
- ICS clock will ***acknowledge***
- ICS clock will send the ***byte count***
- Controller (host) acknowledges
- ICS clock sends first byte ***(Byte 0) through byte 7***
- Controller (host) will need to acknowledge each byte
- Controller (host) will send a stop bit

How to Read:	
Controller (Host)	**ICS (Slave/Receiver)**
Start Bit	
Address $D3_{(H)}$	
	ACK
	Byte Count
ACK	
	Byte 0
ACK	
	Byte 1
ACK	
	Byte 2
ACK	
	Byte 3
ACK	
	Byte 4
ACK	
	Byte 5
ACK	
	Byte 6
ACK	
	Byte 7
Stop Bit	

Notes:

1. The ICS clock generator is a slave/receiver, I^2C component. It can read back the data stored in the latches for verification. **Read-Back will support Intel PIIX4 "Block-Read" protocol**.
2. The data transfer rate supported by this clock generator is 100K bits/sec or less (standard mode)
3. The input is operating at 3.3V logic levels.
4. The data byte format is 8 bit bytes.
5. To simplify the clock generator I^2C interface, the protocol is set to use only "**Block-Writes**" from the controller. The bytes must be accessed in sequential order from lowest to highest byte with the ability to stop after any complete byte has been transferred. The Command code and Byte count shown above must be sent, but the data is ignored for those two bytes. The data is loaded until a Stop sequence is issued.
6. At power-on, all registers are set to a default condition, as shown.



209 mil SSOP

SYMBOL	In Millimeters COMMON DIMENSIONS		In Inches COMMON DIMENSIONS	
	MIN	MAX	MIN	MAX
A	-	2.00	-	.079
A1	0.05	-	.002	-
A2	1.65	1.85	.065	.073
b	0.22	0.38	.009	.015
c	0.09	0.25	.0035	.010
D	SEE VARIATIONS		SEE VARIATIONS	
E	7.40	8.20	.291	.323
E1	5.00	5.60	.197	.220
e	0.65 BASIC		0.0256 BASIC	
L	0.55	0.95	.022	.037
N	SEE VARIATIONS		SEE VARIATIONS	
α	0°	8°	0°	8°

VARIATIONS

N	D mm.		D (inch)	
	MIN	MAX	MIN	MAX
28	9.90	10.50	.390	.413

MO-150 JEDEC 6/1/00 Rev B
Doc.# 10-0033

Ordering Information

ICS93712yF-T

Example:

ICS XXXX y F - PPP - T

- **Designation for tape and reel packaging**
- **Pattern Number (2 or 3 digit number for parts with ROM code patterns)**
- **Package Type**
  F=SSOP
- **Revision Designator** (will not correlate with datasheet revision)
- **Device Type (consists of 3 or 4 digit numbers)**
- **Prefix**
  ICS, AV = Standard Device