LH5164ASH

CMOS 64K (8K × 8) Static RAM

FEATURES

- 8,192 × 8 bit organization
- Access time: 500 ns (MAX.)
- Power consumption:
  - Operating:
    - 60 mW (MAX.) @ 3 V
  - Standby:
    - 3 µW (MAX.) @ 70°C @ 3 V
    - 9 µW (MAX.) @ 85°C @ 3 V
- Fully-static operation
- Three-state outputs
- Wide operating voltage range:
  - 2.5 V to 5.5 V
- TTL compatible I/O
- Wide temp. range
  - t_{OPR}: -40 to +85°C
- Packages:
  - 28-pin, 450-mil SOP
  - 28-pin, 8 × 13 mm^2 TSOP (Type I)

DESCRIPTION

The LH5164ASH is a static RAM organized as 8,192 × 8 bits. It is fabricated using silicon-gate CMOS process technology.

It is designed for 2.5 to 5.5 V low voltage operation and wide temperature range from -40 to +85°C.

PIN CONNECTIONS

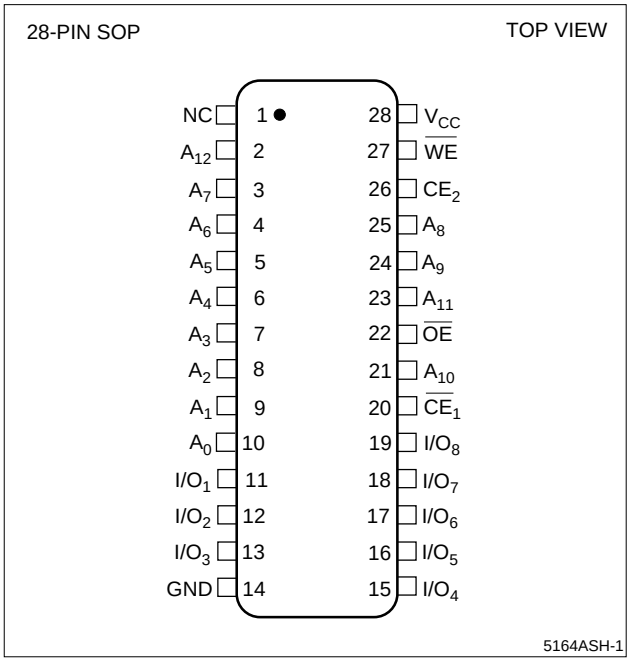


Figure 1. Pin Connections for SOP Package

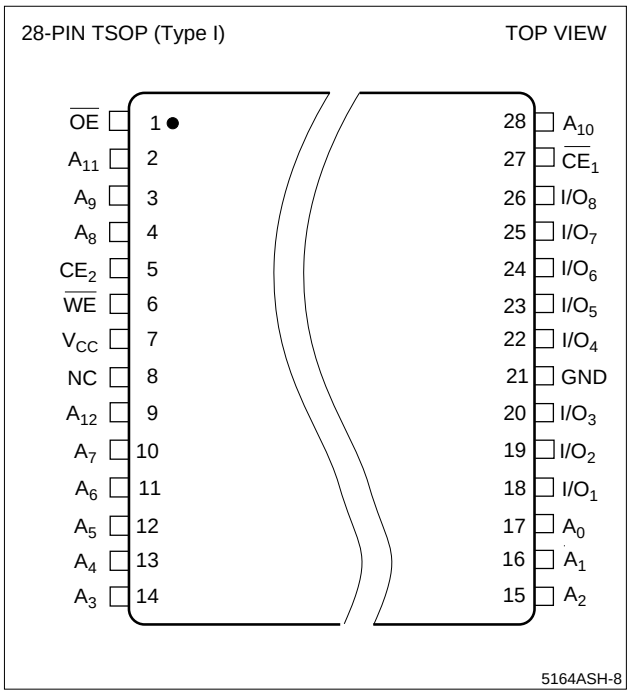


Figure 2. Pin Connections for TSOP Package

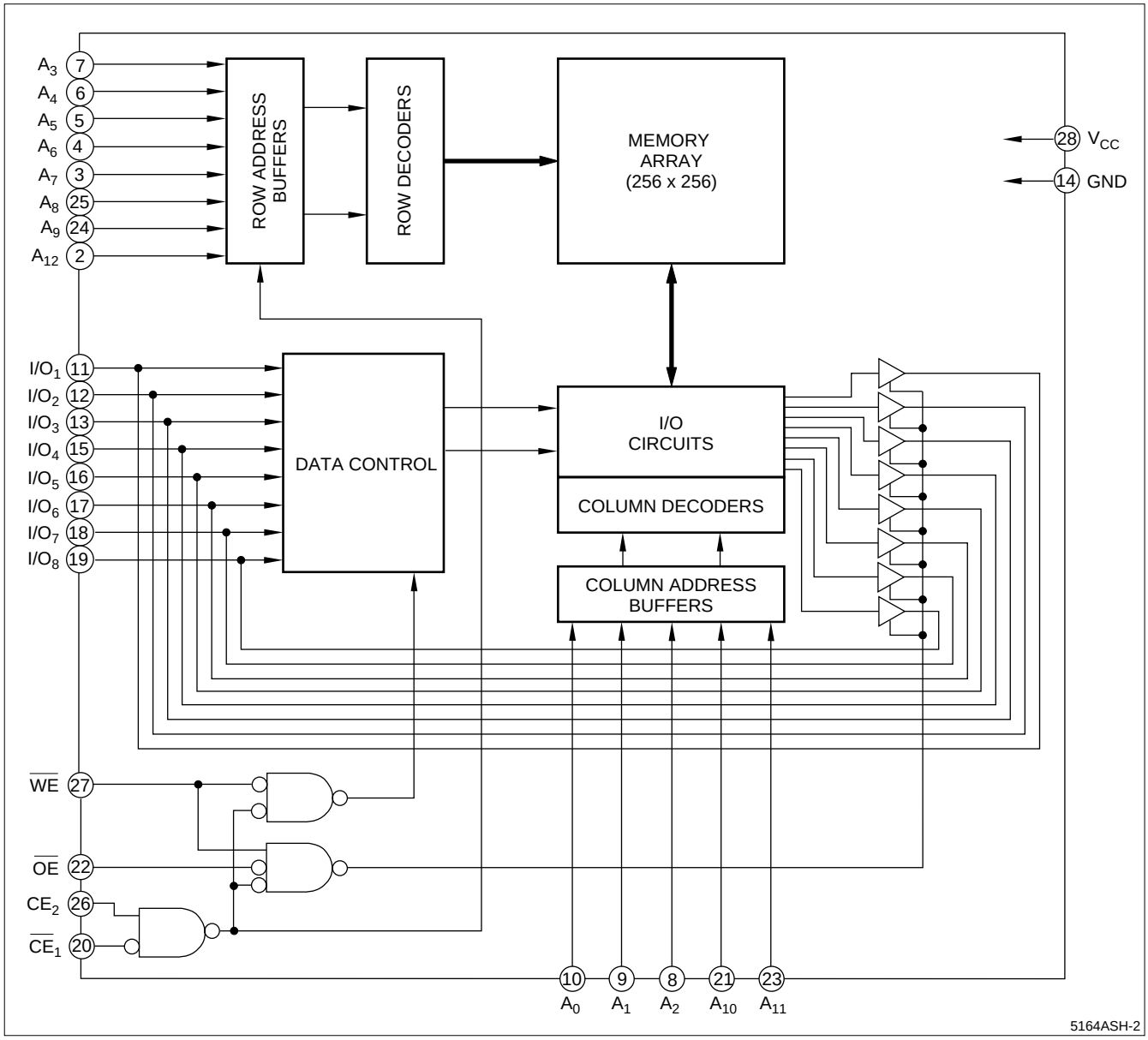


Figure 3. LH5164ASH Block Diagram

PIN DESCRIPTION

SIGNAL	PIN NAME
A_0 - A_{12}	Address inputs
$\overline{CE}_1$ - CE_2	Chip Enable input
$\overline{WE}$	Write Enable input
$\overline{OE}$	Output Enable input

SIGNAL	PIN NAME
I/O_1 - I/O_8	Data inputs and outputs
V_{CC}	Power supply
GND	Ground
NC	No connection

TRUTH TABLE

$\overline{CE_1}$	CE_2	$\overline{WE}$	$\overline{OE}$	MODE	I/O_1 - I/O_8	SUPPLY CURRENT	NOTE
H	X	X	X	Deselect	High-Z	Standby (I_{SB})	1
X	L	X	X	Deselect	High-Z	Standby (I_{SB})	1
L	H	L	X	Write	D_{IN}	Operating (I_{CC})	1
L	H	H	L	Read	D_{OUT}	Operating (I_{CC})	
L	H	H	H	Output disable	High-Z	Operating (I_{CC})	

NOTE:
1. X = H or L

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT	NOTE
Supply voltage	V_{CC}	-0.3 to +7.0	V	1
Input voltage	V_{IN}	-0.3 to V_{CC} +0.3	V	1, 2
Operating temperature	Topr	-40 to +85	°C	
Storage temperature	Tstg	-65 to +150	°C	

NOTES:
1. The maximum applicable voltage on any pin with respect to GND.
2. V_{IN} (MIN.) = -3.0 V for pulse width ≤50 ns.

RECOMMENDED OPERATING CONDITIONS (T_A = -40 to +85°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTE
Supply voltage	V_{CC}	2.5	3.0	5.5	V	
Input voltage (V_{CC} = 2.5 to 4.5 V)	V_{IH}	V_{CC} - 0.5		V_{CC} + 0.3	V	
	V_{IL}	-0.3		0.2	V	1
Input voltage (V_{CC} = 4.5 to 5.5 V)	V_{IH}	2.2		V_{CC} + 0.3	V	
	V_{IL}	-0.3		0.8	V	

NOTE:
1. V_{IN} (MIN.) = -3.0 V for pulse width ≤50 ns.

DC CHARACTERISTICS (T_A = -40 to +85°C, V_{CC} = 2.5 to 5.5 V)

PARAMETER	SYMBOL	CONDITIONS		MIN.	MAX.	UNIT	NOTE
Input leakage current	I_{LI}	V_{IN} = 0 to V_{CC}		-1.0	1.0	µA	
Output leakage current	I_{LO}	$\overline{CE_1}$ = V_{IH} or CE_2 = V_{IL} or $\overline{OE}$ = V_{IH} or $\overline{WE}$ = V_{IL} $V_{I/O}$ = 0 to V_{CC}		-1.0	1.0	µA	
Operating supply current	I_{CC}	$\overline{CE_1}$ = 0.2 V, V_{IN} = 0.2 V or V_{CC} - 0.2 V CE_2 = V_{CC} - 0.2 V, Output open	t_{CYCLE} = 500 ns		20	mA	
		$\overline{CE_1}$ = 0.2 V, V_{IN} = 0.2 V or V_{CC} - 0.2 V CE_2 = V_{CC} - 0.2 V, Output open	t_{CYCLE} = 1.0 µs		10		
		$\overline{CE_1}$ = 0.2 V, V_{IN} = 0.2 V or V_{CC} - 0.2 V CE_2 = V_{CC} - 0.2 V, Output open, V_{CC} = 3.3 V	t_{CYCLE} = 1.0 µs		8		
Standby current	I_{SB}	CE_2 ≤ 0.2 V or $\overline{CE_1}$ ≥ V_{CC} - 0.2 V	T_A ≤ +70°C		1.0	µA	1
			T_A ≤ +85°C		3.0		
	I_{SB1}	$\overline{CE_1}$ = V_{IH} or CE_2 = V_{IL}			5	mA	
Output Low voltage	V_{OL}	I_{OL} = 500 µA			0.5	V	
Output High voltage	V_{OH}	I_{OH} = -500 µA		V_{CC} - 0.5		V	2

NOTES:
1. CE_2 should be ≥ V_{CC} - 0.2 V or ≤ 0.2 V when $\overline{CE_1}$ ≥ V_{CC} - 0.2 V.
2. V_{OH} is 4.5 V (Min.) at V_{CC} > 5 V.

AC CHARACTERISTICS

(1) READ CYCLE (T_A = -40 to +85°C, V_{CC} = 2.5 to 5.5 V)

PARAMETER		SYMBOL	MIN.	MAX.	UNIT
Read cycle time		t_{RC}	500		ns
Address access time		t_{AA}		500	ns
Chip enable access time	($\overline{CE}_1$)	t_{ACE1}		500	ns
	(CE_2)	t_{ACE2}		500	ns
Output enable access time		t_{OE}		200	ns
Output hold time		t_{OH}	10		ns
Chip enable to output in Low-Z	($\overline{CE}_1$)	t_{LZ1}	20		ns
	(CE_2)	t_{LZ2}	20		ns
Output enable to output in Low-Z		t_{OLZ}	10		ns
Chip enable to output in High-Z	($\overline{CE}_1$)	t_{HZ1}	0	60	ns
	(CE_2)	t_{HZ2}	0	60	ns
Output disable to output in High-Z		t_{OHZ}	0	40	ns

(2) WRITE CYCLE (T_A = -40 to +85°C, V_{CC} = 2.5 to 5.5 V)

PARAMETER	SYMBOL	MIN.	MAX.	UNIT
Write cycle time	t_{WC}	500		ns
Chip enable to end of write	t_{CW}	250		ns
Address valid to end of write	t_{AW}	250		ns
Address setup time	t_{AS}	100		ns
Write pulse width	t_{WP}	150		ns
Write recovery time	t_{WR}	50		ns
Data valid to end of write	t_{DW}	100		ns
Data hold time	t_{DH}	0		ns
Output active from end of write	t_{OW}	20		ns
$\overline{WE}$ to output in High-Z	t_{WZ}	0	60	ns
$\overline{OE}$ to output in High-Z	t_{OHZ}	0	40	ns

NOTE:
1. Active output to high-impedance and high-impedance to output active tests specified for a ±200 mV transition from steady state levels into the test load.

AC TEST CONDITIONS

PARAMETER	MODE	NOTE
Input voltage amplitude	0 to V_{CC}	
Input rise/fall time	10 ns	
Timing reference level	1.5 V	
Output load conditions	C_L (100 pF)	1

NOTE:
1. Includes scope and jig capacitance.

CAPACITANCE (T_A = 25°C, f = 1MHz)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Input capacitance	C_{IN}	V_{IN} = 0 V			7	pF
Input/output capacitance	$C_{I/O}$	$V_{I/O}$ = 0 V			10	pF

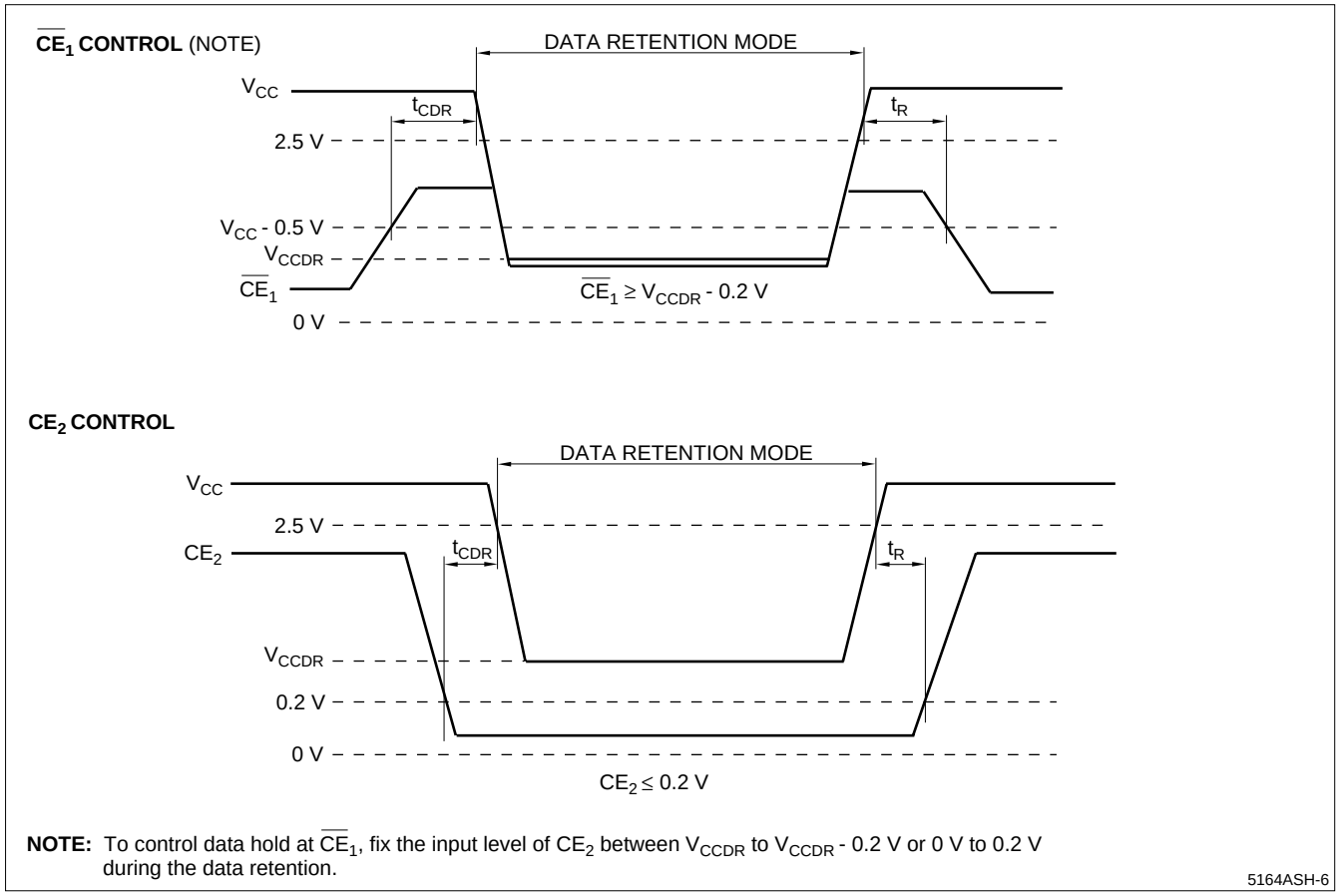
NOTE:
This parameter is sampled and not production tested.

DATA RETENTION CHARACTERISTICS (T_A = -40 to +85°C)

PARAMETER	SYMBOL	CONDITIONS		MIN.	MAX.	UNIT	NOTE
Data retention supply voltage	V_{CCDR}	$CE_2 \le 0.2$ V or $\overline{CE}_1 \ge V_{CCDR} - 0.2$ V		2.0	5.5	V	1
Data retention supply current	I_{CCDR}	V_{CCDR} = 3 V, $CE_2 \le 0.2$ V or $\overline{CE}_1 \ge V_{CCDR} - 0.2$ V	T_A = 25°C		0.2	µA	1
			T_A = 40°C		0.4	µA	
					0.6	µA	
Chip disable to data retention	t_{CDR}			0		ns	
Recovery time	t_R			t_{RC}		ns	2

NOTES:

1. CE_2 should be ≥ V_{CCDR} - 0.2 V or ≤ 0.2 V when $\overline{CE}_1 \ge V_{CCDR}$ - 0.2 V.
2. t_{RC} = Read cycle time



NOTE: To control data hold at $\overline{CE}_1$, fix the input level of CE_2 between V_{CCDR} to V_{CCDR} - 0.2 V or 0 V to 0.2 V during the data retention.

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Figure 4. Low Voltage Data Retention

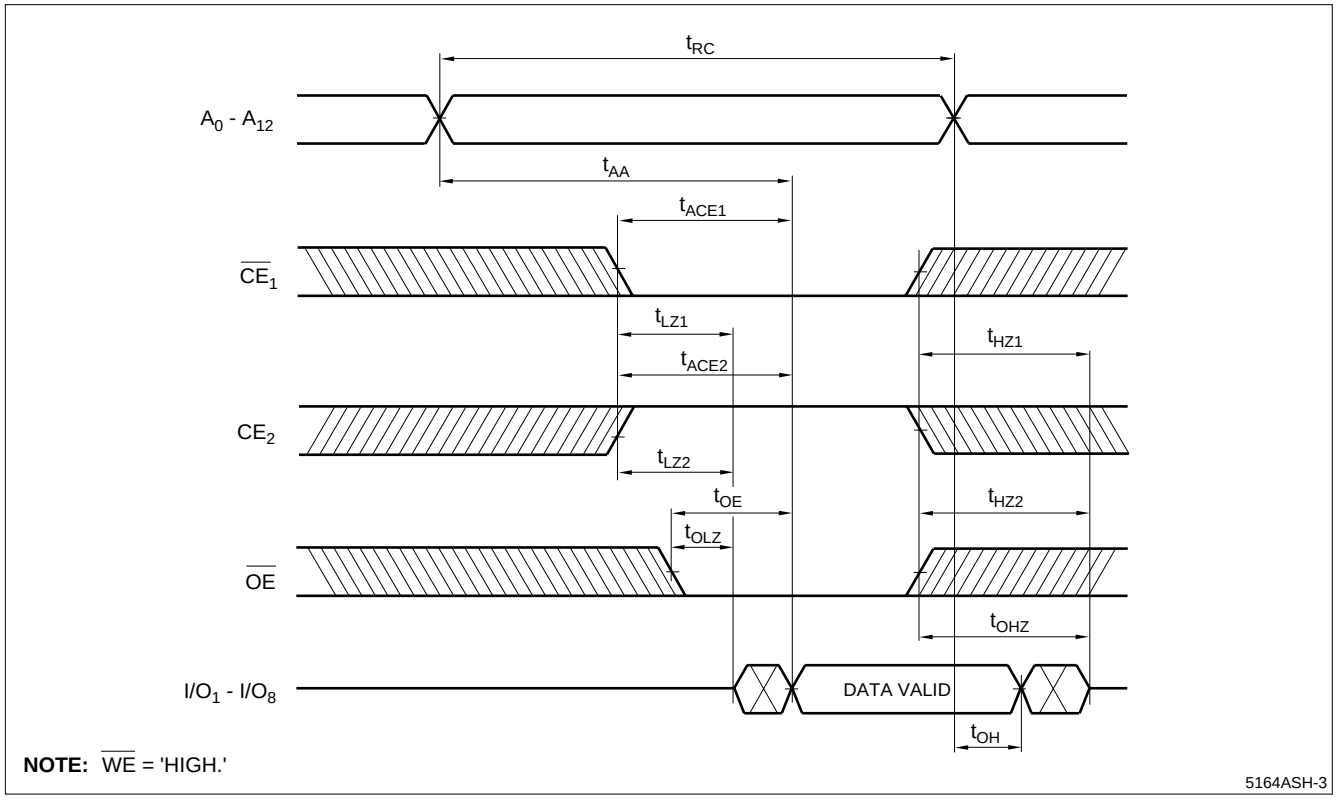
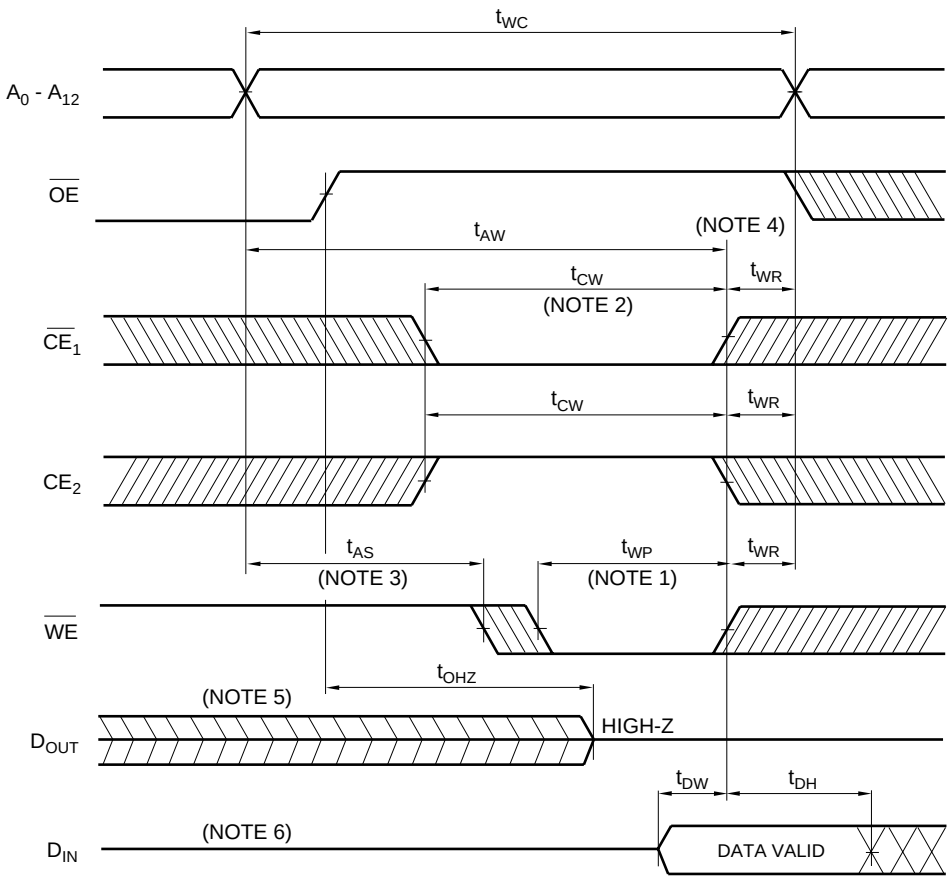


Figure 5. Read Cycle



NOTES:

1. The writing occurs during an overlapping period of $\overline{CE_1}$ = 'LOW,' CE_2 = 'HIGH,' and $\overline{WE}$ = 'LOW' (t_{WP}).
2. t_{CW} is defined as the time from the last occuring transition, either $\overline{CE_1}$ LOW transition or CE_2 HIGH transition, to the time when the writing is finished.
3. t_{AS} is defined as the time from address change to writing start.
4. t_{WR} is defined as the time from writing finish to address change.
5. If $\overline{CE_1}$ LOW transition or CE_2 HIGH transition occurs at the same time or after $\overline{WE}$ LOW transition, the output will remain high-impedance.
6. While I/O pins are in the output state, input signals with the opposite logic level must not be applied.

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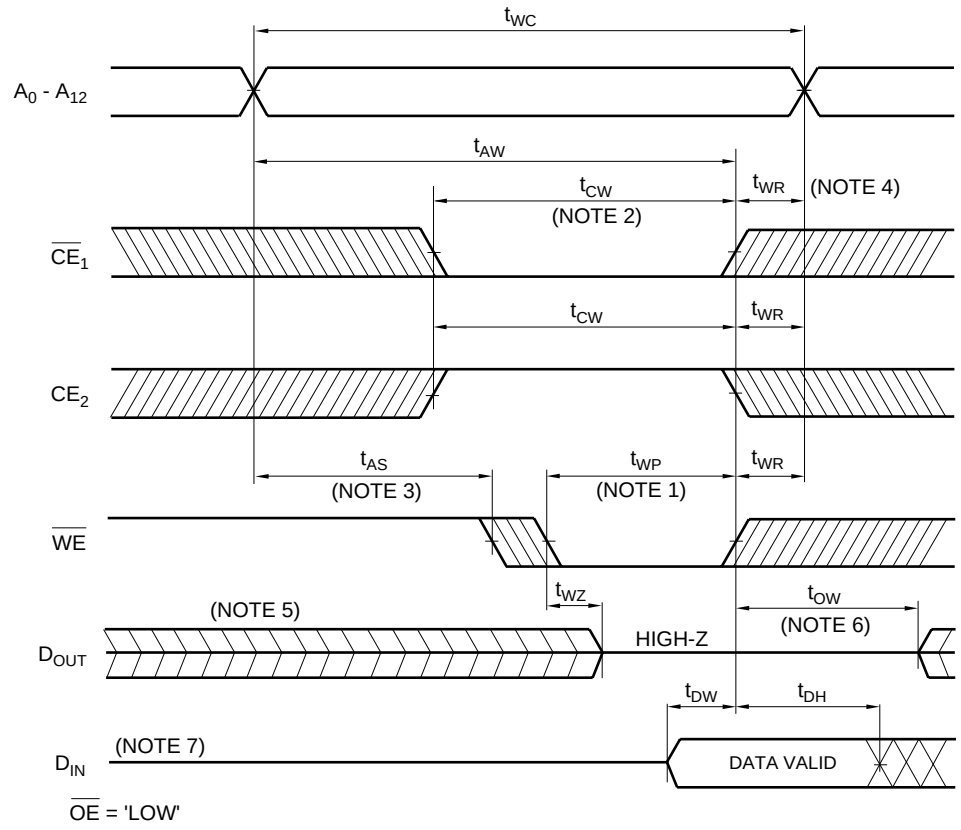
Figure 6. Write Cycle 1 ($\overline{OE}$ Controlled)



NOTES:

1. The writing occurs during an overlapping of $\overline{CE_1}$ = 'LOW,' CE_2 = 'HIGH,' and $\overline{WE}$ = 'LOW' (t_{WP}).
2. t_{CW} is defined as the time from the last occuring transition, either $\overline{CE_1}$ LOW transition or CE_2 HIGH transition, to the time when the writing is finished.
3. t_{AS} is defined as the time from address change to writing start.
4. t_{WR} is defined as the time from writing finish to address change.
5. If $\overline{CE_1}$ LOW transition or CE_2 HIGH transition occurs at the same time or after $\overline{WE}$ LOW transition, the output will remain high-impedance.
6. If $\overline{CE_1}$ HIGH transition or CE_2 LOW transition occurs at the same time or before $\overline{WE}$ HIGH transition, the output will remain high-impedance.
7. While I/O pins are in the output state, input signals with the opposite logic level must not be applied.

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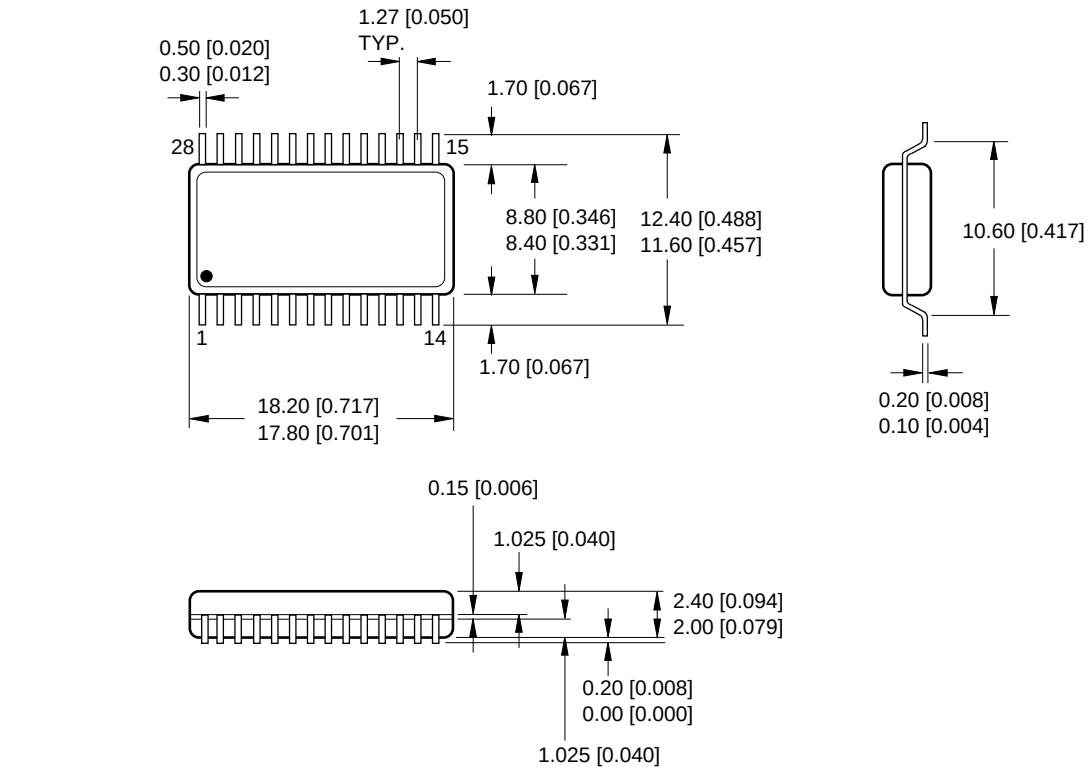
Figure 7. Write Cycle 2 ($\overline{OE}$ Low Fixed)

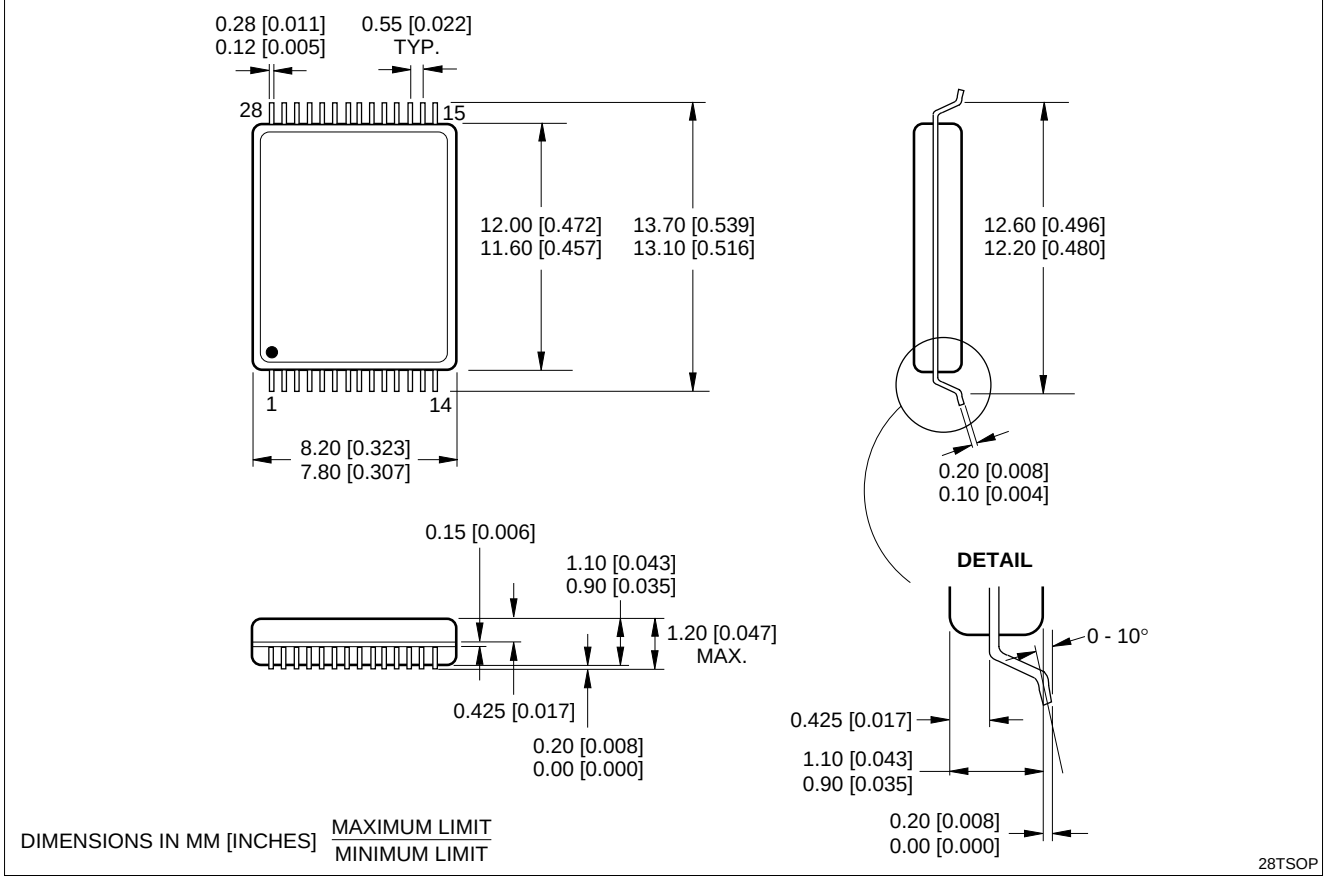
PACKAGE DIAGRAMS

28SOP (SOP028-P-0450)



28-pin, 450-mil SOP

28TSOP (TSOP028-P-0813)



28-pin, 8 × 13 mm^2 TSOP (Type I)

ORDERING INFORMATION