

PBL 3776/1 Dual Controller IC for High Current Stepper Motor Applications

Description

The PBL 3776/1 is a switch-mode (chopper), constant-current controller IC intended for controlling external transistors in a high current stepper motor application. The IC has two channels one for each winding of a two-phase stepper motor. The circuit is similar to Ericsson's PBL 3775/1. PBL 3776/1 is equipped with a Disable input to simplify half-stepping operation.

The PBL 3776/1 contains a clock oscillator, which is common for both driver channels, a set of comparators and flip-flops implementing the switching control, and two output sections each containing four outputs, two source and two sink, intended to drive an external H-bridge.

Voltage supply requirements are +5 V for logic and +10 to +45 V for the outputs. The close match between the two driver channels guarantees consistent output current ratios and motor positioning accuracy.

Key Features

- Suitable to drive any external Mos Fet or bipolar power transistor.
- 0°C to +85°C operation.
- · Few external components.
- Crossconduction prevented by time delay.
- Close matching between channels for high positioning accuracy.
- Digital filter on chip eliminates external filtering components.
- Plastic 24-pin "narrow" DIP package.

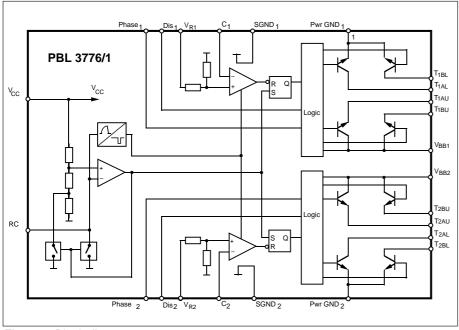
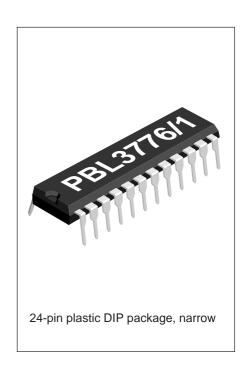


Figure 1. Block diagram.



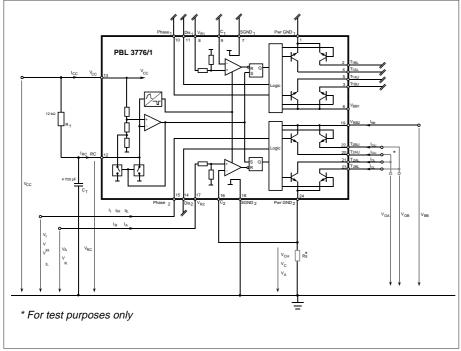


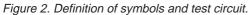
Maximum Ratings

| Parameter | Pin no.* | Symbol | Min | Max | Unit |
|----------------------|----------------------------|-----------------|------|-----------------|------|
| Voltage | | | | | |
| Logic supply | 13 | V _{cc} | 0 | 7 | V |
| Output supply | 6, 19 | V _{BB} | 0 | 45 | V |
| Logic inputs | 10, 11, 14, 15 | V _I | -0.3 | 6 | V |
| Analog inputs | 8, 9, 16, 17 | $V_{_{A}}$ | -0.3 | V _{cc} | V |
| Current | | | | | |
| Output current t=1mS | 2, 3, 4, 5, 20, 21, 22, 23 | I _o | -500 | +500 | mA |
| Logic inputs | 10, 11, 14, 15 | I, | -10 | | mA |
| Analog inputs | 8, 9, 16, 17 | I _A | -10 | | mA |
| Temperature | | | | | |
| Junction temperature | | T _J | | +150 | °C |
| Storage temperature | | Ts | -55 | +150 | °C |

Recommended Operating Conditions

| Parameter | Symbol | Min | Тур | Max | Unit |
|--------------------------------------|----------------------------------|------|-----|------|------|
| Logic supply voltage | V _{cc} | 4.75 | 5 | 5.25 | V |
| Supply voltage | V _{BB} | 10 | | 40 | V |
| Output emitter voltage | V _E | | | 1.0 | V |
| Output current continuous (see text) | I _M | -200 | | +200 | mA |
| Operating ambient temperature | T _A | 0 | | +85 | °C |
| Rise and fall time logic inputs | t _{r.} , t _f | | | 2 | μs |
| Oscillator timing resistor | R _T | 2 | 12 | 20 | kohm |





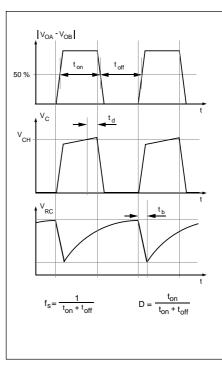


Figure 3. Definition of terms.



Electrical Characteristics

Electrical characteristics over recommended operating conditions, unless otherwise noted. $0^{\circ}C \leq T_{_{j}} \leq +125^{\circ}C$.

| General | | | | | | | |
|---|--------------------|---|--|------|------|-----|-----|
| | | | | | | | |
| Supply current | I _{cc} | 2 | Note 3. | | 65 | 70 | mA |
| Supply current | I _{cc} | 2 | Dis ₁ = Dis ₂ = HIGH. | | 7 | 10 | mA |
| Total power dissipation | P _D | | $V_{BB} = 24 \text{ V}, I_{BB1} = I_{BB2} = 200 \text{ mA}.$ | | 0.2 | 0.3 | W |
| | | | Notes 2, 3. | | | | |
| Thermal shutdown junction tem | perature | Э | Note 2 | | 160 | | °C |
| Turn-off delay | t _d | 3 | $T_A = +25^{\circ}C$, $dV_C/dt \ge 50$ mV/ μ s, | | 1.1 | 2.0 | μs |
| | | | I _{BB} = 100 mA. Note 2. | | | | |
| Logic Inputs | | | | | | | |
| Logic HIGH input voltage | V _{IH} | 2 | | 2.0 | | | V |
| Logic LOW input voltage | V_{IL} | 2 | | | | 0.6 | V |
| Logic HIGH input current | I _{IH} | 2 | V _I = 2.4 V | | | 20 | μΑ |
| Logic LOW input current | I _{IL} | 2 | V ₁ = 0.4 V | -0.2 | -0.1 | | mA |
| Analog Inputs | | | | | | | |
| Input current | I _A | 2 | V _r = 5 V | | 0.5 | 8.0 | mA |
| V _{C1} —V _{C2} mismatch | V_{Cdiff} | 2 | $T_A = 25^{\circ}C$ Note 3 | | 5 | | mV |
| Motor Outputs | | | | | | | |
| Lower transistor saturation volta | age | 8 | I _M = 200 mA | | 0.2 | 0.4 | V |
| Lower transistor leakage currer | nt | 2 | Dis1 = Dis2 = High, T _A = 25°C | | 50 | | μΑ |
| Upper transistor saturation volta | age | 9 | I _M = 200 mA | | 0.9 | 1.2 | V |
| Upper transistor leakage current 2 | | 2 | Dis1 = Dis2 = High, $T_A = 25^{\circ}C$ | | 50 | | μΑ |
| Chopper Oscillator | | | | | | | |
| Chopping frequency | f _s | | $C_{T} = 4700 \text{ pF}, R_{T} = 12 \text{ kohm}$ | | 23.0 | | kHz |
| Digital filter blanking time | t _b | 3 | $C_{T} = 4700 \text{ pF. Note 3.}$ | | 1.0 | | μs |

Thermal Characteristics

| Parameter | Ref. Symbol fig. | Conditions | Min | Тур | Max | Unit |
|-----------|---------------------|------------|-----|-----|-----|------|
| T_{J-A} | R_{thJ-C} | Note 2 | | 28 | | °C/W |
| T_{J-A} | R _{thJ-A} | Note 2 | | 45 | | °C/W |

Notes

- 1. All voltages are with respect to ground. Currents are positive into, negative out of specified terminal.
- 2. Not covered by final test program.
- 3. Switching duty cycle D = 30%, $f_s = 23.0 \text{ kHz}$.



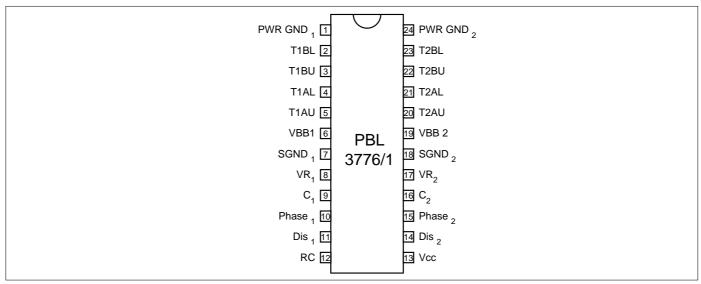


Figure 4. Pin configuration.

Pin Description

| DIP | Symbol | Description |
|-----|-----------------------------------|---|
| 1 | PWR GND ₁ | "Power Ground" from output channel 1. Connected to the ground path (see application examples). |
| 2 | T1BL | Output, channel 1, B side lower transistor. The pin will sink current when phase is high. |
| 3 | T1BU | Output, channel 1, B side upper transistor. The pin will source current when phase is low. |
| 4 | T1AL | Output, channel 1, A side lower transistor. The pin will sink current when phase is low. |
| 5 | T1AU | Output, channel 1, A side upper transistor. The pin will source current when phase is high. |
| 6 | VBB1 | Supply voltage for driving channel 1 outputs. |
| 7 | SGND ₁ | Sense ground channel 1. Logic ground reference and sense ground for the current control feedback-loop. |
| 8 | VR ₁ | Reference voltage, channel 1. Controls the comparator threshold voltage and hence the output current. |
| 9 | C ₁ | Comparator input channel 1. This input senses the instantaneous voltage across the sensing resistor, |
| 10 | Dhaca | filtered by the internal digital filter or an optional external RC network. |
| 10 | Phase ₁ | Controls the direction of channel 1 outputs T1AL, T1AU, T1BL and T1BU. |
| 11 | Dis ₁ | Disable input for channel 1. When HIGH, all four output transistors are turned off, which results in a rapidly decreasing output current to zero. |
| 12 | RC | Clock oscillator RC pin. Connect a 12 kohm resistor to V_{cc} and a 4 700 pF capacitor to ground to obtain the nominal switching frequency of 23.0 kHz and a digital filter blanking time of 1.0 μ s. |
| 13 | Vcc | Logic voltage supply, nominally +5 V. |
| 14 | Dis ₂ | Disable input for channel 2. When HIGH, all four output transistors are turned off, which results in a rapidly decreasing output current to zero. |
| 15 | Phase, | Controls the direction of channel 2 outputs T2AL, T2AU, T2BL and T2BU. |
| 16 | C_2 | Comparator input channel 2. This input senses the instantaneous voltage across the sensing resistor, filtered by the internal digital filter or an optional external RC network. |
| 17 | VR_2 | Reference voltage, channel 2. Controls the comparator threshold voltage and hence the output current. |
| 18 | SGND ₂ | Sense ground channel 1. Logic ground reference and sense ground for the current control feedback-loop. |
| 19 | VBB2 | Supply voltage for driving channel 2 outputs. |
| 20 | T2AU | Output, channel 2, A side upper transistor. The pin will source current when phase is high. |
| 21 | T2AL | Output, channel 2, A side lower transistor. The pin will sink current when phase is low. |
| 22 | T2BU | Output, channel 2, B side upper transistor. The pin will source current when phase is low. |
| 23 | T2BL | Output, channel 2, B side lower transistor. The pin will sink current when phase is high. |
| 24 | $PWR\;GND_{\scriptscriptstyle 2}$ | "Power Ground" from output channel 2. Connected to the ground path (see application examples). |



Functional Description

Each channel of the PBL 3776/1 consists of the following sections:

- An output section with four output transistors, two sourcing and two sinking, intended to drive the four transistors in an external H-bridge.
 Each transistor is capable of driving up to 200 mA continuous current.
- A logic section that controls the output transistors.
- An S-R flip-flop, and a comparator.
 The clock-oscillator is common to both channels.

Constant current control is achieved by switching the output current to the windings. This is done by sensing the peak current through the winding via a current-sensing resistor $R_{\rm s}$, effectively connected in series with the motor winding. As the current increases, a voltage develops across the sensing resistor, which is fed back to the comparator. At the predetermined level, defined by the voltage at the reference input $V_{\rm R}$, the comparator resets the flipflop, which turns off the sourcing output transistor in the circuit. Consequently the

correspond-ing lower external transistor, in the H-bridge, is turned off. The turn-off of one channel is independent of the other channel. The current decreases until the clock oscillator triggers the flipflops of both channels simultaneously, which turns on the output transistors again, and the cycle is repeated.

To prevent erroneous switching due to switching transients at turn-on, the PBL 3776/1 includes a digital filter. The clock oscillator provides a blanking pulse which is used for digital filtering of the voltage transient across the current sensing resistor during turn-on. Due to the high output drive capability, this transient might exceed the max. allowed voltage on the C inputs and damage the circuit. A resistor is placed in the feedback loop in order to prevent this transient from damaging the circuit.

The current paths during turn-on, turn-off and phase shift are shown in figure 6.

Applications Information

Output current

The maximum peak output, sink/source, current is 500 mA. But due to the power handling capacity of the package this

current can only be used for a short period of time (1mS). Recommended max continuous output current is 200 mA/output transistor. This is practical when driving MOS FET power transistors, since a high peak output current capability will rapidly charge/discharge the gate capacitance, while the continuous current usage is very small.

Current control

The regulated output current level to the motor winding is determined by the voltage at the reference input and the value of the sensing resistor, $R_{\rm s}$. The peak current through the sensing resistor (and the motor winding) can be expressed as:

$$I_{M,peak} = 0.1 \cdot V_R / R_S$$
 [A]

With a recommended value of 0.1 ohm for the sense resistor $R_{\rm s}$, a 5 V reference voltage will produce an output current of approximately 5 A. $R_{\rm s}$ should be selected for maximum motor current. Chopping frequency, winding inductance and supply voltage also affect the current, but to much less extent.

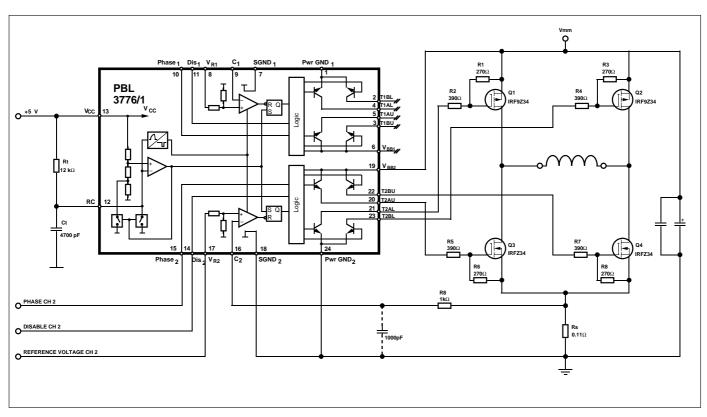


Figure 5. Typical 5 A stepper motor driver application with PBL 3776/1. One channel shown.



For accurate current regulation, the sensing resistor should be a 0.5 - 1.5 W precision resistor, i. e. less than 1% tolerance and low temperature coefficient.

Recirculating diodes

Care must be taken to assure that the recirculating current from the motor winding has a free path at all times, when designing the external H-bridge otherwise may the voltage reach dangerous levels at the outputs. See figure 6. Make sure that there are recirculating diodes included in the transistors, or if not design in external diodes. Also make sure that these diodes are sufficient for the application i.e. regarding recovery time, voltage drop etc.

Current sense filtering

At turn-on a current transient occurs, due to the recovery of the recirculation diodes and the capacitance of the motor winding. To prevent this transient from reseting the flip-flops through the current sensing comparators, the clock oscillator generates a blanking pulse at turn-on. The blanking pulse disables the comparators for a short time. Thereby preventing any voltage transient across the sensing resistor from reseting the flip-flop during the time blanking.

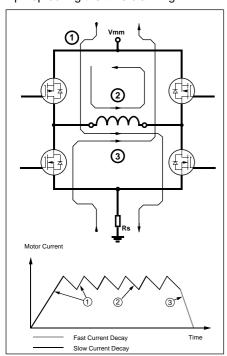


Figure 6. Output stage with current paths during turn-on, turn-off and phase shift.

Select the blanking pulse time to be longer than the duration of the switching transients by selecting a proper C_T value. The time is calculated as: $t_b = 210 \cdot C_T$ [s]

As the C_T value may vary from approximately 2 200 pF to 33 000 pF, a

blanking time ranging from 0.5 μ s to 7 μ s is possible. Nominal value is 4 700 pF, which gives a blanking time of 1.0 μ s.

As the filtering action introduces a small delay, the peak value across the sensing resistor, and hence the peak motor current, will reach a slightly higher level than what is defined by the reference voltage. The filtering delay also limits the minimum possible output current. As the output will be on for a short time each cycle, equal to the digital filtering blanking time plus additional internal delays, a small amount of current will flow through the winding. Typically this current is 1-10 % of the maximum output current set by R_c.

When optimizing low current performance, the filtering may be done by adding an external low pass filter in series with the comparator C input, see figure 5. In this case the digital blanking time should be as short as possible. The recommended filter component values are 1 kohm and 1000 pF. The transient may be reduced by adding external recircula-ting diodes. These diodes should be of the fast switching type. By doing this the filter delay will be minimized. Lowering the switching frequency also helps reduce the minimum output current.

It is recommended to add the resistor R8 in the feedback loop in order to prevent the switching transient from damaging the C inputs. See figure 5.

| | Disable 0 1 | | | |
|------------|--|--------------|--|--|
| 0 Phase | TxBU = 1 TxBL = x TxAU = x TxAU = 0 | All four off | | |
| 1 | TxBU = x TxBL = 0 TxAU = 1 TxAU = x | All four off | | |

Figure 7. Truth table.

To create an absolute zero current, the Dis input should be HIGH.

Switching frequency

The frequency of the clock oscillator is set by the timing components $R_{\scriptscriptstyle T}$ and $C_{\scriptscriptstyle T}$ at the RC-pin. Since $C_{\scriptscriptstyle T}$ sets the digital filter blanking time, the clock oscillator frequency is adjusted by $R_{\scriptscriptstyle T}$. The value of $R_{\scriptscriptstyle T}$ is limited to 2 - 20 kohm. The frequency is approximately calculated as:

$$f_s = 1 / (0.77 \cdot R_T \cdot C_T)$$

Nominal component values of 12 kohm and 4 700 pF results in a clock frequency of 23.0 kHz. A lower frequency will result in higher current ripple, but may improve low level linearity. A higher clock frequency reduces current ripple, but increases the switching losses in the IC and possibly the iron losses in the motor.

Phase inputs

A logic HIGH on a Phase input causes the TxBL pin to sink current, low voltage, and the TxAU pin to source current, high voltage. A logic LOW causes the TxAL to sink current, low voltage, and the TxBU to source current, high voltage. A time delay prevents cross conduction in the H-bridge when changing the Phase input.

See truth table fig. 7.

Dis (Disable) inputs

A logic HIGH on the Dis inputs will turn off all four transistors of the outputs, which results in a rapidly decreasing output current to zero. See truth table fig 7.

V_□ (Reference) inputs

The Vref inputs of the PBL 3776/1 have a voltage divider with a ratio of 1 to 10 to reduce the external reference voltage to an adequate level. The divider consists of closely matched resistors . Nominal input reference voltage is 5 V.

Interference

Due to the switching operation of PBL 3776/1, noise and transients are generated and coupled into adjacent circuitry. To reduce potential interference there are a few basic rules to follow:

 Use separate ground leads for power ground (the ground connection of R_s), the ground leads of PBL 3776/1, and the ground of external analog and digital circuitry. The grounds should be



connected together close to the main filtering capacitor at the power supply.

- Decouple the supply voltages close to the PBL 3776/1 circuit. Use a ceramic capacitor in parallel with an electrolytic type for both V_{CC} and V_{BB}. Route the power supply lines close together.
- Do not place sensitive circuits close to the driver. Avoid physical current loops, and place the driver close to both the motor and the power supply connector. The motor leads could preferably be twisted or shielded.

Motor selection

The PBL 3776/1 is designed for twophase bipolar stepper motors, i.e. motors that have only one winding per phase.

The chopping principle of the PBL 3776/1 is based on a constant frequency and a varying duty cycle. This scheme imposes certain restrictions on motor selection. Unstable chopping can occur if the chopping duty cycle exceeds approximately 50%. See figure 3 for definitions. To avoid this, it is necessary to select a motor with a low winding resistance and inductance, i.e. windings with fewer turns.

It is not possible to use a motor that is rated for the same voltage as the actual supply voltage. Only rated current needs to be considered. Typical motors to be used together with the PBL 3776/1 in a high current application, have a voltage rating of 0.5 to 6 V, while the supply voltage usually ranges from 12 to 40 V.

Low inductance, especially in combination with a high supply voltage, enables high stepping rates. However, to give the same torque capability at low speed, the reduced number of turns in the winding in the low resistive, low inductive motor must be compensated To achieve the best utilization of the motor driver combination it is important to find the correct operation conditions in terms of motor voltage, winding current and stepping mode to fit the motor type and the motor winding.

To find the correct operation conditions for a certain application the following procedure can be used.

1. If low noise and low resonance's or high resolution is required, use half step or even better modified half step, quarter step, etc. In order to implement modified half step or modes with better resolution an external sequence generator must be used. See the testboard manual for TB 313i testboard for more information. If the required stepping rate is high or if low cost is more important than low noise use full step mode.

- 2. Set the motor supply voltage and the winding currents to their maximum values (limited by the motor or the driver). Run the motor in the application at the lowest frequency with maximum load.
- 3. Decrease the current, by decreasing the Vref voltage, until the motor phases out, then raise the current with the

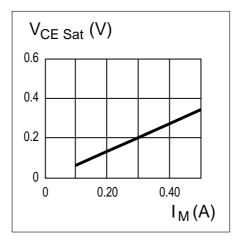


Figure 8. Typical lower transistor saturation voltage vs. output current.

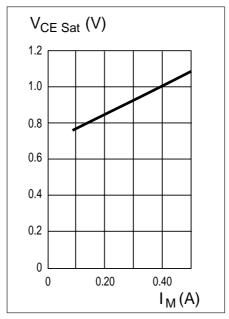


Figure 9. Typical upper transistor saturation voltage vs. output current.

selected torque margin, 25 to 50% as a guideline. This sets a first approximation of the suitable current level.

4. Run the motor at the highest frequency with maximum load. Decrease the motor voltage until the motor phases out. Increase the motor voltage with 15 to 30% as a guideline to find a first estimation of the required motor voltage.

To get an even better estimation continue to adjust the current in the low frequency range and the voltage in the high frequency range. This is a very simplified method for finding the correct operating conditions for the motor but it will be helpful in most cases. If the motor fails to run in the high frequency range at maximum voltage a motor with lower winding resistance should be selected. If the problems occur in the low frequency range a larger motor or a gearbox will have to be used.

by a higher current. A compromise has to be made. Select a motor with the lowest possible winding resistance and inductance, that still gives the required torque, and use as high supply voltage as possible, without exceeding the maximum recommended 40 V. Check that the chopping duty cycle does not exceed 50% at maximum current.

Thermal shutdown

The circuit is equipped with a thermal shutdown function that turns the outputs off at a chip (junction) temperature above 160°C. Normal operation is resumed when the temperature has decreased about 20°C.

Programming

Figure 10 shows the different input and output sequences for full-step, half-step and modified halfstep operations. **Full-step mode.** Both windings are energized at all the time with the same current, $I_{M1} = I_{M2}$. To make the motor take one step, the current direction (and the magnetic field direction) in one phase is reversed. The next step is then taken when the other phase current reverses. The current changes go through a sequence of four different states which equal four full steps until the initial state is reached again.

Half-step mode. In the half-step mode, the current in one winding is brought to zero before a complete current reversal



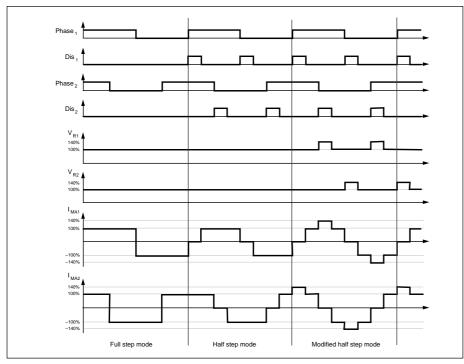


Figure 10. Stepping modes.

for more information on implementing modified half step.

Ordering Information

Package Part No.
Plastic DIP Tube PBL 3776/1NS

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Ericsson Components AB SE-164 81 Kista-Stockholm, Sweden Telephone: +46 8 757 50 00 is made. The motor will then have taken two half steps equalling one full step in rotary movement. The cycle is repeated, but on the other phase. A total of eight states are sequenced until the initial state is reached again.

Half-step mode can overcome potential resonance problems. Resonances appear as a sudden loss of torque at one or more distinct stepping rates and must be avoided so as not to loose control of the motor's shaft position.

One disadvantage with the half-step mode is the reduced torque in the half step positions, in which current flows through one winding only. The torque in this position is approximately 70 % of the full step position torque.

Modified half-step mode. The torque variations in half step mode will be eliminated if the current is increased about 1.4 times in the halfstep position. A constant torque will further reduce resonances and mechanical noise, resulting in better performance, life expectancy and reliability of the mechanical system.

Modifying the current levels must be done by bringing the reference voltage up (or down) from its nominal value correspondingly. This can be done by using DACs or simple resistor divider networks.

See SMD and application handbook