

100302

Low Power Quint 2-Input OR/NOR Gate

General Description

The 100302 is a monolithic quint 2-input OR/NOR gate with common enable. All inputs have 50 kΩ pull-down resistors and all outputs are buffered.

Features

- 43% power reduction of the 100102
- 2000V ESD protection
- Pin/function compatible with 100102
- Voltage compensated operating range = -4.2V to -5.7V
- Available to industrial grade temperature range (PLCC package only)

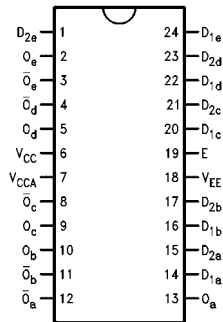
Ordering Code:

Order Number	Package Number	Package Description
100302SC	M24B	24-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide
100302PC	N24E	24-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-010, 0.400 Wide
100302QC	V28A	28-Lead Plastic Lead Chip Carrier (PLCC), JEDEC MO-047, 0.450 Square
100302QI	V28A	28-Lead Plastic Lead Chip Carrier (PLCC), JEDEC MO-047, 0.450 Square Industrial Temperature Range (-40°C to +85°C)

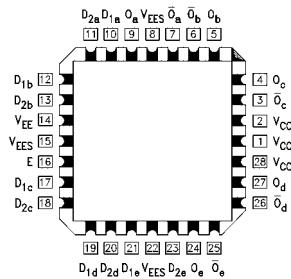
Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagrams

24-Pin DIP/SOIC



28-Pin PLCC

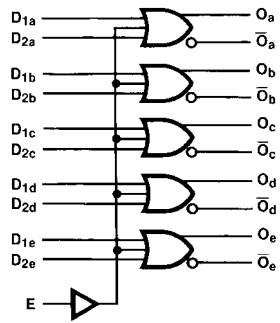


Pin Descriptions

Pin Names	Description
$D_{na}-D_{ne}$	Data Inputs
E	Enable Input
O_a-O_e	Data Outputs
$\bar{O}_a-\bar{O}_e$	Complementary Data Outputs

100302

Logic Symbol



Truth Table

D _{1X}	D _{2X}	E	O _X	\bar{O}_X
L	L	L	L	H
L	L	H	H	L
L	H	L	H	L
L	H	H	H	L
H	L	L	H	L
H	L	H	H	L
H	H	L	H	L
H	H	H	H	L

H = HIGH Voltage Level

L = LOW Voltage Level

Absolute Maximum Ratings(Note 1)

Storage Temperature (T_{STG})	-65°C to +150°C
Maximum Junction Temperature (T_J)	+150°C
V_{EE} Pin Potential to Ground Pin	-7.0V to +0.5V
Input Voltage (DC)	V_{EE} to +0.5V
Output Current (DC Output HIGH)	-50 mA
ESD (Note 2)	≥2000V

Recommended Operating Conditions

Case Temperature (T_C)	Commercial	0°C to +85°C
	Industrial	-40°C to +85°C
Supply Voltage (V_{EE})		-5.7V to -4.2V

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum rating. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 2: ESD testing conforms to MIL-STD-883, Method 3015.

Commercial Version**DC Electrical Characteristics** (Note 3)

$V_{EE} = -4.2V$ to $-5.7V$, $V_{CC} = V_{CCA} = GND$, $T_C = 0^\circ C$ to $+85^\circ C$

Symbol	Parameter	Min	Typ	Max	Units	Conditions	
V_{OH}	Output HIGH Voltage	-1025	-955	-870	mV	$V_{IN} = V_{IH(Max)}$ or $V_{IL(Min)}$	Loading with 50Ω to -2.0V
V_{OL}	Output LOW Voltage	-1830	-1705	-1620	mV		
V_{OHC}	Output HIGH Voltage	-1035			mV	$V_{IN} = V_{IH(Min)}$ or $V_{IL(Max)}$	Loading with 50Ω to -2.0V
V_{OLC}	Output LOW Voltage			-1610	mV		
V_{IH}	Input HIGH Voltage	-1165		-870	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	-1830		-1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50			μA	$V_{IN} = V_{IL(Min)}$	
I_{IH}	Input HIGH Current			240	μA	$V_{IN} = V_{IH(Max)}$	
I_{EE}	Power Supply Current	-45	-36	-20	mA	Inputs OPEN	

Note 3: The specified limits represent the "worst case" value for the parameter. Since these values normally occur at the temperature extremes, additional noise immunity and guardbanding can be achieved by decreasing the allowable system operating ranges. Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

DIP AC Electrical Characteristics

$V_{EE} = -4.2V$ to $-5.7V$, $V_{CC} = V_{CCA} = GND$

Symbol	Parameter	$T_C = 0^\circ C$		$T_C = +25^\circ C$		$T_C = +85^\circ C$		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay	0.50	1.15	0.50	1.15	0.50	1.25	ns	Figures 1, 2 (Note 4)
t_{PHL}	Data to Output								
t_{PLH}	Propagation Delay	0.70	1.90	0.70	1.90	0.80	2.00	ns	
t_{PHL}	Enable to Output								
t_{TLH}	Transition Time	0.40	1.20	0.40	1.20	0.40	1.20	ns	Figures 1, 2
t_{THL}	20% to 80%, 80% to 20%								

Note 4: The propagation delay specified is for single output switching. Delays may vary up to 100 ps with multiple outputs switching.

Commercial Version (Continued) SOIC and PLCC AC Electrical Characteristics

$V_{EE} = -4.2V$ to $-5.7V$, $V_{CC} = V_{CCA} = GND$

Symbol	Parameter	$T_C = 0^\circ C$		$T_C = +25^\circ C$		$T_C = +85^\circ C$		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay Data to Output	0.50	1.05	0.50	1.05	0.50	1.15	ns	Figures 1, 2 (Note 5)
t_{PLH} t_{PHL}	Propagation Delay Enable to Output	0.70	1.80	0.70	1.80	0.80	1.90	ns	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.40	1.10	0.40	1.10	0.40	1.10	ns	Figures 1, 2
t_{OSHL}	Maximum Skew Common Edge Output-to-Output Variation Data to Output Path		250		250		250	ps	PLCC Only (Note 6)
t_{OSHL}	Maximum Skew Common Edge Output-to-Output Variation Enable to Output Path		310		310		310	ps	PLCC Only (Note 6)
t_{OSLH}	Maximum Skew Common Edge Output-to-Output Variation Data to Output Path		200		200		200	ps	PLCC Only (Note 6)
t_{OSLH}	Maximum Skew Common Edge Output-to-Output Variation Enable to Output Path		330		330		330	ps	PLCC Only (Note 6)
t_{OST}	Maximum Skew Opposite Edge Output-to-Output Variation Data to Output Path		250		250		250	ps	PLCC Only (Note 6)
t_{OST}	Maximum Skew Opposite Edge Output-to-Output Variation Enable to Output Path		330		330		330	ps	PLCC Only (Note 6)
t_{PS}	Maximum Skew Pin (Signal) Transition Variation Data to Output Path		200		200		200	ps	PLCC Only (Note 6)
t_{PS}	Maximum Skew Pin (Signal) Transition Variation Enable to Output Path		280		280		280	ps	PLCC Only (Note 6)

Note 5: The propagation delay specified is for single output switching. Delays may vary up to 100 ps with multiple outputs switching.

Note 6: Output-to-Output Skew is defined as the absolute value of the difference between the actual propagation delay for any outputs within the same packaged device. The specifications apply to any outputs switching in the same direction either HIGH-to-LOW (t_{OSHL}), or LOW-to-HIGH (t_{OSLH}), or in opposite directions both HL and LH (t_{OST}). Parameters t_{OST} and t_{PS} guaranteed by design.

Industrial Version**PLCC DC Electrical Characteristics** (Note 7)
 $V_{EE} = -4.2V$ to $-5.7V$, $V_{CC} = V_{CCA} = GND$, $T_C = -40^\circ C$ to $+85^\circ C$

Symbol	Parameter	$T_C = -40^\circ C$		$T_C = 0^\circ C$ to $+85^\circ C$		Units	Conditions	
		Min	Max	Min	Max			
V_{OH}	Output HIGH Voltage	-1085	-870	-1025	-870	mV	$V_{IN} = V_{IH(Max)}$ or $V_{IL(Min)}$	Loading with 50Ω to -2.0V
V_{OL}	Output LOW Voltage	-1830	-1575	-1830	-1620			
V_{OHC}	Output HIGH Voltage	-1095		-1035		mV	$V_{IN} = V_{IH(Min)}$ or $V_{IL(Max)}$	Loading with 50Ω to -2.0V
V_{OLC}	Output LOW Voltage		-1565		-1610			
V_{IH}	Input HIGH Voltage	-1170	-870	-1165	-870	mV	Guaranteed HIGH Signal for ALL Inputs	
V_{IL}	Input LOW Voltage	-1830	-1480	-1830	-1475	mV	Guaranteed LOW Signal for ALL Inputs	
I_{IL}	Input LOW Current	0.05		0.05		μA	$V_{IN} = V_{IL(Min)}$	
I_{IH}	Input HIGH Current		300		240	μA	$V_{IN} = V_{IH(Max)}$	
I_{EE}	Power Supply Current	-45	-20	-45	-20	mA	Inputs OPEN	

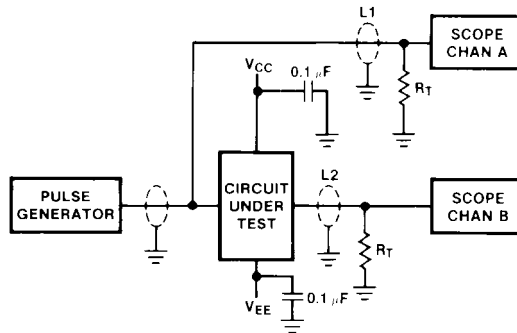
Note 7: The specified limits represent the "worst case" value for the parameter. Since these values normally occur at the temperature extremes, additional noise immunity and guardbanding can be achieved by decreasing the allowable system operating ranges. Conditions for testing shown in the tables are chosen to guarantee operation under the "worst case" conditions.

PLCC AC Electrical Characteristics
 $V_{EE} = -4.2V$ to $-5.7V$, $V_{CC} = V_{CCA} = GND$

Symbol	Parameter	$T_C = -40^\circ C$		$T_C = +25^\circ C$		$T_C = +85^\circ C$		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay	0.40	1.05	0.50	1.05	0.50	1.15	ns	Figures 1, 2 (Note 8)
t_{PHL}	Data to Output								
t_{PLH}	Propagation Delay	0.70	1.80	0.70	1.80	0.80	1.90	ns	
t_{PHL}	Enable to Output								
t_{TLH}	Transition Time	0.30	1.10	0.40	1.10	0.40	1.10	ns	Figures 1, 2
t_{THL}	20% to 80%, 80% to 20%								

Note 8: The propagation delay specified is for single output switching. Delays may vary up to 200 ps with multiple outputs switching.

Test Circuitry



- Notes:**
 $V_{CC}, V_{CCA} = +2V, V_{EE} = -2.5V$
 L1 and L2 = equal length 50Ω impedance lines
 $R_T = 50\Omega$ terminator internal to scope
 Decoupling 0.1 μF from GND to V_{CC} and V_{EE}
 All unused outputs are loaded with 50Ω to GND
 C_L = Fixture and stray capacitance ≤ 3 pF

FIGURE 1. AC Test Circuit

Switching Waveforms

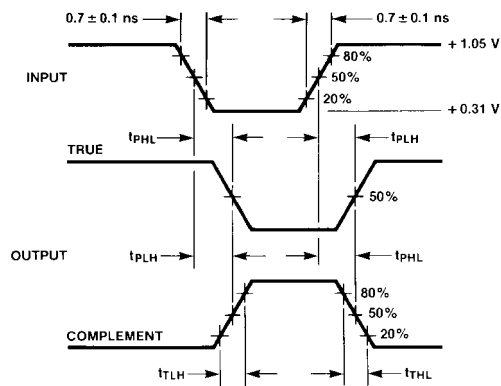
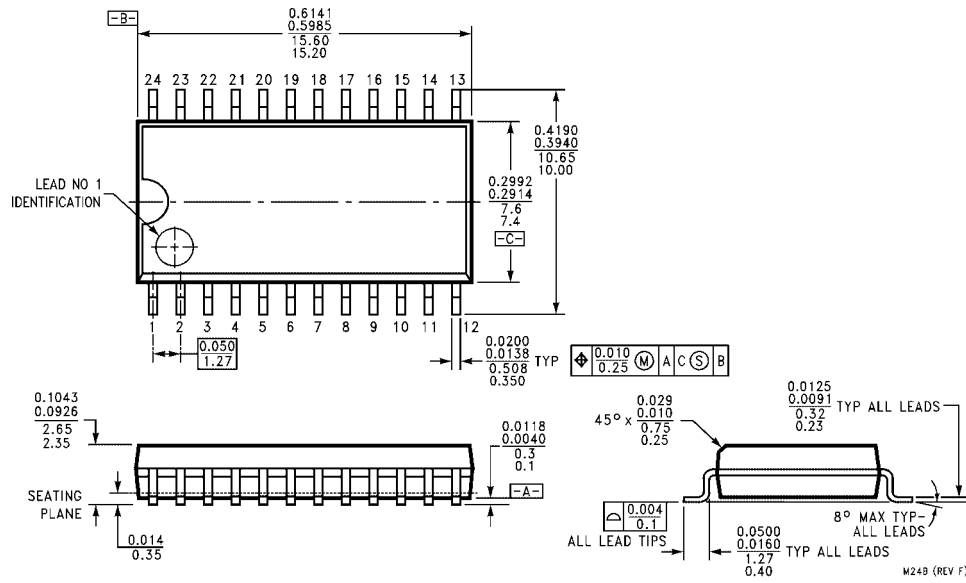
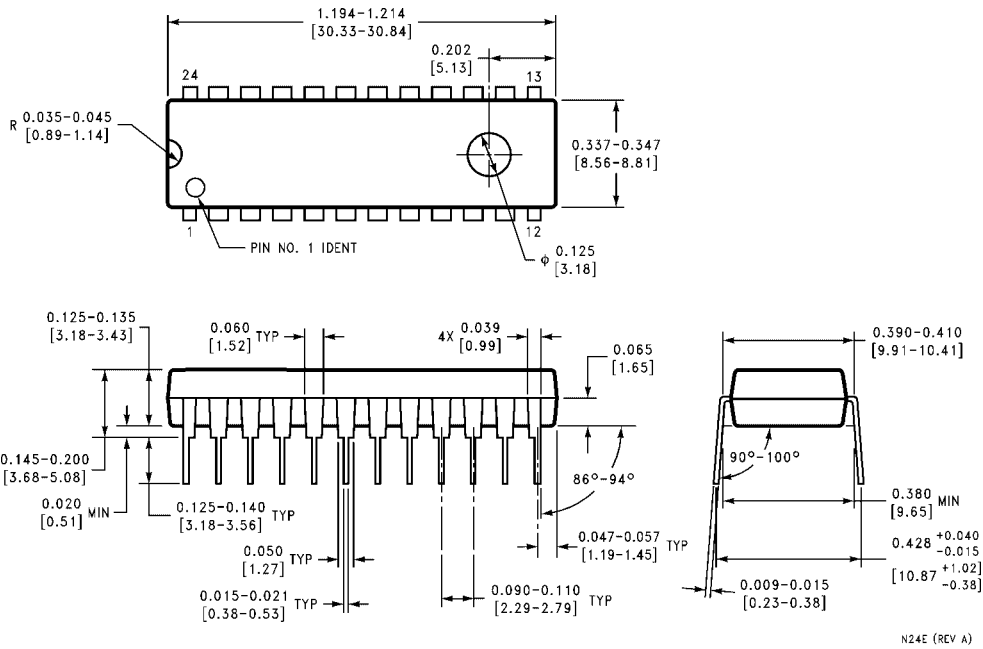


FIGURE 2. Propagation Delay and Transition Times

Physical Dimensions inches (millimeters) unless otherwise noted

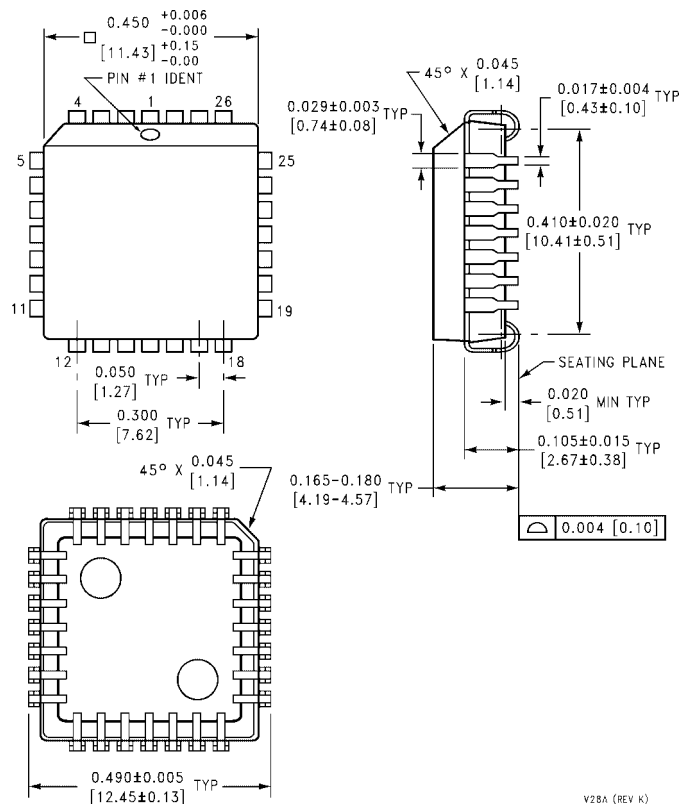


**24-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide
Package Number M24B**



**24-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-010, 0.400 Wide
Package Number N24E**

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



28-Lead Plastic Lead Chip Carrier (PLCC), JEDEC MO-047, 0.450 Square Package Number V28A

Fairchild does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied and Fairchild reserves the right at any time without notice to change said circuitry and specifications.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

www.fairchildsemi.com