

# 100311 Low Skew 1:9 Differential Clock Driver

## General Description

The 100311 contains nine low skew differential drivers, designed for generation of multiple, minimum skew differential clocks from a single differential input (CLKIN,  $\overline{\text{CLKIN}}$ ). If a single-ended input is desired, the  $V_{\text{BB}}$  output pin may be used to drive the remaining input line. A HIGH on the enable pin ( $\overline{\text{EN}}$ ) will force a LOW on all of the  $\text{CLK}_n$  outputs and a HIGH on all of the  $\overline{\text{CLK}}_n$  output pins. The 100311 is ideal for distributing a signal throughout a system without worrying about the original signal becoming too corrupted by undesirable delays and skew.

## Features

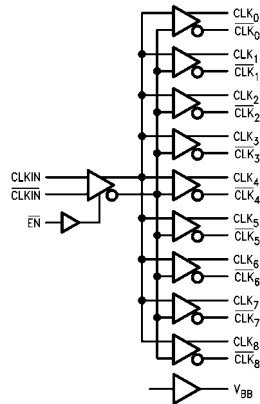
- Low output-to-output skew
- 2000V ESD protection
- 1:9 low skew clock driver
- Differential inputs and outputs
- Available to industrial grade temperature range (PLCC package only)

## Ordering Code:

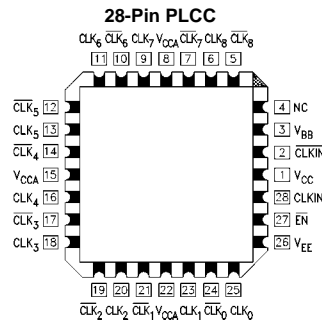
Order Number	Package Number	Package Description
100311QC	V28A	28-Lead Plastic Lead Chip Carrier (PLCC), JEDEC MO-047, 0.450 Square
100311QI	V28A	28-Lead Plastic Lead Chip Carrier (PLCC), JEDEC MO-047, 0.450 Square Industrial Temperature Range (-40°C to +85°C)

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

## Logic Symbol



## Connection Diagram



## Pin Descriptions

Pin Names	Description
CLKIN, $\overline{\text{CLKIN}}$	Differential Clock Inputs
$\overline{\text{EN}}$	Enable
CLK <sub>0-8</sub> , $\overline{\text{CLK}}_0-8$	Differential Clock Outputs
$V_{\text{BB}}$	$V_{\text{BB}}$ Output
NC	No Connect

## Truth Table

CLKIN	$\overline{\text{CLKIN}}$	$\overline{\text{EN}}$	CLK <sub>n</sub>	$\overline{\text{CLK}}_n$
L	H	L	L	H
H	L	L	H	L
X	X	H	L	H

**Absolute Maximum Ratings** (Note 1)

Storage Temperature ( $T_{STG}$ )	-65°C to +150°C
Maximum Junction Temperature ( $T_J$ )	+150°C
Pin Potential to Ground Pin ( $V_{EE}$ )	-7.0V to +0.5V
Input Voltage (DC)	$V_{EE}$ to +0.5V
Output Current (DC Output HIGH)	-50 mA
ESD (Note 2)	$\geq 2000V$

**Recommended Operating Conditions**

Case Temperature ( $T_C$ )	
Commercial	0°C to +85°C
Industrial	-40°C to +85°C
Supply Voltage ( $V_{EE}$ )	-5.7V to -4.2V

**Note 1:** The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum rating. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

**Note 2:** ESD testing conforms to MIL-STD-883, Method 3015.

**Commercial Version****DC Electrical Characteristics** (Note 3)

$V_{EE} = -4.2V$  to  $-5.7V$ ,  $V_{CC} = V_{CCA} = GND$ ,  $T_C = 0^\circ C$  to  $+85^\circ C$

Symbol	Parameter	Min	Typ	Max	Units	Conditions
$V_{OH}$	Output HIGH Voltage	-1025	-955	-870	mV	$V_{IN} = V_{IH}$ (Max) Loading with $50\Omega$ to $-2.0V$
$V_{OL}$	Output LOW Voltage	-1830	-1705	-1620	mV	or $V_{IL}$ (Min)
$V_{OHC}$	Output HIGH Voltage	-1035			mV	$V_{IN} = V_{IH}$ Loading with $50\Omega$ to $-2.0V$
$V_{OLC}$	Output LOW Voltage			-1610	mV	or $V_{IL}$ (Max)
$V_{BB}$	Output Reference Voltage	-1380	-1320	-1260	mV	$I_{V_{BB}} = -300 \mu A$
$V_{DIFF}$	Input Voltage Differential	150			mV	Required for Full Output Swing
$V_{CM}$	Common Mode Voltage	$V_{CC} - 2.0$		$V_{CC} - 0.5$	V	
$V_{IH}$	Input HIGH Voltage	-1165		-870	mV	Guaranteed HIGH Signal for All Inputs
$V_{IL}$	Input LOW Voltage	-1830		-1475	mV	Guaranteed LOW Signal for All Inputs
$I_{IL}$	Input LOW Current	0.50			$\mu A$	$V_{IN} = V_{IL}$ (Min)
$I_{IH}$	Input HIGH Current CLKIN, $\overline{CLKIN}$ EN			100 250	$\mu A$	$V_{IN} = V_{IH}$ (Max)
$I_{CBO}$	Input Leakage Current	-10			$\mu A$	$V_{IN} = V_{EE}$
$I_{EE}$	Power Supply Current	-115		-57	mA	Inputs Open

**Note 3:** The specified limits represent the "worst case" value for the parameter. Since these values normally occur at the temperature extremes, additional noise immunity and guardbanding can be achieved by decreasing the allowable system operating ranges. Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

## Commercial Version (Continued) AC Electrical Characteristics

$V_{EE} = -4.2V$  to  $-5.7V$ ,  $V_{CC} = V_{CCA} = GND$

Symbol	Parameter	$T_C = 0^\circ C$			$T_C = +25^\circ C$			$T_C = +85^\circ C$			Units	Conditions
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
$f_{MAX}$	Max Toggle Frequency CLKIN to $Q_n$	750			750			750			MHz	(Note 4)
$t_{PLH}$ $t_{PHL}$	Propagation Delay, CLKIN <sub>n</sub> to CLK <sub>n</sub> Differential Single-Ended	0.75	0.84	0.95	0.75	0.86	0.95	0.84	0.93	1.04	ns	Figure 3
$t_{PLH}$ $t_{PHL}$	Propagation Delay SEL to Output	0.75	1.03	1.20	0.80	1.05	1.25	0.85	1.12	1.35	ns	Figure 2
$t_{PS}$	LH–HL Skew	10 30			10 30			10 30			ps	(Note 5)(Note 8)
$t_{OSLH}$	Gate–Gate Skew LH	20 50			20 50			20 50				(Note 6)(Note 8)
$t_{OSHL}$	Gate–Gate Skew HL	20 50			20 50			20 50				(Note 6)(Note 8)
$t_{OST}$	Gate–Gate LH–HL Skew	30 60			30 60			30 60				(Note 7)(Note 8)
$t_S$	Setup Time EN <sub>n</sub> to CLKIN <sub>n</sub>	250			250			300			ps	
$t_H$	Hold Time EN <sub>n</sub> to CLKIN <sub>n</sub>	0			0			0			ps	
$t_R$	Release Time EN <sub>n</sub> to CLKIN <sub>n</sub>	300			300			300			ps	
$t_{TLH}$ $t_{THL}$	Transition Time 20% to 80%, 80% to 20%	275	500	750	275	480	750	275	460	750	ps	Figure 4

**Note 4:**  $f_{MAX}$  = the highest frequency at which output  $V_{OL}/V_{OH}$  levels still meet  $V_{IN}$  specifications. The F311 will function @ 1 GHz.

**Note 5:**  $t_{PS}$  describes opposite edge skews, i.e. the difference between the delay of a differential output signal pair's LOW-to-HIGH and HIGH-to-LOW propagation delays. With differential signal pairs, a LOW-to-HIGH or HIGH-to-LOW transition is defined as the transition of the true output or input pin.

**Note 6:**  $t_{OSLH}$  describes in-phase gate-to-gate differential propagation skews with all differential outputs going LOW-to-HIGH;  $t_{OSHL}$  describes the same conditions except with the outputs going HIGH-to-LOW.

**Note 7:**  $t_{OST}$  describes the maximum worst case difference in any of the  $t_{PS}$ ,  $t_{OSLH}$  or  $t_{OST}$  delay paths combined.

**Note 8:** The skew specifications pertain to differential I/O paths.

## Industrial Version

### DC Electrical Characteristics (Note 9)

$V_{EE} = -4.2V$  to  $-5.7V$ ,  $V_{CC} = V_{CCA} = GND$ ,  $T_C = -40^\circ C$  to  $+85^\circ C$

Symbol	Parameter	$T_C = -40^\circ C$		$T_C = 0^\circ C$ to $+85^\circ C$		Units	Conditions	
		Min	Max	Min	Max			
$V_{OH}$	Output HIGH Voltage	-1085	-870	-1025	-870	mV	$V_{IN} = V_{IH}$ (Max) or $V_{IL}$ (Min)	Loading with 50Ω to -2.0V
$V_{OL}$	Output LOW Voltage	-1830	-1575	-1830	-1620	mV	$V_{IN} = V_{IH}$ or $V_{IL}$ (Min)	Loading with 50Ω to -2.0V
$V_{OHC}$	Output HIGH Voltage	-1095		-1035		mV		
$V_{OLC}$	Output LOW Voltage		-1565		-1610	mV		
$V_{BB}$	Output Reference Voltage	-1395	-1255	-1380	-1260	mV	$I_{VBB} = -300 \mu A$	
$V_{DIFF}$	Input Voltage Differential	150		150		mV	Required for Full Output Swing	
$V_{CM}$	Common Mode Voltage	$V_{CC} - 2.0$	$V_{CC} - 0.5$	$V_{CC} - 2.0$	$V_{CC} - 0.5$	V		
$V_{IH}$	Input HIGH Voltage	-1170	-870	-1165	-870	mV	Guaranteed HIGH Signal for All Inputs	

## Industrial Version (Continued)

### DC Electrical Characteristics (Note 9)

$V_{EE} = -4.2V$  to  $-5.7V$ ,  $V_{CC} = V_{CCA} = GND$

Symbol	Parameter	$T_C = -40^\circ C$		$T_C = 0^\circ C$ to $+85^\circ C$		Units	Conditions
		Min	Max	Min	Max		
$V_{IL}$	Input LOW Voltage	-1830	-1480	-1830	-1475	mV	Guaranteed LOW Signal for All Inputs
$I_{IL}$	Input LOW Current	0.50		0.50		$\mu A$	$V_{IN} = V_{IL}$ (Min)
$I_{IH}$	Input HIGH Current CLKIN, $\overline{CLKIN}$ EN		100 250		100 250	$\mu A$	$V_{IN} = V_{IH}$ (Max)
$I_{CBO}$	Input Leakage Current	-10		-10		$\mu A$	$V_{IN} = V_{EE}$
$I_{EE}$	Power Supply Current	-115	-57	-115	-57	mA	Inputs Open
$V_{PP}$	Minimum Input Swing	150		150		mV	
$V_{CMR}$	Common Mode Range	$V_{CC}-2.0$	$V_{CC}-0.5$	$V_{CC}-2.0$	$V_{CC}-0.5$	V	

**Note 9:** The specified limits represent the "worst case" value for the parameter. Since these values normally occur at the temperature extremes, additional noise immunity and guardbanding can be achieved by decreasing the allowable system operating ranges. Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

### AC Electrical Characteristics

$V_{EE} = -4.2V$  to  $-5.7V$ ,  $V_{CC} = V_{CCA} = GND$

Symbol	Parameter	$T_C = -40^\circ C$			$T_C = +25^\circ C$			$T_C = +85^\circ C$			Units	Conditions
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
$f_{MAX}$	Max Toggle Frequency CLKIN to $Q_n$	750			750			750			MHz	(Note 10)
$t_{PLH}$ $t_{PHL}$	Propagation Delay, CLKIN <sub>n</sub> to CLK <sub>n</sub> Differential Single-Ended	0.72 0.62	0.81 0.89	0.92 1.02	0.77 0.67	0.86 0.93	0.95 1.17	0.84 0.74	0.93 1.06	1.04 1.24	ns	Figure 3
$t_{PLH}$ $t_{PHL}$	Propagation Delay SEL to Output	0.70	0.97	1.20	0.80	1.05	1.25	0.85	1.12	1.35	ns	Figure 2
$t_{PS}$	LH-HL Skew		10	30		10	30		10	30	ps	(Note 11)(Note 14)
$t_{OSLH}$	Gate-Gate Skew LH		20	50		20	50		20	50	ps	(Note 12)(Note 14)
$t_{OSHL}$	Gate-Gate Skew HL		20	50		20	50		20	50	ps	(Note 12)(Note 14)
$t_{OST}$	Gate-Gate LH-HL Skew		30	60		30	60		30	60	ps	(Note 13)(Note 14)
$t_S$	Setup Time EN <sub>n</sub> to CLKIN <sub>n</sub>	250			250			300			ps	
$t_H$	Hold Time EN <sub>n</sub> to CLKIN <sub>n</sub>	0			0			0			ps	
$t_R$	Release Time EN <sub>n</sub> to CLKIN <sub>n</sub>	300			300			300			ps	
$t_{TLH}$ $t_{THL}$	Transition Time 20% to 80%, 80% to 20%	275	500	750	275	480	750	275	460	750	ps	Figure 4

**Note 10:**  $f_{MAX}$  = the highest frequency of which output  $V_{OL}/V_{OH}$  levels still meet  $V_{IN}$  specifications. The F311 will function @ 1 GHz

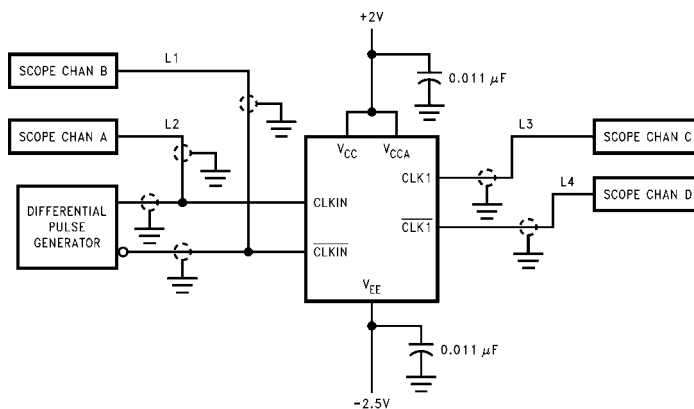
**Note 11:**  $t_{PS}$  describes opposite edge skews, i.e. the difference between the delay of a differential output signal pair's LOW-to-HIGH and HIGH-to-LOW propagation delays. With differential signal pairs, a LOW-to-HIGH or HIGH-to-LOW transition is defined as the transition of the true output or input pin.

**Note 12:**  $t_{OSLH}$  describes in-phase gate differential propagation skews with all differential outputs going LOW-to-HIGH;  $t_{OSHL}$  describes the same conditions except with the outputs going HIGH-to-LOW.

**Note 13:**  $t_{OST}$  describes the maximum worst case difference in any of the  $t_{PS}$ ,  $t_{OSLH}$  or  $t_{OST}$  delay paths combined.

**Note 14:** The skew specifications pertain to differential I/O paths.

### Test Circuit



**Note:**  
 Shown for testing CLKIN to CLK1 in the differential mode.  
 L1, L2, L3 and L4 = equal length 50Ω impedance lines.  
 All unused inputs and outputs are loaded with 50Ω in parallel with ≤ 3 pF to GND.  
 Scope should have 50Ω input terminator internally.

FIGURE 1. AC Test Circuit

### Switching Waveforms

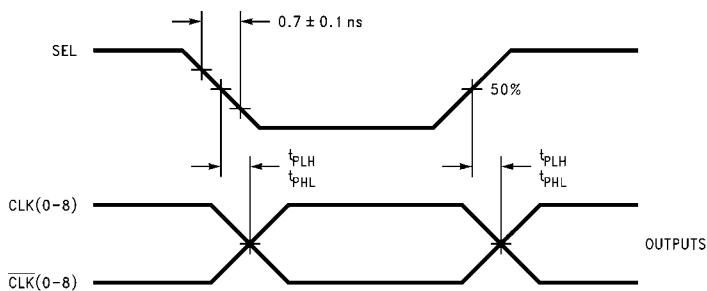


FIGURE 2. Propagation Delay, EN to Outputs

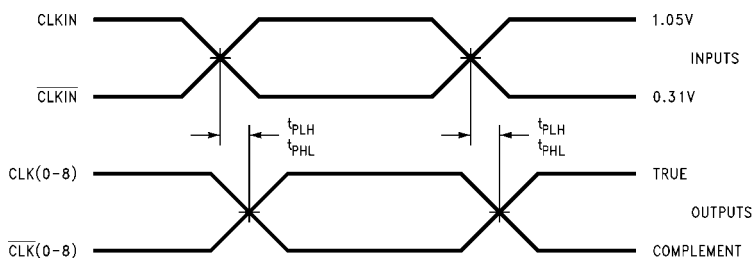


FIGURE 3. Propagation Delay, CLKIN/CLKIN to Outputs

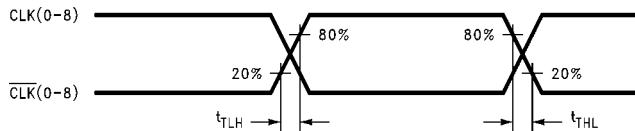
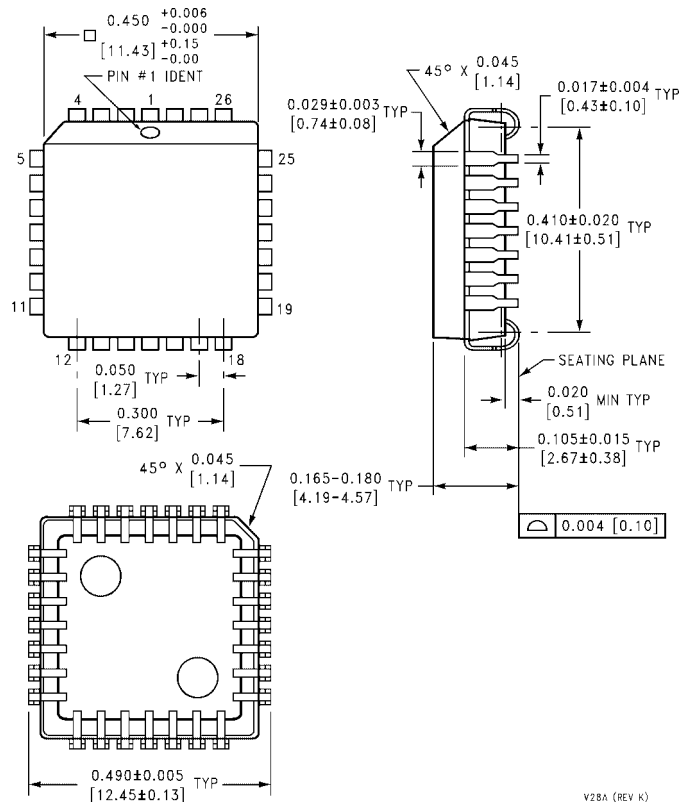


FIGURE 4. Transition Times

**Physical Dimensions** inches (millimeters) unless otherwise noted



V28A (REV K)

**28-Lead Plastic Lead Chip Carrier (PLCC), JEDEC MO-047, 0.450 Square Package Number V28A**

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