1 PRODUCT OVERVIEW

OVERVIEW

The KS57C4104/KS57C4204/KS57C4304 single-chip CMOS microcontroller has been designed for very high performance using Samsung's newest 4-bit CPU core, SAM47 (Samsung Arrangeable Microcontroller).

With an A/D converter, LED direct drive pins, an 8-bit serial I/O interface, and an 8-bit timer/counter, the KS57C4104/KS57C4204/KS57C4304 offers you an excellent design solution for a wide variety of home appliance applications — electric fans, cookers, boilers, and air conditioners, for example.

Up to 35 pins of the 42-pin SDIP or 44-pin QFP package can be dedicated to I/O. Seven vectored interrupts provide fast response to internal and external events.

In addition, the KS57C4104/KS57C4204/KS57C4304's advanced CMOS technology provides for low power consumption and a wide operating voltage range.

OTP

The KS57C4104/KS57C4204/KS57C4304 microcontroller is also available in OTP (One Time Programmable) version, KS57P4104/KS57P4204/KS57P4304. KS57P4104/KS57P4204/KS57P4304 microcontroller has an on-chip 4-Kbyte one-time-programmable EPROM instead of masked ROM. The KS57P4104/KS57P4204/KS57P4304 is comparable to KS57C4104/KS57C4204/KS57C4304, in function, in D.C. electrical characteristics and in pin configuration.

DEVELOPMENT SUPPORT

The Samsung Microcontroller Development System, SMDS, provides you with a complete PC-based development environment for KS57-series microcontrollers that is powerful, reliable, and portable. In addition to its window-based program development structure, the SMDS toolset includes versatile debugging, trace, instruction timing, and performance measurement applications.

The Samsung Generalized Assembler (SAMA) has been designed specifically for the SMDS environment and accepts assembly language sources in a variety of microprocessor formats. SAMA generates industry-standard hex files that also contain program control data for SMDS compatibility.

FEATURES SUMMARY

Memory

- 256 × 4-bit RAM
- 4,096 × 8-bit ROM

35 I/O Pins

- I/O: 31 pins including 8 LED direct drive pins (KS57C4104/C4304)
  18 pins including 8 LED direct drive pins (KS57C4204)
- Input only: 4 pins

A/D Converter

- 6-channel with 8-bit resolution
- 22.89 µs conversion speed at 4.19 MHz

Basic Timer

- One 8-bit basic timer
- Watchdog timer functions
- Four interval clock selection

Timer/Counters

- Two 8-bit timer/counter (TC0, TC1)
- Programmable 8-bit timer
- External event counter
- Arbitrary clock frequency output
- PWM output mode (TC1)

Watch Timer

- One watch timer 8-bit
- Time interval generation: 0.5 s, 3.9 ms at 4.19 MHz
- Four frequency outputs to BUZ pin

8-bit Serial I/O Interface

- 8-bit transmit/receive mode
- 8-bit receive mode
- LSB-first or MSB-first transmission selectable
- Internal or external clock source

Built-in reset circuit (KS57C4304 only)

- Built-in power-on reset circuit

Interrupts

- Five internal vectored interrupts (INTB, INTT0, INTT1, INTS, INTAD)
- Three external vectored interrupts (INT0, INT1, INT4)
- Two quasi-interrupts (INT2, INTW)

Bit Sequential Carrier

- Supports 16-bit serial data transfer in arbitrary format

Memory-Mapped I/O Structure

- Data memory bank 15

Two Power-Down Modes

- Idle mode (only CPU clock stops)
- Stop mode (system oscillation stops)

Oscillation Sources

- Crystal, Ceramic, or RC for system clock
- Crystal, Ceramic: 0.4–6.0 MHz
- RC: 4 MHz (typ)
- CPU clock divider circuit (by 4, 8, or 64)

Instruction Execution Times

- 0.95, 1.91, 15.3 µs at 4.19 MHz
- 0.67, 1.33, 10.7 µs at 6.0 MHz

Operating Temperature

- – 40 °C to 85 °C

Operating Voltage Range

- 1.8 V to 5.5 V (KS57C4104/C4204)
- 2.5 V to 5.5 V (KS57C4304)

Package Type

- 42-pin SDIP, 44-pin QFP (KS57C4104/C4304)
  30-pin SDIP, 28-pin SOP (KS57C4204)

14 ELECTRICAL DATA

OVERVIEW

In this section, information on KS57C4104/C4204/C4304 electrical characteristics is presented as tables and graphics. The information is arranged in the following order:

Standard Electrical Characteristics

— Absolute maximum ratings
— D.C. electrical characteristics
— System clock oscillator characteristics
— Operating voltage range
— A.C. electrical characteristics
— A/D converter electrical characteristics
— I/O capacitance

Stop Mode Characteristics and Timing Waveforms

— RAM data retention supply voltage in stop mode
— Stop mode release timing when initiated by RESET
— Stop mode release timing when initiated by an interrupt request

Miscellaneous Timing Waveforms

— A.C timing measurement points (except for X_{IN})
— Clock timing measurement at X_{IN}
— TCL0/1 timing
— Input timing for RESET signal
— Input timing for external interrupts and quasi-interrupts
— KS57C4304 power-on RESET timing
— Serial data transfer timing

Table 14-1. KS57C4104/C4204 Absolute Maximum Ratings

(T_A = 25 °C)

Parameter	Symbol	Conditions		Rating	Units
Supply Voltage	V_{DD}	–		– 0.3 to + 6.5	V
Input Voltage	V_I	All I/O ports		– 0.3 to V_{DD} + 0.3	V
Output Voltage	V_O	–		– 0.3 to V_{DD} + 0.3	V
Output Current High	I_{OH}	One pin		– 15	mA
		All output pins		– 35	
Output Current Low	I_{OL}	One pin	peak value (note)	+ 30	mA
			rms value	+ 15	
		All pins	peak value (note)	+ 100	
			rms value	+ 60	
Operating Temperature	T_A	–		– 40 to + 85	°C
Storage Temperature	T_{stg}	–		– 65 to + 150	°C

NOTE: The values for Output Current Low (I_{OL}) are calculated as Peak Value $\times \sqrt{\text{Duty}}$.

Table 14-2. KS57C4104/C4204 D.C. Electrical Characteristics

(T_A = – 40 °C to + 85 °C, V_{DD} = 1.8 V to 5.5 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Input High Voltage	V_{IH1}	All input pins except those specified below for V_{IH2}–V_{IH3}	0.7 V_{DD}	–	V_{DD}	V
	V_{IH2}	Ports 0, 1, 3, 6 and RESET	0.8 V_{DD}		V_{DD}	
	V_{IH3}	X_{IN}, X_{OUT}	V_{DD} – 0.1		V_{DD}	
Input Low Voltage	V_{IL1}	All input pins except those specified below for V_{IL2}–V_{IL3}	–	–	0.3 V_{DD}	V
	V_{IL2}	Ports 0, 1, 3, 6 and RESET			0.2 V_{DD}	
	V_{IL3}	X_{IN}, X_{OUT}			0.1	
Output High Voltage	V_{OH}	V_{DD} = 4.5 V to 5.5 V I_{OH} = – 1 mA Ports 0, 2–8	V_{DD} – 1.0	–	–	V
Output Low Voltage	V_{OL}	V_{DD} = 4.5 V to 5.5 V I_{OL} = 15 mA Ports 4 and 5 only	–	0.4	2	V
		I_{OL} = 4 mA All output ports except ports 4 and 5		0.2		
Input High Leakage Current	I_{LIH1}	V_I = V_{DD} All input pins except those specified below for I_{LIH2}	–	–	3	µA
	I_{LIH2}	V_I = V_{DD} X_{IN} and X_{OUT} only			20	
Input Low Leakage Current	I_{LIL1}	V_I = 0 V All input pins except X_{IN} and X_{OUT}, RESET	–	–	– 3	µA
	I_{LIL2}	V_I = 0 V X_{IN} and X_{OUT} only			– 20	
Output High Leakage Current	I_{LOH}	V_O = V_{DD} All output pins	–	–	3	µA
Output Low Leakage Current	I_{LOL}	V_O = 0 V All output pins	–	–	– 3	µA
Pull-up Resistor	R_{L1}	V_I = 0 V; V_{DD} = 5 V except RESET	25	50	100	kΩ
		V_I = 0 V; V_{DD} = 3 V except RESET	50	100	200	
Pull-up Resistor	R_{L2}	V_I = 0 V; V_{DD} = 5 V; RESET	100	250	400	kΩ
		V_I = 0 V; V_{DD} = 3 V; RESET	200	500	800	

Table 14-2. KS57C4104/C4204 D.C. Electrical Characteristics (Continued)

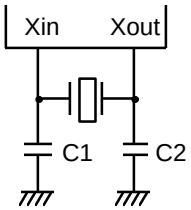
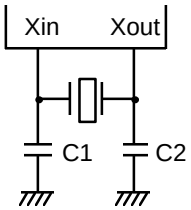
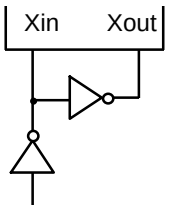
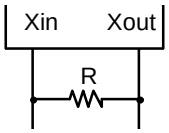
(T_A = – 40 °C to + 85 °C, V_{DD} = 1.8 V to 5.5 V)

Parameter	Symbol	Conditions		Min	Typ	Max	Units
Supply Current (1)	I_{DD1}	Run mode; V_{DD} = 5.0 V ± 10%	6.0MHz	–	3.0	8.0	mA
		Crystal oscillator; C1=C2=22pF	4.19MHz		2.3	5.5	
		V_{DD} = 3 V ± 10%	6.0MHz		1.4	4.0	
			4.19MHz		1.1	3.0	
	I_{DD2}	Idle mode; V_{DD} = 5.0 V ± 10%	6.0MHz	–	1.1	2.5	mA
		Crystal oscillator; C1=C2=22pF	4.19MHz		1.0	1.8	
		V_{DD} = 3 V ± 10%	6.0MHz		0.5	1.5	
			4.19MHz		0.4	1.0	
	I_{DD3}	Stop mode; V_{DD} = 5.0 V ± 10%		–	0.1	5.0	µA
		Stop mode; V_{DD} = 3.0 V ± 10%			0.1	3.0	

NOTES:
1. D.C. electrical values for Supply current (I_{DD1} to I_{DD3}) do not include current drawn through internal pull-up registers, output port drive currents and ADC.
2. The supply current assumes a CPU clock of fx/4.

Table 14-3. KS57C4104/C4204 System Clock Oscillator Characteristics

(T_A = – 40 °C to + 85 °C, V_{DD} = 1.8 V to 5.5 V)

Oscillator	Clock Configuration	Parameter	Test Condition	Min	Typ	Max	Units
Ceramic Oscillator		Oscillation frequency (1)	V_{DD} = 2.7 V to 5.5 V	0.4	–	6.0	MHz
			V_{DD} = 2.0 V to 5.5 V	0.4	–	4.2	
			V_{DD} = 1.8 V to 5.5 V	0.4	–	3.0	
		Stabilization time (2)	V_{DD} = 3.0 V	–	–	4	ms
Crystal Oscillator		Oscillation frequency (1)	V_{DD} = 2.7 V to 5.5 V	0.4	–	6.0	MHz
			V_{DD} = 2.0 V to 5.5 V	0.4	–	4.2	
			V_{DD} = 1.8 V to 5.5 V	0.4	–	3.0	
		Stabilization time (2)	V_{DD} = 3.0 V	–	–	10	ms
External Clock		X_{IN} input frequency (1)	V_{DD} = 2.7 V to 5.5 V	0.4	–	6.0	MHz
			V_{DD} = 2.0 V to 5.5 V	0.4	–	4.2	
			V_{DD} = 1.8 V to 5.5 V	0.4	–	3.0	
		X_{IN} input high and low level width (t_{XH}, t_{XL})	–	83.3	–	1250	ns
RC Oscillator		Oscillation frequency limitation	V_{DD} = 5 V R = 8.2 KΩ	–	4	–	MHz

NOTES:

1. Oscillation frequency and X_{in} input frequency data are for oscillator characteristics only.
2. Stabilization time is the interval required for oscillating stabilization after a power-on occurs, or when stop mode is terminated.

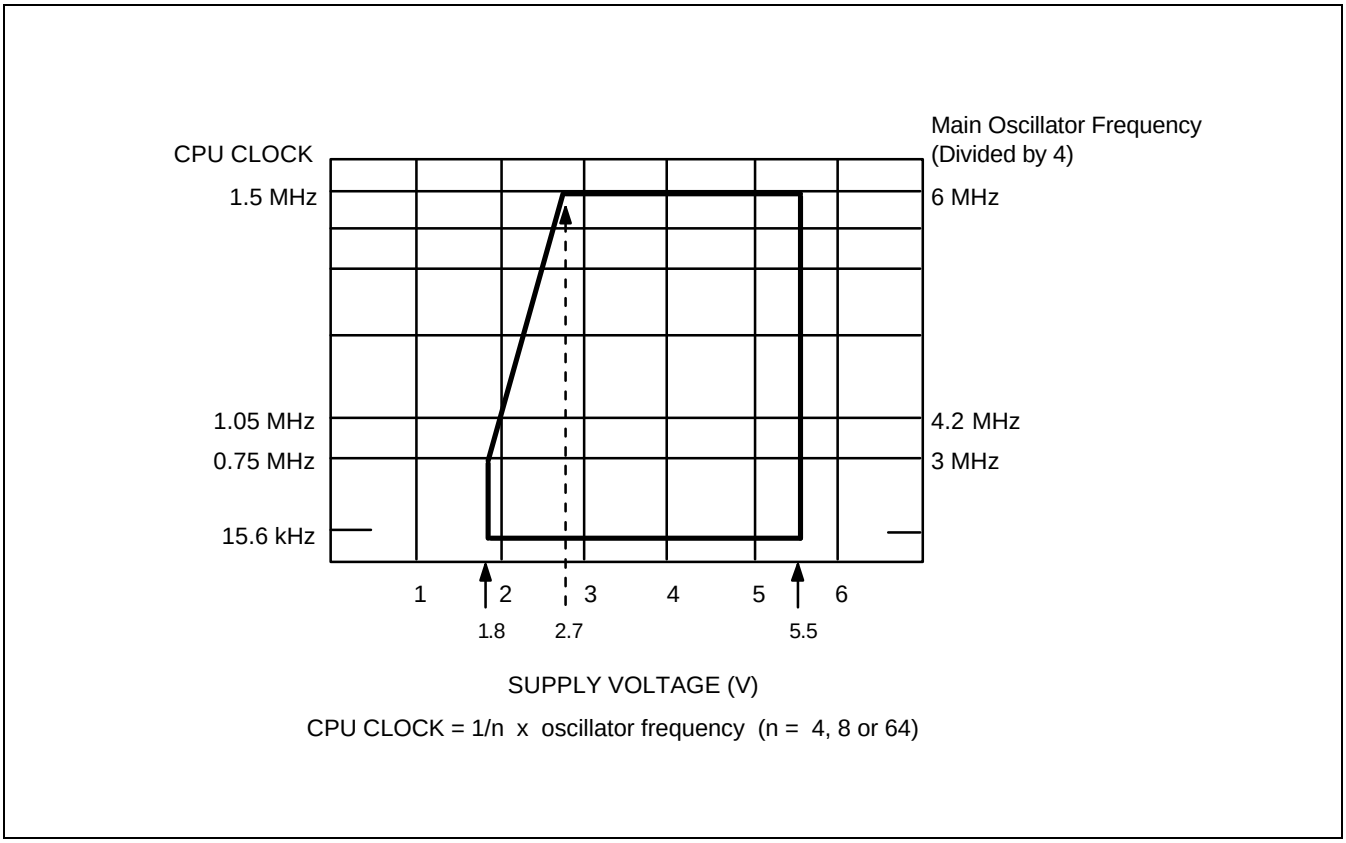


Figure 14-1. KS57C4104/C4204 Standard Operating Voltage Range

Table 14-4. KS57C4104/C4204 A.C. Electrical Characteristics

(T_A = – 40 °C to + 85 °C, V_{DD} = 1.8 V to 5.5 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Instruction Cycle Time	t_{CY}	V_{DD} = 2.7 V to 5.5 V	0.67	–	64	µs
		V_{DD} = 1.8 V to 5.5 V	1.33			
TCL0/1 Input Frequency	f_{TI}	V_{DD} = 2.7 V to 5.5 V	0	–	1.5	MHz
		V_{DD} = 1.8 V to 5.5 V			0.75	MHz
TCL0/1 Input High, Low Width	t_{TIH}, t_{TIL}	V_{DD} = 2.7 V to 5.5 V	0.48	–	–	µs
		V_{DD} = 1.8 V to 5.5 V	1.8			
SCK Cycle Time	t_{KCY}	V_{DD} = 2.7 V to 5.5 V External SCK source	800	–	–	ns
		Internal SCK source	670			
		V_{DD} = 1.8 V to 5.5 V External SCK source	3200			
		Internal SCK source	3800			

Table 14-4. KS57C4104/C4204 A.C. Electrical Characteristics (Continued)

(T_A = – 40 °C to + 85 °C, V_{DD} = 1.8 V to 5.5 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
SCK High, Low Width	t_{KH}, t_{KL}	V_{DD} = 2.7 V to 5.5 V External SCK source	335	–	–	ns
		Internal SCK source	$t_{KCY}/2 - 50$			
		V_{DD} = 1.8 V to 5.5 V External SCK source	1600			
		Internal SCK source	$t_{KCY}/2 - 150$			
SI Setup Time to SCK High	t_{SIK}	V_{DD} = 2.7 V to 5.5 V External SCK source	100	–	–	ns
		Internal SCK source	150			
		V_{DD} = 1.8 V to 5.5 V External SCK source	150			
		Internal SCK source	500			
SI Hold Time to SCK High	t_{KSI}	V_{DD} = 2.7 V to 5.5 V External SCK source	400	–	–	ns
		Internal SCK source	400			
		V_{DD} = 1.8 V to 5.5 V External SCK source	600			
		Internal SCK source	500			
Output Delay for SCK to SO	t_{KSO} (1)	V_{DD} = 2.7 V to 5.5 V External SCK source	–	–	300	ns
		Internal SCK source			250	
		V_{DD} = 1.8 V to 5.5 V External SCK source			1000	
		Internal SCK source			1000	
Interrupt Input High, Low Width	t_{INTH}, t_{INTL}	INT0	(2)	–	–	µs
		INT1, INT2, INT4, KS0–KS3	10			
RESET Input Low Width	t_{RSL}	Input	10	–	–	µs

NOTES:
1. R(1KΩ) and C (100pF) are the load resistance and load capacitance of the SO output line.
2. Minimum value for INT0 is based on a clock of $2t_{CY}$ or 128/fx as assigned by the IMOD0 register setting.

Table 14-5. KS57C4304 Absolute Maximum Ratings

(T_A = 25 °C)

Parameter	Symbol	Conditions		Rating	Units
Supply Voltage	V_{DD}	–		– 0.3 to + 6.5	V
Input Voltage	V_I	All I/O ports		– 0.3 to V_{DD} + 0.3	V
Output Voltage	V_O	–		– 0.3 to V_{DD} + 0.3	V
Output Current High	I_{OH}	One pin		– 15	mA
		All output pins		– 35	
Output Current Low	I_{OL}	One pin	peak value (note)	+ 30	mA
			rms value	+ 15	
		All pins	peak value (note)	+ 100	
			rms value	+ 60	
Operating Temperature	T_A	–		– 40 to + 85	°C
Storage Temperature	T_{stg}	–		– 65 to + 150	°C

NOTE: The values for Output Current Low (I_{OL}) are calculated as Peak Value $\times \sqrt{\text{Duty}}$.

Table 14-6. KS57C4304 D.C. Electrical Characteristics

(T_A = – 40 °C to + 85 °C, V_{DD} = 2.5 V to 5.5 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Input High Voltage	V_{IH1}	All input pins except those specified below for V_{IH2}–V_{IH3}	0.7 V_{DD}	–	V_{DD}	V
	V_{IH2}	Ports 0, 1, 3, 6 and RESET	0.8 V_{DD}		V_{DD}	
	V_{IH3}	X_{IN}, X_{OUT}	V_{DD} – 0.1		V_{DD}	
Input Low Voltage	V_{IL1}	All input pins except those specified below for V_{IL2}–V_{IL3}	–	–	0.3 V_{DD}	V
	V_{IL2}	Ports 0, 1, 3, 6 and RESET			0.2 V_{DD}	
	V_{IL3}	X_{IN}, X_{OUT}			0.1	
Output High Voltage	V_{OH}	V_{DD} = 4.5 V to 5.5 V I_{OH} = – 1 mA Ports 0, 2–8	V_{DD} – 1.0	–	–	V
Output Low Voltage	V_{OL}	V_{DD} = 3.5 V I_{OL} = 15 mA Ports 4 and 5 only	–	0.4	2	V
		I_{OL} = 4 mA All output ports except ports 4 and 5		0.2		
Input High Leakage Current	I_{LIH1}	V_I = V_{DD} All input pins except those specified below for I_{LIH2}	–	–	3	µA
	I_{LIH2}	V_I = V_{DD} X_{IN} and X_{OUT} only			20	
Input Low Leakage Current	I_{LIL1}	V_I = 0 V All input pins except X_{IN} and X_{OUT}, RESET	–	–	– 3	µA
	I_{LIL2}	V_I = 0 V X_{IN} and X_{OUT} only			– 20	
Output High Leakage Current	I_{LOH}	V_O = V_{DD} All output pins	–	–	3	µA
Output Low Leakage Current	I_{LOL}	V_O = 0 V All output pins	–	–	– 3	µA
Pull-Up Resistor	R_{L1}	V_I = 0 V; V_{DD} = 5 V except RESET	25	50	100	kΩ
		V_I = 0 V; V_{DD} = 3 V except RESET	50	100	200	
Pull-Up Resistor	R_{L2}	V_I = 0 V; V_{DD} = 5 V; RESET	100	250	400	kΩ
		V_I = 0 V; V_{DD} = 3 V; RESET	200	500	800	

Table 14-6. KS57C4304 D.C. Electrical Characteristics (Continued)

(T_A = – 40 °C to + 85 °C, V_{DD} = 2.5 V to 5.5 V)

Parameter	Symbol	Conditions		Min	Typ	Max	Units
Supply Current (1)	I_{DD1}	Run mode; V_{DD} = 5.0 V ± 10%	6.0MHz	–	3.1	8.0	mA
		Crystal oscillator; C1 = C2 = 22pF	4.19MHz		2.4	5.5	
		V_{DD} = 3 V ± 10%	6.0MHz		1.5	4.0	
			4.19MHz		1.2	3.0	
	I_{DD2}	Idle mode; V_{DD} = 5.0 V ± 10%	6.0MHz	–	1.2	2.5	mA
		Crystal oscillator; C1 = C2 = 22pF	4.19MHz		1.1	1.8	
		V_{DD} = 3 V ± 10%	6.0MHz		0.6	1.5	
			4.19MHz		0.5	1.0	
	I_{DD3}	Stop mode; V_{DD} = 5.0 V ± 10%		–	120	200	µA
		Stop mode; V_{DD} = 3.0 V ± 10%			100	150	

NOTES:
1. D.C. electrical values for Supply current (I_{DD1} to I_{DD3}) do not include current drawn through internal pull-up registers, output port drive currents and ADC.
2. The supply current assumes a CPU clock of fx/4.

Table 14-7. KS57C4304 Power-On Reset Circuit Characteristics

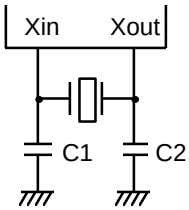
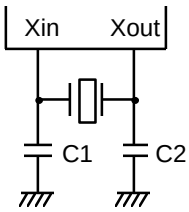
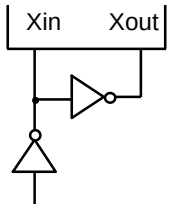
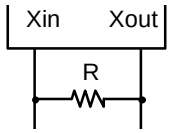
(T_A = – 40 °C to + 85 °C, V_{DD} = 2.5 V to 5.5 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Power-On Reset Voltage High	V_{DDH}		2.5		5.5	V
Power-On Reset Voltage Low	V_{DDL}		0	2.0	2.2	V
Power Supply Voltage Rise Time	t_r		10		(1)	us
Power Supply Voltage Off Time	t_{off}		0.5			s
Power-On Reset Circuit Cunsumption Current (2)	I_{DDPR}	V_{DD} = 5 V ± 10%		120	200	uA
		V_{DD} = 3 V ± 10%		100	150	uA

NOTES:
1. 2^{17}/fx (= 31.3 ms at fx = 4.19 MHz)
2. Current consumed when power-on reset circuit is provided internally.

Table 14-8. KS57C4304 System Clock Oscillator Characteristics

(T_A = – 40 °C to + 85 °C, V_{DD} = 2.5 V to 5.5 V)

Oscillator	Clock Configuration	Parameter	Test Condition	Min	Typ	Max	Units
Ceramic Oscillator		Oscillation frequency (1)	V_{DD} = 2.7 V to 5.5 V	0.4	–	6.0	MHz
			V_{DD} = 2.5 V to 5.5 V	0.4	–	4.2	
		Stabilization time (2)	V_{DD} = 3.0 V	–	–	4	ms
Crystal Oscillator		Oscillation frequency (1)	V_{DD} = 2.7 V to 5.5 V	0.4	–	6.0	MHz
			V_{DD} = 2.5 V to 5.5 V	0.4	–	4.2	
		Stabilization time (2)	V_{DD} = 3.0 V	–	–	10	ms
External Clock		X_{IN} input frequency (1)	V_{DD} = 2.7 V to 5.5 V	0.4	–	6.0	MHz
			V_{DD} = 2.5 V to 5.5 V	0.4	–	4.2	
		X_{IN} input high and low level width (t_{XH}, t_{XL})	–	83.3	–	1250	ns
RC Oscillator		Oscillation frequency limitation	V_{DD} = 5 V R = 8.2 KΩ	–	4	–	MHz

NOTES:

1. Oscillation frequency and X_{in} input frequency data are for oscillator characteristics only.
2. Stabilization time is the interval required for oscillating stabilization after a power-on occurs, or when stop mode is terminated.

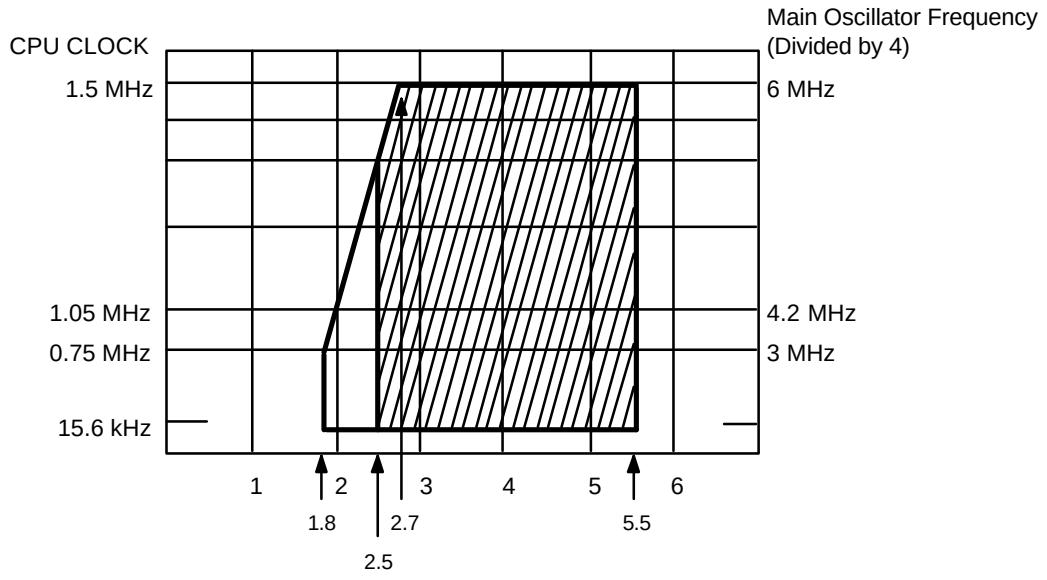


Figure 14-2. KS57C4304 Standard Operating Voltage Range

Table 14-9. KS57C4304 A.C. Electrical Characteristics

(T_A = – 40 °C to + 85 °C, V_{DD} = 2.5 V to 5.5 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Instruction Cycle Time	t_{CY}	V_{DD} = 2.7 V to 5.5 V	0.67	–	64	µs
TCL0/1 Input Frequency	f_{TI0}	V_{DD} = 2.7 V to 5.5 V	0	–	1.5	MHz
TCL0/1 Input High, Low Width	t_{TIH0}, t_{TIL0}	V_{DD} = 2.7 V to 5.5 V	0.48	–	–	µs
SCK Cycle Time	t_{KCY}	V_{DD} = 2.7 V to 5.5 V External SCK source	800	–	–	ns
		Internal SCK source	670			
SCK High, Low Width	t_{KH}, t_{KL}	V_{DD} = 2.7 V to 5.5 V External SCK source	325	–	–	ns
		Internal SCK source	$t_{KCY}/2 – 50$			
SI Setup Time to SCK High	t_{SIK}	V_{DD} = 2.7 V to 5.5 V External SCK source	100	–	–	ns
		Internal SCK source	150			
SI Hold Time to SCK High	t_{KSI}	V_{DD} = 2.7 V to 5.5 V External SCK source	400	–	–	ns
		Internal SCK source	400			
Output Delay for SCK to SO	t_{KSO}	V_{DD} = 2.7 V to 5.5 V External SCK source	–	–	300	ns
		Internal SCK source			250	
Interrupt Input High, Low Width	t_{INTH}, t_{INTL}	INT0	(NOTE)	–	–	µs
		INT1, INT2, INT4, KS0–KS3	10			
RESET Input Low Width	t_{RSL}	Input	10	–	–	µs

NOTE: Minimum value for INT0 is based on a clock of $2t_{CY}$ or 128/fx as assigned by the IMOD0 register setting.

Table 14-10. A/D Converter Electrical Characteristics

(T_A = – 10 °C to + 70 °C, V_{DD} = 3.5 V to 5.5 V, V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Condition	Min	Typ	Max	Units
Resolution	–	–	8	8	8	bit
Absolute accuracy (1)	–	2.5 V < AV_{REF} < V_{DD}	–	–	± 1.5	LSB
Conversion time (2)	t_{CON}	–	–	96/fx (3)	–	µs
Analog input voltage	V_{IAN}	–	AV_{SS}	–	AV_{REF}	V
Analog input impedance	R_{AN}	–	–	1000	–	MΩ

NOTES:
1. Absolute accuracy does not include the quantization error (± 1/2 LSB).
2. Conversion time is the time required from the moment a conversion operation starts until it ends (EOC = 0).
3. 'fx' is the abbreviation for system clock.

Table 14-11. Input/Output Capacitance

(T_A = 25 °C, V_{DD} = 0 V)

Parameter	Symbol	Condition	Min	Typ	Max	Units
Input Capacitance	C_{IN}	f = 1 MHz; Unmeasured pins are returned to V_{SS}	–	–	15	pF
Output Capacitance	C_{OUT}		–	–	15	pF
I/O Capacitance	C_{IO}		–	–	15	pF

Table 14-12. RAM Data Retention Supply Voltage in Stop Mode

(T_A = – 40 °C to + 85 °C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Data retention supply voltage	V_{DDDR}	–	1.8	–	5.5	V
Data retention supply current	I_{DDDR}	–	–	0.1	10	µA
Release signal set time	t_{SREL}	–	0	–	–	ms
Oscillation stabilization time (1)	t_{WAIT}	When released by RESET	–	2^{17}/fx	–	ms
		When released by interrupt	–	(2)	–	ms

NOTES:
1. During oscillation stabilization time, CPU operation must be stopped to avoid unstable operation upon oscillation start.
2. The basic timer causes a delay of 2^{17}/fx after a reset.

TIMING WAVEFORMS

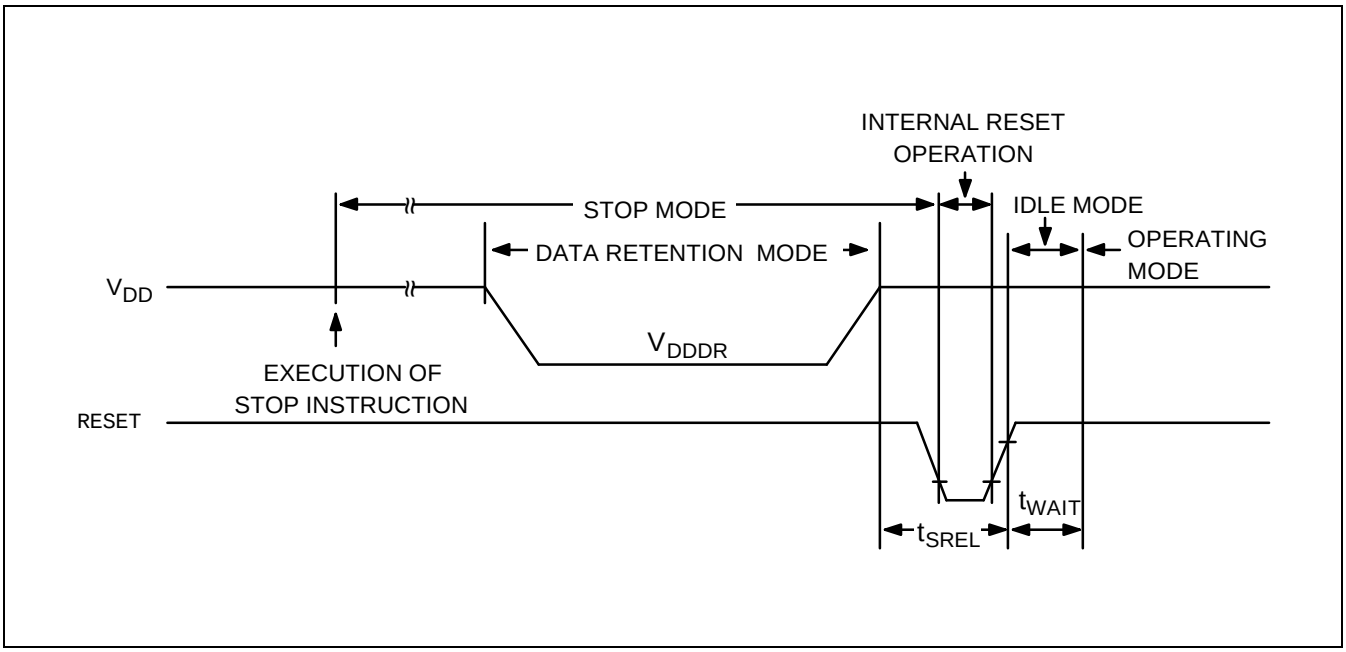


Figure 14-3. Stop Mode Release Timing When Initiated By RESET

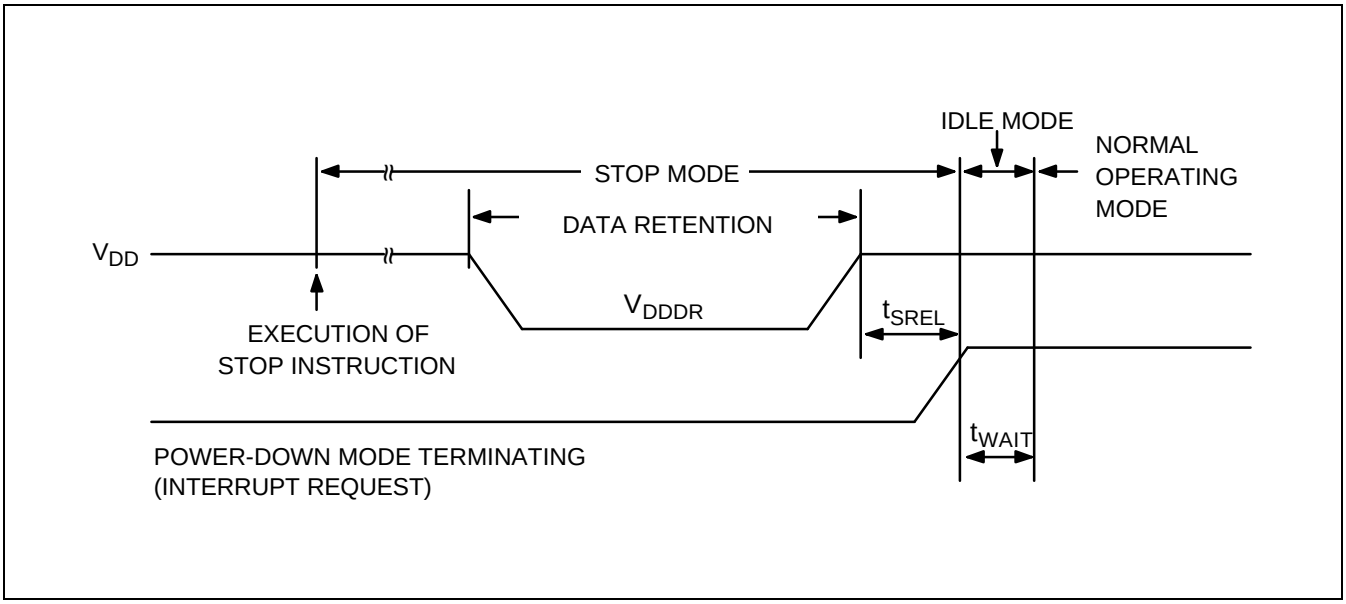


Figure 14-4. Stop Mode Release Timing When Initiated By Interrupt Request

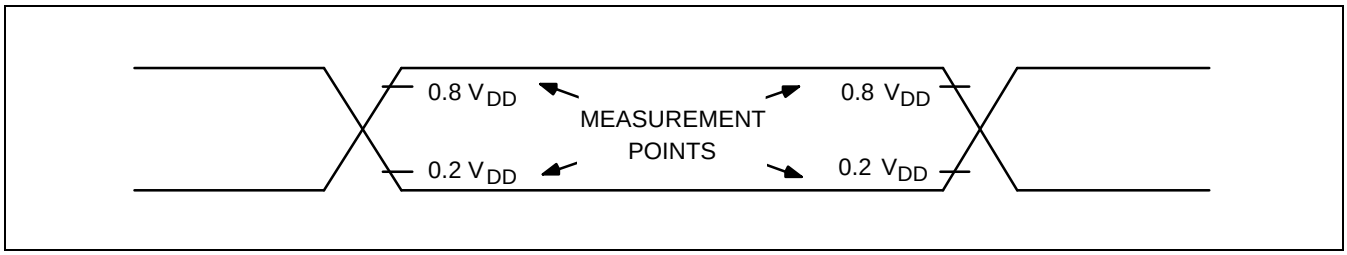


Figure 14-5. A.C. Timing Measurement Points (Except for X_{IN})

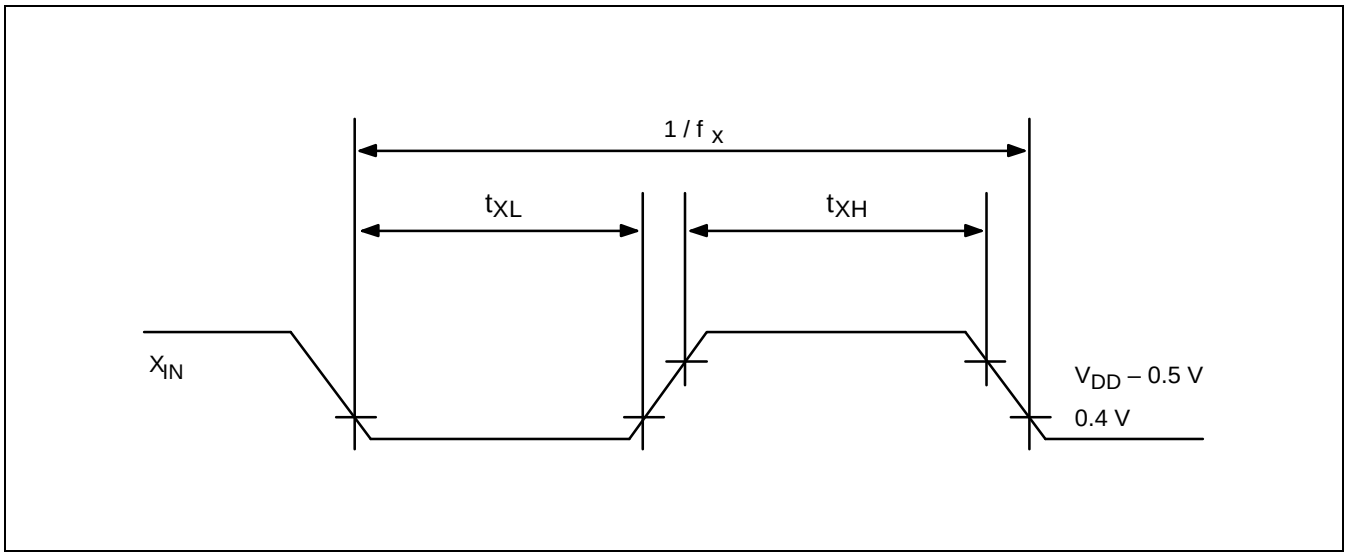


Figure 14-6. Clock Timing Measurement at X_{IN}

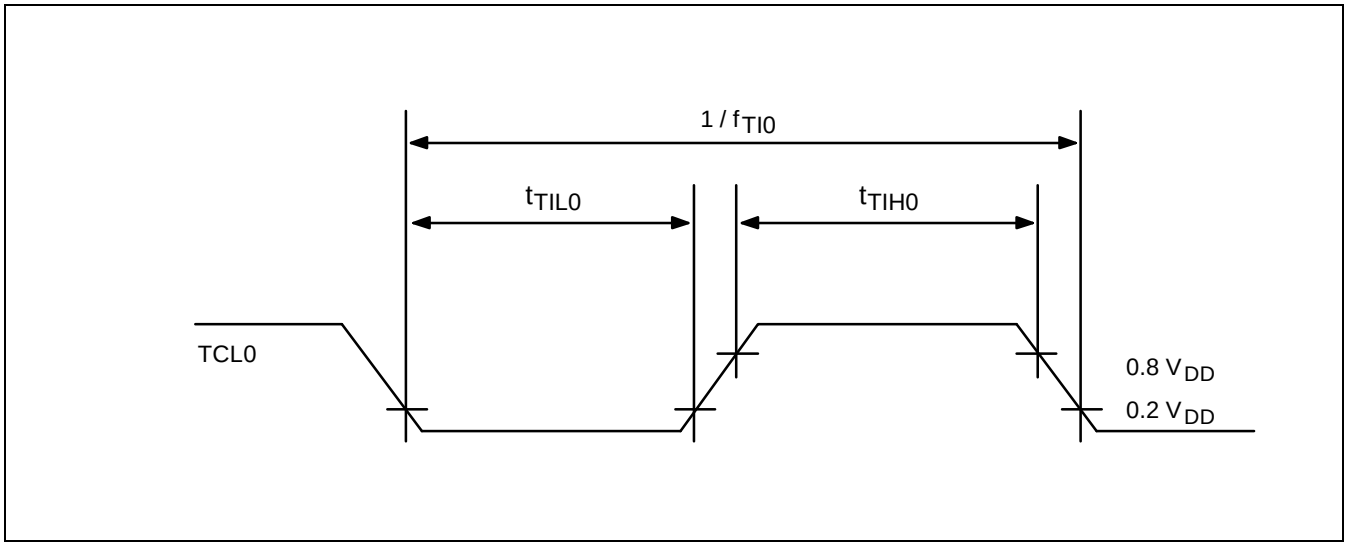


Figure 14-7. TCL0/1 Timing

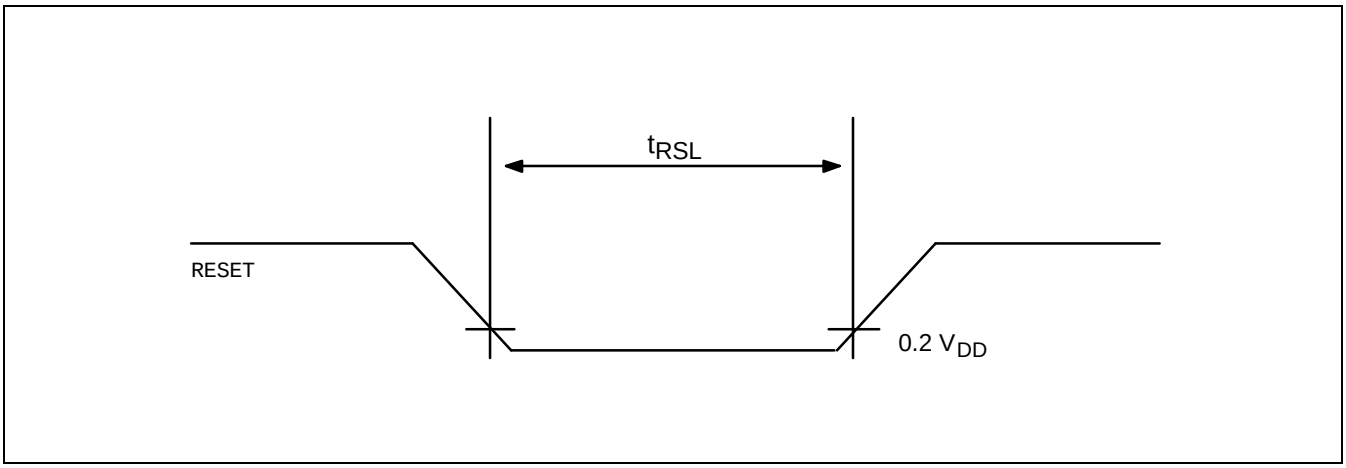


Figure 14-8. Input Timing for RESET Signal

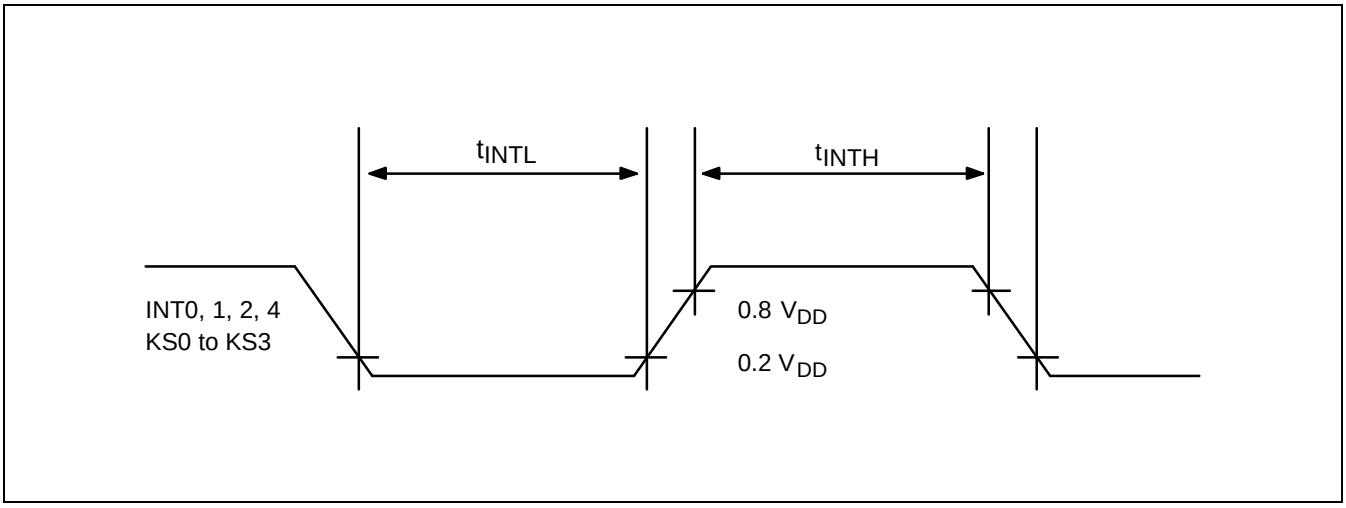


Figure 14-9. Input Timing for External Interrupts and Quasi-Interrupts

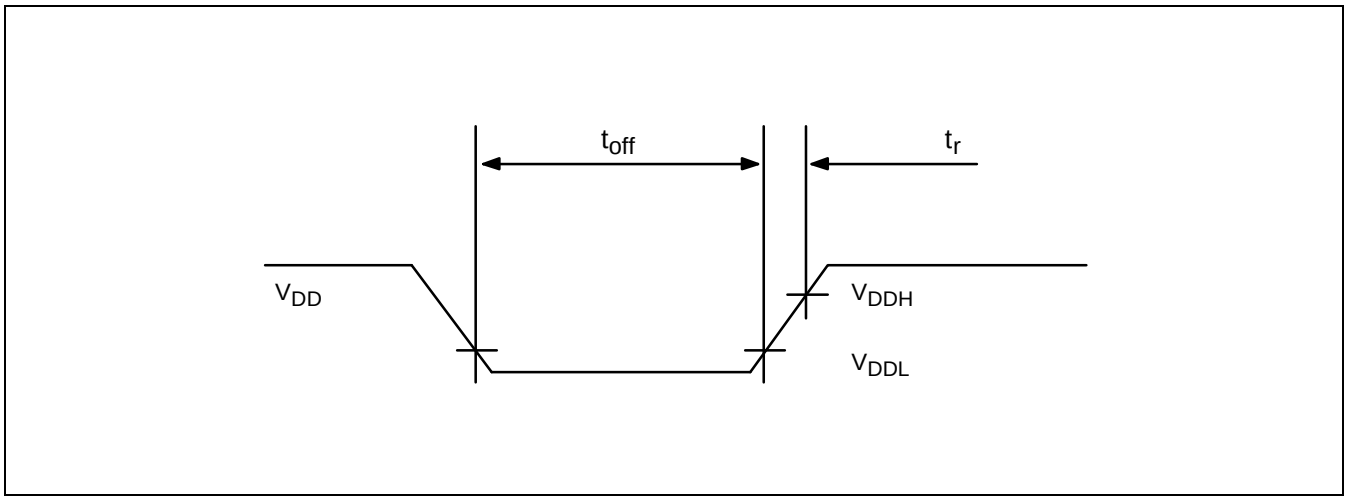


Figure 14-10. KS57C4304 Power-On RESET Timing

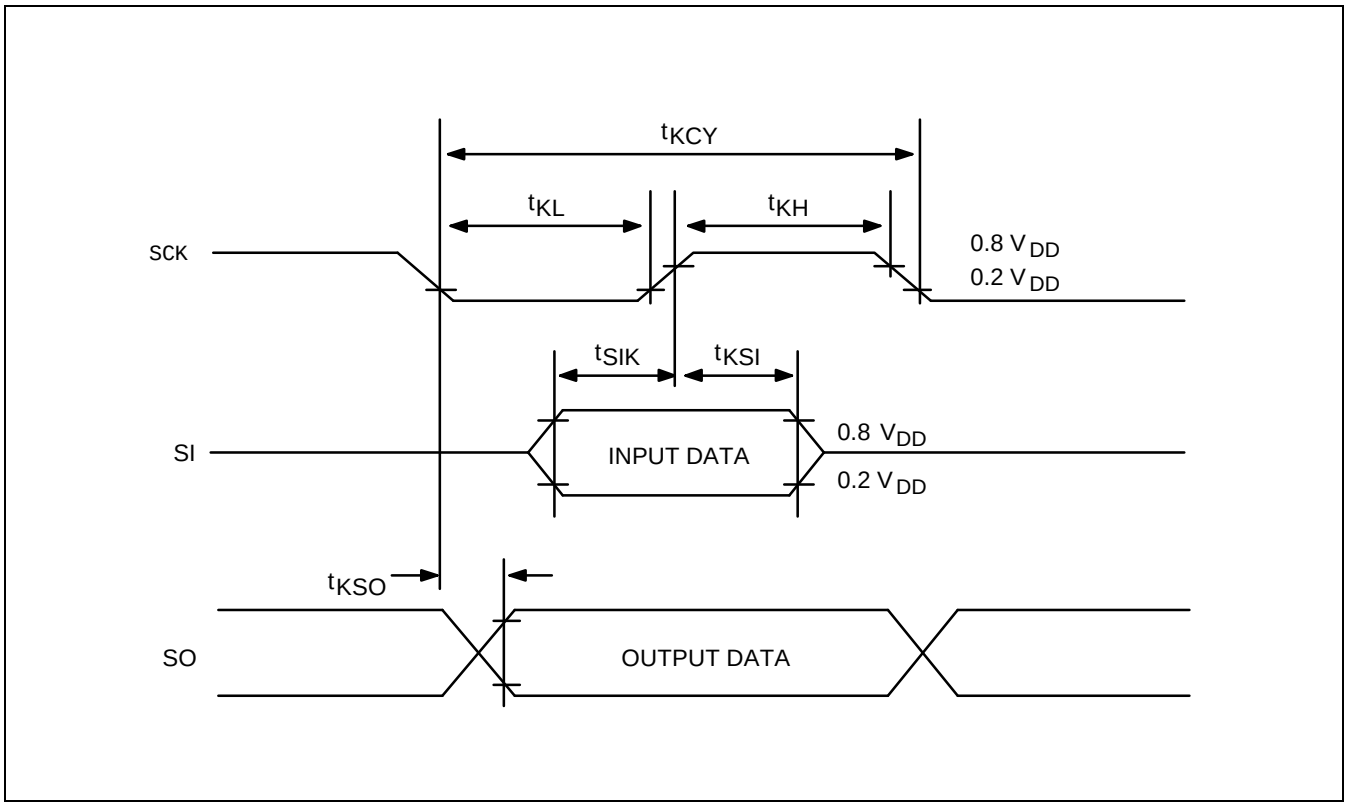


Figure 14-11. Serial Data Transfer Timing

Table 1-1. Comparision Table

Feature	KS57C4104	KS57C4204	KS57C4304
Core	SAM47	SAM47	SAM47
ROM	4 K bytes	Same	Same
RAM	256 nibbles	Same	Same
I/O	35 (4 input only)	21 (3 input only)	35 (4 input only)
POR (1)	None	None	Built in/ Typ: 2.0 V
SIO	8-bit SIO x 1	Same	Same
Timer0	8-bit timer/counter	Same	Same
Timer1(PWM)	8-bit timer/counter (8-bit PWM x 1)	Same	Same
Watchdog timer	Watch-dog 4 selectable interval	Same	Same
ADC	8-bit x 6	8-bit x 4	8-bit x 6
AV_{SS}	None (2)	Same	Same
Interrupt	External x 3 Internal x 5 Quasi x 2 (KS0–KS3)	External x 2 Internal x 5 Quasi x 1 (–)	External x 3 Internal x 5 Quasi x 2 (KS0–KS3)
Power down	Stop/Idle	Same	Same
Oscillator	Crystal, Ceramic, RC	Same	Same
Operating frequency	0.4–6 MHz	Same	Same
Operating voltage	1.8–5.5 V	1.8–5.5 V	2.5–5.5 V
OTP/MTP	OTP	Same	Same
Package	42SDIP/44QFP	30SDIP/28SOP	42SDIP/44QFP

NOTES

1. POR (power on reset)/Typ 2.0 V low voltage detector.
2. Internal A/D converter ground (bonded to V_{SS} internally)

BLOCK DIAGRAM

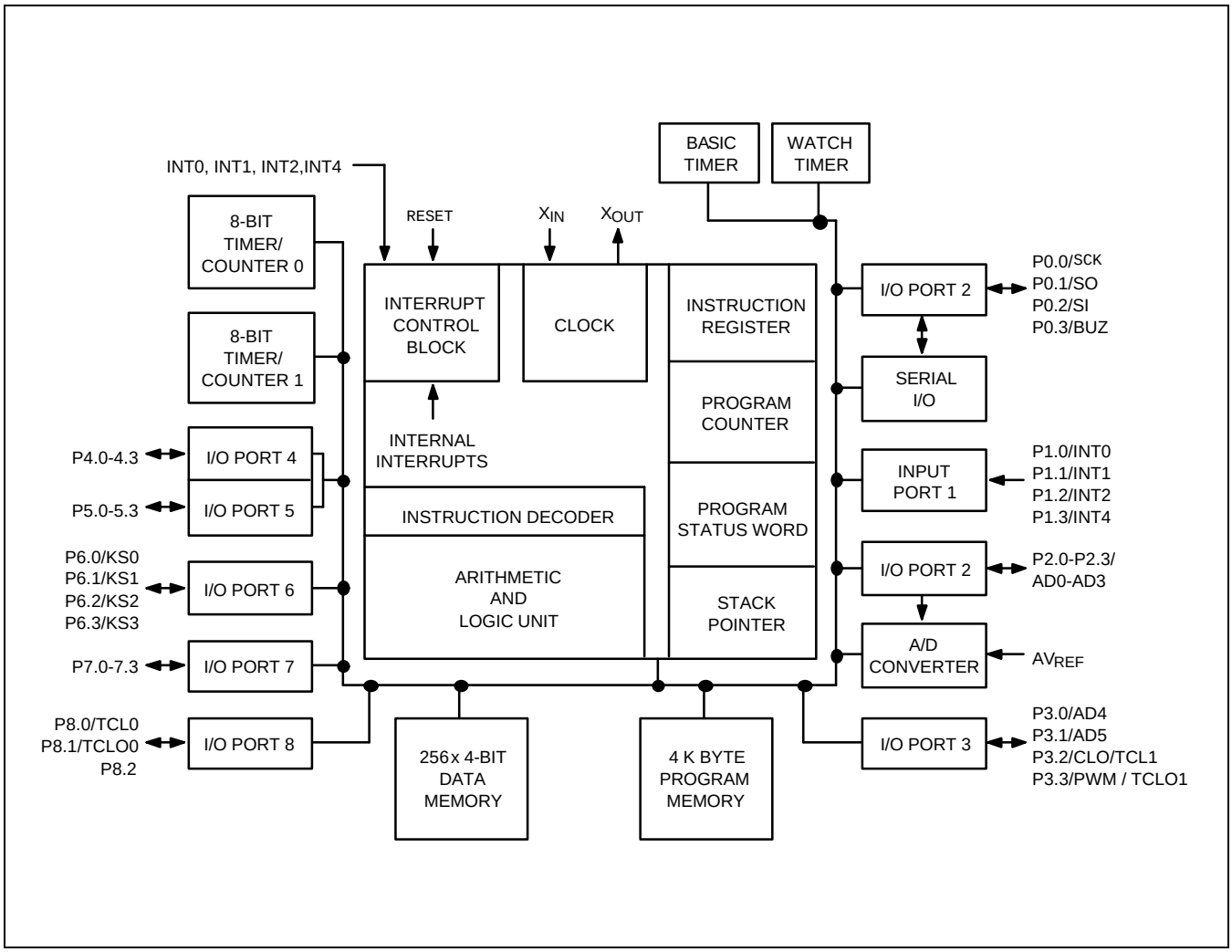


Figure 1-1. KS57C4104/C4204/C4304 Simplified Block Diagram

PIN ASSIGNMENTS

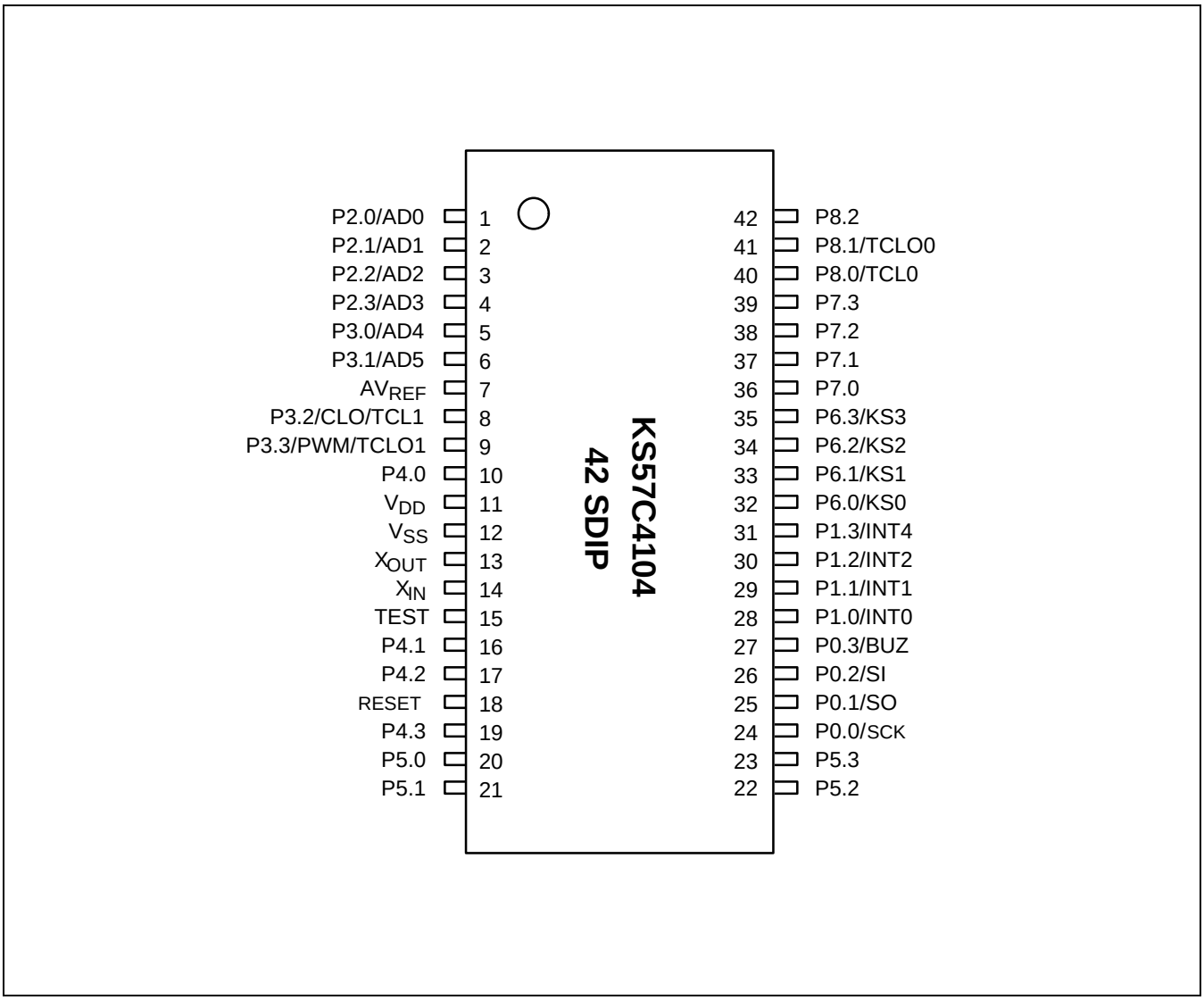


Figure 1-2. KS57C4104 Pin Assignment (42-SDIP)

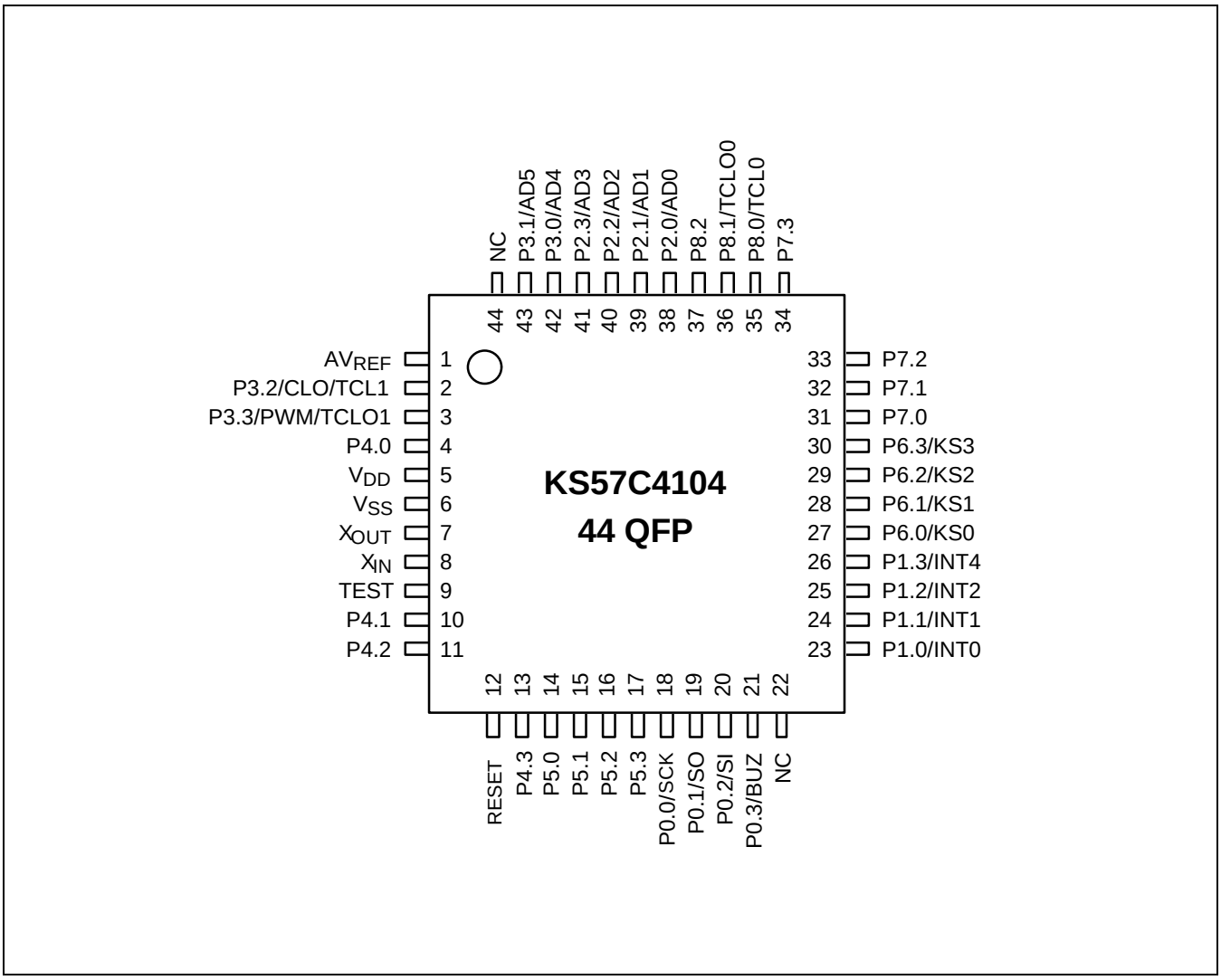


Figure 1-3. KS57C4104 Pin Assignment (44-QFP)

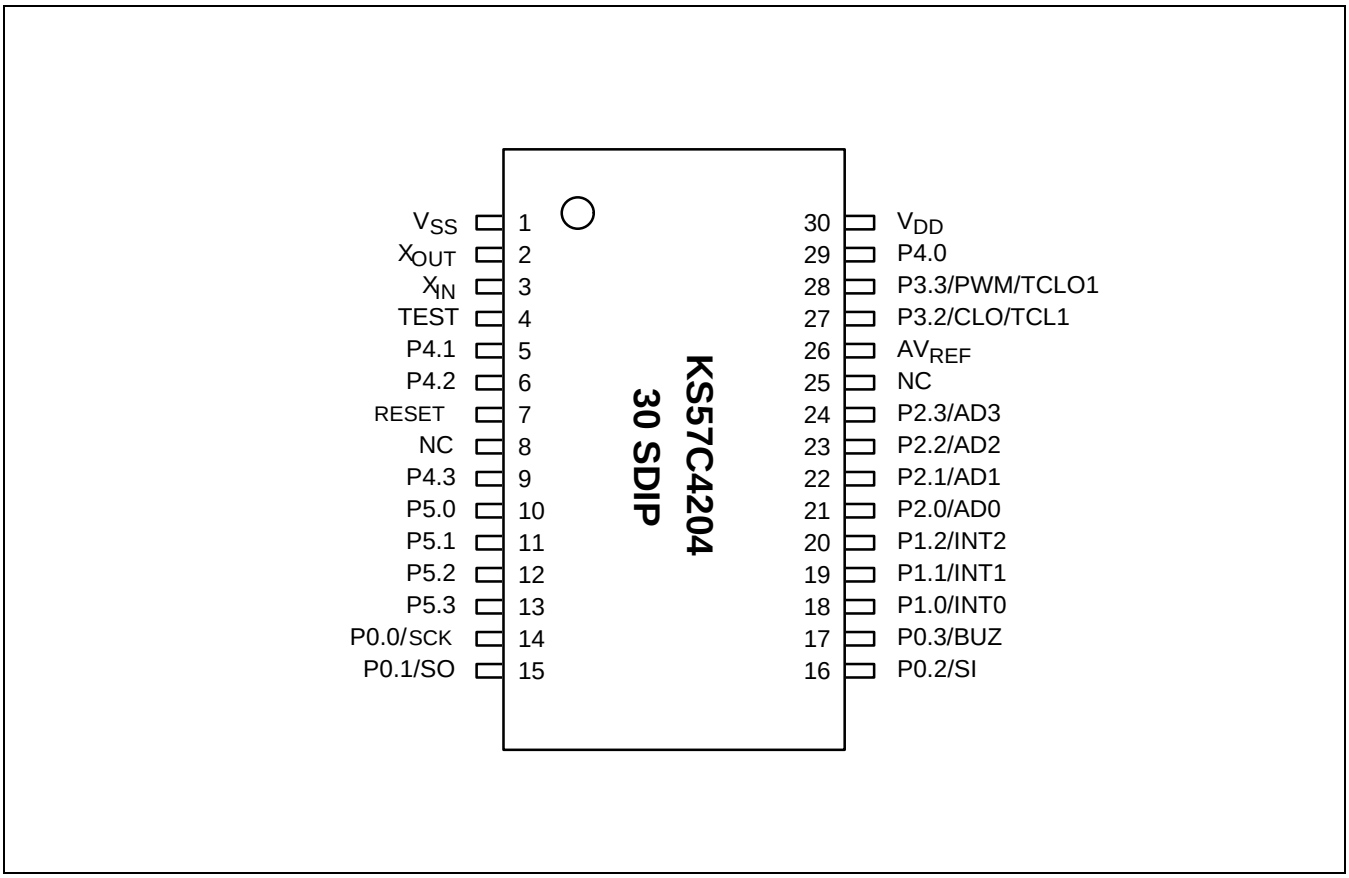


Figure 1-4. KS57C4204 Pin Assignment (30-SDIP)

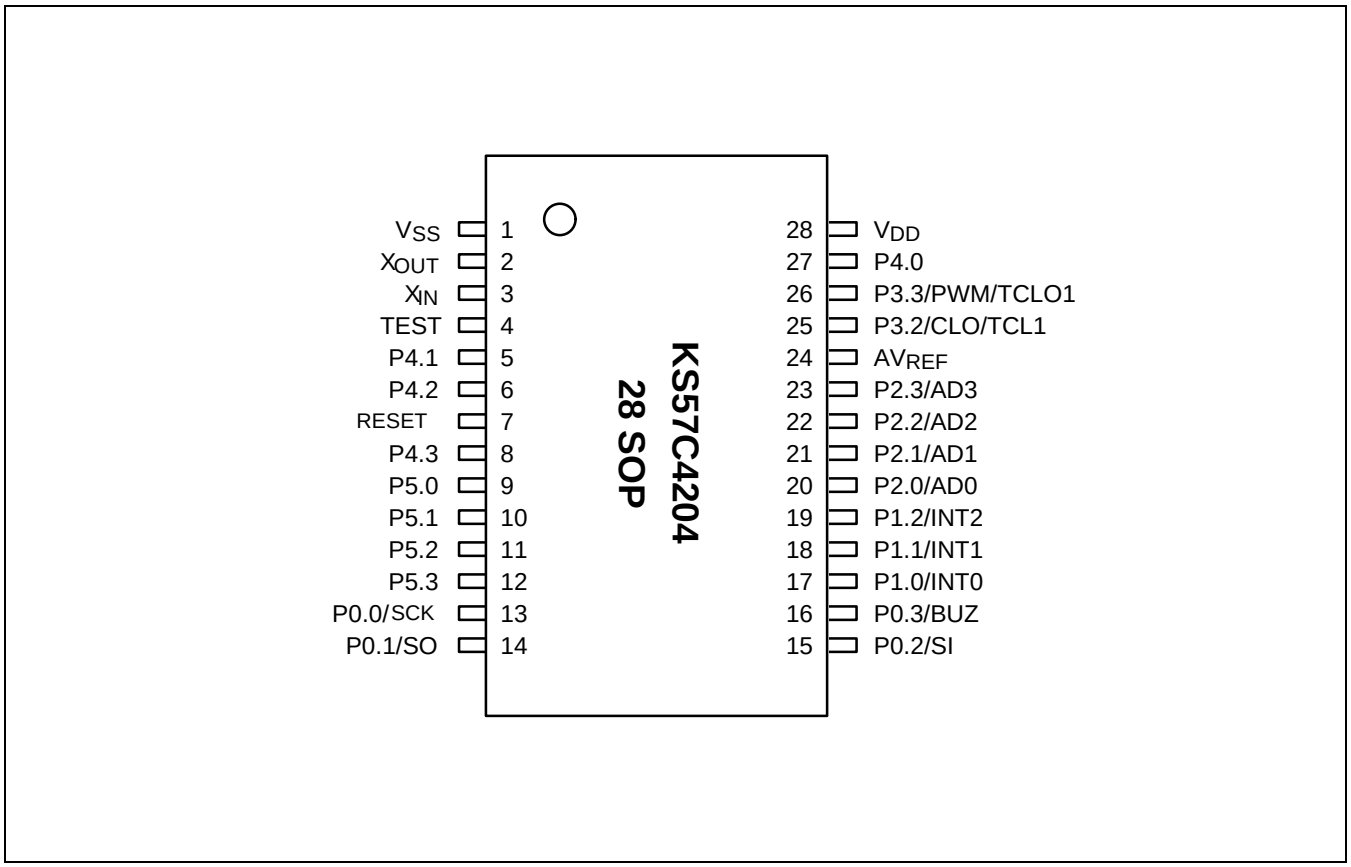


Figure 1-5. KS57C4204 Pin Assignment (28-SOP)

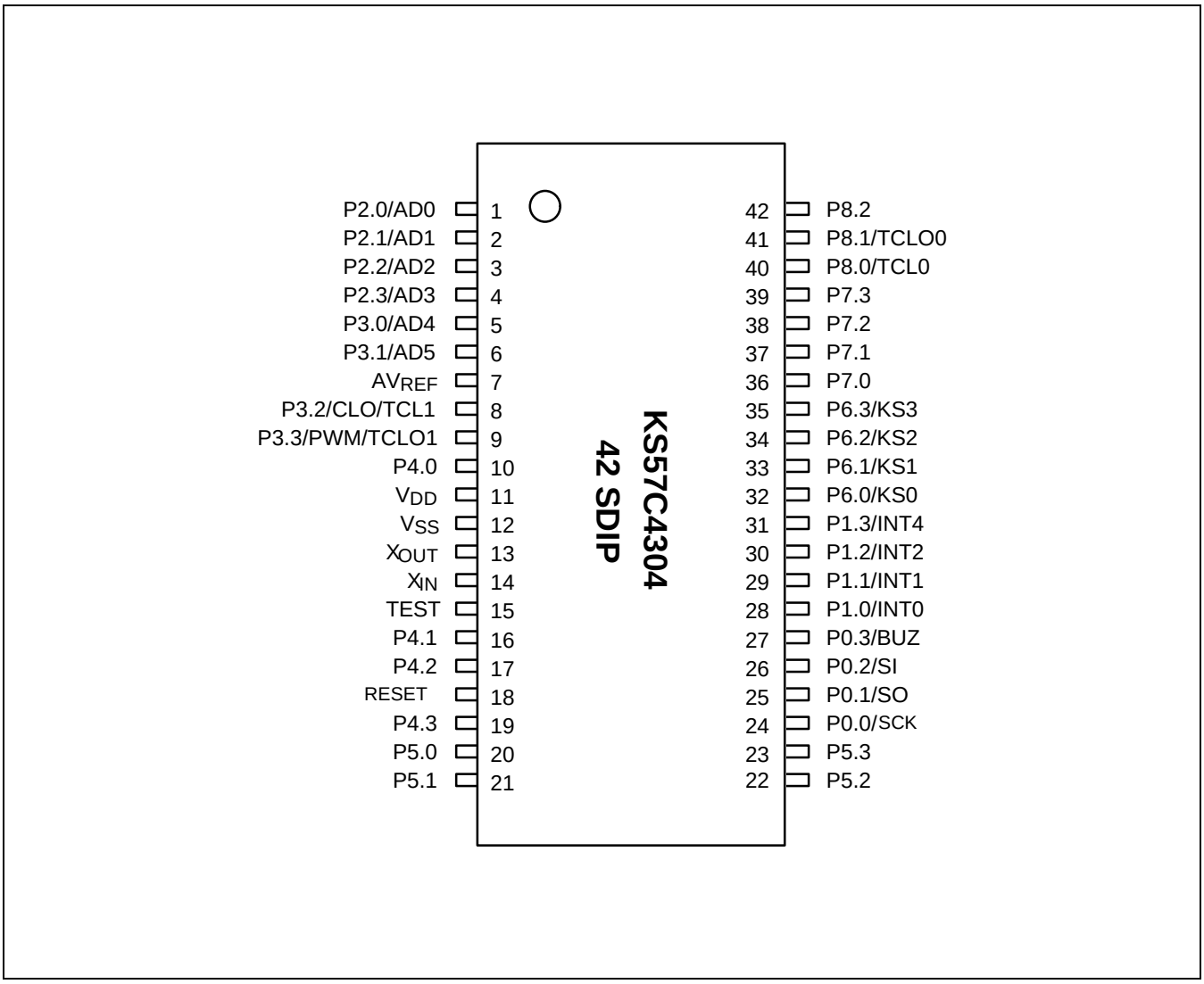


Figure 1-6. KS57C4304 Pin Assignment (42-SDIP)

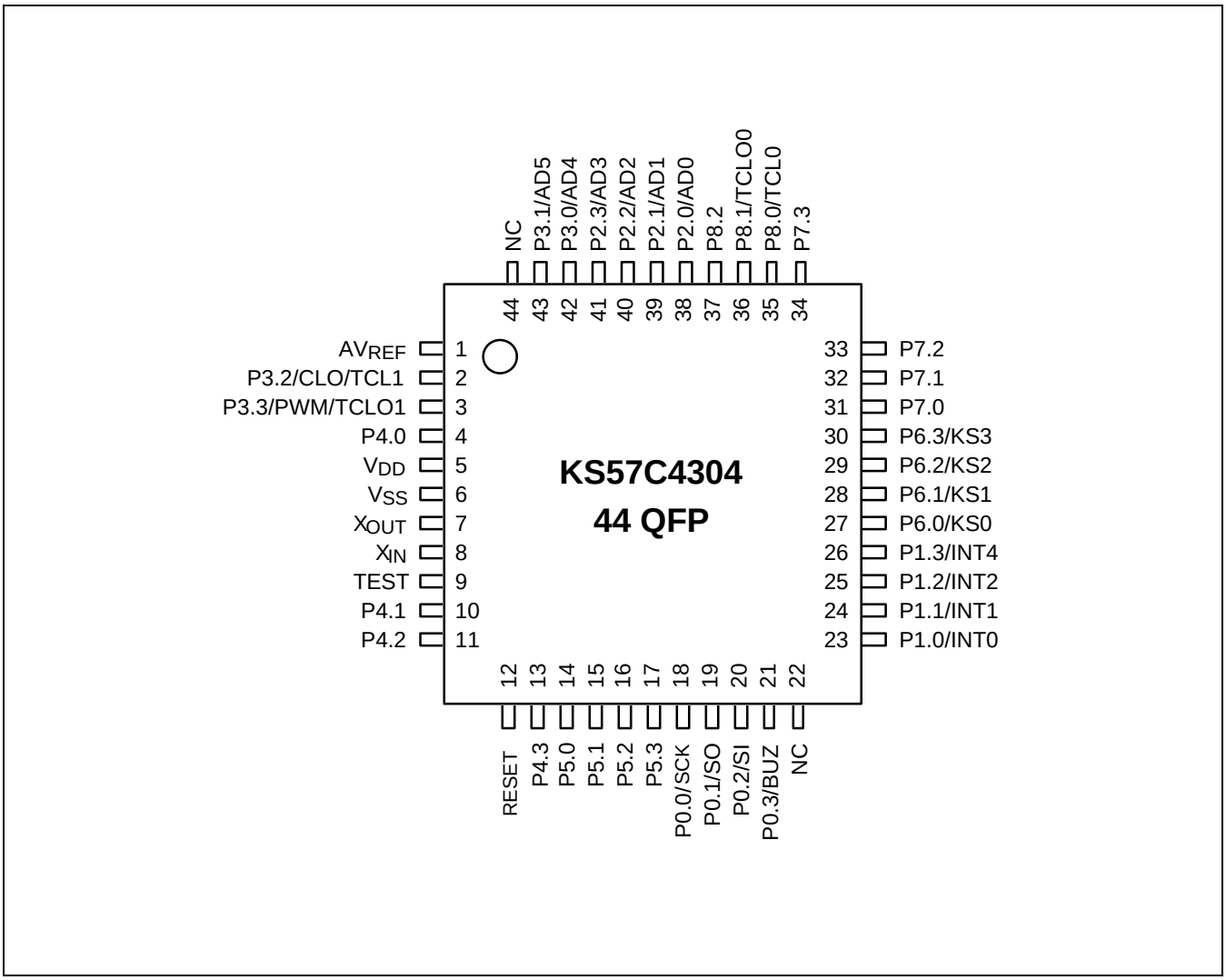


Figure 1-7. KS57C4304 Pin Assignment (44-QFP)

PIN DESCRIPTIONS

Table 1-2. KS57C4104/C4304 Pin Descriptions

Pin Name	Pin Type	Description	Number	Share Pin
P0.0 P0.1 P0.2 P0.3	I/O	4-bit I/O port. 1-bit or 4-bit read/write and test is possible. Individual pins are software configurable as input or output. 4-bit pull-up resistors are software assignable; pull-up resistors are automatically disabled for output pins.	24 (18) 25 (19) 26 (20) 27 (21)	SCK SO SI BUZ
P1.0 P1.1 P1.2 P1.3	I	4-bit input port. 1-bit and 4-bit read and test is possible. 3-bit pull-up resistors are individually assignable by software to pins P1.0, P1.1, and P1.2.	28 (23) 29 (24) 30 (25) 31 (26)	INT0 INT1 INT2 INT4
P2.0 P2.1 P2.2 P2.3	I/O	4-bit I/O port. N-channel open-drain output. 1-bit or 4-bit write and test is possible. Individual pins are software configurable as AD input or output. 4-bit pull-up resistors are software assignable; pull-up resistors are automatically disabled for output pins.	1 (38) 2 (39) 3 (40) 4 (41)	AD0 AD1 AD2 AD3
P3.0 P3.1 P3.2 P3.3	I/O	Same as Port 0 (P0.0–P0.3)	5 (42) 6 (43) 8 (2) 9 (3)	AD4 AD5 CLO/TCL1 PWM/TCLO1
P4.0 P4.1 P4.2 P4.3 P5.0–P5.3	I/O	4-bit I/O ports. Ports 4 and 5 can be configured individually as n-channel open-drain or as CMOS push-pull output by software. 1-bit and 4-bit read/write and test is possible. Ports 4 and 5 can be paired to enable 8-bit data transfer. 4-bit pull-up resistors are software assignable; pull-up resistors are automatically disabled for output pins.	10 (4) 16 (10) 17 (11) 19 (13) 20–23 (14–17)	–
P6.0–P6.3 P7.0–P7.3 P8.0 P8.1 P8.2	I/O	Same as Port 0 except port 8 is a 3-bit I/O port	32–35 (27–30) 36–39 (31–34) 40 (35) 41 (36) 42 (37)	KS0–KS3 – TCL0 TCLO0 –

Table 1-2. KS57C4104/C4304 Pin Descriptions (Continued)

Pin Name	Pin Type	Description	Number	Share Pin
SCK	I/O	Serial I/O interface clock signal	24 (18)	P0.0
SO	I/O	Serial data output	25 (19)	P0.1
SI	I/O	Serial data input	26 (20)	P0.2
BUZ	I/O	2 kHz, 4kHz, 8kHz, or 16 kHz frequency output at the watch timer clock frequency of 32.768 kHz	27 (21)	P0.3
INT0, INT1	I	External interrupts. The triggering edge for INT0 and INT1 is selectable. Only INT0 is synchronized with the system clock.	28–29 (23–24)	P1.0, P1.1
INT2	I	Quasi-interrupt input with rising edge detection	30 (25)	P1.2
INT4	I	External interrupts with detection of rising and falling edges	31 (26)	P1.3
AD0–AD3 AD4–AD5	I/O	A/D converter analog inputs	1–4 (38–41) 5–6 (42–43)	P2.0–P2.3 P3.0–P3.1
TCL0	I/O	External clock input for timer/counter0	40 (35)	P8.0
TCLO0	I/O	Timer/counter clock output	41 (36)	P8.1
CLO	I/O	Clock output	8 (2)	P3.2
TCL1	I/O	External clock input for timer/counter1	8 (2)	P3.2
PWM	I/O	PWM output	9 (3)	P3.3
TCLO1	I/O	Timer/counter clock output1	9 (3)	P3.3
KS0–KS3	I/O	Quasi-interrupt input with falling edge detection	32–35 (27–30)	P6.0–P6.3
V_{DD}	–	Main power supply	11 (5)	–
V_{SS}	–	Ground	12 (6)	–
RESET	I	Reset signal	18 (12)	–
X_{IN}, X_{out}	–	Crystal, ceramic, or RC oscillator signal for system clock.	14, 13 (8, 7)	–
AV_{REF}	–	A/D converter analog reference voltage	7 (1)	–
TEST	I	Test signal input (must be connected to V_{SS})	15 (9)	–
NC	–	No connection (no bonding pin)	(22, 44)	–

NOTE: Parentheses indicate 44-QFP pin number.

Table 1-3. KS57C4204 Pin Descriptions

Pin Name	Pin Type	Description	Number	Share Pin
P0.0 P0.1 P0.2 P0.3	I/O	4-bit I/O port. 1-bit or 4-bit read/write and test is possible. Individual pins are software configurable as input or output. 4-bit pull-up resistors are software assignable; pull-up resistors are automatically disabled for output pins.	14 (13) 15 (14) 16 (15) 17 (16)	SCK SO SI BUZ
P1.0 P1.1 P1.2	I	4-bit input port. 1-bit and 4-bit read and test is possible. 3-bit pull-up resistors are individually assignable by software to pins P1.0, P1.1, and P1.2.	18 (17) 19 (18) 20 (19)	INT0 INT1 INT2
P2.0 P2.1 P2.2 P2.3	I/O	4-bit I/O port. N-channel open-drain output. 1-bit or 4-bit write and test is possible. Individual pins are software configurable as AD input or output. 4-bit pull-up resistors are software assignable; pull-up resistors are automatically disabled for output pins.	21 (20) 22 (21) 23 (22) 24 (23)	AD0 AD1 AD2 AD3
P3.2 P3.3	I/O	Same as Port 0 (P0.0–P0.3)	27 (25) 28 (26)	CLO/TCL1 PWM/TCLO1
P4.0 P4.1 P4.2 P4.3 P5.0–P5.3	I/O	4-bit I/O ports. Ports 4 and 5 can be configured individually as n-channel open-drain or as CMOS push-pull output by software. 1-bit and 4-bit read/write and test is possible. Ports 4 and 5 can be paired to enable 8-bit data transfer. 4-bit pull-up resistors are software assignable; pull-up resistors are automatically disabled for output pins.	29 (27) 5 (5) 6 (6) 9 (8) 10–13 (9–12)	–

Table 1-3. KS57C4204 Pin Descriptions (Continued)

Pin Name	Pin Type	Description	Number	Share Pin
SCK	I/O	Serial I/O interface clock signal	14 (13)	P0.0
SO	I/O	Serial data output	15 (14)	P0.1
SI	I/O	Serial data input	16 (15)	P0.2
BUZ	I/O	2 kHz, 4kHz, 8kHz, or 16 kHz frequency output at the watch timer clock frequency of 32.768 kHz	17 (16)	P0.3
INT0, INT1	I	External interrupts. The triggering edge for INT0 and INT1 is selectable. Only INT0 is synchronized with the system clock.	18, 19 (17, 18)	P1.0, P1.1
INT2	I	Quasi-interrupt input with rising edge detection	20 (19)	P1.2
AD0–AD3	I/O	A/D converter analog inputs	21–24 (20–23)	P2.0–P2.3
CLO	I/O	Clock output	27 (25)	P3.2
TCL1	I/O	External clock input for timer/counter1	27 (25)	P3.2
PWM	I/O	PWM output	28 (26)	P3.3
TCLO1	I/O	Timer/counter clock output1	28 (26)	P3.3
V_{DD}	–	Main power supply	30 (28)	–
V_{SS}	–	Ground	1 (1)	–
RESET	I	Reset signal	7 (7)	–
X_{IN}, X_{OUT}	–	Crystal, ceramic, or RC oscillator signal for system clock.	3, 2 (3, 2)	–
AV_{REF}	–	Internal A/D converter analog reference voltage	26 (24)	–
TEST	I	Test signal input (must be connected to $V_{SS)}$	4 (4)	–
NC	–	No connection (no bonding pin)	8, 25	–

NOTE: Parentheses indicate 28-SOP pin number.

Table 1-4. Overview of KS57C4104/C4204/C4304 Pin Data

Pin Names	Share Pins	I/O Type	Reset Value	Circuit Type
P0.0–P0.3	SCK, SO, SI, BUZ	I/O	Input	Type D
P1.0 P1.1 P1.2	INT0 (note) INT1 (note) INT2 (note)	I	Input	Type A-1
P1.3	INT4	I	Input	Type A
P2.0–P2.3	AD0–AD3	I/O	AD input	Type F-3
P3.0 P3.1 P3.2 P3.3	AD4 AD5 CLO/TCL1 TCLO1/PWM	I/O	Input	Type F Type F Type D Type D
P4.0–P4.3 P5.0–P5.3	–	I/O	Input	Type E
P6.0 P6.1 P6.2 P6.3	KS0 (note) KS1 (note) KS2 (note) KS3 (note)	I/O	Input	Type D
P7.0–P7.3	–	I/O	Input	Type D
P8.0 P8.1 P8.2	TCL0 (note) TCLO0 –	I/O	Input	Type D
V_{DD}, V_{SS}	–	–	–	–
X_{IN}, X_{OUT}	–	–	–	–
RESET	–	I	–	Type B-2 (note)
AV_{REF}	–	–	–	–
TEST	–	I	–	–
NC	–	–	–	–

NOTE: A noise filter circuit is built-in.

PIN CIRCUIT DIAGRAMS

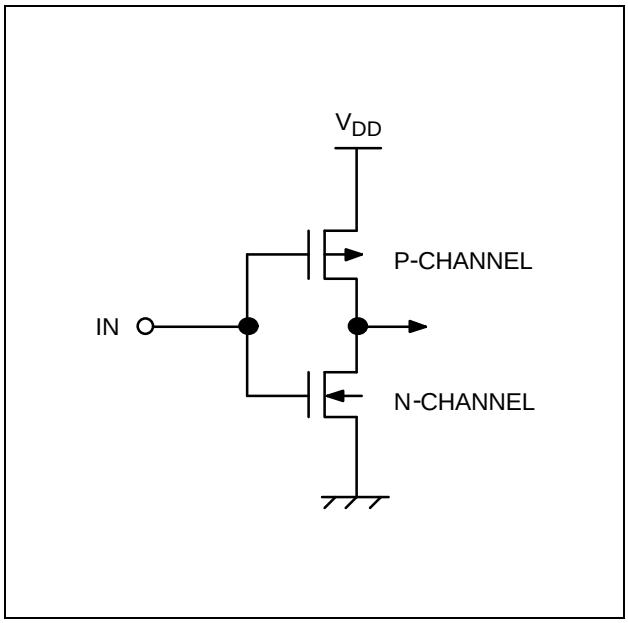


Figure 1-8. Pin Circuit Type A

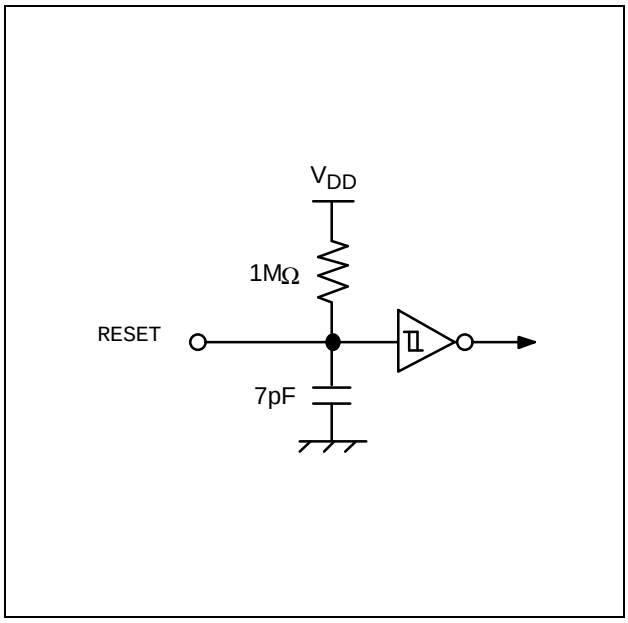


Figure 1-10. Pin Circuit Type B-2

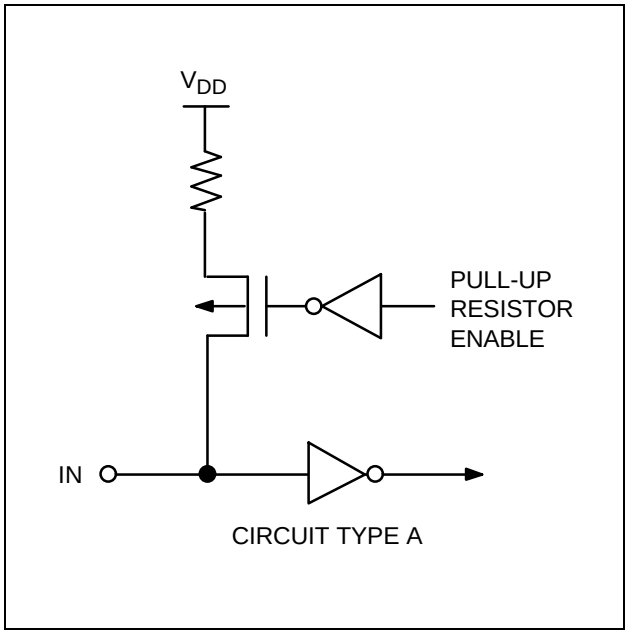


Figure 1-9. Pin Circuit Type A-1

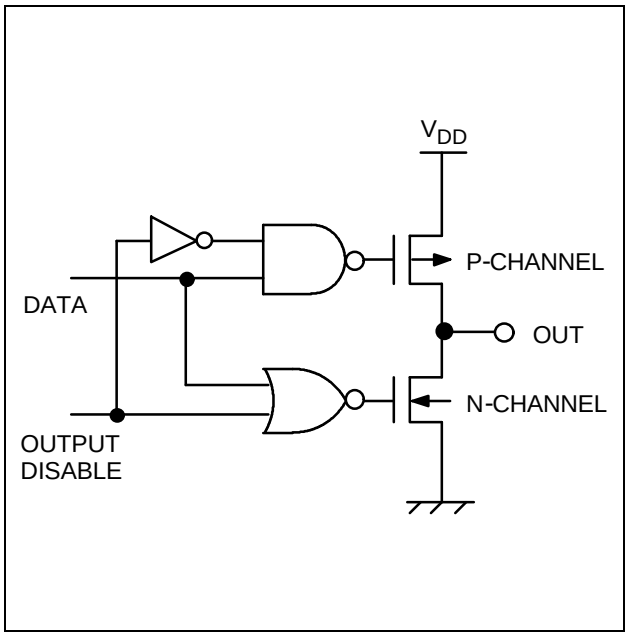


Figure 1-11. Pin Circuit Type C

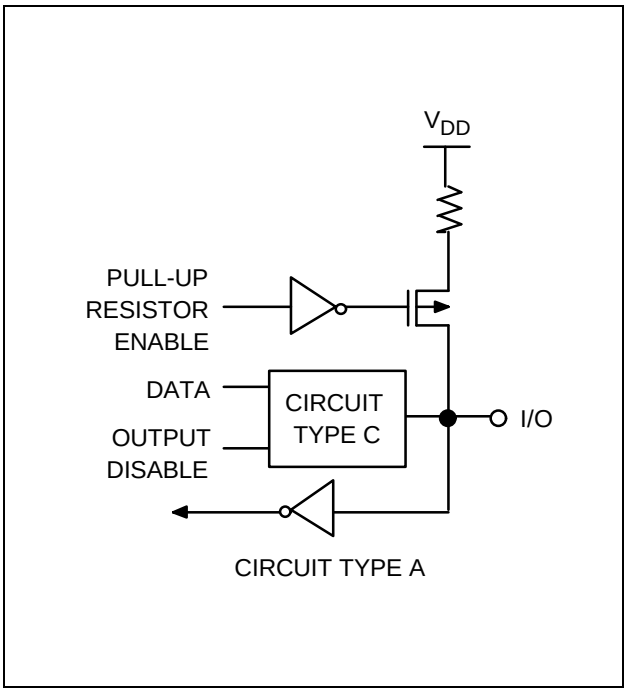


Figure 1-12. Pin Circuit Type D

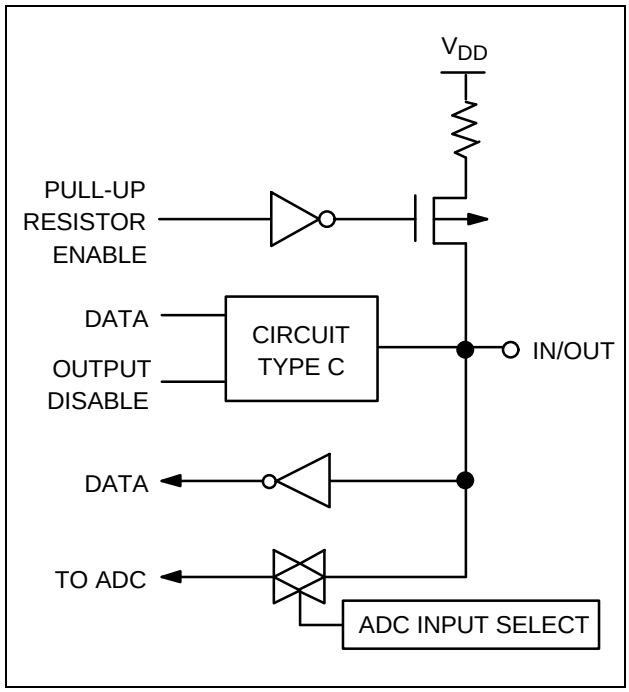


Figure 1-14. Pin Circuit Type F

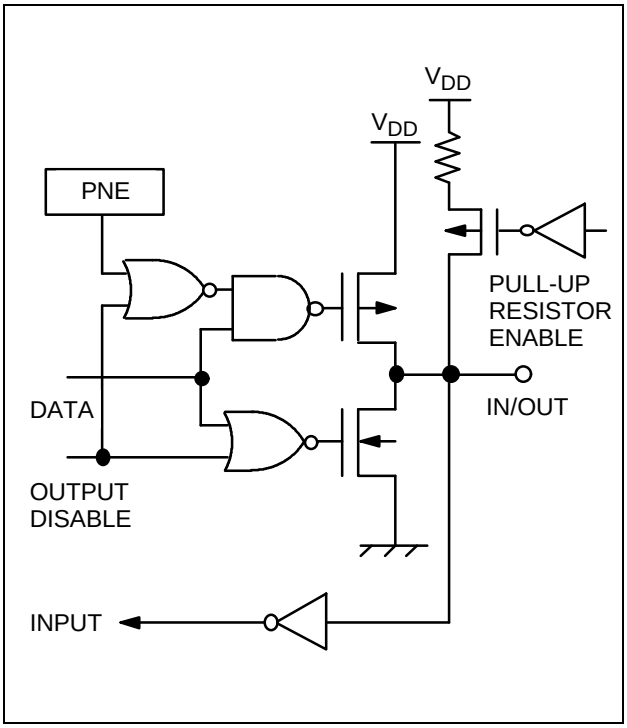


Figure 1-13. Pin Circuit Type E

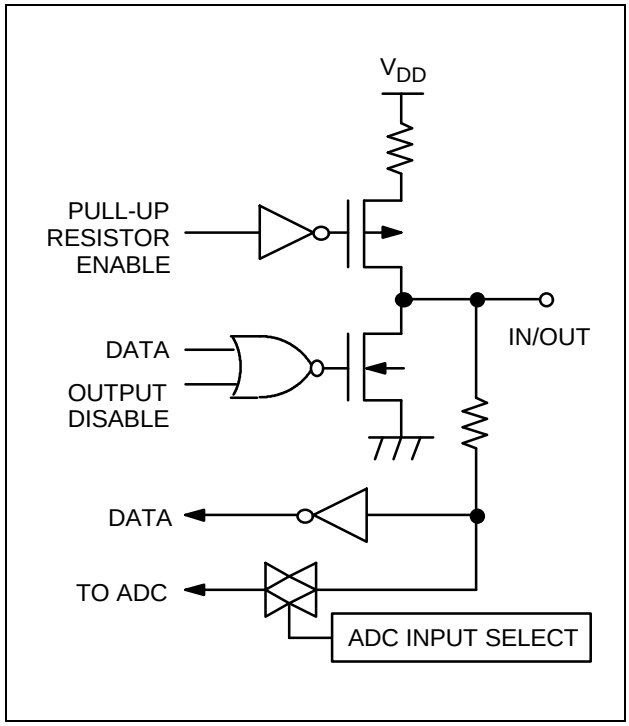


Figure 1-15. Pin Circuit Type F-3

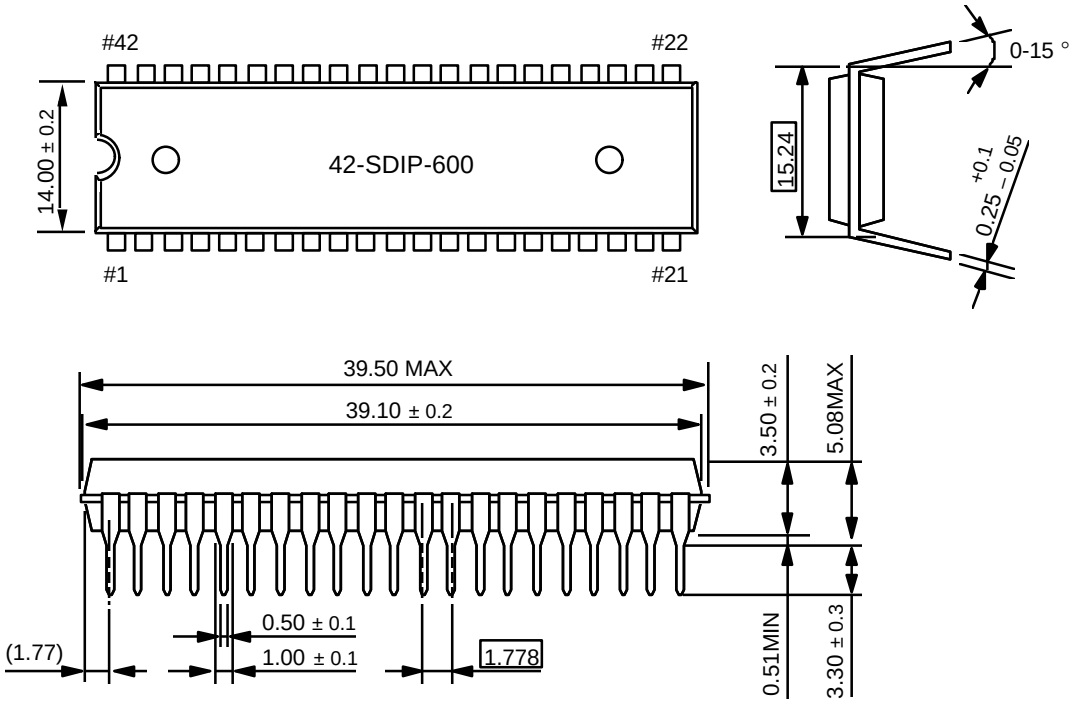
NOTES

15 MECHANICAL DATA

This section contains the following information about the device package:

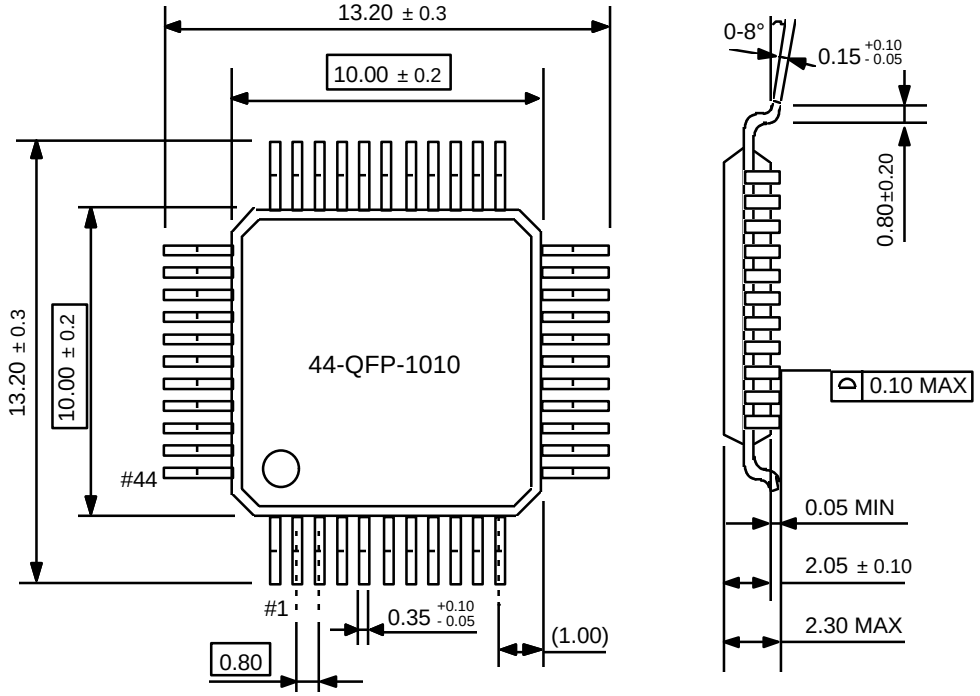
— Package dimensions in millimeters

— Pad diagram



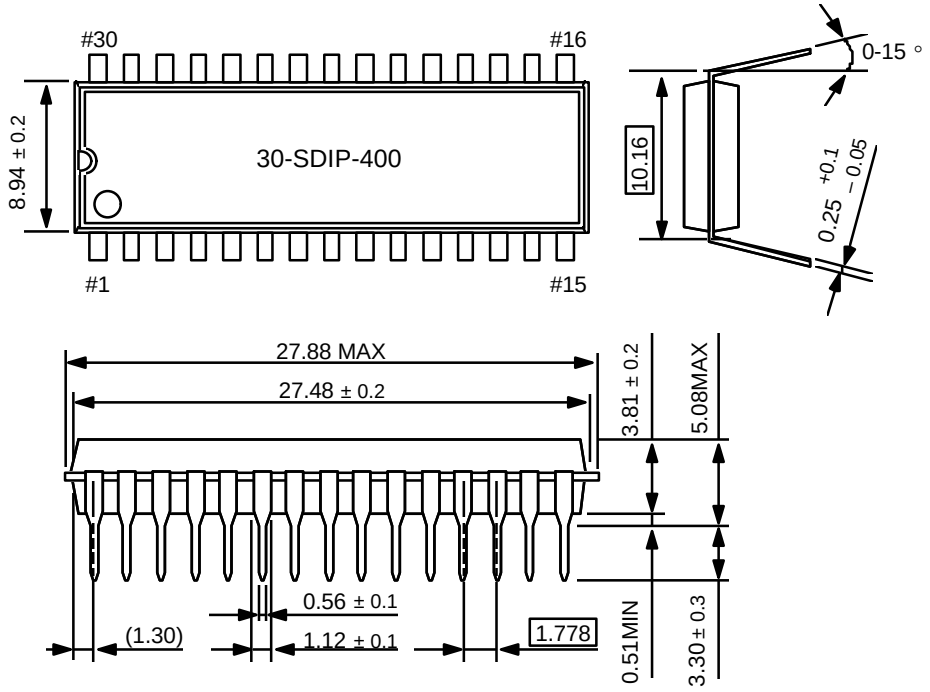
NOTE: Dimensions are in millimeters.

Figure 15-1. 42-SDIP-600 Package Dimensions



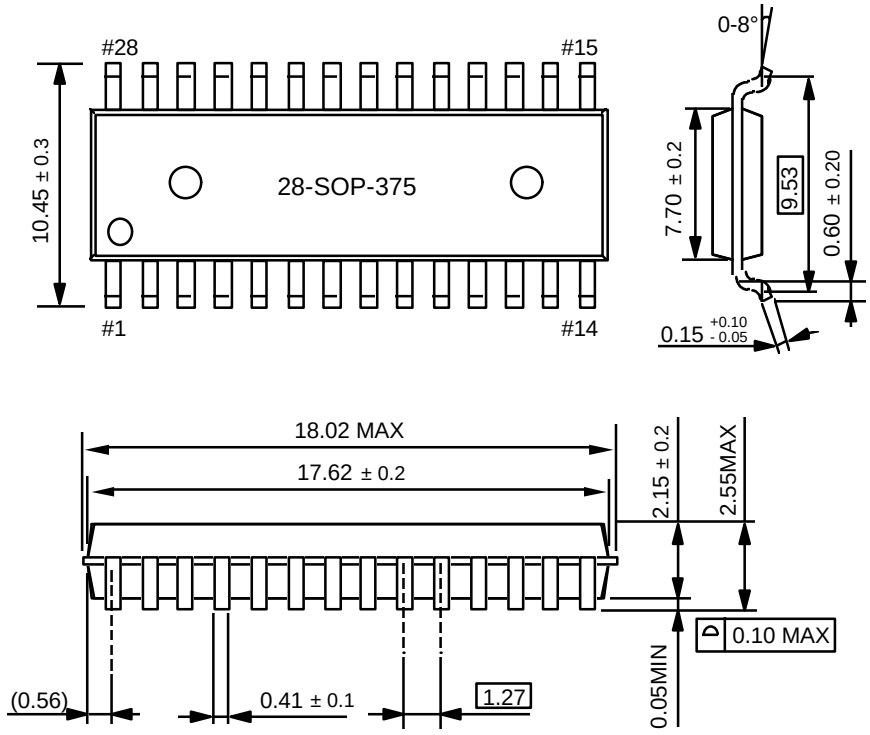
NOTE: Dimensions are in millimeters.

Figure 15-2. 44-QFP-1010 Package Dimensions



NOTE: Dimensions are in millimeters.

Figure 15-3. 30-SDIP-400 Package Dimensions



NOTE: Dimensions are in millimeters.

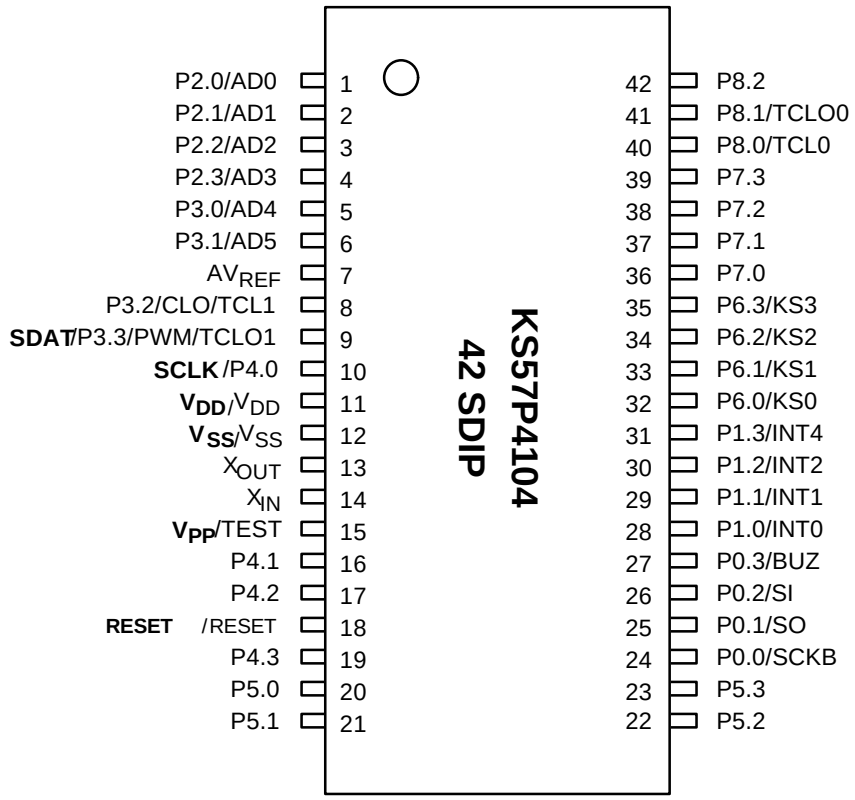
Figure 15-4. 28-SOP-375 Package Dimensions

16 KS57P4104/P4204/P4304 OTP

OVERVIEW

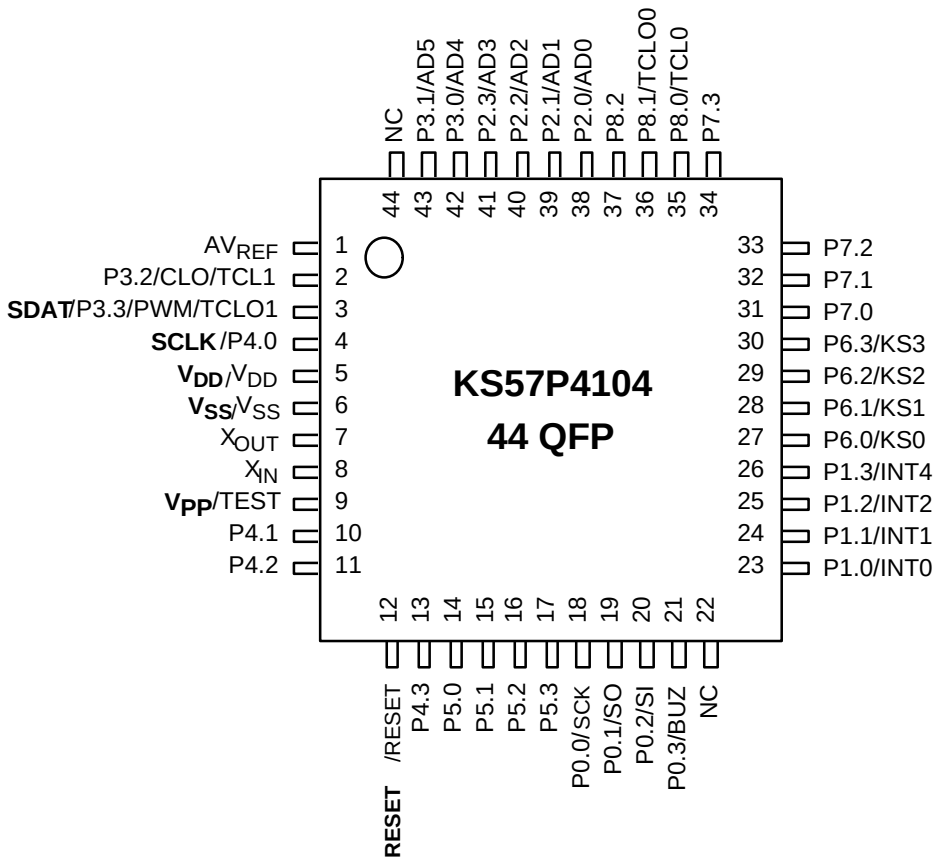
The KS57P4104/P4204/P4304 single-chip CMOS microcontroller is the OTP (One Time Programmable) version of the KS57C4104/C4204/C4304 microcontroller. It has an on-chip OTP ROM instead of masked ROM. Samsung′s own serial protocol used for OTP program pin information regarding OTP program can be referred OTP pin description.

The KS57P4104/P4204/P4304 is fully compatible with the KS57C4104/C4204/C4304, in function, in D.C. electrical characteristics and in pin configuration. Because of its simple programming requirements, the KS57P4104/P4204/P4304 is ideal for use as an evaluation chip for the KS57C4104/C4204/C4304.



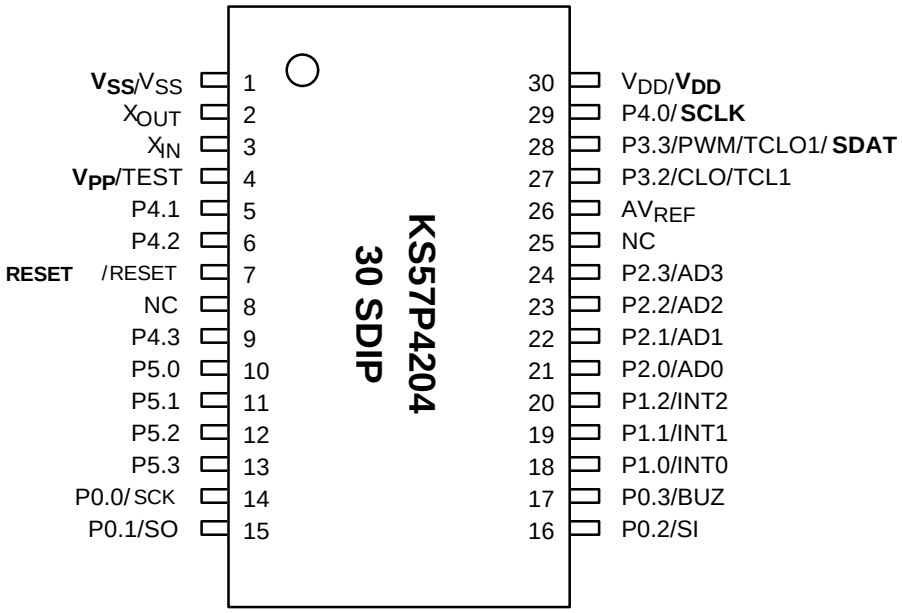
NOTE: The bolds indicate an OTP pin name.

Figure 16-1. KS57P4104 Pin Assignments (42-SDIP)



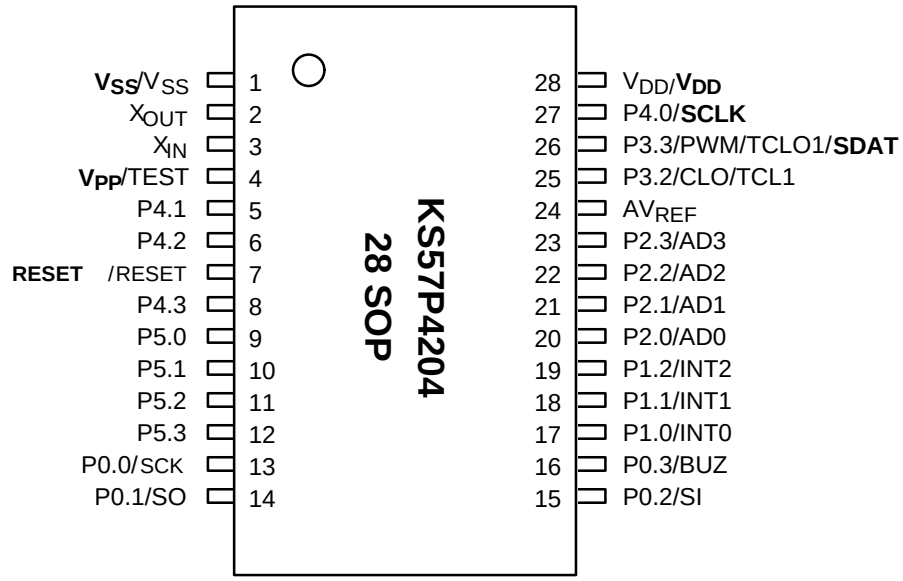
NOTE: The bolds indicate an OTP pin name.

Figure 16-2. KS57P4104 Pin Assignments (44-QFP)



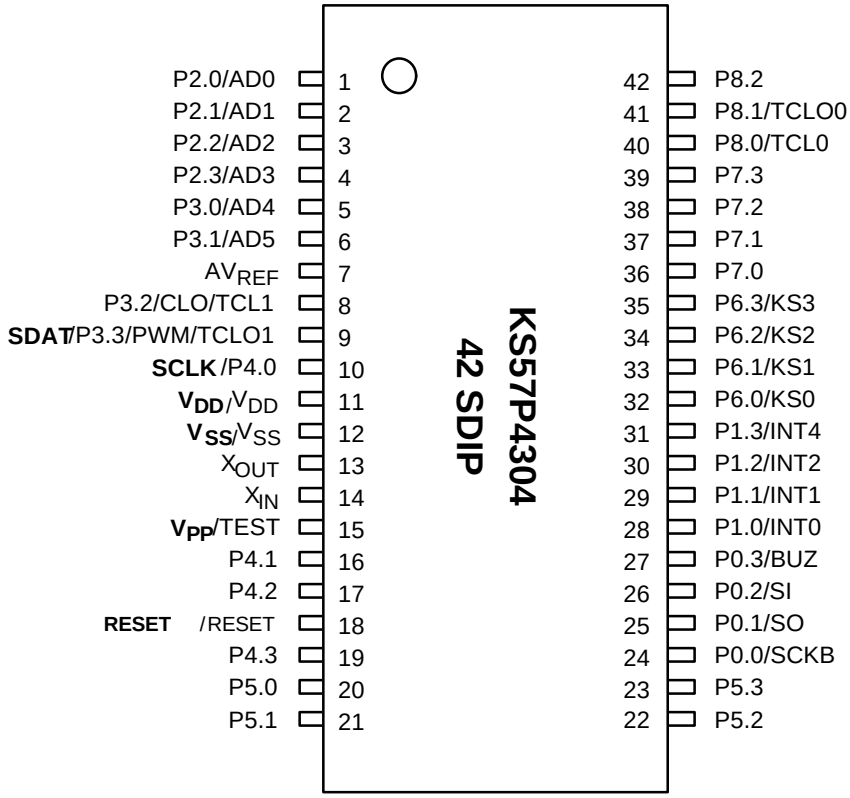
NOTE: The bolds indicate an OTP pin name.

Figure 16-3. KS57P4204 Pin Assignments (30-SDIP)



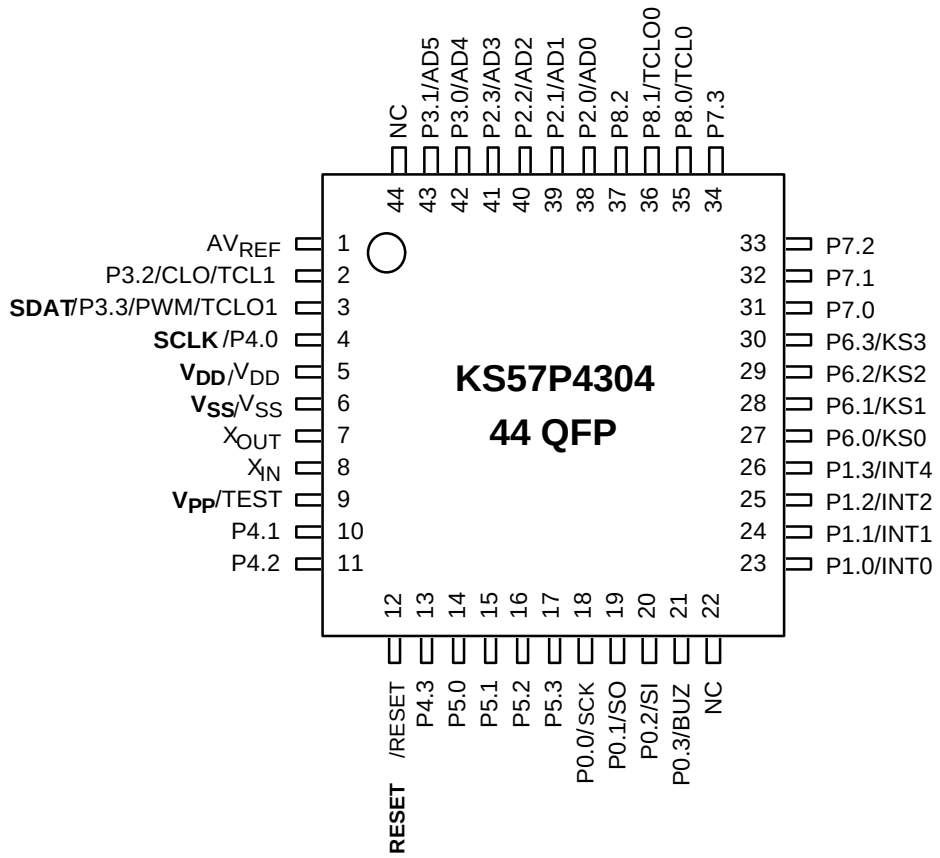
NOTE: The bolds indicate an OTP pin name.

Figure 16-4. KS57P4204 Pin Assignments (28-SOP)



NOTE: The bolds indicate an OTP pin name.

Figure 16-5. KS57P4304 Pin Assignments (42-SDIP)



NOTE: The bolds indicate an OTP pin name.

Figure 16-6. KS57P4304 Pin Assignments (44-QFP)

Table 16-1. Pin Descriptions of KS57P4104/P4304 Used to Read/Write the EPROM

Main Chip	During Programming			
Pin Name	Pin Name	Pin No.	I/O	Function
P3.3	SDAT	9 (3)	I/O	Serial data pin. Output port when reading and input port when writing. Can be assigned as a Input / push-pull output port.
P4.0	SCLK	10 (4)	I/O	Serial clock pin. Input only pin.
TEST	V_{PP} (TEST)	15 (9)	I	Power supply pin for EPROM cell writing (indicates that OTP enters into the writing mode). When 12.5 V is applied, OTP is in writing mode and when 5 V is applied, OTP is in reading mode. (Option)
RESET	RESET	18 (12)	I	Chip initialization
V_{DD}/V_{SS}	V_{DD}/V_{SS}	11/12 (5/6)	I	Logic power supply pin. V_{DD} should be tied to +5 V during programming.

NOTE: Parentheses indicate 44-QFP pin number.

Table 16-2. Pin Descriptions of KS57P4204 Used to Read/Write the EPROM

Main Chip	During Programming			
Pin Name	Pin Name	Pin No.	I/O	Function
P3.3	SDAT	28 (26)	I/O	Serial data pin. Output port when reading and input port when writing. Can be assigned as a Input / push-pull output port.
P4.0	SCLK	29 (27)	I/O	Serial clock pin. Input only pin.
TEST	V_{PP} (TEST)	4 (4)	I	Power supply pin for EPROM cell writing (indicates that OTP enters into the writing mode). When 12.5 V is applied, OTP is in writing mode and when 5 V is applied, OTP is in reading mode. (Option)
RESET	RESET	7 (7)	I	Chip initialization
V_{DD}/V_{SS}	V_{DD}/V_{SS}	30/1 (28/1)	I	Logic power supply pin. V_{DD} should be tied to +5 V during programming.

NOTE: Parentheses indicate 28-SOP pin number.

Table 16-3. Comparison of KS57P4104/P4204 and KS57C4104/C4204 Features

Characteristic	KS57P4104/P4204	KS57C4104/C4204
Program Memory	4 K byte EPROM	4 K byte mask ROM
Operating Voltage (V_{DD})	1.8 V to 5.5 V	1.8 V to 5.5 V
OTP Programming Mode	V_{DD} = 5 V, V_{PP}(TEST)=12.5V	
Pin Configuration	42 SDIP, 44 QFP, 30 SDIP, 28 SOP	42 SDIP, 44 QFP, 30 SDIP, 28 SOP
EPROM Programmability	User Program 1 time	Programmed at the factory

Table 16-4. Comparison of KS57P4304 and KS57C4304 Features

Characteristic	KS57P4304	KS57C4304
Program Memory	4 K byte EPROM	4 K byte mask ROM
Operating Voltage (V_{DD})	2.5 V to 5.5 V	2.5 V to 5.5 V
OTP Programming Mode	V_{DD} = 5 V, V_{PP}(TEST)=12.5V	
Pin Configuration	42 SDIP, 44 QFP	42 SDIP, 44 QFP
EPROM Programmability	User Program 1 time	Programmed at the factory

OPERATING MODE CHARACTERISTICS

When 12.5 V is supplied to the V_{PP}(TEST) pin of the KS57P4104/P4204/P4304, the EPROM programming mode is entered. The operating mode (read, write, or read protection) is selected according to the input signals to the pins listed in Table 16-4 below.

Table 16-5. Operating Mode Selection Criteria

V_{DD}	V_{PP} (TEST)	REG/ MEM	Address (A15-A0)	R/W	Mode
5 V	5 V	0	0000H	1	EPROM read
	12.5 V	0	0000H	0	EPROM program
	12.5 V	0	0000H	1	EPROM verify
	12.5 V	1	0E3FH	0	EPROM read protection

NOTE: "0" means Low level; "1" means High level.

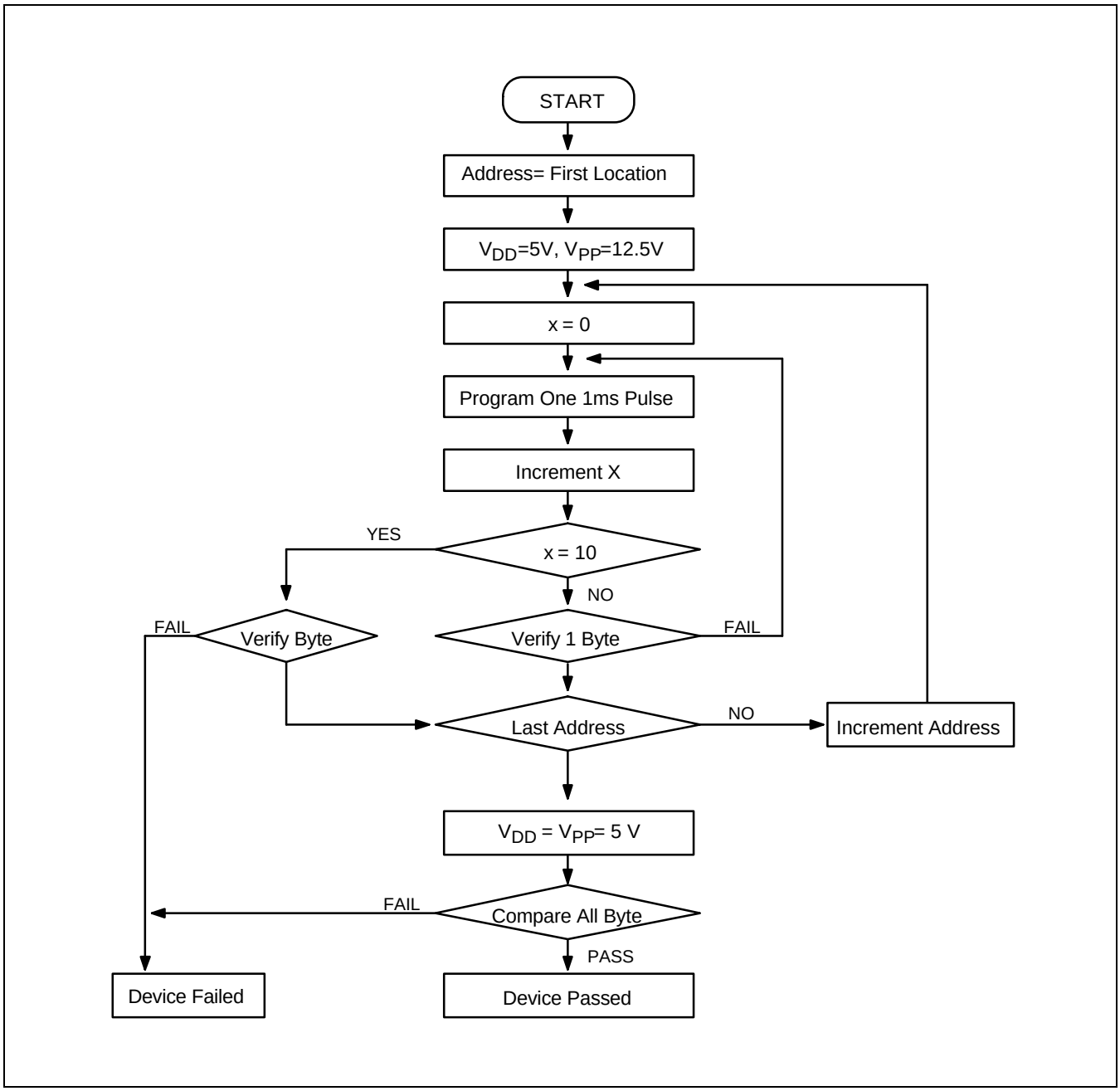


Figure 16-7. OTP Programming Algorithm

Table 16-6. KS57P4104/P4204 D.C. Electrical Characteristics

(T_A = – 40 °C to + 85 °C, V_{DD} = 1.8 V to 5.5 V)

Parameter	Symbol	Conditions		Min	Typ	Max	Units
Supply Current (1)	I_{DD1}	Run mode; V_{DD} = 5.0 V ± 10%	6.0MHz	–	3.0	8.0	mA
		Crystal oscillator; C1=C2=22pF	4.19MHz		2.3	5.5	
		V_{DD} = 3 V ± 10%	6.0MHz		1.4	4.0	
			4.19MHz		1.1	3.0	
	I_{DD2}	Idle mode; V_{DD} = 5.0 V ± 10%	6.0MHz	–	1.1	2.5	mA
		Crystal oscillator; C1=C2=22pF	4.19MHz		1.0	1.8	
		V_{DD} = 3 V ± 10%	6.0MHz		0.5	1.5	
			4.19MHz		0.4	1.0	
	I_{DD3}	Stop mode; V_{DD} = 5.0 V ± 10%		–	0.1	5.0	µA
		Stop mode; V_{DD} = 3.0 V ± 10%			0.1	3.0	

NOTES:
1. D.C. electrical values for Supply current (I_{DD1} to I_{DD3}) do not include current drawn through internal pull-up registers, output port drive currents and ADC.
2. The supply current assumes a CPU clock of fx/4.

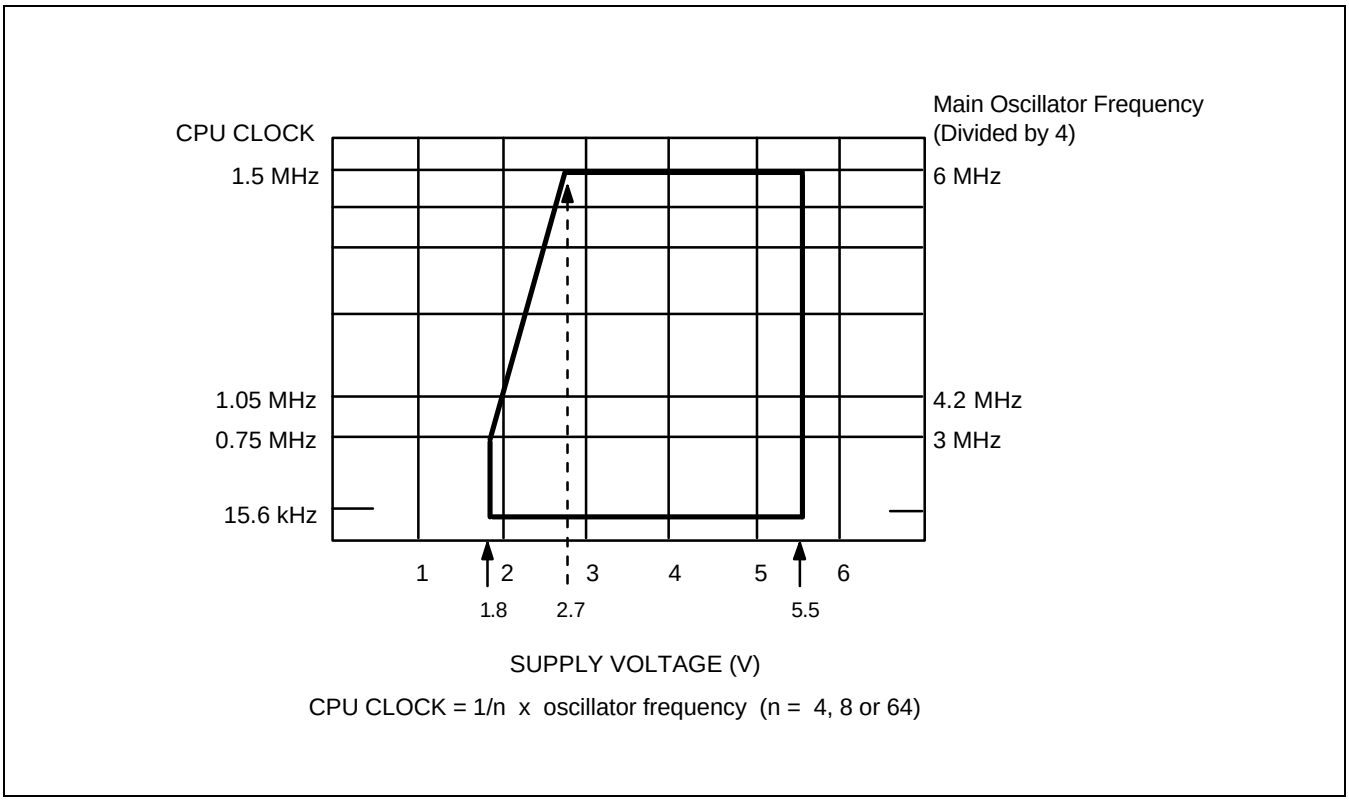


Figure 16-8. KS57P4104/P4204 Standard Operating Voltage Range

Table 16-7. KS57P4304 D.C. Electrical Characteristics

(T_A = – 40 °C to + 85 °C, V_{DD} = 2.5 V to 5.5 V)

Parameter	Symbol	Conditions		Min	Typ	Max	Units
Supply Current (1)	I_{DD1}	Run mode; V_{DD} = 5.0 V ± 10%	6.0MHz	–	3.1	8.0	mA
		Crystal oscillator; C1=C2=22pF	4.19MHz		2.4	5.5	
		V_{DD} = 3 V ± 10%	6.0MHz		1.5	4.0	
			4.19MHz		1.2	3.0	
	I_{DD2}	Idle mode; V_{DD} = 5.0 V ± 10%	6.0MHz	–	1.2	2.5	mA
		Crystal oscillator; C1=C2=22pF	4.19MHz		1.1	1.8	
		V_{DD} = 3 V ± 10%	6.0MHz		0.6	1.5	
			4.19MHz		0.5	1.0	
	I_{DD3}	Stop mode; V_{DD} = 5.0 V ± 10%		–	120	200	µA
		Stop mode; V_{DD} = 3.0 V ± 10%			100	150	

NOTES:
1. D.C. electrical values for Supply current (I_{DD1} to I_{DD3}) do not include current drawn through internal pull-up registers, output port drive currents and ADC.
2. The supply current assumes a CPU clock of fx/4.

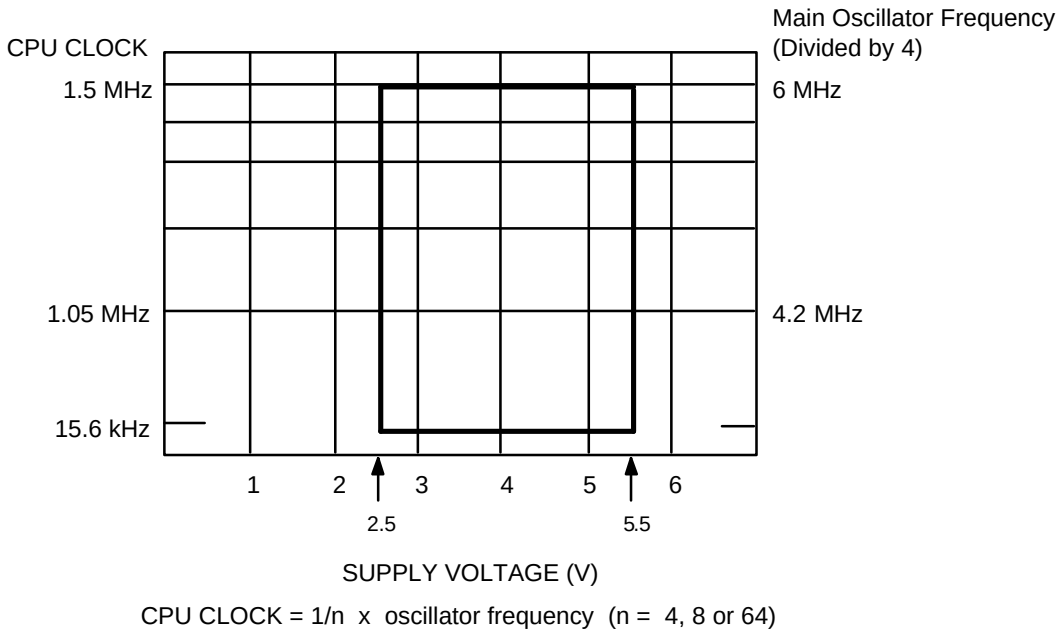


Figure 16-9. KS57P4304 Standard Operating Voltage Range