

SANYO

No. ※4245A

## Controller LSI for On-screen Displays

## Preliminary

## Overview

The LC74711 is a CMOS LSI for applications involving microcomputer control of on-screen character and graphics displays. Built-in character ROM supplies 128 alphanumeric characters and each character is generated in a 12 by 18 pixel format. The display is capable of supporting a maximum of 288 characters within a 24 characters by 12 line array.

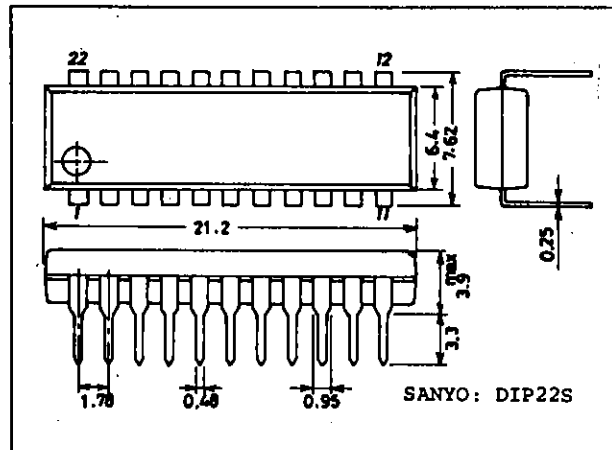
## Functions and Applications

- (1) Screen construction 24 characters X 12 lines
- (2) Number of characters displayed  
Maximum 288 characters capacity
- (3) Display control ROM (line ROM)  
64 lines (line unit control: 24 character construction)
- (4) Display RAM 176 characters (supporting extended character selection)
- (5) Character construction  
12 (horizontal) X 18 (vertical) pixels
- (6) Character set 128 types of characters
- (7) Character size 4 horizontal types and 4 vertical types
- (8) Display starting position  
64 types horizontally and 64 types vertically
- (9) Blinking Character units
- (10) Blinking types 2 types with approximate 1.0 sec and 0.5 sec cycles and 3-type selection for 25%, 50% and 75% duty
- (11) Blanking Font complete blanking (12 X 18 pixels)
- (12) Background color 8 background tints (during internal synchronizing operation: 4 fsc when using crystal oscillator)
- (13) External control input Serial data input
- (14) Synchronizing signal Internal synchronizing, supports external synchronizing changeover
- (15) Built-in synchronizing separator circuit
- (16) Video output NTSC system composite video output
- (17) Superimpose Characters superimposed over composite video output
- (18) Package DIP-22S

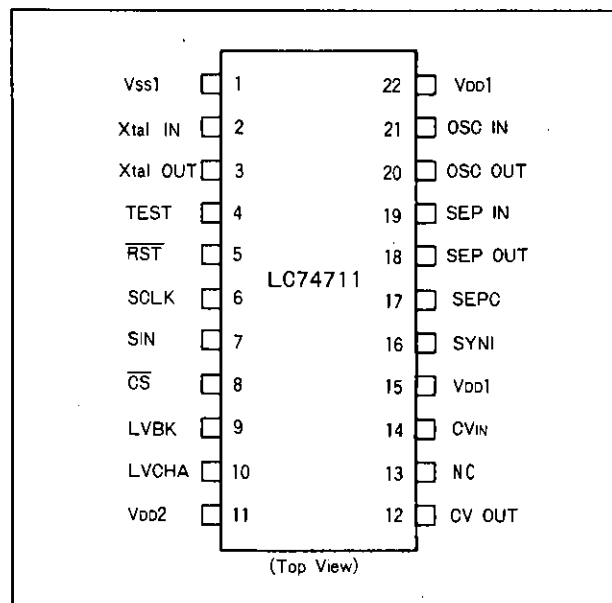
## Package Dimensions

unit : mm

## 3059-DIP22S



## Pin Assignment



## Specifications

### Absolute Maximum Ratings

Item	Symbol	Conditions/Pins	Rating Values	unit
Maximum supply voltage	$V_{DD\ max}$	$V_{DD1}, V_{DD2}$	$V_{SS}-0.3$ to $V_{SS}+7.0$	V
Maximum input voltage	$V_{IN\ max}$	All Input pins	$V_{SS}-0.3$ to $V_{DD}+0.3$	V
Maximum output voltage	$V_{OUT\ max}$		$V_{SS}-0.3$ to $V_{DD}+0.3$	V
Allowable power dissipation	$Pd\ max$	$T_a = 25^\circ C$	300	mW
Operating temperature	$Topr$		-30 to +70	$^\circ C$
Storage temperature	$Tstg$		-40 to +125	$^\circ C$

### Allowable Operating Ranges at $T_a = -30$ to $+70^\circ C$

Item	Symbol	Conditions/Pins	Rating Values			unit
			min	typ	max	
Supply voltage	$V_{DD1}$	$V_{DD1}$ pin	4.5	5.0	5.5	V
	$V_{DD2}$	$V_{DD2}$ pin	4.5	5.0	$1.27V_{DD1}$	V
Input "H" level voltage	$V_{IH}$	$\overline{CS}, SIN, \overline{RST}, SCLK, SEPIN$ pin	$0.8V_{DD1}$		$V_{DD1}+0.3$	V
Input "L" level voltage	$V_{IL}$	$\overline{CS}, SIN, \overline{RST}, SCLK, SEPIN$ pin	$V_{SS}-0.3$		$0.2V_{DD1}$	V
Composite video input voltage	$V_{IN1}$	$CV_{IN}$ pin		$2V_{P-P}$		V
	$V_{IN2}$	SYNI pin		$2V_{P-P}$	$2.5V_{P-P}$	
Oscillation frequency	$F_{OSC1}$	Xtal oscillation pin (2 fsc)		7.159		MHz
	$F_{OSC2}$	Xtal oscillation pin (4 fsc)		14.318		MHz
	$F_{OSC3}$	LC oscillation pin (when using LC oscillation)	5	7	10	MHz

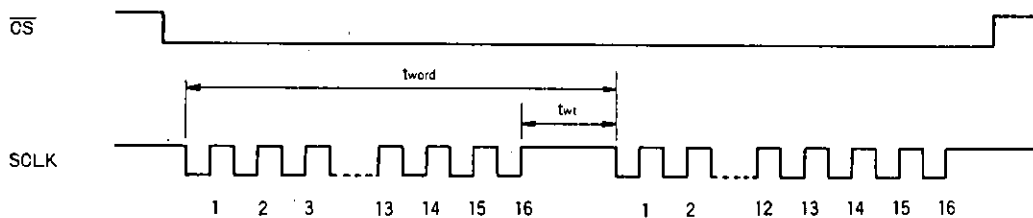
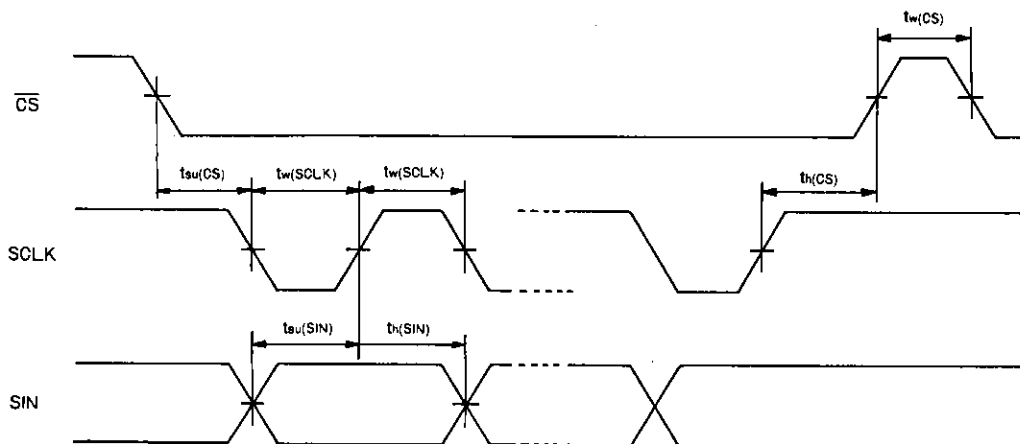
### Electrical Characteristics at $T_a = -30$ to $+70^\circ C$ , default of $V_{DD1} = 5$ V

Item	Symbol	Pins	Conditions	Rating Values			unit
				min	typ	max	
Output off leak current	$I_{leak}$	CV OUT pin				10	$\mu A$
Output "H" level voltage	$V_{OH1}$	SEP OUT pin	$V_{DD1} = 4.5V, I_{OH} = -1.0mA$	3.5			V
Output "L" level voltage	$V_{OL1}$	SEP OUT pin	$V_{DD1} = 4.5V, I_{OL} = 1.0mA$			1.0	V
Input current	$I_{IH}$	$\overline{CS}, SIN, \overline{RST}, SCLK, SEPIN$ pin	$V_{IN} = V_{DD1}$			1	$\mu A$
	$I_{IL}$	OSCIN pin	$V_{IN} = V_{SS}$	-1			$\mu A$
Current consumption during operation	$I_{DD1}$	$V_{DD1}$ pin	All output are OPEN Xtal = 14.318MHz, LC = 7MHz			10	mA
	$I_{DD2}$	$V_{DD2}$ pin	$V_{DD2} = 5.0V$			15	mA

### Timing Characteristics at $T_a = -30$ to $+70^\circ C, V_{DD1} = 5 \pm 0.5$ V

Item	Symbol	Conditions/Pins	Rating Values			unit
			min	typ	max	
Input minimum pulse width	$t_w$ (SCLK)	SCLK pin	200			ns
	$t_w$ (CS)	$\overline{CS}$ pin (with $\overline{CS}$ set to "H" period)	1			$\mu s$
Data setup time	$t_{su}$ (CS)	$\overline{CS}$ pin	200			ns
	$t_{su}$ (SIN)	SIN pin	200			ns
Data hold time	$t_h$ (CS)	$\overline{CS}$ pin	2			$\mu s$
	$t_h$ (SIN)	SIN pin	200			ns
Single word and write time	$t_{word}$	16-bit write time	10			$\mu s$
	$t_{wt}$	RAM data write time	1			$\mu s$

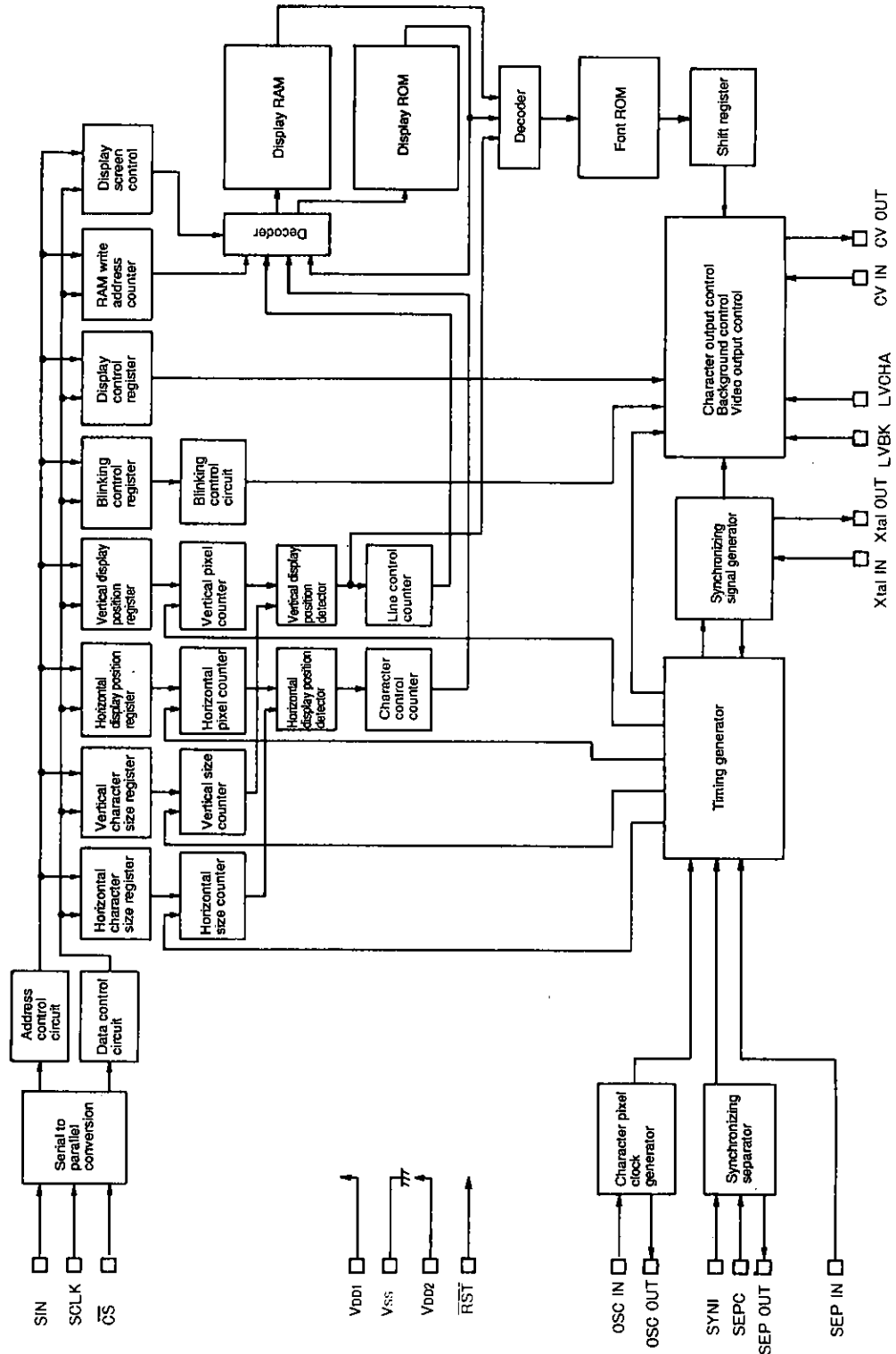
Serial Data Input Timing



## Pin Functions

Pin No.	Pin Symbol	Pin name	Functions
1	V <sub>SS1</sub>	Ground pin	Pin for connecting to ground (GND) (grounding pin for digital system).
2	Xtal IN	Xtal oscillation pin	Pin for connecting to capacitor or crystal of crystal oscillator for internal synchronizing signal oscillation applications.
3	Xtal OUT		
4	TEST	Test output pin	Pin for test data output.
5	$\overline{\text{RST}}$	Reset input pin	Pin for system reset input (hysteresis input).
6	SCLK	Clock input pin	Pin for clock input using serial data input (hysteresis input).
7	SIN	Data input pin	Pin for serial data input (hysteresis input). Input in 16-bit units.
8	$\overline{\text{CS}}$	Enable input pin	Pin for enable input for serial data processing (hysteresis input). "L" serial data input switches to enable.
9	LVBK	Blanking level adjustment input pin	Pin for level input for blanking level adjusting.
10	LVCHA	Character level adjustment input pin	Pin for level input for character level adjusting.
11	V <sub>DD2</sub>	Supply pin	Pin for power supply for adjusting signal level of composite video (power supply for analog system).
12	CV OUT	Video signal output pin	Pin for composite video signal output.
13	NC		Non connection.
14	CV IN	Video signal input pin	Pin for composite video signal input.
15	V <sub>DD1</sub>	Power supply pin	Pin for power supply (+5V).
16	SYNI	Synchronizing separator circuit input pin	Pin for input of separator circuit composite synchronizing signal.
17	SEPC	Synchronizing separator circuit adjustment pin	Pin for adjusting synchronizing separator circuit (connecting capacitor).
18	SEP OUT	Composite synchronizing signal output pin	Pin for output of composite synchronizing signal for synchronizing separator circuit.
19	SEP IN	Vertical synchronizing signal input pin	Pin for input of vertical synchronizing signal and integrating output signal of SEP OUT pin. Applied when connecting an integrating circuit to the SEP OUT pin.
20	OSC OUT	LC oscillation pin	Pin for connecting a capacitor or oscillator coil for pixel clock generation and character output applications.
21	OSC IN		
22	V <sub>DD1</sub>	Power supply pin (+5V)	Pin for power supply (+5V).

System Block Diagram



**Screen Construction**

Display mode supports 24 characters and 12 lines.

Maximum number of displayed characters is 288 characters.

When character size is enlarged, the maximum number of characters displayed is reduced to less than 288 characters.

Display line ROM (12-line setting) or display RAM (176 characters).

- Displays using line ROM specify the fixed character set.
- Extended character set are available using display RAM and program setting of characters.

		24 characters																							
	00	01	02	03	04	05	06	07	08	09	10	11	12	13	14	15	16	17	18	19	20	21	22	23	
	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	
	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	64	65	66	67	68	69	70	71	
	72	73	74	75	76	77	78	79	80	81	82	83	84	85	86	87	88	89	90	91	92	93	94	95	
	96	97	98	99	100	101	102	103	104	105	106	107	108	109	110	111	112	113	114	115	116	117	118	119	
	120	121	122	123	124	125	126	127	128	129	130	131	132	133	134	135	136	137	138	139	140	141	142	143	
12 lines	144	145	146	147	148	149	150	151	152	153	154	155	156	157	158	159	160	161	162	163	164	165	166	167	
	168	169	170	171	172	173	174	175	176	177	178	179	180	181	182	183	184	185	186	187	188	189	190	191	
	192	193	194	195	196	197	198	199	200	201	202	203	204	205	206	207	208	209	210	211	212	213	214	215	
	216	217	218	219	220	221	222	223	224	225	226	227	228	229	230	231	232	233	234	235	236	237	238	239	
	240	241	242	243	244	245	246	247	248	249	250	251	252	253	254	255	256	257	258	259	260	261	262	263	
	264	265	266	267	268	269	270	271	272	273	274	275	276	277	278	279	280	281	282	283	284	285	286	287	

**Memory Construction (display RAM and control RAM)**

Memory addresses and data 16-bit processing.

Addresses 0 (000 HEX) to 175 (OAF HEX) are reserved for display memory (RAM) data.

Addresses 176 (0B0 HEX) to 191 (0BF HEX) are reserved for display control register data.

Address	DA F	DA E	DA D	DA C	DA B	DA A	DA 9	DA 8	DA 7	DA 6	DA 5	DA 4	DA 3	DA 2	DA 1	DA 0	Notes
000 (000h)	0	0	0	0	0	0	0	0	BLANK	C <sub>6</sub>	C <sub>5</sub>	C <sub>4</sub>	C <sub>3</sub>	C <sub>2</sub>	C <sub>1</sub>	C <sub>0</sub>	Display RAM
	<div style="display: flex; justify-content: space-around; align-items: center;"> <div style="border: 1px solid black; padding: 2px;">Blinking</div> <div style="border: 1px solid black; padding: 2px;">Character code</div> </div>																
175 (OAFh)	0	0	0	0	0	0	0	0	BLANK	C <sub>6</sub>	C <sub>5</sub>	C <sub>4</sub>	C <sub>3</sub>	C <sub>2</sub>	C <sub>1</sub>	C <sub>0</sub>	
176 (0B0h)	0	0	0	0	0	ADRA	ADR9	ADR8	ADR7	ADR6	ADR5	ADR4	ADR3	ADR2	ADR1	ADR0	Display line ROM setting for first character of first line
177 (0B1h)	0	0	0	0	0	ADRA	ADR9	ADR8	ADR7	ADR6	ADR5	ADR4	ADR3	ADR2	ADR1	ADR0	Display line ROM setting for first character of second line
178 (0B2h)	0	0	0	0	0	ADRA	ADR9	ADR8	ADR7	ADR6	ADR5	ADR4	ADR3	ADR2	ADR1	ADR0	Display line ROM setting for first character of third line
179 (0B3h)	0	0	0	0	0	ADRA	ADR9	ADR8	ADR7	ADR6	ADR5	ADR4	ADR3	ADR2	ADR1	ADR0	Display line ROM setting for first character of fourth line
180 (0B4h)	0	0	0	0	0	ADRA	ADR9	ADR8	ADR7	ADR6	ADR5	ADR4	ADR3	ADR2	ADR1	ADR0	Display line ROM setting for first character of fifth line
181 (0B5h)	0	0	0	0	0	ADRA	ADR9	ADR8	ADR7	ADR6	ADR5	ADR4	ADR3	ADR2	ADR1	ADR0	Display line ROM setting for first character of sixth line
182 (0B6h)	0	0	0	0	0	ADRA	ADR9	ADR8	ADR7	ADR6	ADR5	ADR4	ADR3	ADR2	ADR1	ADR0	Display line ROM setting for first character of seventh line
183 (0B7h)	0	0	0	0	0	ADRA	ADR9	ADR8	ADR7	ADR6	ADR5	ADR4	ADR3	ADR2	ADR1	ADR0	Display line ROM setting for first character of eighth line
184 (0B8h)	0	0	0	0	0	ADRA	ADR9	ADR8	ADR7	ADR6	ADR5	ADR4	ADR3	ADR2	ADR1	ADR0	Display line ROM setting for first character of ninth line
185 (0B9h)	0	0	0	0	0	ADRA	ADR9	ADR8	ADR7	ADR6	ADR5	ADR4	ADR3	ADR2	ADR1	ADR0	Display line ROM setting for first character of tenth line
186 (0BAh)	0	0	0	0	0	ADRA	ADR9	ADR8	ADR7	ADR6	ADR5	ADR4	ADR3	ADR2	ADR1	ADR0	Display line ROM setting for first character of eleventh line
187 (0BBh)	0	0	0	0	0	ADRA	ADR9	ADR8	ADR7	ADR6	ADR5	ADR4	ADR3	ADR2	ADR1	ADR0	Display line ROM setting for first character of twelfth line
188 (0BCh)	0	0	0	0	HSZ 31	HSZ 30	HSZ 21	HSZ 20	HSZ 11	HSZ 10	HP5	HP4	HP3	HP2	HP1	HP0	Horizontal display position Horizontal character size
189 (0BDh)	0	0	0	0	VSZ 31	VSZ 30	VSZ 21	VSZ 20	VSZ 11	VSZ 10	VP5	VP4	VP3	VP2	VP1	VP0	Vertical display position Vertical character size
190 (0BEh)	0	0	0	0	INT / NON	LC / XTAL	2fsc / 4fsc	OSC STP	DSP ON	—	SYS RST	—	—	PHASE 2	PHASE 1	PHASE 0	Video signal and other
191 (0BFh)	0	0	0	0	TST MOD	—	—	BLK 1	BLK 0	—	BLINK 2	BLINK 1	BLINK 0	EX	CB0FF	BC0L	Control register

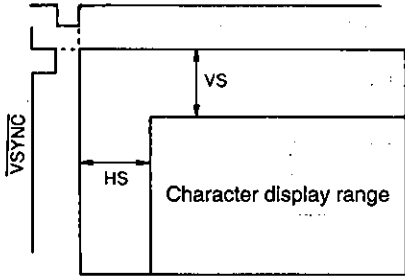
(1) Address 188 (0 BC<sub>HEX</sub>)

DA 0 to C	Register Name	Contents		Notes									
		Setting	Function										
0	HP0 (LSB)	0	When the horizontal display starting position is set to HS, $HS = T_C \times (4 \sum_{n=0}^5 2^n HP_n)$ T <sub>C</sub> : represents oscillation cycle of OSC IN and OUT oscillator during operation mode	Horizontal display starting position sets using 6-bit found at HP5 to HP0. Single bit significance is 4T <sub>C</sub> .									
		1											
1	HP1	0											
		1											
2	HP2	0											
		1											
3	HP3	0											
		1											
4	HP4	0											
		1											
5	HP5 (MSB)	0											
		1											
6	HSZ10	0	<table border="1"> <tr> <td>HSZ11 \ HSZ10</td> <td>0</td> <td>1</td> </tr> <tr> <td>0</td> <td>1T<sub>C</sub>/1 dot</td> <td>2T<sub>C</sub>/1 dot</td> </tr> <tr> <td>1</td> <td>3T<sub>C</sub>/1 dot</td> <td>4T<sub>C</sub>/1 dot</td> </tr> </table>	HSZ11 \ HSZ10	0	1	0	1T <sub>C</sub> /1 dot	2T <sub>C</sub> /1 dot	1	3T <sub>C</sub> /1 dot	4T <sub>C</sub> /1 dot	First line horizontal character size.
		HSZ11 \ HSZ10	0	1									
0	1T <sub>C</sub> /1 dot	2T <sub>C</sub> /1 dot											
1	3T <sub>C</sub> /1 dot	4T <sub>C</sub> /1 dot											
1													
7	HSZ11	0	<table border="1"> <tr> <td>HSZ21 \ HSZ20</td> <td>0</td> <td>1</td> </tr> <tr> <td>0</td> <td>1T<sub>C</sub>/1 dot</td> <td>2T<sub>C</sub>/1 dot</td> </tr> <tr> <td>1</td> <td>3T<sub>C</sub>/1 dot</td> <td>4T<sub>C</sub>/1 dot</td> </tr> </table>	HSZ21 \ HSZ20	0	1	0	1T <sub>C</sub> /1 dot	2T <sub>C</sub> /1 dot	1	3T <sub>C</sub> /1 dot	4T <sub>C</sub> /1 dot	Second line horizontal character size.
		HSZ21 \ HSZ20		0	1								
0	1T <sub>C</sub> /1 dot	2T <sub>C</sub> /1 dot											
1	3T <sub>C</sub> /1 dot	4T <sub>C</sub> /1 dot											
1													
8	HSZ20	0	<table border="1"> <tr> <td>HSZ31 \ HSZ30</td> <td>0</td> <td>1</td> </tr> <tr> <td>0</td> <td>1T<sub>C</sub>/1 dot</td> <td>2T<sub>C</sub>/1 dot</td> </tr> <tr> <td>1</td> <td>3T<sub>C</sub>/1 dot</td> <td>4T<sub>C</sub>/1 dot</td> </tr> </table>	HSZ31 \ HSZ30	0	1	0	1T <sub>C</sub> /1 dot	2T <sub>C</sub> /1 dot	1	3T <sub>C</sub> /1 dot	4T <sub>C</sub> /1 dot	Lines 3 to 12 horizontal character sizes.
		HSZ31 \ HSZ30		0	1								
0	1T <sub>C</sub> /1 dot	2T <sub>C</sub> /1 dot											
1	3T <sub>C</sub> /1 dot	4T <sub>C</sub> /1 dot											
1													
A	HSZ30	0	<table border="1"> <tr> <td>HSZ31 \ HSZ30</td> <td>0</td> <td>1</td> </tr> <tr> <td>0</td> <td>1T<sub>C</sub>/1 dot</td> <td>2T<sub>C</sub>/1 dot</td> </tr> <tr> <td>1</td> <td>3T<sub>C</sub>/1 dot</td> <td>4T<sub>C</sub>/1 dot</td> </tr> </table>	HSZ31 \ HSZ30	0	1	0	1T <sub>C</sub> /1 dot	2T <sub>C</sub> /1 dot	1	3T <sub>C</sub> /1 dot	4T <sub>C</sub> /1 dot	
		HSZ31 \ HSZ30		0	1								
0	1T <sub>C</sub> /1 dot	2T <sub>C</sub> /1 dot											
1	3T <sub>C</sub> /1 dot	4T <sub>C</sub> /1 dot											
1													
B	HSZ31	0											
		1											
C	—	0											
		1											

Note: \* When reset using the  $\overline{RST}$  pin, all registers are set to 0 (zero).



(2) Address 189 (0 BD<sub>HEX</sub>)

DA 0 to C	Register Name	Contents		Notes									
		Setting	Function										
0	VP0 (LSB)	0	When the vertical display starting position is set to VS, $VS = H \times (4 \sum_{n=0}^5 VPn)$ H: represents horizontal synchronizing pulse cycle 	Vertical display starting position sets using 6-bit found at VP5 to VP0. Single bit significance is 4H.									
		1											
1	VP1	0											
		1											
2	VP2	0											
		1											
3	VP3	0											
		1											
4	VP4	0											
		1											
5	VP5 (MSB)	0											
		1											
6	VSZ10	0	<table border="1"> <tr> <td>VSZ11 \ VSZ10</td> <td>0</td> <td>1</td> </tr> <tr> <td>0</td> <td>1H/1 dot</td> <td>2H/1 dot</td> </tr> <tr> <td>1</td> <td>3H/1 dot</td> <td>4H/1 dot</td> </tr> </table>	VSZ11 \ VSZ10	0	1	0	1H/1 dot	2H/1 dot	1	3H/1 dot	4H/1 dot	First line vertical character size.
		VSZ11 \ VSZ10	0	1									
0	1H/1 dot	2H/1 dot											
1	3H/1 dot	4H/1 dot											
1													
7	VSZ11	0	<table border="1"> <tr> <td>VSZ21 \ VSZ20</td> <td>0</td> <td>1</td> </tr> <tr> <td>0</td> <td>1H/1 dot</td> <td>2H/1 dot</td> </tr> <tr> <td>1</td> <td>3H/1 dot</td> <td>4H/1 dot</td> </tr> </table>	VSZ21 \ VSZ20	0	1	0	1H/1 dot	2H/1 dot	1	3H/1 dot	4H/1 dot	Second line vertical character size.
		VSZ21 \ VSZ20	0	1									
0	1H/1 dot	2H/1 dot											
1	3H/1 dot	4H/1 dot											
1													
8	VSZ20	0	<table border="1"> <tr> <td>VSZ31 \ VSZ30</td> <td>0</td> <td>1</td> </tr> <tr> <td>0</td> <td>1H/1 dot</td> <td>2H/1 dot</td> </tr> <tr> <td>1</td> <td>3H/1 dot</td> <td>4H/1 dot</td> </tr> </table>	VSZ31 \ VSZ30	0	1	0	1H/1 dot	2H/1 dot	1	3H/1 dot	4H/1 dot	Lines 3 to 12 vertical character sizes.
		VSZ31 \ VSZ30	0	1									
0	1H/1 dot	2H/1 dot											
1	3H/1 dot	4H/1 dot											
1													
9	VSZ21	0	<table border="1"> <tr> <td>VSZ31 \ VSZ30</td> <td>0</td> <td>1</td> </tr> <tr> <td>0</td> <td>1H/1 dot</td> <td>2H/1 dot</td> </tr> <tr> <td>1</td> <td>3H/1 dot</td> <td>4H/1 dot</td> </tr> </table>	VSZ31 \ VSZ30	0	1	0	1H/1 dot	2H/1 dot	1	3H/1 dot	4H/1 dot	Lines 3 to 12 vertical character sizes.
		VSZ31 \ VSZ30	0	1									
0	1H/1 dot	2H/1 dot											
1	3H/1 dot	4H/1 dot											
1													
A	VSZ30	0	<table border="1"> <tr> <td>VSZ31 \ VSZ30</td> <td>0</td> <td>1</td> </tr> <tr> <td>0</td> <td>1H/1 dot</td> <td>2H/1 dot</td> </tr> <tr> <td>1</td> <td>3H/1 dot</td> <td>4H/1 dot</td> </tr> </table>	VSZ31 \ VSZ30	0	1	0	1H/1 dot	2H/1 dot	1	3H/1 dot	4H/1 dot	Lines 3 to 12 vertical character sizes.
		VSZ31 \ VSZ30	0	1									
0	1H/1 dot	2H/1 dot											
1	3H/1 dot	4H/1 dot											
1													
B	VSZ31	0	<table border="1"> <tr> <td>VSZ31 \ VSZ30</td> <td>0</td> <td>1</td> </tr> <tr> <td>0</td> <td>1H/1 dot</td> <td>2H/1 dot</td> </tr> <tr> <td>1</td> <td>3H/1 dot</td> <td>4H/1 dot</td> </tr> </table>	VSZ31 \ VSZ30	0	1	0	1H/1 dot	2H/1 dot	1	3H/1 dot	4H/1 dot	Lines 3 to 12 vertical character sizes.
		VSZ31 \ VSZ30	0	1									
0	1H/1 dot	2H/1 dot											
1	3H/1 dot	4H/1 dot											
1													
C	—	0											
		1											

Note: \* When reset using the  $\overline{\text{RST}}$  pin, all registers are set to 0 (zero).

(3) Address 190 (0 BE<sub>HEX</sub>)

DA 0 to C	Register Name	Contents				Notes																																		
		Setting	Function																																					
0	PHASE0	0	<table border="1"> <thead> <tr> <th>PHASE2</th> <th>PHASE1</th> <th>PHASE0</th> <th>Background tint</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>0</td> <td><math>\pi/2</math></td> </tr> <tr> <td>0</td> <td>0</td> <td>1</td> <td><math>\pi</math></td> </tr> <tr> <td>0</td> <td>1</td> <td>0</td> <td><math>3\pi/2</math></td> </tr> <tr> <td>0</td> <td>1</td> <td>1</td> <td>In-phase</td> </tr> <tr> <td>1</td> <td>0</td> <td>0</td> <td><math>\pi/4</math></td> </tr> <tr> <td>1</td> <td>0</td> <td>1</td> <td><math>3\pi/4</math></td> </tr> <tr> <td>1</td> <td>1</td> <td>0</td> <td><math>5\pi/4</math></td> </tr> <tr> <td>1</td> <td>1</td> <td>1</td> <td><math>7\pi/4</math></td> </tr> </tbody> </table>	PHASE2	PHASE1	PHASE0	Background tint	0	0	0	$\pi/2$	0	0	1	$\pi$	0	1	0	$3\pi/2$	0	1	1	In-phase	1	0	0	$\pi/4$	1	0	1	$3\pi/4$	1	1	0	$5\pi/4$	1	1	1	$7\pi/4$	Background tint
		PHASE2		PHASE1	PHASE0	Background tint																																		
0	0	0		$\pi/2$																																				
0	0	1		$\pi$																																				
0	1	0		$3\pi/2$																																				
0	1	1		In-phase																																				
1	0	0		$\pi/4$																																				
1	0	1		$3\pi/4$																																				
1	1	0	$5\pi/4$																																					
1	1	1	$7\pi/4$																																					
1	Background color phase responding to color burst.																																							
1	PHASE1	0																																						
		1																																						
2	PHASE2	0																																						
		1																																						
3	—	0																																						
		1																																						
4	—	0																																						
		1																																						
5	SYSRST	0			$\overline{\text{CS}}$ pin resets for "L" and cancels reset using "H".																																			
		1	All registers reset and display set to off																																					
6	—	0																																						
		1																																						
7	DSPON	0	Character display off																																					
		1	Character display on																																					
8	OSCSTP	0	Crystal oscillator circuit and LC oscillator circuit is not stopped	External synchronizing mode enabled only when character display is off.																																				
		1	Crystal oscillator circuit and LC oscillator circuit is stopped																																					
9	$\overline{2fsc}$ /4fsc	0	Clock frequency 2 fsc	Crystal oscillator circuit oscillation frequency.																																				
		1	Clock frequency 4 fsc																																					
A	$\overline{\text{LC}}$ /XTAL	0	Using LC oscillation for pixel clock	When the LC oscillation circuit is not used, OSC IN pin is fixed at V <sub>DD</sub> .																																				
		1	Using crystal oscillation for pixel clock																																					
B	$\overline{\text{INT}}$ /NON	0	Interlaced (312.5 H/1 field)	Changeover is permitted between interlace and non-interlaced displays.																																				
		1	Non-interlaced (313 H/1 field)																																					
C	—	0																																						
		1																																						

Note: \* When reset using the  $\overline{\text{RST}}$  pin, all registers are set to 0 (zero).

(4) Address 191 (0BF<sub>HEX</sub>)

DA 0 to C	Register Name	Contents		Notes										
		Setting	Function											
0	BCOL	0	With background tint (only enabled with internal synchronizing)											
		1	No background tint (background level setting only)											
1	CBOFF	0	Burst signal always output											
		1	When BCOL is set to "H", burst signal also does not output											
2	EX	0	External synchronizing		HSYNC and VSYNC signal changeover to external or internal supported.									
		1	Internal synchronizing											
3	BLINK0	0	<table border="1" style="display: inline-table; vertical-align: middle;"> <tr> <td style="text-align: center;">BLINK0 BLINK1</td> <td style="text-align: center;">0</td> <td style="text-align: center;">1</td> </tr> <tr> <td style="text-align: center;">0</td> <td>Blinking off</td> <td>25% duty</td> </tr> <tr> <td style="text-align: center;">1</td> <td>50% duty</td> <td>75% duty</td> </tr> </table>		BLINK0 BLINK1	0	1	0	Blinking off	25% duty	1	50% duty	75% duty	Blinking duty comparative variability.
		BLINK0 BLINK1			0	1								
0	Blinking off	25% duty												
1	50% duty	75% duty												
1														
4	BLINK1	0												
		1												
5	BLINK2	0	Blinking cycle approximately 0.5 s		Variable blinking cycle.									
		1	Blinking cycle approximately 1 s											
6	—	0												
		1												
7	BLK0	0	<table border="1" style="display: inline-table; vertical-align: middle;"> <tr> <td style="text-align: center;">BLK0 BLK1</td> <td style="text-align: center;">0</td> <td style="text-align: center;">1</td> </tr> <tr> <td style="text-align: center;">0</td> <td>Blanking off</td> <td>Character size</td> </tr> <tr> <td style="text-align: center;">1</td> <td>Trimming size</td> <td>Total overall size</td> </tr> </table>	BLK0 BLK1	0	1	0	Blanking off	Character size	1	Trimming size	Total overall size	Variable blanking size.	
		BLK0 BLK1		0	1									
0	Blanking off	Character size												
1	Trimming size	Total overall size												
1														
8	BLK1	0												
		1												
9	—	0												
		1												
A	—	0												
		1												
B	TSTMOD	0	Normal operation mode	Fixes to zero (0) condition.										
		1	Test operation mode											
C	—	0												
		1												

Note: \* When reset using the  $\overline{\text{RST}}$  pin, all registers are set to 0 (zero).

**Memory Construction (Display Line ROM)**

Memory addresses are arrayed within 0 (000 HEX) to 1535 (5FF HEX) and have an 8-bit data construction.

Address	bit DA F	DA E	DA D	DA C	DA B	DA A	DA 9	DA 8	DA 7	DA 6	DA 5	DA 4	DA 3	DA 2	DA 1	DA 0	Notes	
0000 (000h)	0	0	0	0	0	0	0	0	ROM/RAM	ADR6	ADR5	ADR4	ADR3	ADR2	ADR1	ADR0	Display line ROM setting for first character and first line.	
0023 (017h)	0	0	0	0	0	0	0	0	ROM/RAM	ADR6	ADR5	ADR4	ADR3	ADR2	ADR1	ADR0	Display line ROM setting for twenty-fourth character and first line.	
0024 (018h)	0	0	0	0	0	0	0	0	ROM/RAM	ADR6	ADR5	ADR4	ADR3	ADR2	ADR1	ADR0	Display line ROM setting for first character and second line.	
<div style="border: 1px solid black; display: inline-block; padding: 5px;"> <table border="1" style="border-collapse: collapse;"> <tr> <td style="text-align: center;">ROM/RAM</td> <td style="text-align: center;">Character code</td> </tr> </table> </div>																	ROM/RAM	Character code
ROM/RAM	Character code																	
1535 (5FFh)	0	0	0	0	0	0	0	0	ROM/RAM	ADR6	ADR5	ADR4	ADR3	ADR2	ADR1	ADR0	Display line ROM setting for twenty-fourth character and sixty-fourth line.	

DA 0 to 8	Register Name	Contents		Notes
		Setting	Function	
0	ADR0	0	Character ROM address setting When display control RAM is specified, DA7 equals "1" and ADR0 to ADR 6 are set to "0" Character ROM address setting range is 0 to 127 (7F HEX)	
		1		
1	ADR1	0		
		1		
2	ADR2	0		
		1		
3	ADR3	0		
		1		
4	ADR4	0		
		1		
5	ADR5	0		
		1		
6	ADR6	0		
		1		
7	ROM/RAM	0	Character ROM is accessed and read directly	
		1	Character ROM is accessed and read through display RAM	

## Line Address Table for Display Line ROM



Line	Address	Line	Address
1 line	00HEX (0000)	33 line	300HEX (0768)
2 line	18HEX (0024)	34 line	318HEX (0792)
3 line	30HEX (0048)	35 line	330HEX (0816)
4 line	48HEX (0072)	36 line	348HEX (0840)
5 line	60HEX (0096)	37 line	360HEX (0864)
6 line	78HEX (0120)	38 line	378HEX (0888)
7 line	90HEX (0144)	39 line	390HEX (0912)
8 line	A8HEX (0168)	40 line	3A8HEX (0936)
9 line	C0HEX (0192)	41 line	3C0HEX (0960)
10 line	D8HEX (0216)	42 line	3D8HEX (0984)
11 line	F0HEX (0240)	43 line	3F0HEX (1008)
12 line	108HEX (0264)	44 line	408HEX (1032)
13 line	120HEX (0288)	45 line	420HEX (1056)
14 line	138HEX (0312)	46 line	438HEX (1080)
15 line	150HEX (0336)	47 line	450HEX (1104)
16 line	168HEX (0360)	48 line	468HEX (1128)
17 line	180HEX (0384)	49 line	480HEX (1152)
18 line	198HEX (0408)	50 line	498HEX (1176)
19 line	1B0HEX (0432)	51 line	4B0HEX (1200)
20 line	1C8HEX (0456)	52 line	4C8HEX (1224)
21 line	1E0HEX (0480)	53 line	4E0HEX (1248)
22 line	1F8HEX (0504)	54 line	4F8HEX (1272)
23 line	210HEX (0528)	55 line	510HEX (1296)
24 line	228HEX (0552)	56 line	528HEX (1320)
25 line	240HEX (0576)	57 line	540HEX (1344)
26 line	258HEX (0600)	58 line	558HEX (1368)
27 line	270HEX (0624)	59 line	570HEX (1392)
28 line	288HEX (0648)	60 line	588HEX (1416)
29 line	2A0HEX (0672)	61 line	5A0HEX (1440)
30 line	2B8HEX (0696)	62 line	5B8HEX (1464)
31 line	2D0HEX (0720)	63 line	5D0HEX (1488)
32 line	2E8HEX (0744)	64 line	5E8HEX (1512)

**Screen Construction (Sample Display)**

Setting of 12-line display using display line ROM (64 lines).

Within line ROM, setting of extended characters is made available through display control RAM.

Display control RAM addresses are automatically allocated to display array from 0 to 175 (AF<sub>HEX</sub>).

-  (thick line) indicates character setting using display control RAM.
-  (thin line) indicates character setting using line ROM.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	
1	ROM 00C	ROM 011	ROM 022	ROM 033	ROM 042	ROM 055	ROM 066	ROM 077	ROM 088	ROM 099	ROM 0A0	ROM 0B1	ROM 0C2	ROM 0D3	ROM 0E4	RAM 0F5	RAM 106	RAM 117	RAM 128	RAM 139	RAM 14A	RAM 15B	RAM 16C	RAM 17D	RAM 18E
2	ROM 19E	RAM 0A0	RAM 0B1	RAM 0C2	RAM 0D3	RAM 0E4	RAM 0F5	RAM 106	RAM 117	RAM 128	RAM 139	RAM 14A	RAM 15B	RAM 16C	RAM 17D	RAM 18E	RAM 19F	RAM 200	RAM 211	RAM 222	RAM 233	RAM 244	RAM 255	RAM 266	RAM 277
3	RAM 288	RAM 299	RAM 30A	RAM 31B	RAM 32C	RAM 33D	RAM 34E	RAM 35F	RAM 360	RAM 371	RAM 382	RAM 393	RAM 3A4	RAM 3B5	RAM 3C6	RAM 3D7	RAM 3E8	RAM 3F9	RAM 40A	RAM 41B	RAM 42C	RAM 43D	RAM 44E	RAM 45F	RAM 460
4	RAM 471	RAM 482	RAM 493	RAM 4A4	RAM 4B5	RAM 4C6	RAM 4D7	RAM 4E8	RAM 4F9	RAM 50A	RAM 51B	RAM 52C	RAM 53D	RAM 54E	RAM 55F	RAM 560	RAM 571	RAM 582	RAM 593	RAM 5A4	RAM 5B5	RAM 5C6	RAM 5D7	RAM 5E8	RAM 5F9
5	RAM 60A	RAM 61B	RAM 62C	RAM 63D	RAM 64E	RAM 65F	RAM 660	RAM 671	RAM 682	RAM 693	RAM 6A4	RAM 6B5	RAM 6C6	RAM 6D7	RAM 6E8	RAM 6F9	RAM 70A	RAM 71B	RAM 72C	RAM 73D	RAM 74E	RAM 75F	RAM 760	RAM 771	RAM 782
6	RAM 793	RAM 804	RAM 815	RAM 826	RAM 837	RAM 848	RAM 859	RAM 86A	RAM 87B	RAM 88C	RAM 89D	RAM 8AE	RAM 8BF	RAM 8C0	RAM 8D1	RAM 8E2	RAM 8F3	RAM 904	RAM 915	RAM 926	RAM 937	RAM 948	RAM 959	RAM 96A	RAM 97B
7	RAM 98C	RAM 99D	RAM 9AE	RAM 9BF	RAM 9C0	RAM 9D1	RAM 9E2	RAM 9F3	RAM 904	RAM 915	RAM 926	RAM 937	RAM 948	RAM 959	RAM 96A	RAM 97B	RAM 98C	RAM 99D	RAM 9AE	RAM 9BF	RAM 9C0	RAM 9D1	RAM 9E2	RAM 9F3	RAM 904
8	RAM 915	RAM 926	RAM 937	RAM 948	RAM 959	RAM 96A	RAM 97B	RAM 98C	RAM 99D	RAM 9AE	RAM 9BF	RAM 9C0	RAM 9D1	RAM 9E2	RAM 9F3	RAM 904	RAM 915	RAM 926	RAM 937	RAM 948	RAM 959	RAM 96A	RAM 97B	RAM 98C	RAM 99D
9	RAM 9AE	RAM 9BF	RAM 9C0	RAM 9D1	RAM 9E2	RAM 9F3	RAM 904	RAM 915	RAM 926	RAM 937	RAM 948	RAM 959	RAM 96A	RAM 97B	RAM 98C	RAM 99D	RAM 9AE	RAM 9BF	RAM 9C0	RAM 9D1	RAM 9E2	RAM 9F3	RAM 904	RAM 915	RAM 926
10	RAM 937	RAM 948	RAM 959	RAM 96A	RAM 97B	RAM 98C	RAM 99D	RAM 9AE	RAM 9BF	RAM 9C0	RAM 9D1	RAM 9E2	RAM 9F3	RAM 904	RAM 915	RAM 926	RAM 937	RAM 948	RAM 959	RAM 96A	RAM 97B	RAM 98C	RAM 99D	RAM 9AE	RAM 9BF
11	RAM 96A	RAM 97B	RAM 98C	RAM 99D	RAM 9AE	RAM 9BF	RAM 9C0	RAM 9D1	RAM 9E2	RAM 9F3	RAM 904	RAM 915	RAM 926	RAM 937	RAM 948	RAM 959	RAM 96A	RAM 97B	RAM 98C	RAM 99D	RAM 9AE	RAM 9BF	RAM 9C0	RAM 9D1	RAM 9E2
12	RAM 9F3	RAM 904	RAM 915	RAM 926	RAM 937	RAM 948	RAM 959	RAM 96A	RAM 97B	RAM 98C	RAM 99D	RAM 9AE	RAM 9BF	RAM 9C0	RAM 9D1	RAM 9E2	RAM 9F3	RAM 904	RAM 915	RAM 926	RAM 937	RAM 948	RAM 959	RAM 96A	RAM 97B

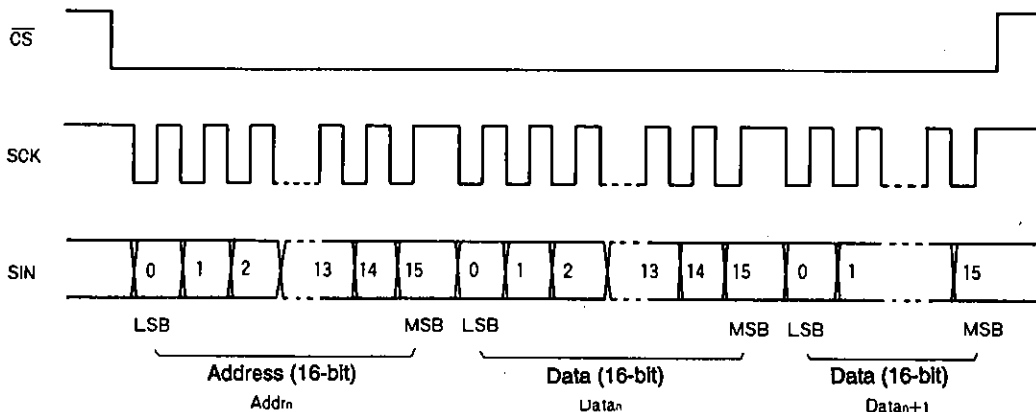
**Input Timing of External Control Data**

Input format is set at 16-bit, serial input for address and data input.

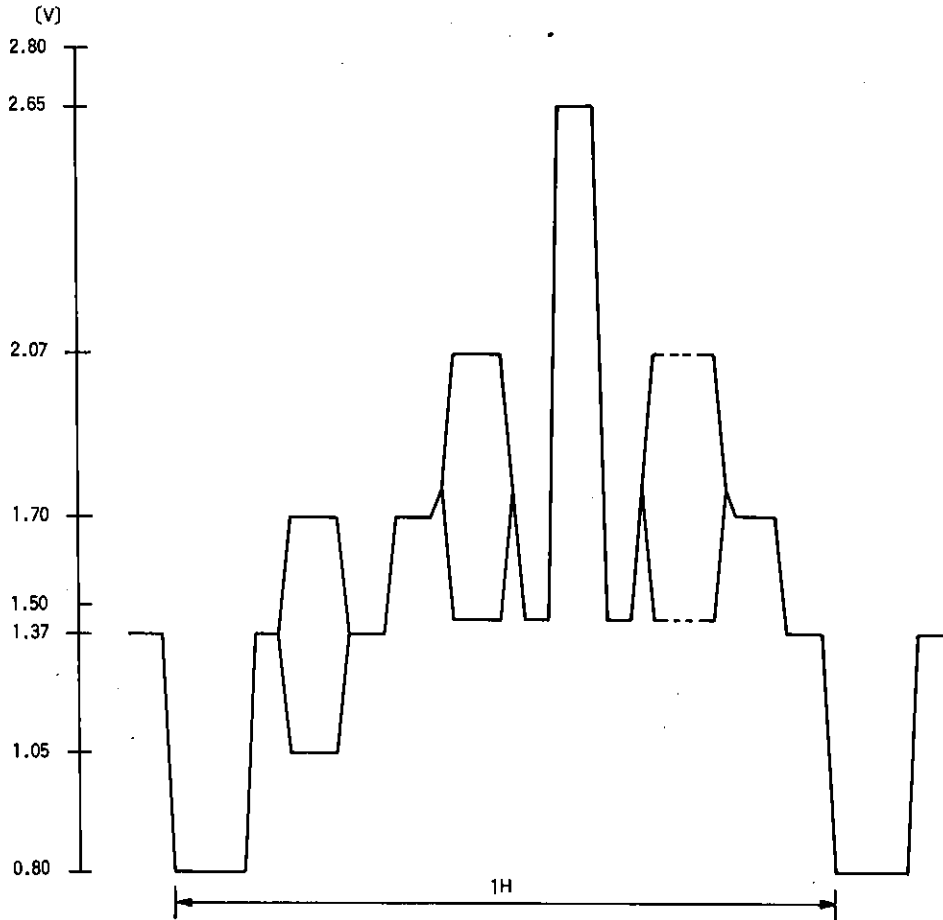
**Address and Data Serial Input**

- ① Address Input with 16-bit Construction
  - Lower 8 bits are reserved for address assignments while the upper 8 bits are fixed to "0".
- ② Data Input with 16-bit Construction
  - Lower 8 bits having addresses 000<sub>HEX</sub> through 0AF<sub>HEX</sub> are reserved for data assignments while the upper 8 bits are fixed to "0".
  - Lower 11 bits having addresses 0B0<sub>HEX</sub> through 0BB<sub>HEX</sub> are reserved for data assignments while the upper 5 bits are fixed to "0".
  - Lower 12 bits having addresses 0BC<sub>HEX</sub> through 0BF<sub>HEX</sub> are reserved for data assignments while the upper 4 bits are fixed to "0".
- ③ Data Input Format
 

After the onset of  $\overline{CS}$ , the first 16 bits are processed as address information, and thereafter information is processed as data in 16-bit units. Addresses are automatically allocated in 16-bit increments.



Composite Video Signal Output Level (Internal generation level: synchronization chip level = 0.8 V)



Output Level	Output Voltage (V <sub>DC</sub> )
Character level	2.650
Background color "H" level	2.075
Burst "L" level	1.700
Background color "L" level	1.500
Trimming level	1.500
Pedestal level	1.375
Burst "L" level	1.050
Synchronization chip level	0.800

V<sub>DD2</sub> = 5.000V<sub>DC</sub>

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