ZXMN6A09K

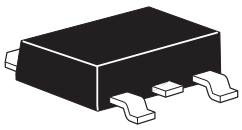
60V N-CHANNEL ENHANCEMENT MODE MOSFET IN DPAK

SUMMARY

$V_{(BR)DSS}$ =60V : $R_{DS(on)}$=0.045Ω; I_D=11.2A

DESCRIPTION

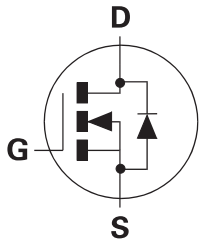
This new generation of Trench MOSFETs from Zetex utilizes a unique structure that combines the benefits of low on-resistance with fast switching speed. This makes them ideal for high efficiency, low voltage power management applications.



DPAK

FEATURES

- Low on-resistance
- Fast switching speed
- Low threshold
- Low gate drive
- D-Pak (T0-252) package



APPLICATIONS

- DC-DC Converters
- Power Management functions
- Disconnect switches
- Motor control

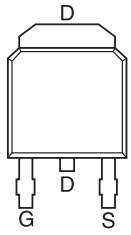
ORDERING INFORMATION

DEVICE	REEL SIZE	TAPE WIDTH	QUANTITY PER REEL
ZXMN6A09KTC	13”	16mm	2500 units

DEVICE MARKING

- ZXMN
  6A09K

PINOUT



TOP VIEW

ABSOLUTE MAXIMUM RATINGS

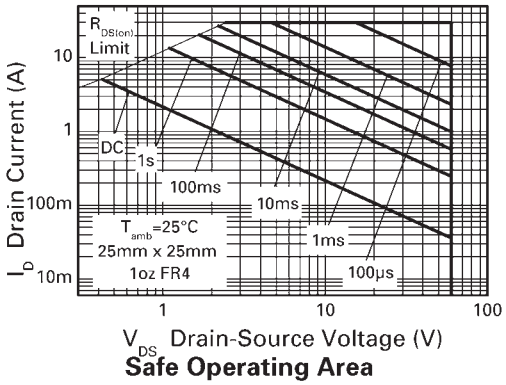
PARAMETER	SYMBOL	LIMIT	UNIT
Drain-source voltage	V_{DSS}	60	V
Gate-source voltage	V_{GS}	±20	V
Continuous drain current @ V_{GS} =10V; T_A=25°C (b) @ V_{GS} =10V; T_A=70°C (b) @ V_{GS} =10V; T_A=25°C (a)	I_D	11.2 9.0 7.3	A
Pulsed drain current (c)	I_{DM}	40	A
Continuous source current (body diode) (b)	I_S	10.8	A
Pulsed source current (body diode) (c)	I_{SM}	40	A
Power dissipation at T_A =25°C (a) Linear derating factor	P_D	4.3 34.4	W mW/°C
Power dissipation at T_A =25°C (b) Linear derating factor	P_D	10.1 80.8	W mW/°C
Power dissipation at T_A =25°C (d) Linear derating factor	P_D	2.15 17.2	W mW/°C
Operating and storage temperature range	T_j, T_{stg}	-55 to +150	°C

THERMAL RESISTANCE

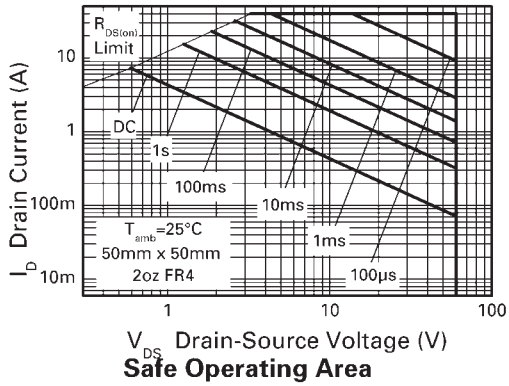
PARAMETER	SYMBOL	VALUE	UNIT
Junction to ambient (a)	$R_{\Theta JA}$	29	°C/W
Junction to ambient (b)	$R_{\Theta JA}$	12.3	°C/W
Junction to ambient (d)	$R_{\Theta JA}$	58	°C/W

NOTES
(a) For a device surface mounted on 50mm x 50mm x 1.6mm FR4 PCB with high coverage of single sided 2oz copper, in still air conditions.
(b) For a device surface mounted on FR4 PCB measured at t ≤ 10 sec.
(c) Repetitive rating 50mm x 50mm x 1.6mm FR4 PCB, D=0.02 pulse width=300μs - pulse width limited by maximum junction temperature.
(d) For a device surface mounted on 50mm x 50mm x 1.6mm FR4 PCB with high coverage of single sided 1oz copper, in still air conditions.

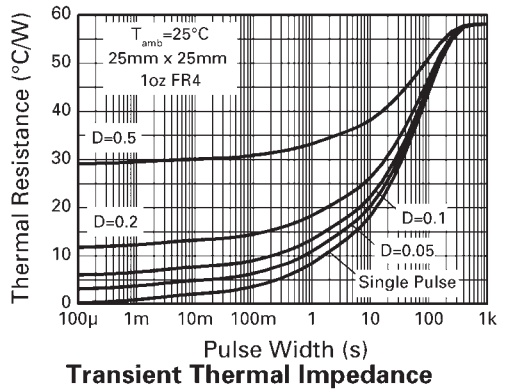
TYPICAL CHARACTERISTICS



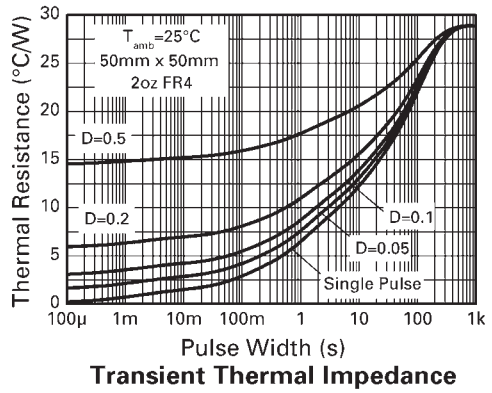
Safe Operating Area



Safe Operating Area



Transient Thermal Impedance



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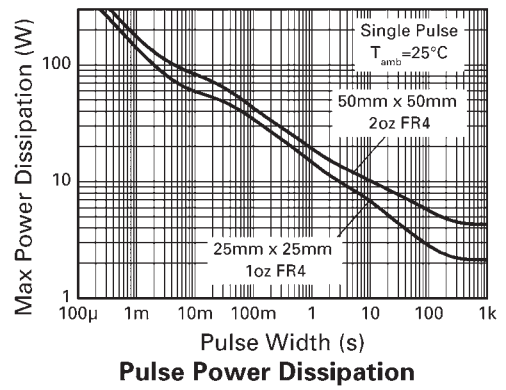
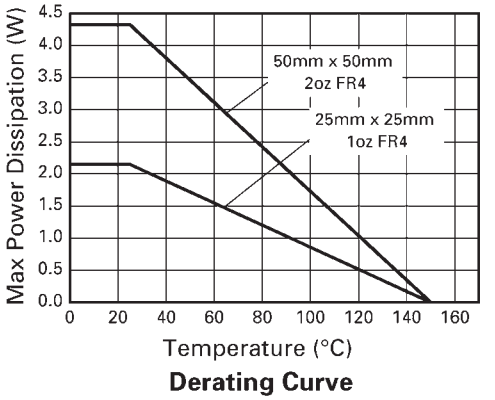


Pulse Power Dissipation



Derating Curve

ELECTRICAL CHARACTERISTICS (at T_{amb} = 25°C unless otherwise stated)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITIONS
STATIC						
Drain-source breakdown voltage	$V_{(BR)DSS}$	60			V	I_D= 250μA, V_{GS}=0V
Zero gate voltage drain current	I_{DSS}			1	μA	V_{DS}= 60V, V_{GS}=0V
Gate-body leakage	I_{GSS}			100	nA	V_{GS}=±20V, V_{DS}=0V
Gate-source threshold voltage	$V_{GS(th)}$	1.0			V	I_D= 250μA, V_{DS}=V_{GS}
Static drain-source on-state resistance (1)	$R_{DS(on)}$			0.045	Ω	V_{GS}= 10V, I_D= 7.3A
				0.070	Ω	V_{GS}= 4.5V, I_D = 5.6A
Forward transconductance (1) (3)	g_{fs}		15		S	V_{DS}= 15V, I_D= 7.3A
DYNAMIC (3)						
Input capacitance	C_{iss}		1426		pF	V_{DS}= 30V, V_{GS}=0V f=1MHz
Output capacitance	C_{oss}		134		pF	
Reverse transfer capacitance	C_{rss}		64		pF	
SWITCHING(2) (3)						
Turn-on-delay time	$t_{d(on)}$		4.8		ns	V_{DD}= 30V, I_D= 1A R_G≅6.0Ω, V_{GS}= 10V (refer to test circuit)
Rise time	t_r		4.6		ns	
Turn-off delay time	$t_{d(off)}$		32.5		ns	
Fall time	t_f		14.5		ns	
Total gate charge	Q_g		15		nC	V_{DS}= 30V, V_{GS}= 4.5V I_D= 5.6A
Total gate charge	Q_g		29		nC	V_{DS}= 30V, V_{GS}= 10V I_D= 7.3A
Gate-source charge	Q_{gs}		7.0		nC	
Gate drain charge	Q_{gd}		4.7		nC	
SOURCE-DRAIN DIODE						
Diode forward voltage (1)	V_{SD}		0.85	0.95	V	T_j=25°C, I_S= 6.6A, V_{GS}=0V
Reverse recovery time (3)	t_{rr}		25.6		ns	T_j=25°C, I_S= 3A, di/dt=100A/μs
Reverse recovery charge (3)	Q_{rr}		26.0		nC	

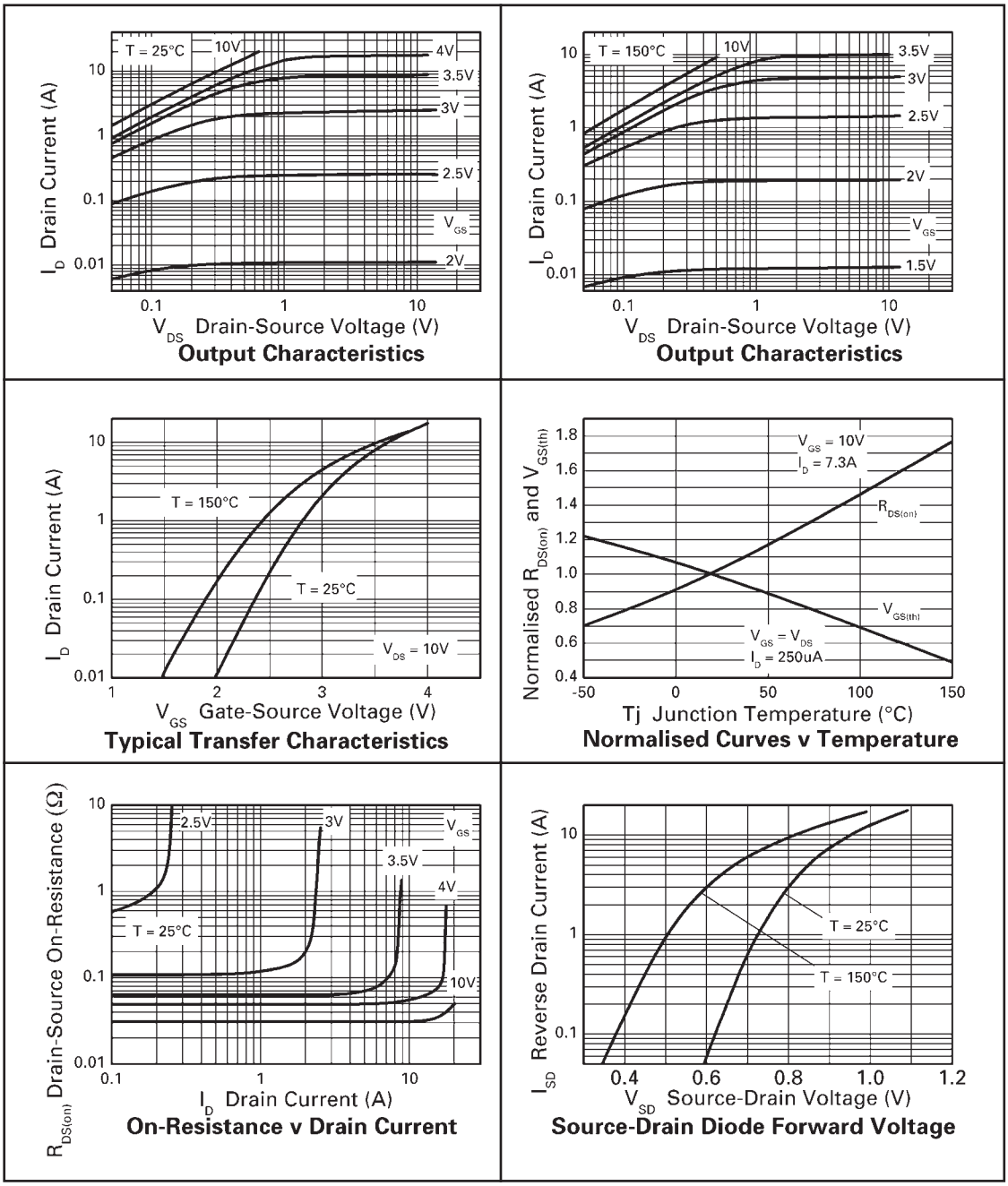
NOTES

(1) Measured under pulsed conditions. Pulse width ≤ 300μs; duty cycle ≤ 2%.

(2) Switching characteristics are independent of operating junction temperature.

(3) For design aid only, not subject to production testing.

TYPICAL CHARACTERISTICS



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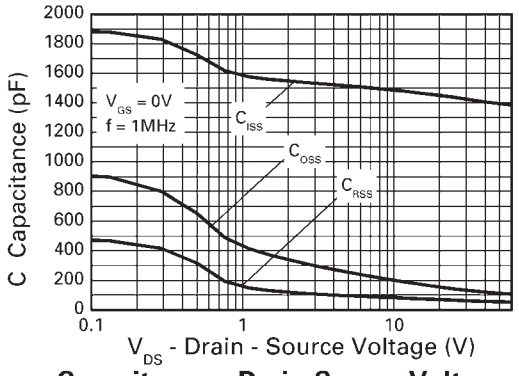
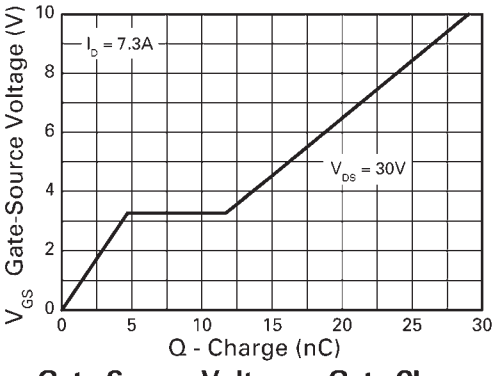
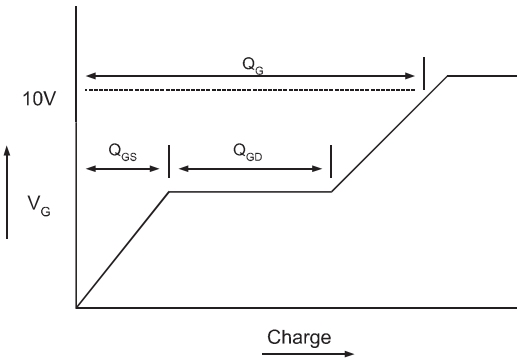


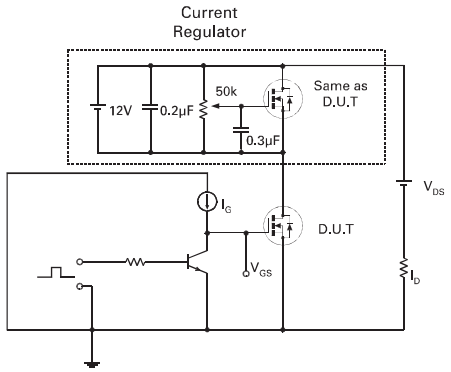
Capacitance v Drain-Source Voltage



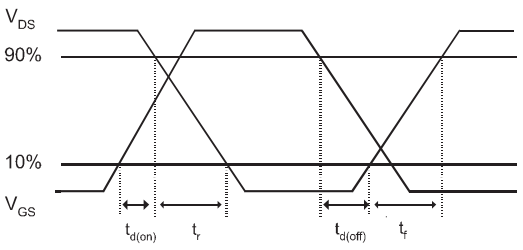
Gate-Source Voltage v Gate Charge



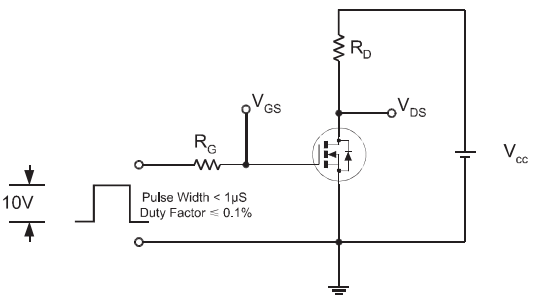
Basic Gate Charge Waveform



Gate Charge Test Circuit

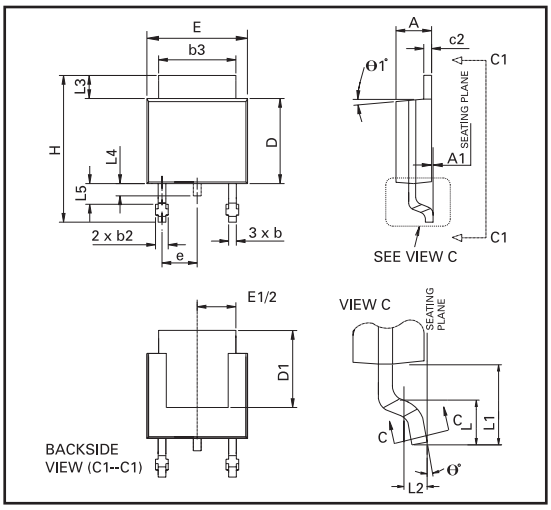


Switching Time Waveforms



Switching Time Test Circuit

PACKAGE OUTLINE



Controlling dimensions are in millimeters. Approximate conversions are given in inches

PACKAGE DIMENSIONS

DIM	Millimeters		Inches		DIM	Millimeters		Inches	
	Min	Max	Min	Max		Min	Max	Min	Max
A	2.18	2.38	0.086	0.094	e	2.30 BSC		0.090 BSC	
A1	—	0.127	—	0.005	H	9.40	10.41	0.370	0.410
b	0.635	0.89	0.025	0.035	L	1.40	1.78	0.055	0.070
b2	0.762	1.114	0.030	0.045	L1	2.74 REF		0.108 REF	
b3	5.20	5.46	0.205	0.215	L2	0.051 BSC		0.020 BSC	
c	0.457	0.609	0.018	0.024	L3	0.89	1.27	0.035	0.050
c2	0.457	0.584	0.018	0.023	L4	0.635	1.01	0.025	0.040
D	5.97	6.22	0.235	0.245	L5	1.14	1.52	0.045	0.060
D1	5.20	—	0.205	—	θ1°	0°	10°	0°	10°
E	6.35	6.73	0.250	0.265	θ°	0°	15°	0°	15°
E1	4.32	—	0.170	—	—	—	—	—	—

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