19-3139; Rev 3; 1/05

Nanopower µP Supervisory Circuits with Manual Reset and Watchdog Timer

General Description

The MAX6854/MAX6855/MAX6856/MAX6858/MAX6860–MAX6869 ultra-low-current (170nA, typ) microprocessor (µP) supervisory circuits combine voltage monitoring, watchdog timer, and manual reset input functions in a 5-pin SOT23 package. These devices assert a reset signal whenever the monitored voltage drops below the factory-trimmed reset threshold voltage, manual reset is asserted, or the watchdog timer expires. The reset output remains asserted for a minimum timeout period after V_{CC} rises above the reset threshold and manual reset is deasserted. Factory-trimmed reset threshold voltages are offered from +1.575V to +4.625V in approximately 100mV increments (see *Threshold Suffix Guide*). Each device is offered with six minimum reset timeout options, ranging from 10ms to 1200ms.

The MAX6854/MAX6855/MAX6856/MAX6858/MAX6860–MAX6869 are offered in a variety of configurations (see the *Selector Guide*). The MAX6854/MAX6855/MAX6856/MAX6861–MAX6869 provide a manual reset input, $\overline{MR}$. The MAX6864–MAX6869 offer a watchdog timer that monitors activity at the WDI input to prevent code execution errors. The MAX6864–MAX6869 offer watchdog timeout options of 3.3s or 209s (typ). The MAX6861/MAX6862/MAX6863 feature a pin-selectable reset delay period of 10ms or 150ms (min). Push-pull active-low, push-pull active-high, and open-drain active-low reset outputs are available.

Applications

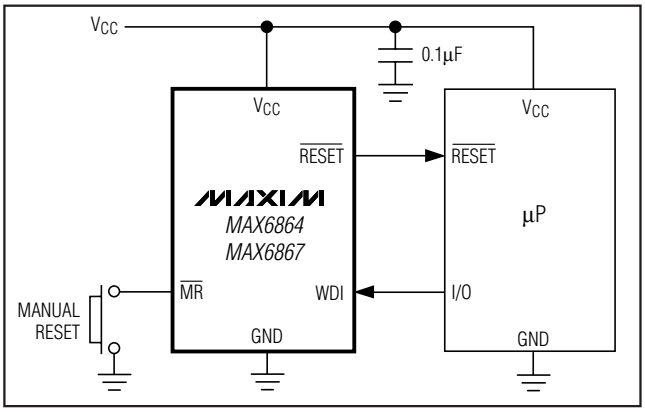
Portable/Battery-Powered Equipment

PDAs/Cell Phones

MP3 Players/Pagers

Glucose Monitors/Patient Monitors

Typical Operating Circuit



Features

- **Ultra-Low 170nA (typ) Supply Current**
- **Reset Thresholds from +1.575V to +4.625V in Approximately 100mV Increments**
- **Six Minimum Reset Timeout Period Options from 10ms to 1200ms**
- **Manual Reset Option**
- **Watchdog Timer Option**
- **Pin-Selectable 10ms/150ms (min) Reset Timeout Period (MAX6861/MAX6862/MAX6863)**
- **Immune to Short V_{CC} Transients**
- **Guaranteed Reset Valid to V_{CC} = +1.1V**
- **Three Reset Output Options:**
  - **Push-Pull $\overline{RESET}$**
  - **Push-Pull RESET**
  - **Open-Drain $\overline{RESET}$**
- **No External Components**
- **Small 5-Pin SOT23 Package**
- **Pin Compatible to the TPS3836/TPS3837/TPS3838 (MAX6861/MAX6862/MAX6863)**

Ordering Information

PART†	TEMP RANGE	PIN-PACKAGE
MAX6854UK_ _D_-T	-40°C to +85°C	5 SOT23-5
MAX6855UK_ _D_-T	-40°C to +85°C	5 SOT23-5

†*Insert reset threshold suffix (see Table 2, Threshold Suffix Guide) after UK. Insert the number corresponding to the desired reset timeout period (see Table 4, Reset Timeout Period) after D.*

Note: *Sample stock is generally held on standard versions only (see Table 5, Standard Versions Table). Standard versions have an order increment of 2500 pieces. Nonstandard versions have an order increment of 10,000 pieces. Contact factory for availability of nonstandard versions.*

Pin Configurations appear at end of data sheet.

Selector Guide appears at end of data sheet.

Ordering Information continued at end of data sheet.

Nanopower µP Supervisory Circuits with Manual Reset and Watchdog Timer

ABSOLUTE MAXIMUM RATINGS

V_{CC}, Open-Drain $\overline{RESET}$ to GND .....-0.3V to +6.0V
$\overline{MR}$, Push-Pull $\overline{RESET}$, RESET,
WDI, CT, I.C.....-0.3V to (V_{CC} + 0.3V)
Input Current, Output Current (all pins).....±20mA
Continuous Power Dissipation (T_A = +70°C)
5-Pin SOT23 (derate 7.1mW/°C above +70°C).....571mW

Operating Temperature Range .....-40°C to +85°C
Junction Temperature .....+150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = 1.2V to 5.5V, T_A = -40°C to +85°C, unless otherwise specified. Typical values are at V_{CC} = 2.5V, T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Supply Voltage	V_{CC}	$T_A \geq 0°C$		1.1		5.5	V
		T_A = -40°C to +85°C		1.2		5.5	
Supply Current	I_{CC}	$V_{CC} > V_{TH}$, no load, reset output deasserted (Note 2)	V_{CC} = 5.0V		210	400	nA
			V_{CC} = 3.3V		190	380	
			V_{CC} = 1.8V		170	370	
		$V_{CC} < V_{TH}$, no load, reset output asserted			7	15	µA
V_{CC} Reset Threshold	V_{TH}	V_{CC} falling (see Table 2)		V_{TH} - 2.5%	V_{TH}	V_{TH} + 2.5%	V
Reset Threshold Hysteresis	V_{HYST}	Reset asserted to reset deasserted			0.5		$\%V_{TH}$
Reset Timeout Period	t_{RP}	$V_{CC} = V_{TH}$ + 150mV (Figures 2 and 3)	D1	10	15	25	ms
			D2	40	60	80	
			D3	150	225	300	
			D4	1200	1800	2400	
			D5	300	450	600	
			D6	600	900	1200	
V_{CC} to Reset Delay	t_{RD}	V_{CC} falling from (V_{TH} + 100mV) to (V_{TH} - 100mV) at 10mV/µs			40		µs
$\overline{RESET}$ Output Voltage	V_{OL}	$V_{CC} \geq$ 1.1V, I_{SINK} = 50µA, $\overline{RESET}$ asserted, $T_A \geq 0°C$				0.3	V
		$V_{CC} \geq$ 1.2V, I_{SINK} = 100µA, $\overline{RESET}$ asserted				0.3	
		$V_{CC} \geq$ 2.12V, I_{SINK} = 1.2mA, $\overline{RESET}$ asserted				0.3	
	V_{OH}	$V_{CC} \geq$ 1.71V, I_{SOURCE} = 200µA, $\overline{RESET}$ deasserted, push-pull $\overline{RESET}$ only		0.8 x V_{CC}			
		$V_{CC} \geq$ 2.38V, I_{SOURCE} = 500µA, $\overline{RESET}$ deasserted, push-pull $\overline{RESET}$ only		0.8 x V_{CC}			
Open-Drain $\overline{RESET}$ Leakage Current	I_{LKG}	$\overline{RESET}$ deasserted				25	nA

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = 1.2V to 5.5V, T_A = -40°C to +85°C, unless otherwise specified. Typical values are at V_{CC} = 2.5V, T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
RESET Output Voltage	V_{OH}	$V_{CC} \geq 1.1V$, I_{SOURCE} = 10µA, RESET asserted, $T_A \geq 0°C$	0.8 x V_{CC}			V
		$V_{CC} \geq 1.2V$, I_{SOURCE} = 10µA, RESET asserted	0.8 x V_{CC}			
		$V_{CC} \geq 1.53V$, I_{SOURCE} = 200µA, RESET asserted	0.8 x V_{CC}			
		$V_{CC} \geq 2.12V$, I_{SOURCE} = 500µA, RESET asserted	0.8 x V_{CC}			
	V_{OL}	$V_{CC} \geq 1.71V$, I_{SINK} = 500µA, RESET deasserted			0.3	
		$V_{CC} \geq 2.38V$, I_{SINK} = 1.2mA, RESET deasserted			0.3	
CT Input Current		CT = GND or V_{CC}			20	nA
CT Input Voltage	V_{IH}		0.8 x V_{CC}			V
	V_{IL}				0.2 x V_{CC}	
MANUAL RESET INPUT						
$\overline{MR}$ Input Voltage	V_{IH}		0.7 x V_{CC}			V
	V_{IL}				0.3 x V_{CC}	
$\overline{MR}$ Minimum Pulse Width	t_{MPW}		1			µs
$\overline{MR}$ Glitch Rejection				200		ns
$\overline{MR}$ to Reset Delay	t_{MRD}			250		ns
$\overline{MR}$ Pullup Resistance			5	10	20	kΩ
WATCHDOG TIMER (MAX6864–MAX6869)						
WDI Input Voltage	V_{IH}		0.7 x V_{CC}			V
	V_{IL}				0.3 x V_{CC}	
WDI Input Current		WDI = GND or V_{CC}			20	nA
WDI Pulse Width	t_{WDI}	(Note 3)	150			ns
Watchdog Timeout Period	t_{WD}	S	1.5	3.3	7.75	s
		L	95	209	487	

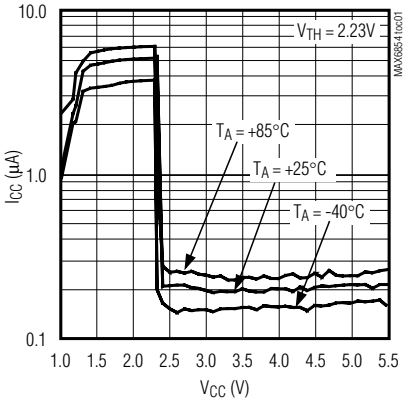
Note 1: Devices are tested at T_A = +25°C. Specifications for T_A = -40°C to +85°C are guaranteed by design.
Note 2: For the MAX6864–MAX6869, the watchdog period is 1s with t_{RISE} and t_{FALL} < 50ns.
Note 3: Guaranteed by design.

Nanopower µP Supervisory Circuits with Manual Reset and Watchdog Timer

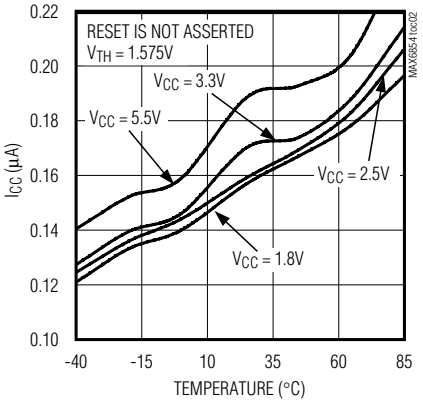
Typical Operating Characteristics

(V_{CC} = +2.5V, T_A = +25°C, unless otherwise noted.)

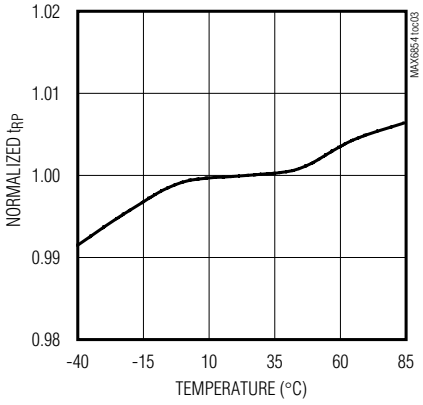
SUPPLY CURRENT vs. SUPPLY VOLTAGE



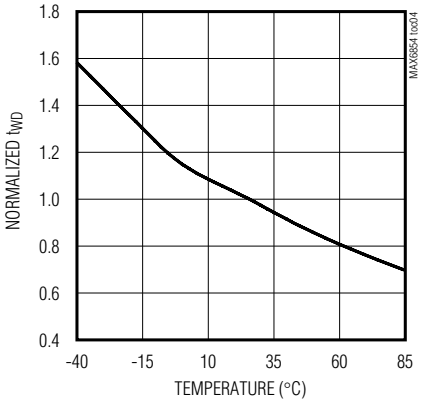
SUPPLY CURRENT vs. TEMPERATURE



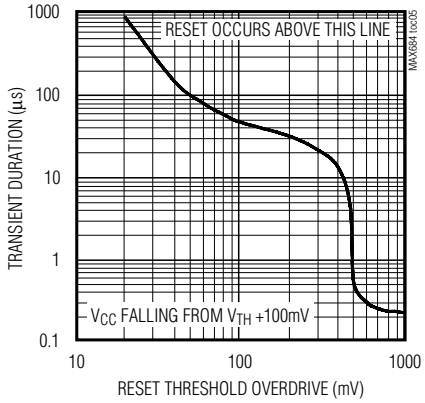
NORMALIZED RESET TIMEOUT PERIOD vs. TEMPERATURE



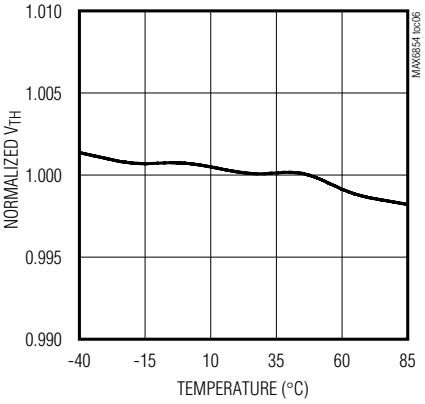
NORMALIZED WATCHDOG TIMEOUT PERIOD vs. TEMPERATURE



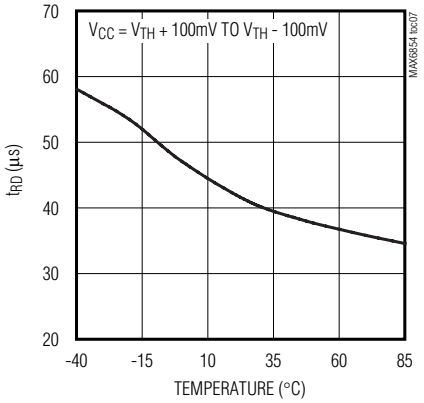
MAXIMUM V_{CC} TRANSIENT DURATION vs. RESET THRESHOLD OVERDRIVE



NORMALIZED RESET THRESHOLD VOLTAGE vs. TEMPERATURE



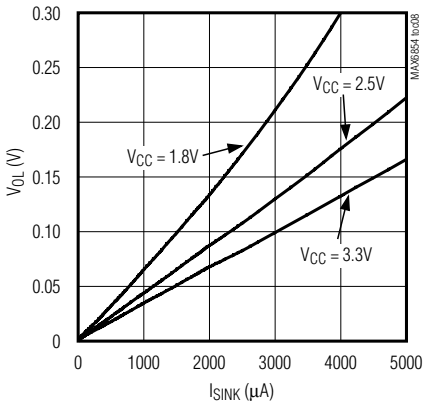
V_{CC} TO RESET DELAY vs. TEMPERATURE



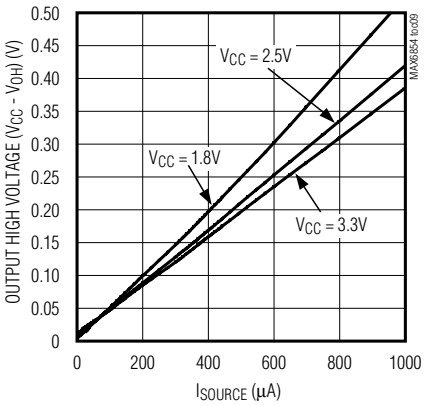
Typical Operating Characteristics (continued)

(V_{CC} = +2.5V, T_A = +25°C, unless otherwise noted.)

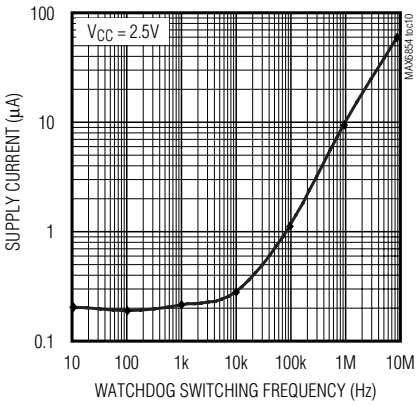
OUTPUT LOW VOLTAGE vs. SINK CURRENT



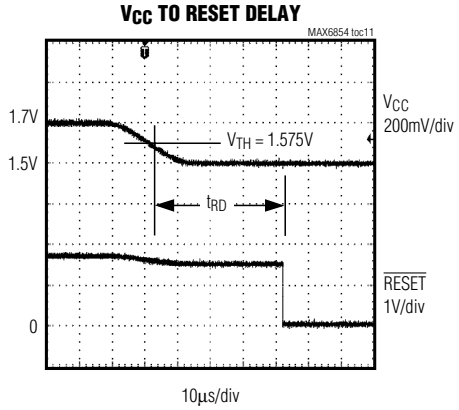
OUTPUT HIGH VOLTAGE vs. SOURCE CURRENT



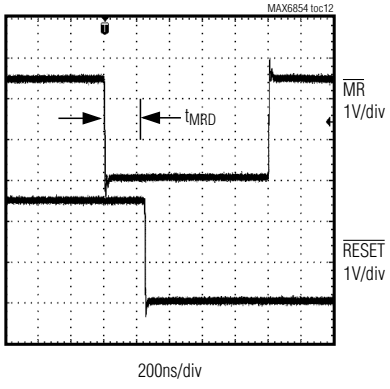
SUPPLY CURRENT vs. WATCHDOG SWITCHING FREQUENCY



VCC TO RESET DELAY



MANUAL RESET DELAY



MAX6854/MAX6855/MAX6856 Pin Description

PIN		NAME	FUNCTION
MAX6854/ MAX6856	MAX6855		
1	—	$\overline{\text{RESET}}$	Active-Low Open-Drain or Push-Pull Reset Output. $\overline{\text{RESET}}$ transitions from high to low when V_{CC} drops below the selected reset threshold or $\overline{\text{MR}}$ is pulled low. $\overline{\text{RESET}}$ remains low for the reset timeout period after V_{CC} exceeds the device reset threshold and $\overline{\text{MR}}$ deasserts. Push-pull $\overline{\text{RESET}}$ outputs are referenced to V_{CC}. Open-drain $\overline{\text{RESET}}$ outputs require an external pullup resistor.
2, 4	2, 4	GND	Ground. Connect all GND inputs to the same potential.
3	3	$\overline{\text{MR}}$	Active-Low Manual Reset Input. Drive $\overline{\text{MR}}$ low to initiate a reset. The reset output remains asserted while $\overline{\text{MR}}$ is held low and for the reset timeout period after $\overline{\text{MR}}$ transitions high. Leave $\overline{\text{MR}}$ unconnected or connect to V_{CC} if unused. $\overline{\text{MR}}$ is internally pulled up to V_{CC} through 10kΩ.
5	5	V_{CC}	Supply Voltage. Input for V_{CC} reset monitor. For noisy systems, bypass V_{CC} with a 0.1µF capacitor to GND.
—	1	RESET	Active-High Push-Pull Reset Output. RESET transitions from low to high when V_{CC} drops below the selected reset threshold or $\overline{\text{MR}}$ is pulled low. RESET remains high for the reset timeout period after V_{CC} exceeds the device reset threshold and $\overline{\text{MR}}$ deasserts. RESET is referenced to V_{CC}.

MAX6858/MAX6860 Pin Description

PIN	NAME	FUNCTION
MAX6858/ MAX6860		
1, 2	I.C.	Internally Connected. For increased noise immunity, connect I.C. to GND.
3	GND	Ground
4	$\overline{\text{RESET}}$	Active-Low Open-Drain or Push-Pull Reset Output. $\overline{\text{RESET}}$ transitions from high to low when V_{CC} drops below the selected reset threshold. $\overline{\text{RESET}}$ remains low for the reset timeout period after V_{CC} exceeds the device reset threshold. Push-pull $\overline{\text{RESET}}$ outputs are referenced to V_{CC}. Open-drain $\overline{\text{RESET}}$ outputs require an external pullup resistor.
5	V_{CC}	Supply Voltage. Input for V_{CC} reset monitor. For noisy systems, bypass V_{CC} with a 0.1µF capacitor to GND.

MAX6861/MAX6862/MAX6863 Pin Description

PIN		NAME	FUNCTION
MAX6861/ MAX6863	MAX6862		
1	1	CT	Reset Timeout Select Input. Connect CT low to select the D1 reset timeout output period (see Tables 1 and 4). Connect CT high (normally V_{CC}) to select the D3 reset timeout period.
2	2	GND	Ground
3	3	$\overline{MR}$	Active-Low Manual Reset Input. Drive $\overline{MR}$ low to initiate a reset. The reset output remains asserted while $\overline{MR}$ is held low and for the reset timeout period after $\overline{MR}$ transitions high. Leave $\overline{MR}$ unconnected or connect to V_{CC} if unused. $\overline{MR}$ is internally pulled up to V_{CC} through 10kΩ.
4	—	$\overline{RESET}$	Active-Low Open-Drain or Push-Pull Reset Output. $\overline{RESET}$ transitions from high to low when V_{CC} drops below the selected reset threshold or $\overline{MR}$ is pulled low. $\overline{RESET}$ remains low for the reset timeout period after V_{CC} exceeds the device reset threshold and $\overline{MR}$ deasserts. Push-pull $\overline{RESET}$ outputs are referenced to V_{CC}. Open-drain $\overline{RESET}$ outputs require an external pullup resistor.
5	5	V_{CC}	Supply Voltage. Input for V_{CC} reset monitor. For noisy systems, bypass V_{CC} with a 0.1µF capacitor to GND.
—	4	RESET	Active-High Push-Pull Reset Output. RESET transitions from low to high when V_{CC} drops below the selected reset threshold or $\overline{MR}$ is pulled low. RESET remains high for the reset timeout period after V_{CC} exceeds the device reset threshold and $\overline{MR}$ deasserts. RESET is referenced to V_{CC}.

MAX6864/MAX6865/MAX6866 Pin Description

PIN		NAME	FUNCTION
MAX6864/ MAX6866	MAX6865		
1	—	$\overline{\text{RESET}}$	Active-Low Open-Drain or Push-Pull Reset Output. $\overline{\text{RESET}}$ transitions from high to low when V_{CC} drops below the selected reset threshold, $\overline{\text{MR}}$ is pulled low, or the watchdog timer expires. $\overline{\text{RESET}}$ remains low for the reset timeout period after V_{CC} exceeds the device reset threshold, $\overline{\text{MR}}$ deasserts, or after the watchog timer expires. Push-pull $\overline{\text{RESET}}$ outputs are referenced to V_{CC}. Open-drain $\overline{\text{RESET}}$ outputs require an external pullup resistor.
2	2	GND	Ground
3	3	$\overline{\text{MR}}$	Active-Low Manual Reset Input. Drive $\overline{\text{MR}}$ low to initiate a reset. The reset output remains asserted while $\overline{\text{MR}}$ is held low and for the reset timeout period after $\overline{\text{MR}}$ transitions high. Leave $\overline{\text{MR}}$ unconnected or connect to V_{CC} if unused. $\overline{\text{MR}}$ is internally pulled up to V_{CC} through 10kΩ.
4	4	WDI	Watchdog Input. If WDI remains high or low for longer than the watchdog timeout period, the internal watchdog timer expires, and a reset is triggered for the reset timeout period. The internal watchdog timer clears whenever reset is asserted, the manual reset is asserted, or WDI sees a rising or falling edge.
5	5	V_{CC}	Supply Voltage. Input for V_{CC} reset monitor. For noisy systems, bypass V_{CC} with a 0.1µF capacitor to GND.
—	1	RESET	Active-High Push-Pull Reset Output. RESET transitions from low to high when V_{CC} drops below the selected reset threshold, $\overline{\text{MR}}$ is pulled low, or the watchdog timer expires. RESET remains high for the reset timeout period after V_{CC} exceeds the device reset threshold, $\overline{\text{MR}}$ deasserts, or after the watchdog timer expires. RESET is referenced to V_{CC}.

MAX6867/MAX6868/MAX6869 Pin Description

PIN		NAME	FUNCTION
MAX6867/ MAX6869	MAX6868		
1	1	WDI	Watchdog Input. If WDI remains high or low for longer than the watchdog timeout period, the internal watchdog timer expires, and a reset is triggered for the reset timeout period. The internal watchdog timer clears whenever reset is asserted, the manual reset is asserted, or WDI sees a rising or falling edge.
2	2	GND	Ground
3	3	$\overline{MR}$	Active-Low Manual Reset Input. Drive $\overline{MR}$ low to initiate a reset. The reset output remains asserted while $\overline{MR}$ is held low and for the reset timeout period after $\overline{MR}$ transitions high. Leave $\overline{MR}$ unconnected or connect to V_{CC} if unused. $\overline{MR}$ is internally pulled up to V_{CC} through 10kΩ.
4	—	$\overline{RESET}$	Active-Low Open-Drain or Push-Pull Reset Output. $\overline{RESET}$ transitions from high to low when V_{CC} drops below the selected reset threshold, $\overline{MR}$ is pulled low, or the watchdog timer expires. $\overline{RESET}$ remains low for the reset timeout period after V_{CC} exceeds the device reset threshold, $\overline{MR}$ deasserts, or after the watchdog timer expires. Push-pull $\overline{RESET}$ outputs are referenced to V_{CC}. Open-drain $\overline{RESET}$ outputs require an external pullup resistor.
5	5	V_{CC}	Supply Voltage. Input for V_{CC} reset monitor. For noisy systems, bypass V_{CC} with a 0.1µF capacitor to GND.
—	4	RESET	Active-High Push-Pull Reset Output. RESET transitions from low to high when V_{CC} drops below the selected reset threshold, $\overline{MR}$ is pulled low, or the watchdog timer expires. RESET remains high for the reset timeout period after V_{CC} exceeds the device reset threshold, $\overline{MR}$ deasserts, or after the watchdog timer expires. RESET is referenced to V_{CC}.

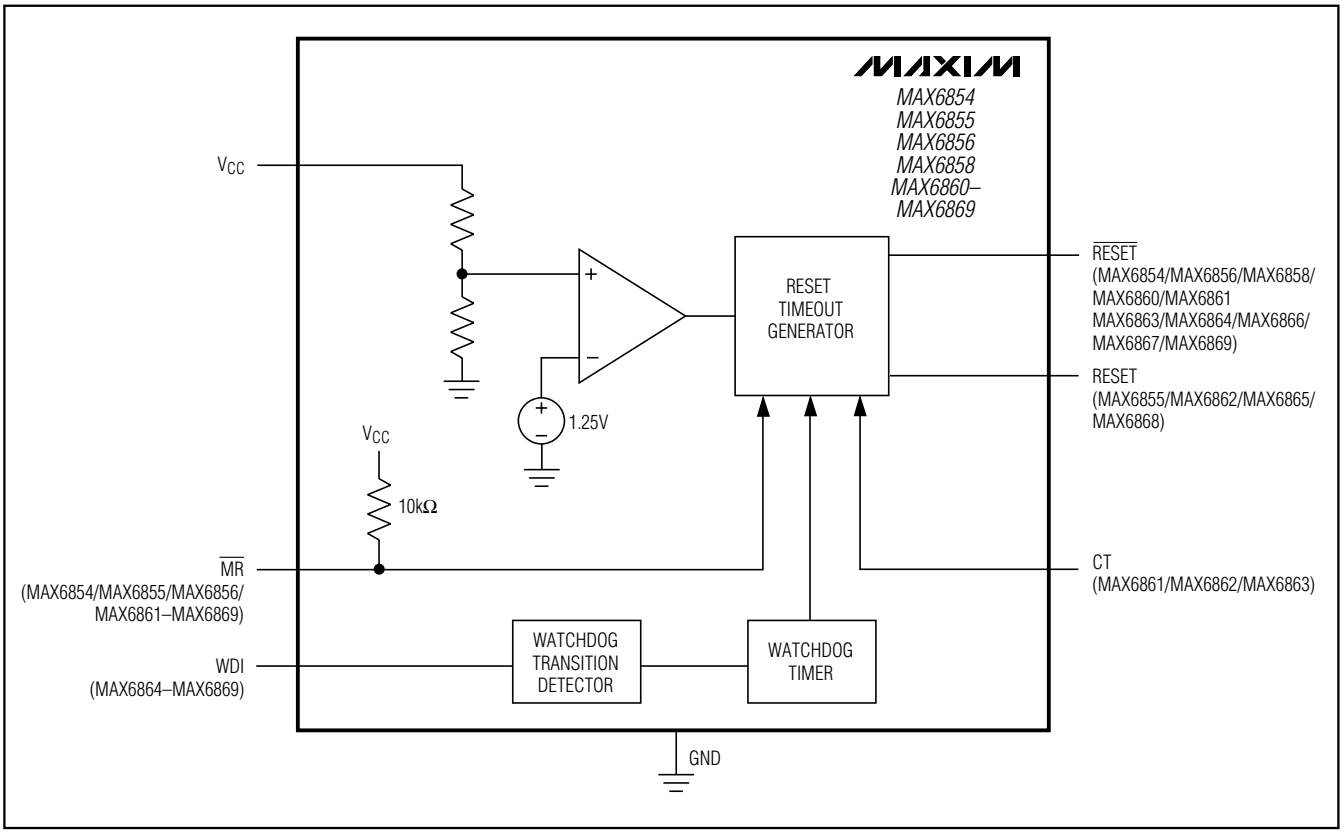


Figure 1. Functional Diagram

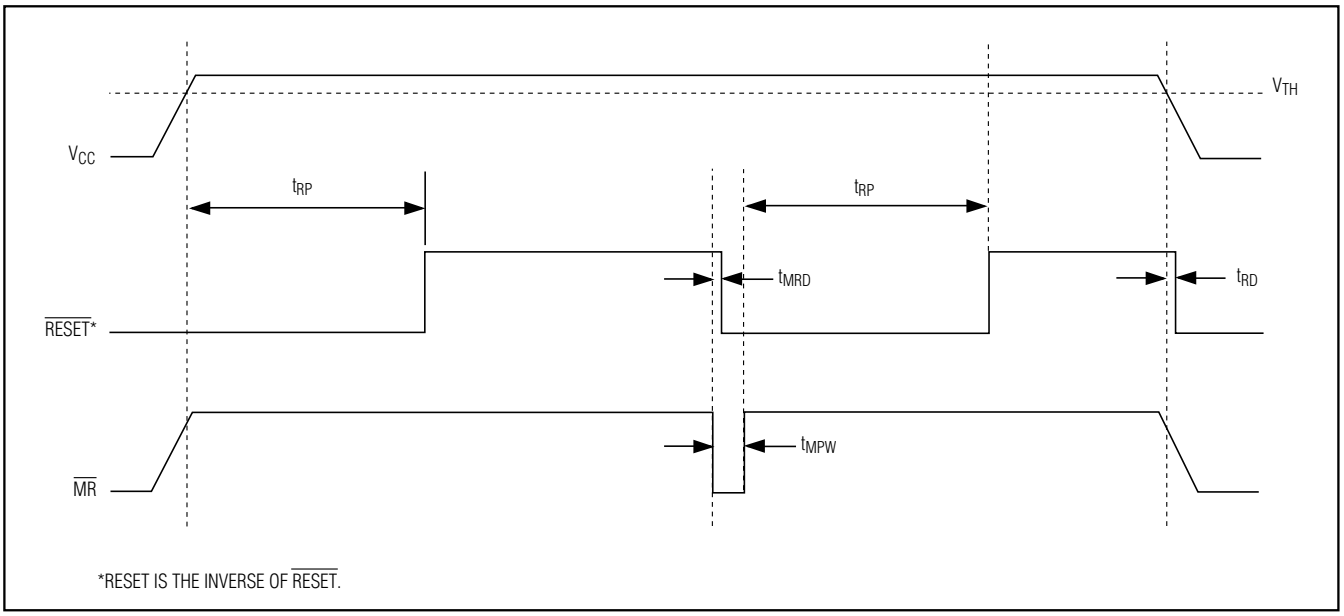


Figure 2. $\overline{\text{RESET}}$ *Timing Relationship*

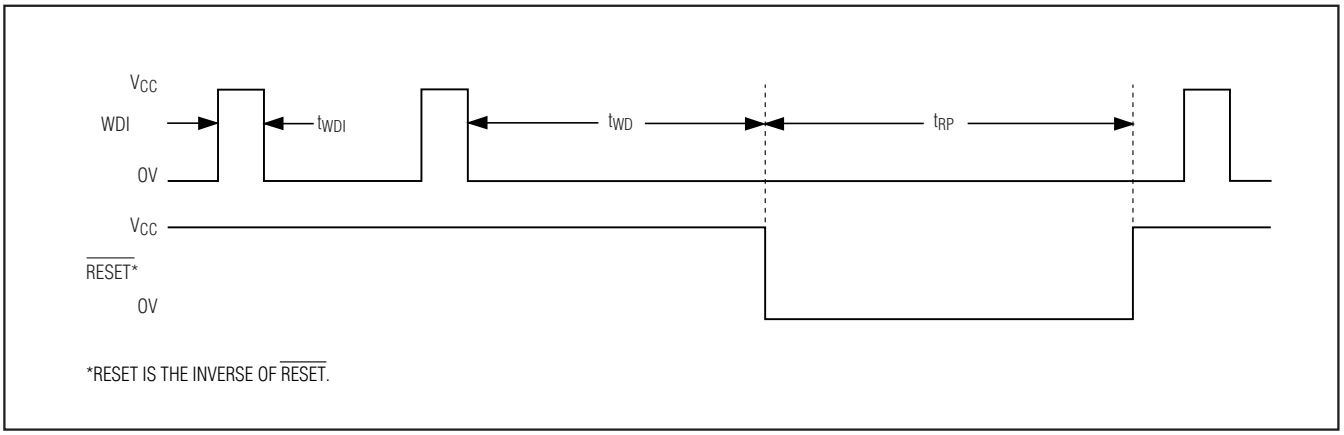


Figure 3. Detailed Watchdog Input Timing Relationship

Detailed Description

RESET/RESET Output

A µP's reset input starts the µP in a known state. The MAX6854/MAX6855/MAX6856/MAX6858/MAX6860–MAX6869 µP supervisory circuits assert a reset to prevent code-execution errors during power-up, power-down, and brownout conditions. The MAX6854/MAX6855/MAX6856/MAX6858/MAX6860–MAX6869 reset output is guaranteed to be valid for V_{CC} down to 1.1V.

Whenever V_{CC} falls below the reset threshold, the reset output asserts low for $\overline{RESET}$ and high for RESET. Once V_{CC} exceeds the reset threshold, an internal timer keeps the reset output asserted for the specified reset timeout period, then after this interval the reset output deasserts (see Figure 2).

Manual Reset Input

Many µP-based products require manual reset capability, allowing the operator, a test technician, or external logic circuitry to initiate a reset. The MAX6854/MAX6855/MAX6856/MAX6861–MAX6869 feature an $\overline{MR}$ input. A logic low on $\overline{MR}$ asserts a reset. Reset remains asserted while $\overline{MR}$ is low and for the timeout period, t_{RP}, after $\overline{MR}$ returns high. The devices provide an internal 10kΩ pullup from $\overline{MR}$ to V_{CC}. Leave $\overline{MR}$ unconnected or connect to V_{CC} if unused. $\overline{MR}$ can be driven with CMOS logic levels or with open-drain/collector outputs. Connect a normally open momentary switch from $\overline{MR}$ to GND to implement a manual reset function; external debounce circuitry is not required. If $\overline{MR}$ is driven by long cables or the device is used in a noisy environment, connect a 0.1µF capacitor from $\overline{MR}$ to GND to provide additional noise immunity.

Watchdog Input

The MAX6864–MAX6869's watchdog timer circuitry monitors the µP's activity. If the µP does not toggle (low-to-high or high-to-low) the watchdog input (WDI) within the watchdog timeout period (t_{WDI}), reset asserts for the reset timeout period (t_{RP}). The internal timer is cleared when reset asserts, when manual reset is asserted, or by a rising or falling edge on WDI. The watchdog input detects pulses as short as 150ns. While reset is asserted the watchdog timer does not count. As soon as reset deasserts, the watchdog timer resumes counting (Figure 3).

Applications Information

Selecting the Reset Timeout Period

The reset timeout period for the MAX6854/MAX6855/MAX6856/MAX6858/MAX6860/MAX6864–MAX6869 is fixed (see Table 4). The MAX6861/MAX6862/MAX6863 feature a reset timeout select input, CT. Connect CT according to Table 1 to select between the available 10ms and 150ms (min) reset timeout periods. The timeout period can be changed while a reset timeout period is in progress, but will not update until the reset timeout period has expired.

Table 1. MAX6861/MAX6862/MAX6863 Reset Timeout Period Selection

CT CONNECTION	MIN	TYP	MAX	UNITS
LOW	10	15	25	ms
HIGH	150	225	300	

Nanopower µP Supervisory Circuits with Manual Reset and Watchdog Timer

Transient Immunity

In addition to issuing a reset to the µP during power-up, power-down, and brownout conditions, the MAX6854/MAX6855/MAX6856/MAX6858/MAX6860–MAX6869 are relatively immune to short-duration supply transients, or glitches. The *Maximum V_{CC} Transient Duration vs. Reset Threshold Overdrive* graph in the *Typical Operating Characteristics* shows this relationship.

The area below the curve of the graph is the region in which these devices typically do not generate a reset pulse. This graph was generated using a falling pulse applied to V_{CC}, starting 100mV above the actual reset threshold, V_{TH}, and ending below this threshold (reset-threshold overdrive). As the magnitude of the transient increases, the maximum allowable pulse width decreases. Typically, a 100mV V_{CC} transient duration of 40µs or less does not cause a reset.

Interfacing to Other Voltages for Logic Compatibility

The open-drain $\overline{RESET}$ output can be used to interface to a µP with other logic levels. As shown in Figure 4, the open-drain output can be connected to voltages from 0 to 5.5V.

Generally, the pullup resistor connected to $\overline{RESET}$ connects to the supply voltage that is being monitored at the IC's V_{CC} input. However, some systems use the open-drain output to level-shift from the monitored supply to reset circuitry powered by another supply voltage. Keep in mind that as the supervisor's V_{CC} decreases, so does the IC's ability to sink current at $\overline{RESET}$.

Ensuring a Valid $\overline{RESET}$ Down to V_{CC} = 0V (Push-Pull $\overline{RESET}$)

When V_{CC} falls below 1.1V, $\overline{RESET}$'s current-sinking capability declines drastically. The high-impedance CMOS logic inputs connected to $\overline{RESET}$ can drift to undetermined voltages. This presents no problems in most applications, since most µPs and other circuitry do not operate with V_{CC} below 1.1V.

In those applications where $\overline{RESET}$ must be valid down to 0, add a pulldown resistor between $\overline{RESET}$ and GND for the MAX6854/MAX6858/MAX6861/MAX6864/MAX6867 push-pull outputs. The resistor sinks any stray leakage currents, holding $\overline{RESET}$ low (Figure 5). Choose a pulldown resistor that accommodates leakages, such that $\overline{RESET}$ is not significantly loaded and is capable of pulling to GND. The external pulldown cannot be used with the open-drain reset outputs.

Watchdog Software Considerations

One way to help the watchdog timer monitor software execution more closely is to set and reset the watchdog

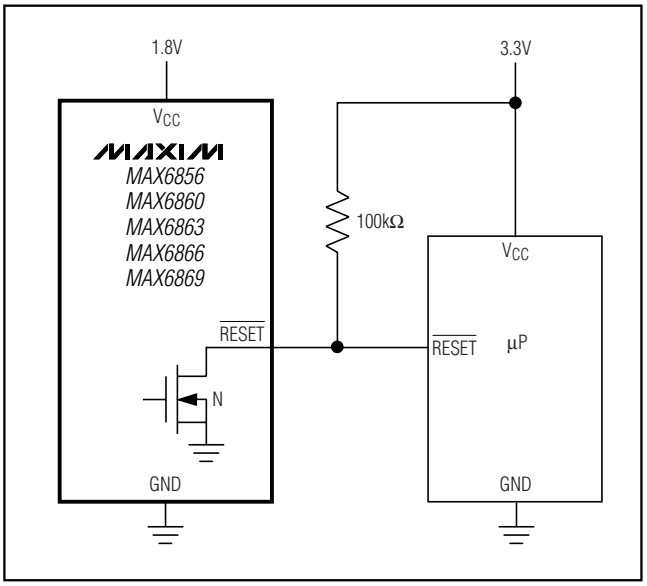


Figure 4. Interfacing with Other Voltage Levels

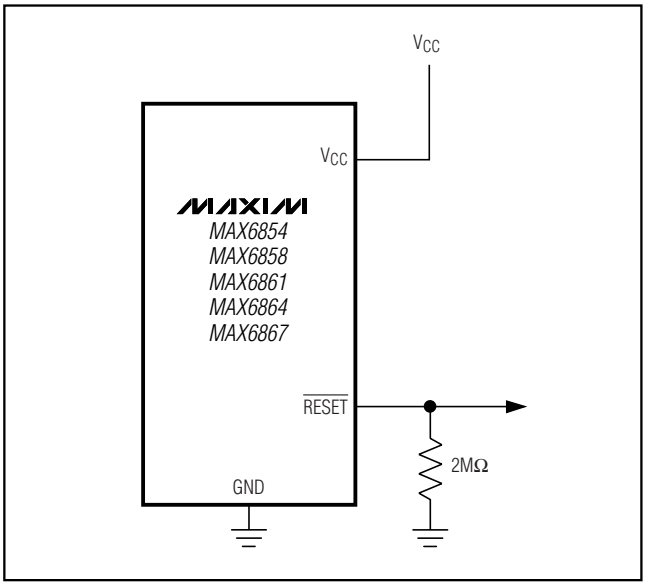


Figure 5. Ensuring $\overline{RESET}$ Valid to V_{CC} = Ground

input at different points in the program, rather than pulsing the watchdog input high-low-high or low-high-low. This technique avoids a stuck loop, in which the watchdog timer would continue to be reset inside the loop, keeping the watchdog from timing out.

Figure 6 shows an example of a flow diagram where the I/O driving the watchdog input is set high at the beginning of the program, set low at the beginning of every subroutine or loop, then set high again when the program returns to the beginning. If the program should hang in any subroutine, the problem would quickly be corrected, since the I/O is continually set low and the watchdog timer is allowed to time out, causing a reset or interrupt to be issued.

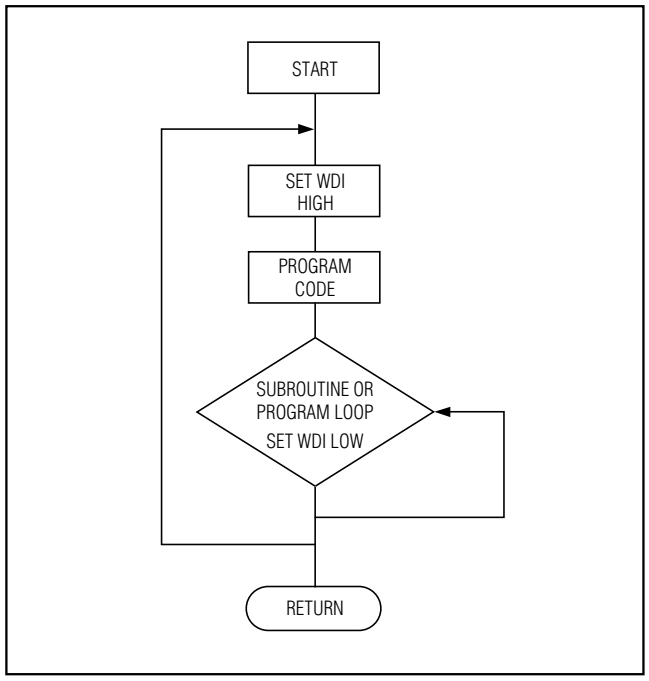


Figure 6. Watchdog Flow Diagram

Table 2. Threshold Suffix Guide

SUFFIX	V_{CC} THRESHOLD FALLING			UNITS
	MIN	TYP	MAX	
46	4.509	4.625	4.741	V
45	4.388	4.500	4.613	
44	4.266	4.375	4.484	
43	4.193	4.300	4.408	
42	4.095	4.200	4.305	
41	3.998	4.100	4.203	
40	3.900	4.000	4.100	
39	3.802	3.900	3.998	
38	3.705	3.800	3.895	
37	3.608	3.700	3.793	
36	3.510	3.600	3.690	
35	3.413	3.500	3.588	
34	3.315	3.400	3.485	
33	3.218	3.300	3.383	
32	3.120	3.200	3.280	
31	2.998	3.075	3.152	
30	2.925	3.000	3.075	
29	2.852	2.925	2.998	
28	2.730	2.800	2.870	
27	2.633	2.700	2.768	
26	2.559	2.625	2.691	
25	2.438	2.500	2.563	
24	2.340	2.400	2.460	
23	2.255	2.313	2.371	
225	2.180	2.235	2.290	
22	2.133	2.188	2.243	
21	2.048	2.100	2.153	
20	1.950	2.000	2.050	
19	1.853	1.900	1.948	
18	1.755	1.800	1.845	
17	1.623	1.665	1.707	
16	1.536	1.575	1.614	

Table 3. Watchdog Timeout

SUFFIX	WATCHDOG TIMEOUT PERIOD			
	MIN	TYP	MAX	UNITS
S	1.5	3.3	7.75	s
L	95	209	487	

Nanopower µP Supervisory Circuits with Manual Reset and Watchdog Timer

Table 4. Reset Timeout Periods

TIMEOUT OPTION	RESET TIMEOUT PERIODS			
	MIN	TYP	MAX	UNITS
D1	10	15	25	ms
D2	40	60	80	
D3	150	225	300	
D4	1200	1800	2400	
D5	300	450	600	
D6	600	900	1200	

Table 5. Standard Versions

PART	TOP MARK
MAX6854UK16D3	AEFS
MAX6854UK23D3	AEFY
MAX6854UK26D3	AEFZ
MAX6854UK29D3	AEGA
MAX6854UK31D3	AEGB
MAX6856UK16D3	AEGR
MAX6856UK23D3	AEGS
MAX6856UK26D3	AEGT
MAX6856UK29D3	AEGU
MAX6856UK31D3	AEGV
MAX6861UK17	AEKO
MAX6861UK225	AEKS
MAX6861UK26	AEKP
MAX6861UK29	AEKQ
MAX6862UK17	AEOS
MAX6862UK225	AEOT
MAX6862UK26	AEOU
MAX6862UK29	AEOV
MAX6863UK17	AEOW
MAX6863UK225	AEOX
MAX6863UK26	AEOY
MAX6863UK29	AEOZ
MAX6864UK16D3S	AEGC
MAX6864UK23D3S	AEGD
MAX6864UK26D3S	AEGE
MAX6864UK29D3S	AEGF
MAX6864UK31D3S	AEGG
MAX6866UK16D3S	AEGW
MAX6866UK23D3S	AEGX
MAX6866UK26D3S	AEGY
MAX6866UK29D3S	AEFT
MAX6866UK31D3S	AEGZ

Ordering Information (continued)

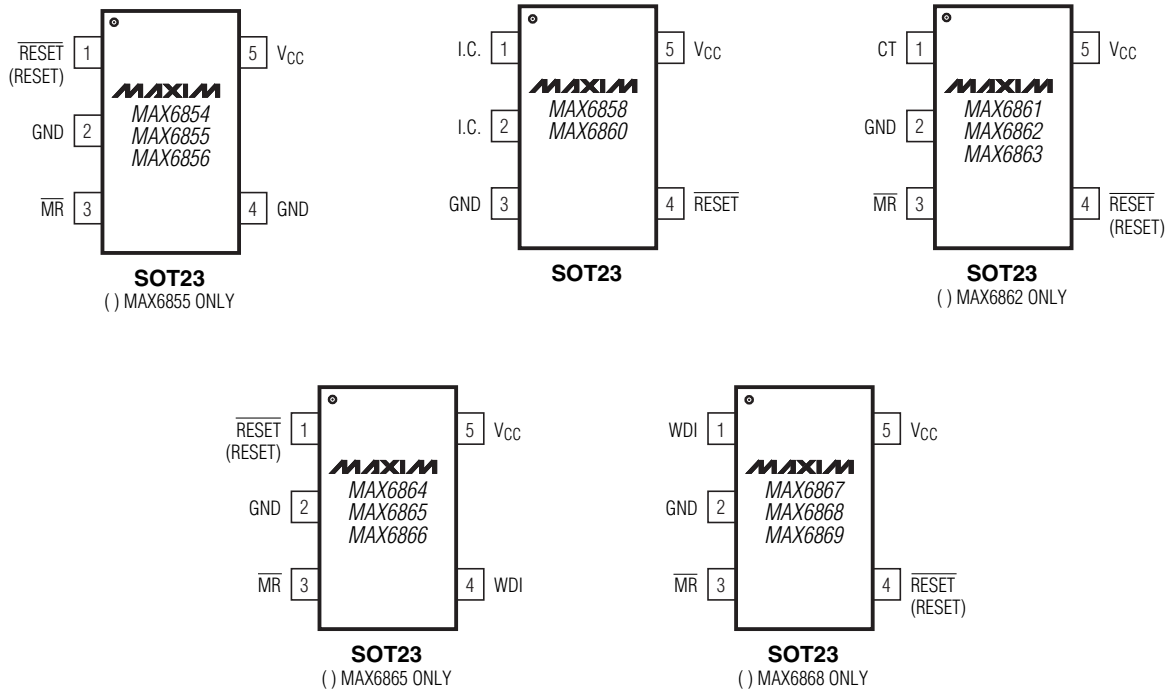
PART†	TEMP RANGE	PIN-PACKAGE
MAX6856UK_ _D_-T	-40°C to +85°C	5 SOT23-5
MAX6858UK_ _D_-T	-40°C to +85°C	5 SOT23-5
MAX6860UK_ _D_-T	-40°C to +85°C	5 SOT23-5
MAX6861UK_ _-T	-40°C to +85°C	5 SOT23-5
MAX6862UK_ _-T	-40°C to +85°C	5 SOT23-5
MAX6863UK_ _-T	-40°C to +85°C	5 SOT23-5
MAX6864UK_ _D_ _-T	-40°C to +85°C	5 SOT23-5
MAX6865UK_ _D_ _-T	-40°C to +85°C	5 SOT23-5
MAX6866UK_ _D_ _-T	-40°C to +85°C	5 SOT23-5
MAX6867UK_ _D_ _-T	-40°C to +85°C	5 SOT23-5
MAX6868UK_ _D_ _-T	-40°C to +85°C	5 SOT23-5
MAX6869UK_ _D_ _-T	-40°C to +85°C	5 SOT23-5

†*Insert reset threshold suffix (see Table 2, Threshold Suffix Guide) after UK. Insert the number corresponding to the desired reset timeout period (see Table 4, Reset Timeout Period) after D. Insert the letter corresponding to the desired watchdog timeout period (S or L, see Table 3) into the blank following the reset timeout period suffix for the MAX6864–MAX6869.*

Note: *Sample stock is generally held on standard versions only (see Table 5, Standard Versions Table). Standard versions have an order increment of 2500 pieces. Nonstandard versions have an order increment of 10,000 pieces. Contact factory for availability of nonstandard versions.*

Pin Configurations

TOP VIEW



SOT23
( ) MAX6855 ONLY

SOT23

SOT23
( ) MAX6862 ONLY

SOT23
( ) MAX6865 ONLY

SOT23
( ) MAX6868 ONLY

Nanopower µP Supervisory Circuits with Manual Reset and Watchdog Timer

Selector Guide

PART	RESET OUTPUT			$\overline{MR}$	WDI	CT
	PUSH-PULL ACTIVE LOW	PUSH-PULL ACTIVE HIGH	OPEN-DRAIN ACTIVE LOW			
MAX6854	√	—	—	√	—	—
MAX6855	—	√	—	√	—	—
MAX6856	—	—	√	√	—	—
MAX6858	√	—	—	—	—	—
MAX6860	—	—	√	—	—	—
MAX6861	√	—	—	√	—	√
MAX6862	—	√	—	√	—	√
MAX6863	—	—	√	√	—	√
MAX6864	√	—	—	√	√	—
MAX6865	—	√	—	√	√	—
MAX6866	—	—	√	√	√	—
MAX6867	√	—	—	√	√	—
MAX6868	—	√	—	√	√	—
MAX6869	—	—	√	√	√	—

Chip Information

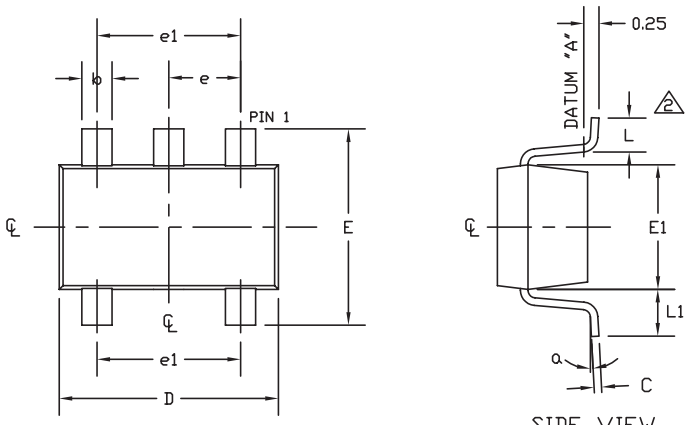
TRANSISTOR COUNT: 2848

PROCESS: BiCMOS

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)

SOT-23 5L .EPS



SYMBOL	MIN	MAX
A	0.90	1.45
A1	0.00	0.15
A2	0.90	1.30
b	0.35	0.50
C	0.08	0.20
D	2.80	3.00
E	2.60	3.00
E1	1.50	1.75
L	0.35	0.60
L1	0.60 REF	
e	0.95 BSC.	
e1	1.90 BSC.	
α	0°	8°

NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. FOOT LENGTH MEASURED AT INTERCEPT POINT BETWEEN DATUM A & LEAD SURFACE.
3. PACKAGE OUTLINE EXCLUSIVE OF MOLD FLASH & METAL BURR. MOLD FLASH, PROTRUSION OR METAL BURR SHOULD NOT EXCEED 0.25 MM.
4. PACKAGE OUTLINE INCLUSIVE OF SOLDER PLATING.
5. MEETS JEDEC MO178, VARIATION AA.
6. LEADS TO BE COPLANAR WITHIN 0.10 mm.
7. SOLDER THICKNESS MEASURED AT FLAT SECTION OF LEAD BETWEEN 0.08mm AND 0.15mm FROM LEAD TIP.

DALLAS SEMICONDUCTOR MAXIM

PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE, SOT-23, 5L

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0057	E	1/1