YAMAHA LSI

YSS216B

KP2

Karaoke Processor 2

■ OUTLINE

YSS216B is an LSI used to carry out digital signal processing for "karaoke" systems.
Using a 256k DRAM connected externally, this LSI executes signal processing such as Key Control, Voice cancel, microphone Echo, and Surround, with easy control.
With A/D and D/A converters integrated, this LSI can handle input and output of analong audio signals in addition to digital audio signals.

■ FEATURES

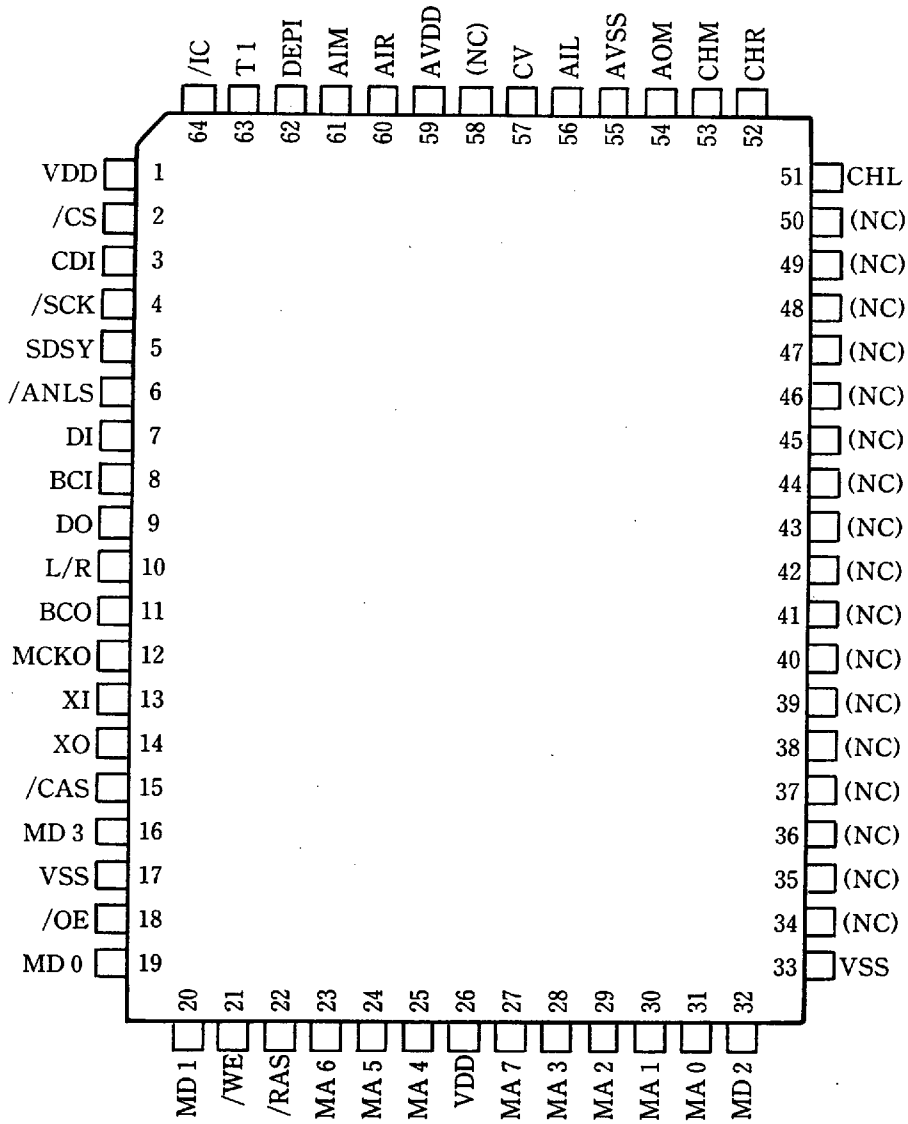
- Built-in 3-channel 15-bit floating A/D converters and 1-channel D/A converter handle audio signals from L, R and microphone channels.
- Digital signals can be input directly, and it is possible to output digital signals to oversampling filter or DACs.
- By YM7110(LVFM) interface, it can handle the digitized LD analog sound signals.
- A 256k(64k*4) DRAM can be connected for external memory.
- De-emphasis processing for digital audio input signals.
- Mixing, fade-in and fade-out processing for digital/analog signals.
- Voice cancel processing for attenuating center-positioned voice.
- Key control processing up to a maximum ±3 whole tone by a quarter tone.
- Microphone echo processing up to a maximum 200ms.
- Surround signal processing with 4 preset patterns.
- Easy control by setting register through the microprocessor serial interface.
- Master clock is 16.9344MHz and sampling frequency is 44.1kHz.
- 5V single power supply, Si-gate C-MOS process.
- 64-pin plastic QFP (YSS216B-F).

YAMAHA CORPORATION

9945524 0002767 628

YSS216B CATALOG
CATALOG No. : LSI-4SS216B3
1995. 10

■ PIN CONFIGURATION



<64pin QFP Top View>

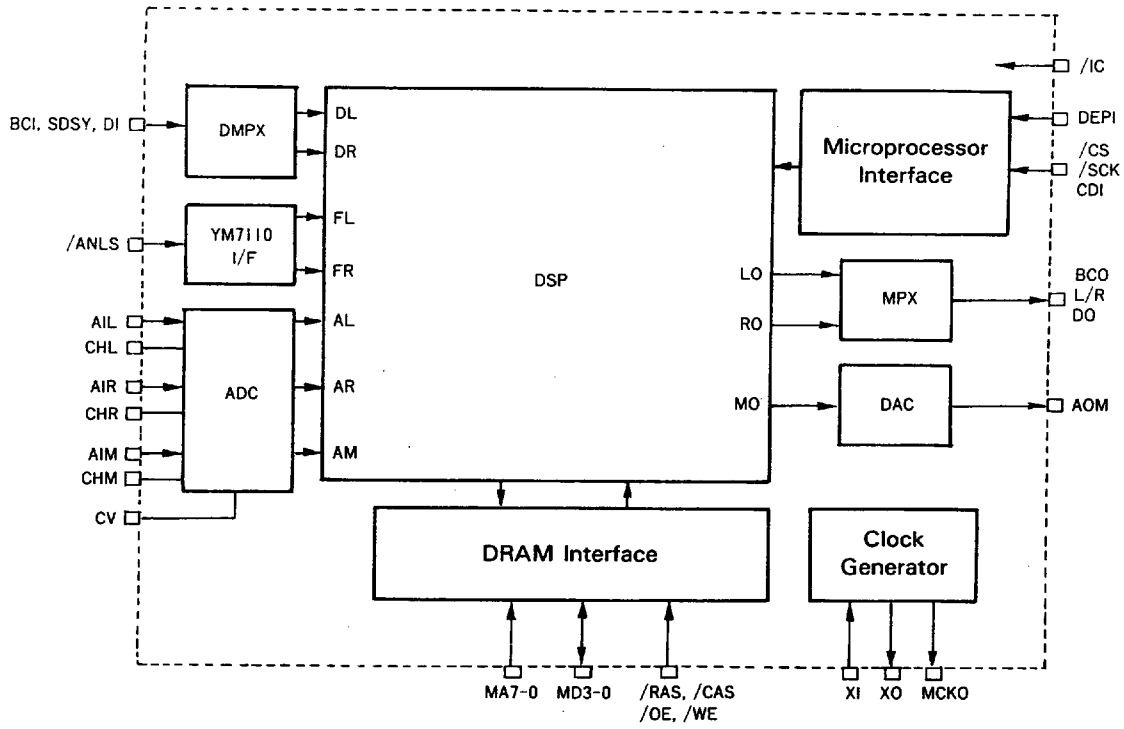
■ PIN DESCRIPTION

No.	Name	I/O	Function
1	VDD	—	+5V power supply (digital block)
2	/CS	I	Microprocessor interface chip select
3	CDI	I	Microprocessor interface serial data
4	/SCK	I	Microprocessor interface serial clock
5	SDSY	I+	Digital audio signal input word clock
6	/ANLS	I+	Digital audio signal input YM7110 data input
7	DI	I+	Digital audio signal input serial data
8	BCI	I+	Digital audio signal input bit clock
9	DO	O	Digital audio signal output serial data
10	L/R	O	Digital audio signal output word clock
11	BCO	O	Digital audio signal output bit clock
12	MCKO	O	Master clock output (16.9344MHz)
13	XI	I	X'tal oscillator connecting terminal, or clock input (16.9344MHz)
14	XO	O	X'tal oscillator connecting terminal
15	/CAS	O	External DRAM interface CAS
16	MD3	I/O	External DRAM interface data 3
17	VSS	—	Ground (digital block)
18	/OE	O	External DRAM interface OE
19	MD0	I/O	External DRAM interface data 0
20	MD1	I/O	External DRAM interface data 1
21	/WE	O	External DRAM interface WE
22	/RAS	O	External DRAM interface RAS
23	MA6	O	External DRAM interface address 6
24	MA5	O	External DRAM interface address 5
25	MA4	O	External DRAM interface address 4
26	VDD	—	+5V power supply (digital block)
27	MA7	O	External DRAM interface address 7
28	MA3	O	External DRAM interface address 3
29	MA2	O	External DRAM interface address 2
30	MA1	O	External DRAM interface address 1
31	MA0	O	External DRAM interface address 0
32	MD2	I/O	External DRAM interface data 2
33	VSS	—	Ground (digital block)
34	(NC)		
:	:		
50	(NC)		

No.	Name	I/O	Function
51	CHL	– A	Sample/hold capacitor connecting terminal of AIL input
52	CHR	– A	Sample/hold capacitor connecting terminal of AIR input
53	CHM	– A	Sample/hold capacitor connecting terminal of AIM input
54	AOM	OA	Analog audio signal MIC channel DAC output
55	AVSS	– A	Ground (ADC, DAC block, connect to VSS, externally)
56	AIL	IA	Analog audio signal L channel ADC input
57	CV	– A	Center voltage of ADC
58	(NC)		
59	AVDD	– A	+5V power supply (ADC, DAC block, connect to VDD externally)
60	AIR	IA	Analog audio signal R channel ADC input
61	AIM	IA	Analog audio signal MIC channel ADC input
62	DEPI	I	De-emphasis control input (H: ON, L: OFF)
63	T1	I+	LSI test terminal (Do not connect.)
64	/IC	I	Initial clear input (low active)

NOTE) I+; Pulled-up input, A; Analog terminal

■ BLOCK DIAGRAM



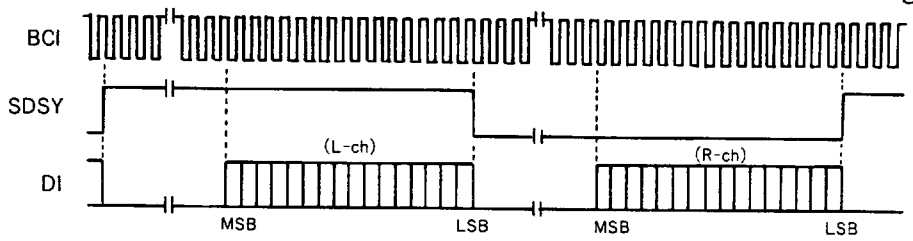
■ FUNCTION DESCRIPTION

1. Clocks XI, XO, MCKO

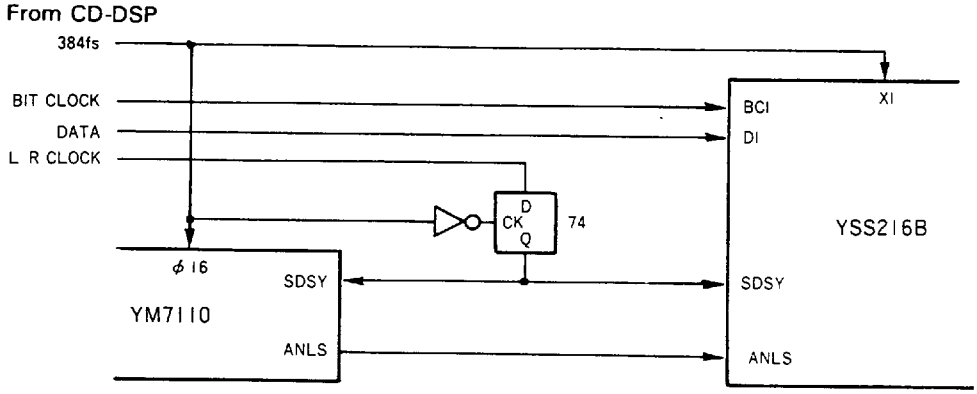
Using XI, XO terminals, X'tal oscillator circuit is constructed.
Oscillating frequency is 16.9344MHz.
Also, external clock can be input to XI terminal.
XI clock is output through MCKO terminal.

2. Digital inputs BCI, SDSY, DI,/ANLS

Digital audio data is input to BCI, SDSY and DI terminals as following format.



BCI, SDSY and DI must be synchronized to XI clock.
/ANLS is YM7110 (LVFM) data input terminal.
Connect as follows.



3. Analog inputs AIL, AIR, AIM, CHL, CHR, CHM, CV

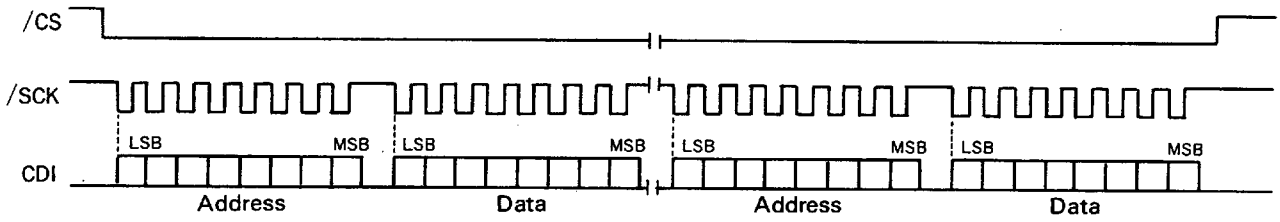
L, R and MIC analog signals are input to AIL, AIR and AIM terminals respectively. Sampling frequency of A/D converter is 44.1kHz.
Connect sample/hold capacitors for A/D conversion to CHL, CHR and CHM terminals.
CV terminal indicates center voltage of A/D converter. Connect a capacitor for stabilizing.
Each analog input signal must be biased by this voltage.
When T1 terminal is set to 'L', noise gates operate for AIL, AIR and AIM channel converters.
In this mode, A/D data are DC-cut by HPF (fc=32Hz), and then processed as follows:

When A/D data>0, data is decreased by 1 from LSB.
When A/D data=0, data is not processed.
When A/D data=0−LSB, data is increased by 1 on LSB.
When A/D data<0−LSB, data is increased by 2 on LSB.

HPF of AIM channel is always at work regardless of setting of T1 terminal.

4. *Microprocessor interface* /CS, /SCK, CDI, DEPI

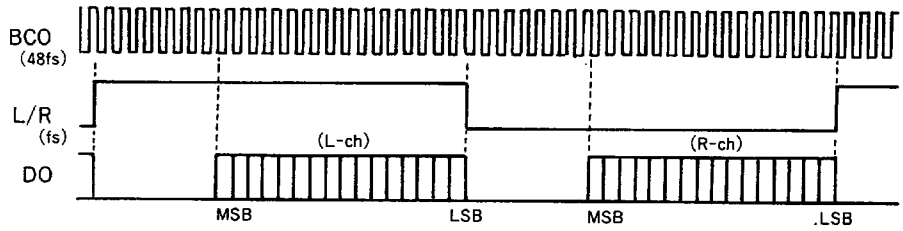
To write data to internal register, this LSI has 8-bit serial interface.
Write register address and data together as following format.



When DEPI is set to 'H', digital inputs undergo de-emphasis processing.
The DEPI signal, logical-summed by bit 1 (de-emphasis ON/OFF) of internal FCR, controls de-emphasis processing.

5. Digital outputs BCO, L/R, DO

After each sound processing, data is output through BCO, L/R and DO terminals as following format.



6. Analog output AOM

AOM is a DAC output terminal of mic echo signal.
Sampling frequency of D/A converter is 44.1kHz.
It outputs voltage output. Connect sample/hold capacitor and execute buffering by using Op-Amp. with high impedance input.

7. DRAM interface MA7~MA0, MD3~MD0, /RAS, /CAS, /WE, /OE

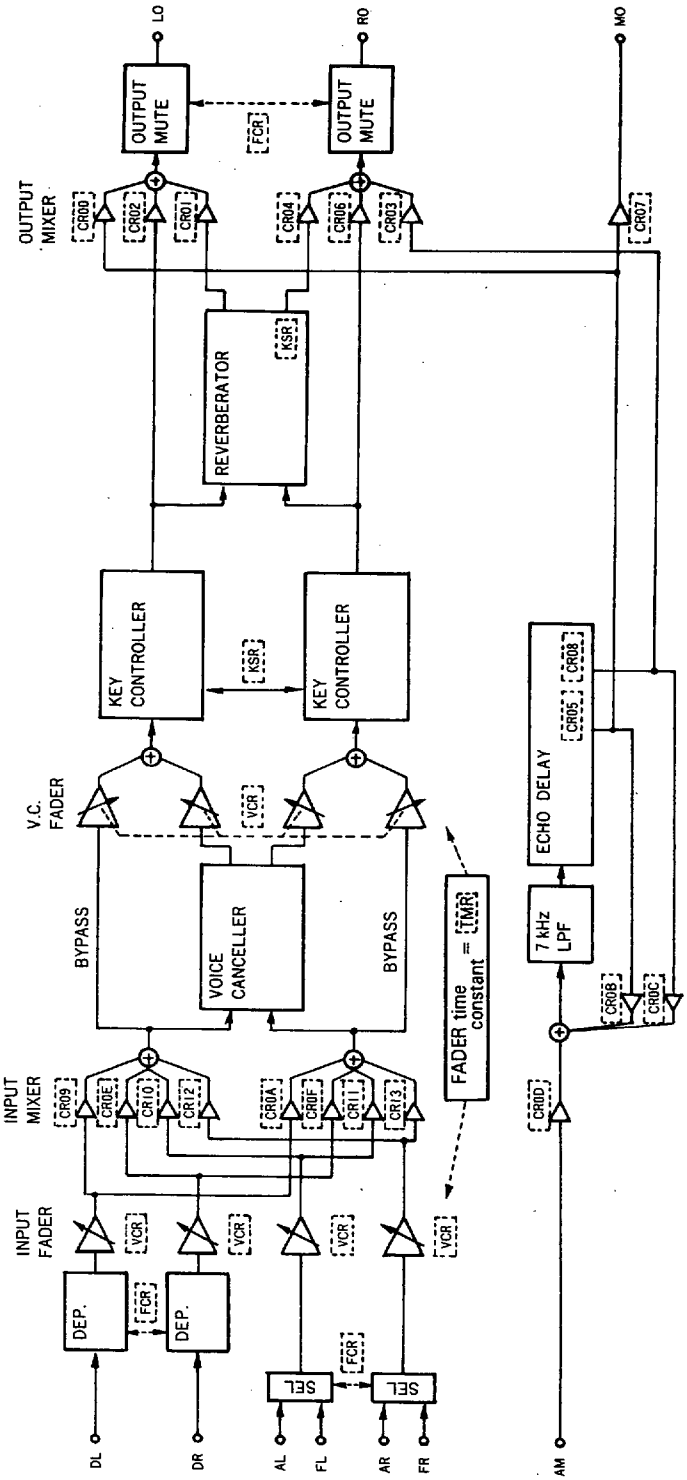
This LSI needs a 256kbit (64k*4-bit) DRAM.
It is used on page mode access.
Use of MB81464-12 (FUJITSU), μPD41464-12 (NEC) or equivalent is recommended.

8. Initial clear /IC

This LSI requires initial clear when turning on the power.

■ CONTROL DESCRIPTION

1. Signal flow



2. *Register description*

Each part of this LSI is controlled by setting data to 24 byte registers as follows.

ADDR HEX	NAME	FUNCTION
$00	FCR	Function control register
$01	KSR	Key, surround control register
$02	VCR	Multi-sound, voice cancel register
$03	TMR	Time constant Register
$20 ↓ $33	CR00 ↓ CR13	Coefficient register (effective only when FCR bit 2=0)

Each block of the signal flow is controlled by the register marked in dotted frame in that block.

- Function control register (FCR)

  This register is for hardware setting.

bit 0 (LSB)	Select ADC data input/YM7110 data input '1'=ADC data input (AIL, AIR) '0'=YM7110 data input (/ANLS)
bit 1	Digital input de-emphasis processing ON/OFF '1'=OFF '0'=ON
bit 2	Select coefficients '1'=preset data used '0'=data set to coefficient registers CR00~CR13 used
bit 3	Output muting ON/OFF '1'=muting OFF (fade-in within 23.2ms) '0'=muting ON (fade-out within 23.2ms)
bit 4	Internal accumulator clear '1'=zero clear '0'=normal
bit 5	Digital audio input synchronizing setting '1'=internal synchronization (when BCI, SDSY and DI not used) '0'=external synchronization (when BCI, SDSY and DI used)
bit 6	Select de-emphasis coefficients '1'=normal (fs=44.1kHz) '0'=CD-I (fs=37.8kHz)
bit 7 (MSB)	don't care.

Note) bit 0~bit 6 are set to '1' when initial clear.

- Key, surround control register (KSR)
  Specify key shift rate of key controller by using lower 5 bits.
  Select surround pattern of reverberator by using upper 2 bits.
  bit 7 (MSB) is "don't care".

bit 4 3 2 1 0	key shift rate	
0 1 1 1 1	9 1/2	up
0 1 1 1 0	1 octave	up
0 1 1 0 1	3 1/2	up
0 1 1 0 0	3	up
0 1 0 1 1	2 3/4	up
0 1 0 1 0	2 1/2	up
0 1 0 0 1	2 1/4	up
0 1 0 0 0	2	up
0 0 1 1 1	1 3/4	up
0 0 1 1 0	1 1/2	up
0 0 1 0 1	1 1/4	up
0 0 1 0 0	1	up
0 0 0 1 1	3/4	up
0 0 0 1 0	1/2	up
0 0 0 0 1	1/4	up
0 0 0 0 0	no effect	

bit 4 3 2 1 0	key shift rate	
1 1 1 1 1	1/4	down
1 1 1 1 0	1/2	down
1 1 1 0 1	3/4	down
1 1 1 0 0	1	down
1 1 0 1 1	1 1/4	down
1 1 0 1 0	1 1/2	down
1 1 0 0 1	1 3/4	down
1 1 0 0 0	2	down
1 0 1 1 1	2 1/4	down
1 0 1 1 0	2 1/2	down
1 0 1 0 1	2 3/4	down
1 0 1 0 0	3	down
1 0 0 1 1	3 1/2	down
1 0 0 1 0	1 octave	down
1 0 0 0 1	7	down
1 0 0 0 0	9 1/2	down

unit: whole tone

This LSI has 4 types of surround patterns.
Each surround effect varies depending on mixing ratio to direct sound, input sources and so on.

bit 6 5	Surround Pattern	Description
0 0	Simulation stereo	Monaural source (L channel) is made pseudo stereophonic.
0 1	Live	Using (L-R) signal, presence is added.
1 0	Movie	Using (L-R) signal, surround effect is emphasized.
1 1	Karaoke	Reverberation is added to (L+R) signal as well.

(Note) Each pattern name and its description are tentative.
All of these patterns use about 50ms delay.

bit 0 ~ bit 6 are set to '0' when initial clear.

- Multi sound, voice cancel control register (VCR)
  Input fader is started by setting lower 4 bits.

bit 3	bit 2	bit 1	bit 0
ANALOG R	ANALOG L	DIGITAL R	DIGITAL L

'1'=fade-in start
'0'=fade-out start

bit 4	Voice cancel fader start setting '1'=cross fade to voice canceler output side '0'=cross fade to bypass side
bit 5 ~ bit 7 (MSB)	don't care.

bit 0~bit 4 are reset to '0' when initial clear.
(then input fader is in fade-out state.)

- Time constant Register (TMR)
  Fade in/out time is set for input fader and voice cancel fader.

bit 7 6 5 4 3 2 1 0	HEX	fading time
1 1 1 1 1 1 1 1	FF	0.09 s
1 1 1 0 1 1 1 0	EE	0.10 s
0 0 1 1 0 0 0 0	30	0.50 s
0 0 0 1 1 0 0 0	18	0.99 s
0 0 0 1 0 0 0 0	10	1.49 s
0 0 0 0 1 1 0 0	0C	1.98 s
0 0 0 0 1 0 0 0	08	2.97 s
0 0 0 0 0 1 1 0	06	3.96 s
0 0 0 0 0 1 0 0	04	5.94 s
0 0 0 0 0 0 1 1	03	7.92 s
0 0 0 0 0 0 0 0	00	23.2ms

As bit 0~bit 7 are reset to '0' when initial clear, be sure to set fading time.

- Coefficient registers (CR00 ~ CR13)

  CR05, CR08 are for setting delay time of mic echo.

  Other registers than these are for setting attenuation value which determines mixing ratio of input and output and feed-back gain of mic echo.

  (1) Delay time setting (CR05, CR08)

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
C_7	C_6	C_5	C_4	C_3	C_2	C_1	0

(Note) bit 0 must be '0'

$$\text{Delay time} = \left(\sum_{N=1}^{7} C_N \times 2^N\right) * \frac{64}{44.1} \text{ [ms]}$$

$$\text{Where} \quad 0 \leqq \sum_{N=1}^{7} C_N \times 2^N \leqq 138$$

(2) Attenuation value setting (CR00 ~ CR04, CR06, CR07, CR09 ~ CR13)

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
C_7	C_6	C_5	C_4	C_3	C_2	C_1	C_0

$$\text{Coefficient value} = (-1) \times C_7 + \sum_{N=0}^{6} C_N \times 2^{N-7}$$

When C7 ~ C0 = 01111111, however, the coefficient value becomes 0.99976 ($\sum_{N=0}^{11} 2^{N-12}$)

(3) Coefficient preset value

This LSI has a set of preset values corresponding to each coefficient register.

When using it, data needs not be sent to the coefficient register. Control is possible only with 4 registers.

Use bit 2 of FCR register to select these preset values or values set in coefficient registers for actual signal processing.

As the state at initial clear is for using preset values (FCR bit 2=1), when using coefficient register values, set the data for coefficient registers and then set FCR bit 2 to "0".

- Coefficient preset values

Coef.	Value	Coef.	Value	Coef.	Value
CR00	00H	CR08	00H	CR10	7FH
CR01	00H	CR09	00H	CR11	00H
CR02	7FH	CR0A	00H	CR12	00H
CR03	00H	CR0B	32H	CR13	7FH
CR04	00H	CR0C	00H		
CR05	68H	CR0D	40H		
CR06	7FH	CR0E	00H		
CR07	7FH	CR0F	00H		

■ ELECTRICAL CHARACTERISTICS

1. Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Power supply voltage	V_{DD}	−0.3 ~ 7.0	V
Input voltage	V_I	−0.3 ~ V_{DD}+0.3	V
Operating temperature	T_{op}	0 ~ 70	°C
Storage temperature	T_{stg}	−50 ~ 125	°C

2. Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power supply voltage	V_{DD}	4.75	5.00	5.25	V
Operating temperature	T_{op}	0	25	70	°C

3. DC Characteristics

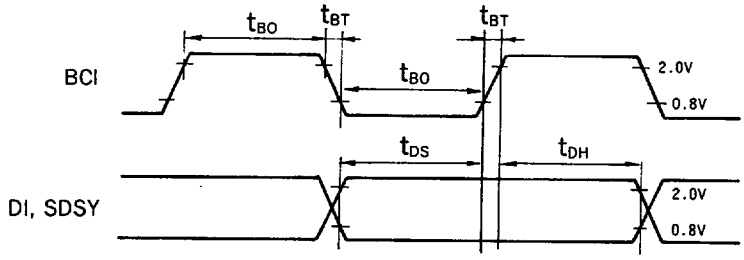
Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Power supply current	I_{DD}	V_{DD}=5.0V			80	mA
Input voltage H level (1)	V_{IH1}	(*1)	2.0			V
Input voltage H level (2)	V_{IH2}	(*2)	3.5			V
Input voltage L level (1)	V_{IL1}	(*1)			0.8	V
Input voltage L level (2)	V_{IL2}	(*2)			0.8	V
Input leakage current	I_{LI}		−10		10	μA
Output voltage H level (1)	V_{OH1}	I_{OH} = −0.4mA (*3)	V_{DD} − 1.0			V
Output voltage H level (2)	V_{OH2}	I_{OH} = −0.4mA (*4)	2.8			V
Output voltage L level	V_{OL}	I_{OL}=1.6mA			0.4	V

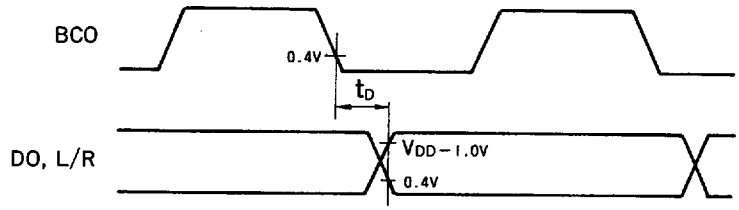
(*1) Applicable to input terminals except XI, /IC, T1.
(*2) Applicable to XI, /IC, T1 terminals.
(*3) Applicable to output terminals except MA0 ~ MA7, /RAS, /CAS, /WE, /OE, MD0 ~ MD3.
(*4) Applicable to MA0 ~ MA7, /RAS, /CAS, /WE, /OE, MD0 ~ MD3 terminals.

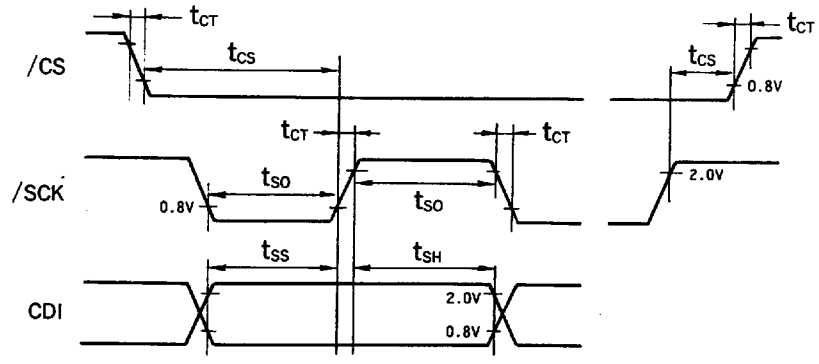
4. AC Characteristics

Parameter		Symbol	Min.	Typ.	Max.	Unit
XI	Input frequency	fc	12.0	16.9344	17.0	MHz
XI	Duty	Rc		50		%
BCI	Frequency	fBC	1.0		4.3	MHz
BCI	ON/OFF time	tBO	100			ns
	Transition time	tBT			20	ns
DI, SDSY	Setup time	tDS	100			ns
	Hold time	tDH	100			ns
DO, L/R	Access time	tD	−20		20	ns
/CS	Setup time	tCS	1/50fs			s
/SCK	ON/OFF time	tSO	1/50fs			s
/CS, /SCK	Transition time	tCT			1/150fs	s
CDI	Setup time	tSS	1/100fs			s
	Hold time	tSH	1/100fs			s

(Note) fs=fc/384





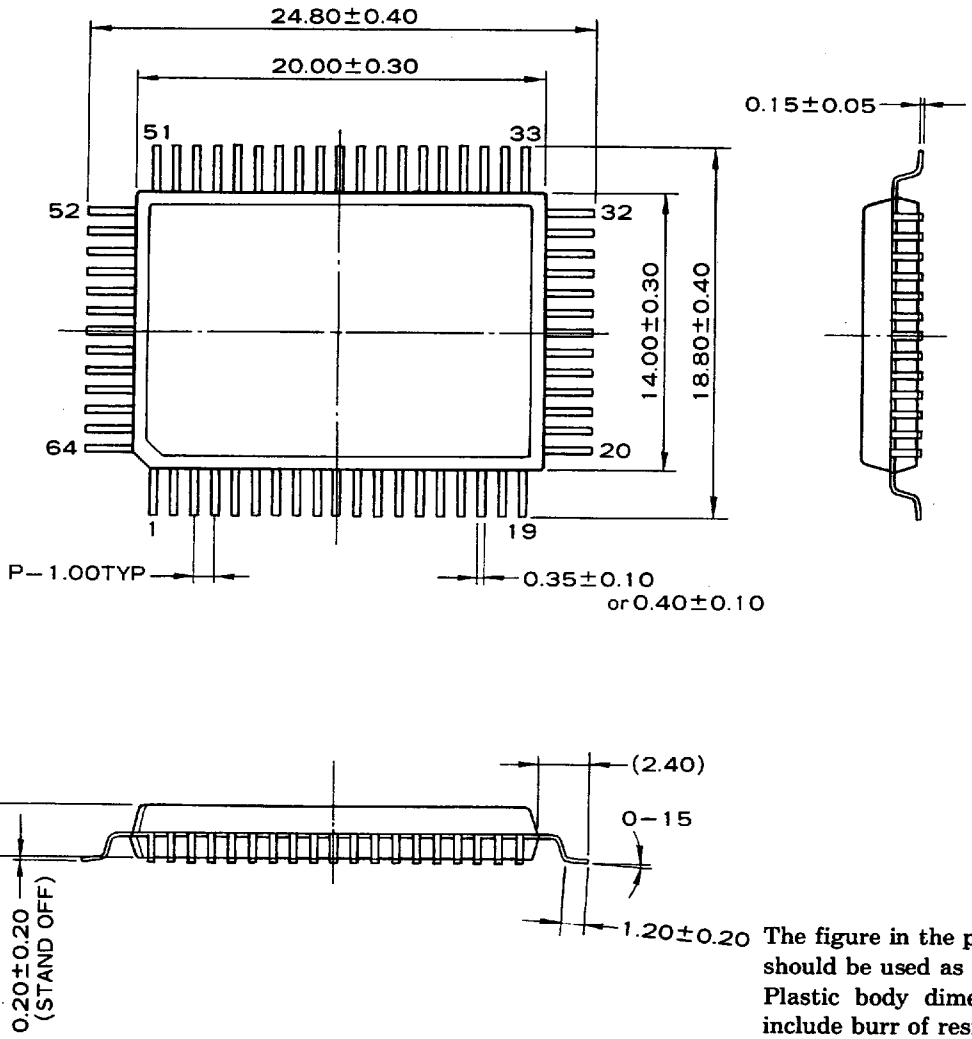


5. **Analog Characteristics** (Condition: Ta=25°C, V_{DD}=5.0V)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Analog input voltage	V_{IA}	(*1)		4.75		V
Analog output voltage	V_{OA}	(*2)		4.75		V
CV terminal voltage	V_C			2.5		V
Total harmonic distortion	THD+N	1kHz, 0dB (*3)		0.5	1.0	%
		1kHz, −30dB (*3)		0.8	1.5	%
Signal to noise ratio	S/N	S=0dB (*3)	73	80		dB

(*1) peak to peak, applicable to AIL, AIR, AIM terminals.
(*2) peak to peak, applicable to AOM terminal.
(*3) when 0dB=4.75Vpp and each A/D input → AOM D/A output through.

■ EXTERNAL DIMENSIONS



The figure in the parenthesis ( ) should be used as a reference.
Plastic body dimensions do not include burr of resin.
UNIT: mm

Note : The LSIs for surface mount need especial consideration on strage and soldering conditions. For detailed information, please contact your nearest agent of yamaha.

Note) The specifications of this product are subject to improvement changes without prior notice.