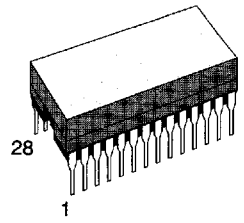
SGS-THOMSON MICROELECTRONICS

MK48Z08,18
MK48Z09,19

S G S-THOMSON

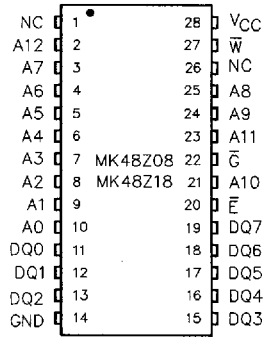
CMOS 8K x 8 ZEROPOWER SRAM

- INTEGRATED ULTRA LOW POWER SRAM, POWER-FAIL CONTROL CIRCUIT AND BATTERY.
- UNLIMITED WRITE-CYCLES.
- READ-CYCLE TIME EQUALS WRITE-CYCLE TIME.
- PREDICTED WORST CASE BATTERY LIFE OF 11 YEARS @ 70°C.
- PIN AND FUNCTION COMPATIBLE WITH JEDEC STANDARD 8K X 8 SRAMS.
- AUTOMATIC POWER-FAIL CHIP DESELECT/WRITE PROTECTION.
- CHOICE OF TWO WRITE PROTECT VOLTAGES :
  - MK48Z08/09 - 4.50V ≤ V_{PFD} ≤ 4.75V
  - MK48Z18/19 - 4.20V ≤ V_{PFD} ≤ 4.50V



PHDIP28 WITH BATTERY TOP HAT (B)

Figure 1. Pin Connections



DESCRIPTION

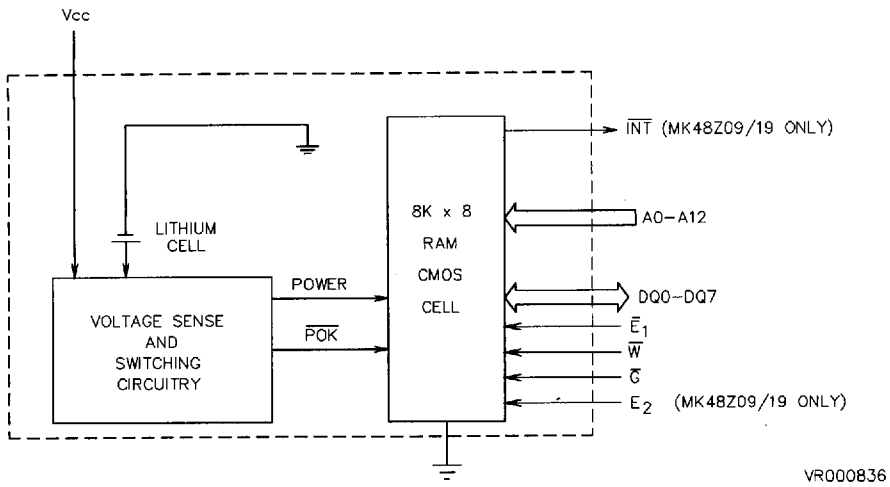
The MK48Z08/18/09/19 ZEROPOWER™ RAM combines an 8K x 8 full CMOS SRAM and a long life lithium carbon mono-fluoride battery in a single plastic DIP package. The MK48Z08/18/09/19 is a Non Volatile, pin and function equivalent to any JEDEC standard 8K x 8 SRAM. It also easily fits into many EPROM and EEPROM sockets, providing the non-volatility of the PROMs without any requirement for special write timing, or limitations on the number of writes that can be performed.

In addition, the MK48Z08/18/09/19 has its own Power-fail Detect circuit. The circuit deselects the device whenever V_{CC} is below tolerance, providing a high degree of data security in the midst of unpredictable system operations brought on by low V_{CC}.

PIN NAMES

A0-A12	Address Inputs
$\overline{E}_1$, E_2	Chip Enables
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable
DQ0-DQ7	Data Inputs/Outputs
$\overline{INT}$	Power Fail Interrupt
V_{CC} / GND	5 Volts / Ground
NC	Not Connected

Figure 2. Block Diagram



TRUTH TABLE (MK48Z08/18)

Vcc	E	G	W	Mode	DQ	Power
< Vcc (max)	VIH	X	X	Deselect	High Z	Standby
	VIL	X	VIL	Write	DIN	Active
> Vcc(min)	VIL	VIL	VIH	Read	DOUT	Active
	VIL	VIH	VIH	Read	High Z	Active
< VPFD (min) > VSO	X	X	X	Deselect	High Z	CMOS Standby
≤ VSO	X	X	X	Deselect	High Z	Battery Back-up

TRUTH TABLE (MK48Z09/19)

Vcc	E1	E2	G	W	Mode	DQ	Power
< Vcc (max)	VIH	X	X	X	Deselect	High Z	Standby
	X	VIL	X	X	Deselect	High Z	Standby
	VIL	VIH	X	VIL	Write	DIN	Active
> Vcc(min)	VIL	VIH	VIL	VIH	Read	DOUT	Active
	VIL	VIH	VIH	VIH	Read	High Z	Active
< VPFD (min) > VSO	X	X	X	X	Deselect	High Z	CMOS Standby
≤ VSO	X	X	X	X	Deselect	High Z	Battery Back-up

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
P_D	Total Power Dissipation	1.0	W
I_{OUT}	Output Current per Pin	20	mA
V_{DD}	Voltage on any Pin Relative to GND	–0.3 to +7.0	V
T_{STG}	Ambient Storage (V_{CC} Off) Temperature	–40 to 85	°C
T_A	Ambient Operating Temperature	0 to 70	°C

Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to the absolute maximum rating conditions for extended periods of time may affect reliability.

***CAUTION** : Negative undershoots below –0.3 volts are not allowed on any pin while in the Battery Back-up mode.*

RECOMMENDED DC OPERATING CONDITIONS ($0°C \le T_A \le 70°C$)

Symbol	Parameter	Min.	Max.	Unit	Notes
V_{CC}	Supply Voltage (MK48Z08/09)	4.75	5.5	V	1
V_{CC}	Supply Voltage (MK48Z18/19)	4.5	5.5	V	1
GND	Supply Voltage	0	0	V	1
V_{IH}	Logic "1" Voltage All Inputs	2.2	V_{CC} + 0.3V	V	1
V_{IL}	Logic "0" Voltage All Inputs	–0.3	0.8	V	1, 2

DC ELECTRICAL CHARACTERISTICS

($0°C \le T_A \le +70°C$; $V_{CC\ min} \le V_{CC} \le V_{CC\ max}$)

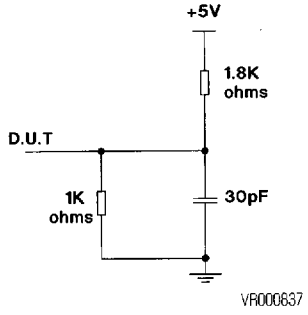
Symbol	Parameter	Min.	Max.	Unit	Notes
I_{CC1}	Average V_{CC} Power Supply Current		80, 125	mA	3, 6
I_{CC2}	TTL Standby Current ($\overline{E}_1 = V_{IH}$ or $E_2 = V_{IL}$)		3	mA	
I_{CC3}	CMOS Standby Current ($\overline{E}_1 = V_{CC}$ –0.2V)		3	mA	4
I_{IL}	Input Leakage Current (Any Input)	–1	1	µA	5
I_{OL}	Output Leakage Current	–5	5	µA	5
V_{OH}	Output Logic "1" Voltage (I_{OUT} = –1.0mA)	2.4		V	
V_{OL}	Output Logic "0" Voltage (I_{OUT} = +2.1mA)		0.4	V	
V_{INT}	$\overline{INT}$ Logic "0" Voltage (I_{OUT} = +0.5mA)		0.4	V	

AC TEST CONDITIONS

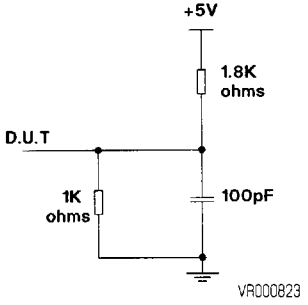
Input Levels	0.0V to 3.0V
Transition Times	5ns
Input and Output Timing Reference Levels	1.5V

OUTPUT LOAD DIAGRAM

MK48Z08-70



MK48Z08,18,09,19



CAPACITANCE

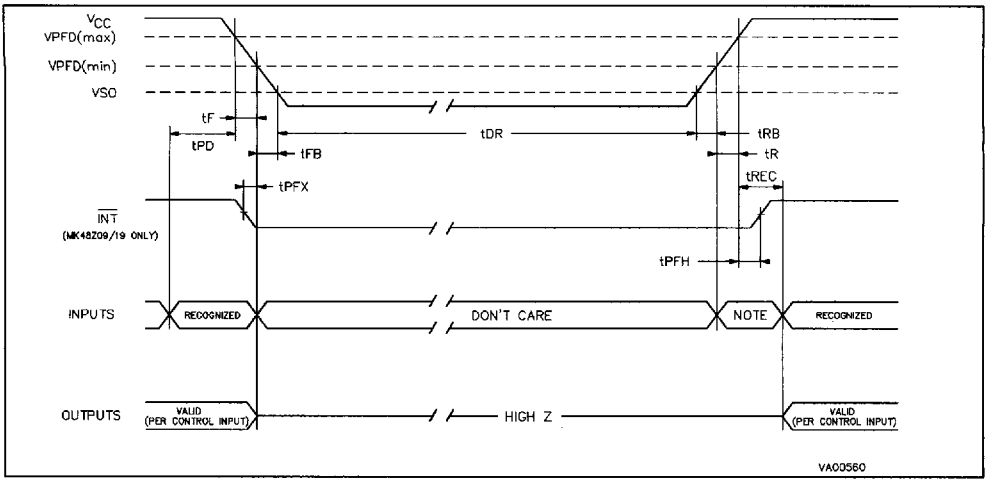
(T_A = 25°C)

Symbol	Parameter	Max.	Unit	Notes
C_I	Capacitance On All Pins (except DQ)	10.0	pF	7
C_Q	Capacitance On DQ Pins	10.0	pF	7, 8

Notes :

1. All voltages referenced to GND.
2. Negative spikes of -1.0 volt allowed for up to 10ns once per Cycle.
3. I_{CC1} measured with outputs open.
4. 1mA typical.
5. Measured with $V_{CC} \geq V_I \geq$ GND and outpus deselected.
6. 80mA@ 100ns, & 125mA @ 70ns.
7. Effective capacitance calculated from the equation $C = I\Delta t/\Delta V$ with ΔV = 3 volts and power supply at 5.0V.
8. Measured with outputs deselected.

Figure 3. Power Down/Up Timing



Note: Inputs may not be recognized at this time. Caution should be taken to keep $\overline{E}_1$ high or E_2 low as V_{CC} rises past V_{PFD}(min). Some systems may perform inadvertent write cycles after V_{CC} rises above V_{PFD}(min)but before normal system operations begins. Even though a power on reset is being applied to the processor a reset condition may not occur until after the system clock is running.

AC ELECTRICAL CHARACTERISTICS (Power Up/Down Timing)

($0°C \le T_A \le +70°C$)

Symbol	Parameter	Min.	Max.	Units	Note
t_{PD}	$\overline{E}_1$ or $\overline{W}$ at V_{IH} or E_2 at V_{IL} before Power Down	0		µs	
t_F	V_{PFD} (max) to V_{PFD} (min) V_{CC} Fall Time	300		µs	2
t_{FB}	V_{PFD} (min) to V_{SO} V_{CC} Fall Time	10		µs	3
t_R	V_{PFD} (min) to V_{PFD} (max) V_{CC} Rise Time	0		µs	
t_{RB}	V_{SO} to V_{PFD} (min) V_{CC} Rise Time	1		µs	
t_{REC}	$\overline{E}_1$ or $\overline{W}$ at V_{IH} or E_2 at V_{IL} after Power Up	1		ms	
t_{PFX}	$\overline{INT}$ Low to Auto Deselect	10	40	µs	
t_{PFH}	V_{PFD} (max) to $\overline{INT}$ High		120	µs	4

DC ELECTRICAL CHARACTERISTICS (Power Up/Down Trip Points)

($0°C \le T_A \le +70°C$)

Symbol	Parameter	Values			Unit	Note
		Min.	Typ.	Max.		
V_{PFD}	Power-fail Deselect Voltage (MK48Z08/09)	4.5	4.6	4.75	V	1
V_{PFD}	Power-fail Deselect Voltage (MK48Z18/19)	4.2	4.3	4.5	V	1
V_{SO}	Battery Back-up Switchover Voltage		3.0		V	1
t_{DR}	Expected Data Retention Time	11			YEARS	

Notes : 1. All voltages referenced to GND.
2. V_{PFD} (max) to V_{PFD} (min) fall time of less than t_F may result in deselection/write protection not occurring until 200 µs after V_{CC} passesV_{PFD} (min).
3. V_{PFD} (min) to V_{SO} fall time of less than t_{FB} may cause corruption of RAM data.
4. INT may go high anytime after V_{CC} exceeds V_{PFD} (min) and is guaranteed to go high t_{PFH} after V_{CC} exceeds V_{PFD} (max).

READ MODE

The MK48Z08/18/09/19 is in the Read Mode whenever $\overline{W}$ (Write Enable) is high, $\overline{E}_1$(Chip Enable 1) is low, and E_2(Chip Enable 2) is high (MK48Z09/19). The device architecture allows ripple-through access of data from eight of 65,536 locations in the static storage array. Thus, the unique address specified by the 13 Address Inputs defines which one of the 8,192 bytes of data is to be accessed. Valid data will be available at the Data I/O pins within t_{AVQV} after the last address input signal is stable, providing that the Chip Enable and Output Enable access times are satisfied.

If Chip Enable or Output Enable access times are not yet met, valid data will be available at the latter of Chip Enable Access Time (t_{ELQV}) or at Output Enable Access Time (t_{GLQV}). The state of the eight three-state Data I/O signals is controlled by Chip Enable and Output Enable. If the Outputs are activated before t_{AVQV}, the data lines will be driven to an indeterminate state until t_{AVQV}. If the Address Inputs are changed while Chip Enable and Output Enable remain low, output data will remain valid for Output Hold from Address (t_{AXQX}) but will go indeterminate until the next Address Access.

AC ELECTRICAL CHARACTERISTICS (Read Cycle)

($0°C \le T_A \le +70°C$; $V_{CC\ min} \le V_{CC} \le V_{CC\ max}$)

Symbol	Parameter	MK48Z08-70		MK48Zxx-10		Unit	Note
		Min.	Max.	Min.	Max.		
t_{E1LQX}	Chip Enable 1 to Q Low-Z	10		10		ns	
t_{E2HQX}	Chip Enable 2 to Q Low-Z	10		10		ns	
t_{AXQX}	Output Hold from Address	5		5		ns	
t_{GLQX}	Output Enable to Q Low-Z	5		5		ns	
t_{AVAV}	Read Cycle Time	70		100		ns	
t_{AVQV}	Address Access Time		70		100	ns	
t_{E1LQV}	Chip Enable 1 Access Time		70		100	ns	
t_{E2HQV}	Chip Enable 2 Access Time		70		100	ns	
t_{GLQV}	Output Enable Access Time		20		50	ns	
t_{E1HQZ}	Chip Enable 1 to Q High-Z		20		50	ns	
t_{E2LQZ}	Chip Enable 2 to Q High-Z		20		50	ns	
t_{GHQZ}	Output Disable to Q High-Z		15		40	ns	

Figure 4. Read Timing n° 1 (Address Access)

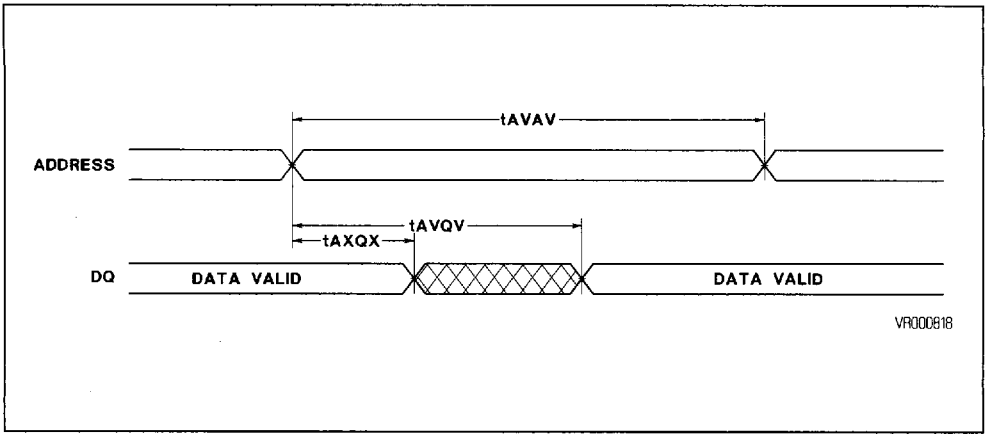
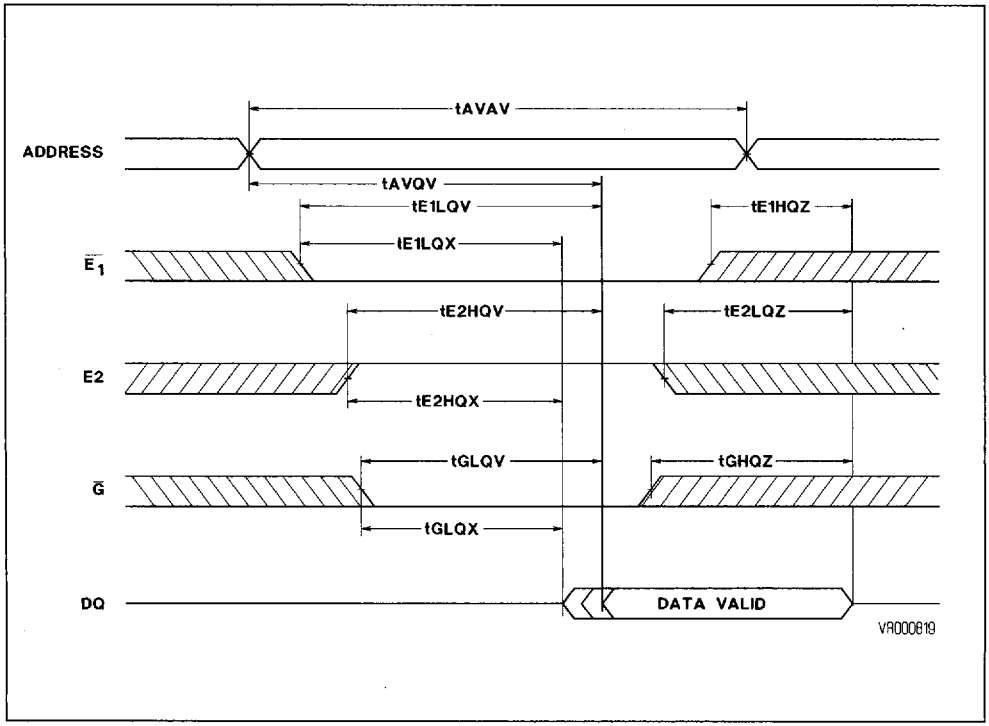


Figure 5. Read Timing n° 2



WRITE MODE

The MK48Z08/18/09/19 is in the Write Mode whenever Write Enable and Chip Enable are active. The start of a write is referenced to the latter occurring falling edge of $\overline{W}$ or $\overline{E}_1$ or rising edge of E_2 (MK48Z09/19). A write is terminated by the earlier rising edge of $\overline{W}$ or $\overline{E}_1$, or the falling edge of E_2 (MK48Z09/19). The addresses must be held valid throughout the cycle. $\overline{E}_1$ or $\overline{W}$ must return high or E_2 low for minimum of t_{E1HAX} or t_{E2LAX} prior to the initiation of another read or write cycle. Data-in must be valid t_{DVWH} prior to the end of write and remain valid for t_{WHDX} afterwards.

Because $\overline{G}$ is a Don't Care in the Write Mode and a low on $\overline{W}$ will return the outputs to High-Z, $\overline{G}$ can be tied low and two-wire RAM control can be implemented. A low on $\overline{W}$ will disable the outputs t_{WLQZ} after $\overline{W}$ goes low. Take care to avoid bus contention when operating with two-wire control.

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AC ELECTRICAL CHARACTERISTICS (Write Cycle)

($0°C \leq T_A \leq +70°C$; $V_{CC\ min} \leq V_{CC} \leq V_{CC\ max}$)

Symbol	Parameter	MK48Z08-70		MK48Zxx-10		Unit	Notes
		Min.	Max.	Min.	Max.		
t_{AVWL}	Address Set-Up Time to $\overline{W}$ Low	0		0		ns	
t_{AVE1L}	Address Set-Up Time to Chip Enable Active	0		0		ns	
t_{AVE2H}		0		0		ns	
t_{E1HAX}	Write Recovery from Chip Enable (Address Hold Time)	10		10		ns	2
t_{E2LAX}		10		10		ns	2
t_{WHDX}	Data Hold Time	5		5		ns	1, 2
t_{AVAV}	Write Cycle Time	70		100		ns	
t_{AVWH}	Address Valid to $\overline{W}$ High	50		80		ns	
t_{WLWH}	Write Pulse Width	50		80		ns	
t_{WHAX}	Address Hold after End of Write	10		10		ns	1
t_{E1LE1H}	Chip Enable Active to End of Write	50		80		ns	2
t_{E2HE2L}		50		80		ns	2
t_{DVWH}	Data Valid to End of Write	40		50		ns	1, 2
t_{WHQX}	End of Write to Q Low-Z	10		10		ns	
t_{WLQZ}	$\overline{W}$ Low to Q High-Z		40		50	ns	

Notes :

1. In a $\overline{W}$ Controlled Cycle.
2. In a $\overline{E}_1$, E_2 Controlled Cycle.

Figure 6. Write Control Write Cycle Timing

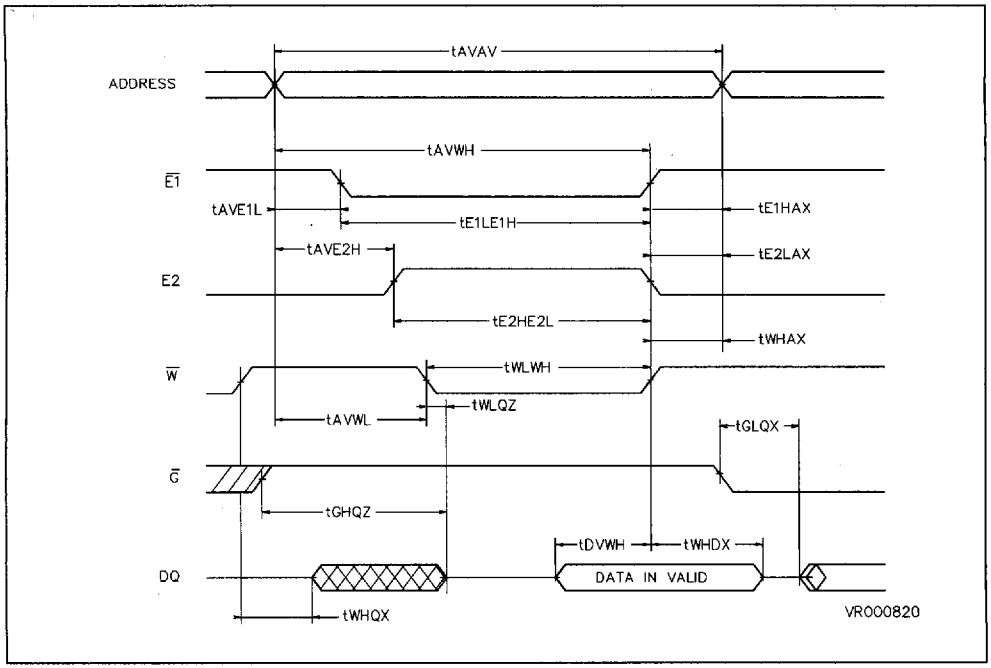
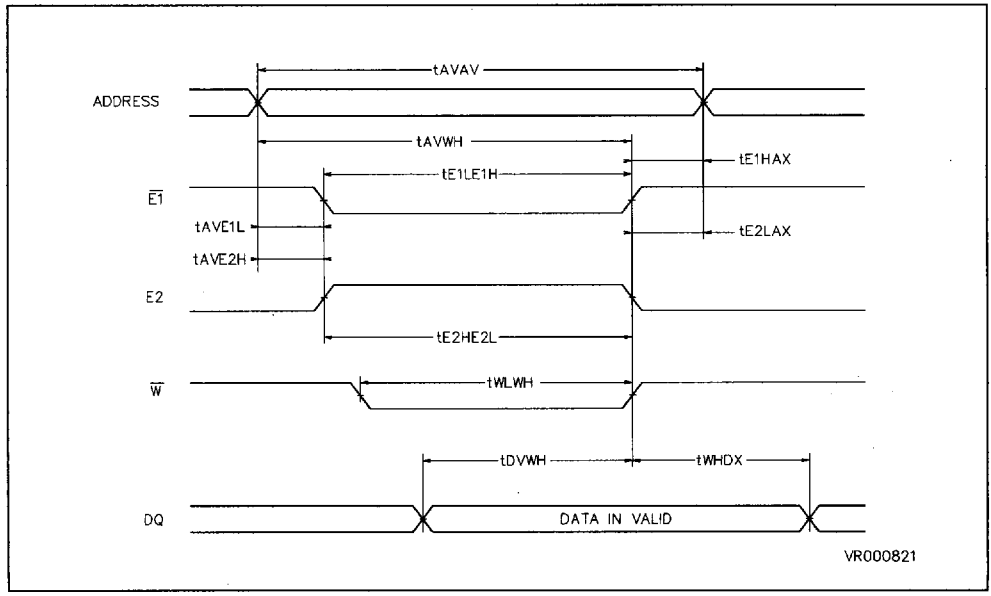


Figure 7. Chip Enable Control Write Cycle Timing



DATA RETENTION MODE

With V_{CC} applied, the MK48Z08/18/09/19 operates as a conventional BYTEWIDE™ Static RAM. Should the supply voltage decay, the RAM will automatically power-fail deselect, write protecting itself when V_{CC} falls within the V_{PFD}(max), V_{PFD}(min) window.

Note : A mid-write cycle power failure may corrupt data at the currently addressed location, but does not jeopardize the rest of the RAM's content. At voltages below V_{PFD}(Min), the user can be assured the memory will be in a write protected state, provided the V_{CC} fall time is not less than t_F. The MK48Z08/18/09/19 may respond to transient noise spikes that reach into the deselect window if this should occur during the time the device is sampling V_{CC}. Therefore decoupling of the power supply lines is recommended.

The power switching circuit connects external V_{CC} to the RAM and disconnects the battery when V_{CC} rises above V_{SO}. Normal RAM operation can resume t_{REC} after V_{CC} exceeds V_{PFD}(max). Caution should be taken to keep $\overline{E}_1$ high (MK48Z08/18) or E_2 low (MK48Z09/19) as V_{CC} rises past V_{PFD}(min) as some systems may perform inadvertent write cycles after V_{CC} rises but before normal system operation begins.

POWER FAIL INTERRUPT

The MK48Z09/19 continuously monitors V_{CC}. When V_{CC} falls to the power fail detect trip point of the MK48Z09/19 an interrupt is immediately generated. An internal clock provides a delay no less than 10µs but no greater than 40 µs before automatically deselecting the MK48Z09/19. The $\overline{INT}$ pin is an open drain output and requires an external pull up resistor.

PREDICTING BACK-UP SYSTEM LIFE

The useful life of the battery in the MK48Z08/18/09/19 is expected to ultimately come to an end for one of two reasons : either because it has been discharged while providing current to an external load ; or because the effects of aging render the cell useless before it can actually be discharged. Fortunately, these two effects are virtually unrelated, allowing discharge, or Capacity Consumption, and the effects of aging, or Storage Life, to be treated as two independent but simultaneous mechanisms, the earlier of which defines Back-up System life.

With V_{CC} on, the battery is disconnected from the RAM and aging effects become the determining factor in battery life. With V_{CC} off, leakage currents in the RAM provide the only load on the Battery during battery back-up. For the MK48Z08/18/09/19, the leakage currents are so low that the Back-up System Life of the device is simply the Storage Life of the cell. The Storage Life of the cell is a function of temperature.

PREDICTING STORAGE LIFE

Figure 8 illustrates how temperature affects Storage Life of the MK48Z08/18/09/19 battery. The life of the battery is controlled by temperature and is virtually unaffected by leakage currents drawn by the MK48Z08/18/09/19.

Storage Life predictions presented in Figure 8 are extrapolated from temperature accelerated life-test data collected in over 100 million device hours of continuing bare cell and encapsulated cell battery testing by SGS-THOMSON. Obviously, temperature accelerated testing cannot identify non-temperature dependent failure mechanisms. However, in view of the fact that no random cell failures have been recorded in any of SGS-THOMSON's on going battery testing since it began in 1982, we believe the chance of such failure mechanisms surfacing is extremely small. For the purpose of the testing, a cell failure is defined as the inability of a cell stabilized at 25°C to produce a 2.4 volt closed-circuit voltage across a 250K load resistance.

A Special Note : The summary presented in Figure 8 represents a conservative analysis of the data presently available. While SGS-THOMSON is most likely in possession of the largest collection of battery life data of this kind in the world, the results presented should not be considered absolute or final ; they can be expected to change as yet more data becomes available. We believe that future read points of life test presently under way and improvements in the battery technology itself will result in a continuing improvement of these figures.

Two end of life curves are presented in Figure 8. They are labeled "Average" ($t_{50\%}$) and ($t_{1\%}$). These terms relate to the probability that a given number of failures will have accumulated by a particular point in time. If, for example, expected life at 70°C is at issue, Figure 8 indicates that a particular MK48Z08/18/09/19 has a 1% chance of having a battery failure 11 years into its life and a 50% chance of failure at the 20 year mark. Conversely, given a sample of devices, 1% of them can be expected to experience a battery failure within 11 years ; 50% of them can be expected to experience a failure within 20 years.

The $t_{1\%}$ figure represents the practical onset of wear out, and is therefore suitable for use in what would normally be thought of as a worst-case analysis. The $t_{50\%}$ figure represents "normal" or "average" life. It is, therefore, accurate to say that the average device will last "$t_{50\%}$".

Battery life is defined as beginning at the date of manufacture. Each MK48Z08/18/09/19 is marked with a nine digit manufacturing date code in the form H99XXYYZZ, example: H995B9231 is H -fabricated in Carrollton, TX; 9 - assembled in Muar, Malaysia; 9- tested in Muar, Malaysia; 5B - lot designator; 9231 - assembled in the year 1992, work week 31.

Calculating Predicted Storage Life of the Battery

As Figure 8 indicates, the predicted Storage Life of the battery in the MK48Z08/18/09/19 is a function of temperature.

Because the ambient temperature profile is dependent upon application controlled variables, only the user can estimate predicted Storage Life in a given design. As long as ambient temperature is held reasonably constant, expected Storage Life can be read directly from Figure 8. If the MK48Z08/18/09/19 spends an appreciable amount of time at a variety of temperatures, the following equation should be used to estimate Storage Life.

T-46-23-12

Example Predicted Storage Life Calculation

$$\text{Predicted Storage Life} = 1 / \{ [(TA_1 / TT) / SL_1] + [(TA_2 / TT) / SL_2] + \ldots + [(TA_N / TT) / SL_N] \}$$

Where TA_1, TA_2, TA_N, = Time at Ambient Temperature 1, 2, etc.

TT = Total Time = $TA_1 + TA_2 + \ldots + TA_N$

SL_1, SL_2, SL_N = Predicted Storage Life at Temp. 1, Temp. 2, etc. (See Figure 8)

Example Predicted Storage Life Calculation

A cash register/terminal operates in an environment where the MK48Z08/18/09/19 is exposed to temperatures of 55°C or less for 8322 hrs./yr.; and temperatures greater than 60°C, but less than 70°C, for the remaining 438 hrs./yr.

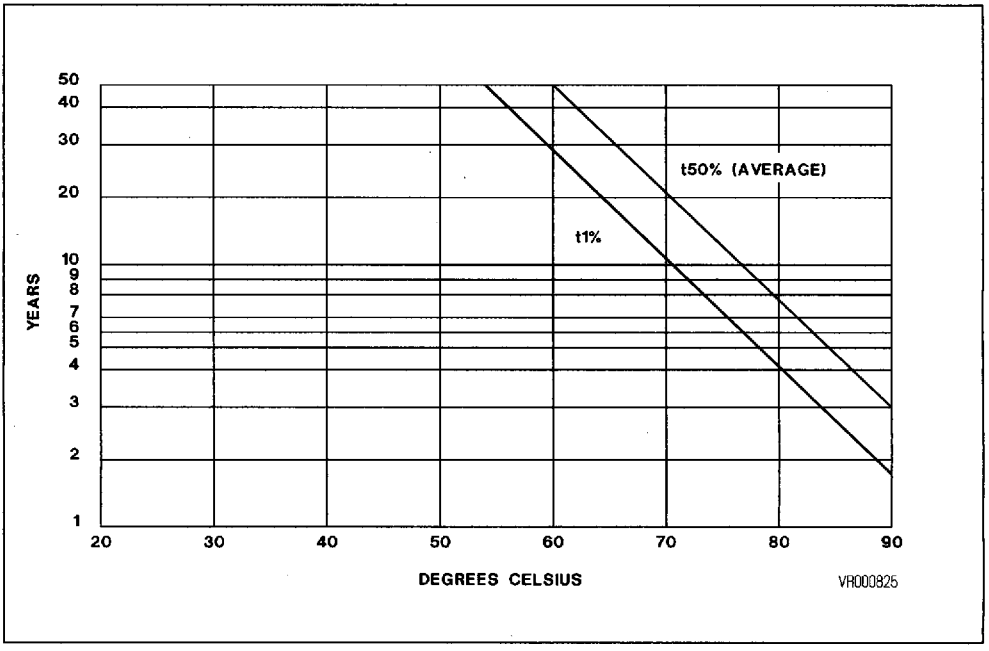
Reading Predicted $t_{1\%}$ values from Figure 8; SL_1 = 41 yrs., SL_2 = 11.4 yrs.,

Total Time (TT) = 8760 hrs./yr. TA_1 = 8322 hrs./yr. TA_2 = 438 hrs./yr. .

Predicted Typical Storage Life $\geq 1 / \{ [(8322 / 8760) / 41] + [(438 / 8760) / 11.4]$

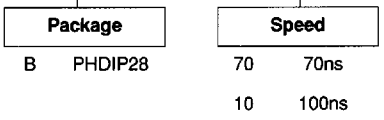
Predicted Typical Storage Life $\geq$ 36 years

Figure 8. Predicted Battery Storage Life Versus Temperature



ORDERING INFORMATION

Example: MK48Z08 B 70



Package		Speed	
B	PHDIP28	70	70ns
		10	100ns

For a list of available options of Package and Speed refer to the Selector Guide in this Data Book or the current Memory Shortform that will be periodically up-dated.

For further information or any aspect of this device, please contact our Sales Office nearest to you.