Final

PAL10H20EG8-6/PAL10020EG8-6

ECL Latched Programmable Array Logic

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- High-performance; t_{PD} = 6 ns
- Eight user-programmable output logic macrocells for latched or combinatorial operation
- A registered version of the device is available as PAL10H20EV8 or PAL10020EV8 (see AMD Publication No. 06176)
- Up to twenty inputs and eight outputs
- Individually user-programmable output polarity
- Varied product-term distribution for increased design flexibility
- Individual product term for output enable
- Asynchronous-RESET and PRESET capability
- Power-up RESET capability
- PRELOAD for improved testability
- Special designed-in test features for factory AC and DC testing
- Proven fuses ensure high programming yield, fast programming and unsurpassed reliability
- 10KH/100K ECL options
- 50-ohm drive with wired-OR capability
- 24-pin 300-mil SKINNYDIP® and 28-pin chip carrier packages
- Supported by PALASM® software

GENERAL DESCRIPTION

The PAL10H20EG8/PAL10020EG8 is an advanced bipolar ECL Programmable Array Logic (PAL®) device. It uses the familiar sum-of-products (AND-OR) single array logic structure, allowing users to program custom logic functions. Fabricated with AMD's new advanced bipolar oxide-isolation process technology, and utilizing the innovative architectural features of the PAL22V10, the PAL10H20EG8/PAL10020EG8 represents the most advanced ECL PAL device available on the market today.

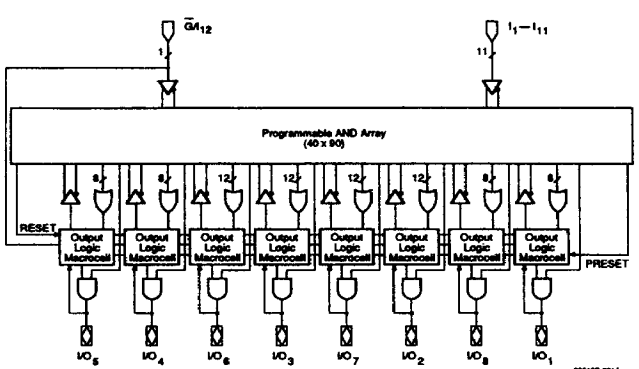
The PAL10H20EG8/PAL10020EG8 contains up to twenty inputs and eight outputs. It incorporates AMD's unique output logic macrocell (as in the PAL22V10), which allows the user to define and program the architecture of each output on an individual basis. Each output is user-programmable for either latched or combinatorial operation. Each output also has user-programmable output-polarity control, further simplifying the design. The flexibility of the programmable output logic macrocells permits the system designer to tailor the device to particular application requirements.

Increased logic power has been built into the PAL10H20EG8/PAL10020EG8 by providing a varied number of logical product terms per output. Four outputs have twelve logical product terms each, and the other four have eight logical product terms each. This varied allocation of logical product terms allows complex functions to be implemented in a single ECL PAL device. Each output also has a separate output-enable product term.

System operation has been enhanced by the addition of asynchronous-PRESET and RESET product terms for the PAL10H20EG8/PAL10020EG8. These product terms are common to all latched outputs.

The PAL10H20EG8/PAL10020EG8 incorporates power-up RESET on all latched outputs. It also has the ability to PRELOAD latches to any desired state during testing. PRELOAD permits full logical verification during testing.

BLOCK DIAGRAM



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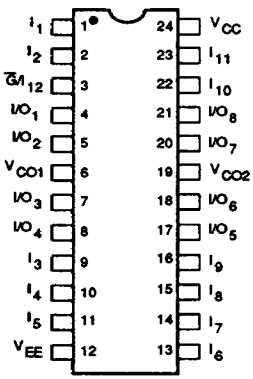
CONNECTION DIAGRAMS
Top View

SKINNYDIP



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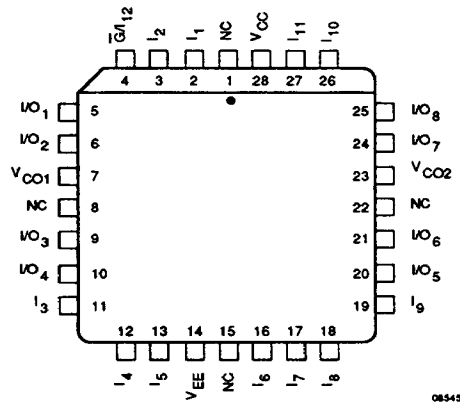
PLCC



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Note: Pin 1 is marked for orientation.

PIN DESCRIPTION

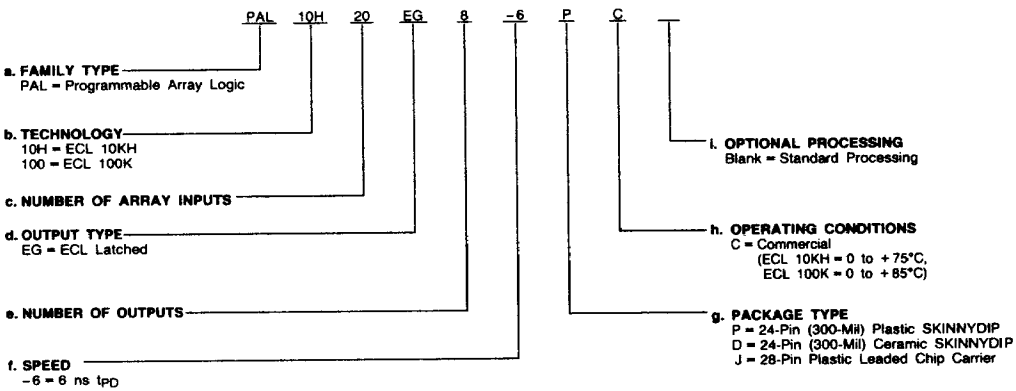
$I_1 - I_{11}$	Dedicated Input Pins (11)	V_{CC}	Circuit Ground
$I/O_1 - I/O_8$	Bidirectional Input/Output Pins (8)	V_{CO1}, V_{CO2}	Circuit Ground Pins for Outputs (2)
$\overline{G}/I_{12}$	$\overline{\text{Gate}}$ or Input Pin	V_{EE}	Negative Supply Voltage
NC	No Connect		

ORDERING INFORMATION

PAL Products

AMD PAL products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

a. Family Type
b. Technology
c. Number of Array Inputs
d. Output Type
e. Number of Outputs
f. Speed
g. Package Type
h. Operating Conditions
i. Optional Processing



Valid Combinations	
PAL10H20EG8-6	PC, DC, JC
PAL10020EG8-6	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

Note: marked with AMD logo

FUNCTIONAL DESCRIPTION

The PAL10H20EG8/PAL10020EG8 is an advanced bipolar ECL PAL device. It contains a programmable fuse array organized in the familiar sum-of-products (AND-OR) structure.

The block diagram in Figure 1 illustrates the basic architecture of the PAL10H20EG8/PAL10020EG8. There are up to twenty external inputs and eight outputs. The inputs are connected to a programmable-AND array. Initially, the AND gates are connected, via fuses, to both the true and complement of every input. By selective programming of the fuses, the AND gates may be "connected" to only the true inputs, the complement inputs, or to neither type of input. When both the true and complement fuses are left intact, a logical-FALSE results at the output of the AND gate. An AND gate with all the fuses programmed will assume the logical-TRUE state. The outputs of the AND gates are connected to fixed-OR gates.

There are an average of ten product terms per OR gate (output), distributed in a varied fashion. Four outputs have eight product terms each while the other four have twelve product terms each. This varied distribution of product terms allows more complex logic functions to be implemented.

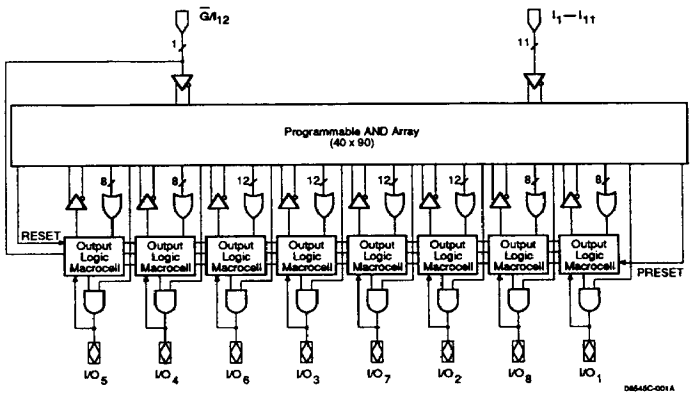
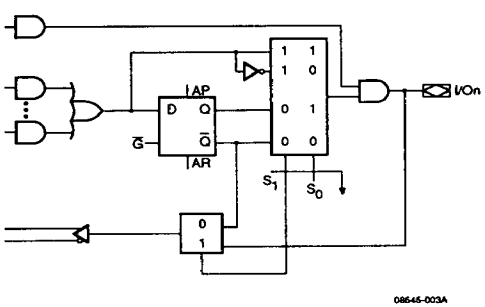


Figure 1. Block Diagram

Output Logic Macrocells

A useful feature of the PAL10H20EG8/PAL10020EG8 is its versatile programmable output logic macrocell. It allows the user to program the outputs on an individual basis in a very flexible manner.

The PAL10H20EG8/PAL10020EG8 output logic macrocell incorporates a latch that is transparent when $\overline{G}$ is LOW. As shown in the output logic macrocell diagram, each macrocell contains two programmable fuses (S_0 and S_1) for programming the output functions. S_1 controls whether the output will be latched or combinatorial. S_0 controls the output polarity (active-HIGH or active-LOW). Depending on the states of these two fuses, an individual output operates in one of four modes: Latched/Active-LOW, Latched/Active-HIGH, Combinatorial/Active-LOW, and Combinatorial/Active-HIGH. Each output is also provided with a separate output enable product term.



Enable term	$\overline{G}$	D	Active-HIGH Output
L	X	X	L (disable)
H	L	L	L (transparent)
H	L	H	H (transparent)
H	H	X	Q (latch)

Figure 2. PAL10H20EG8/PAL10020EG8 Output Logic Macrocell

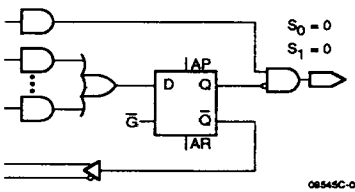


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Figure 3-1. Latched/Active-LOW

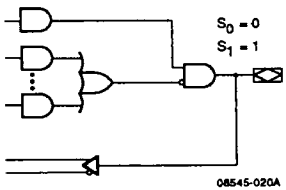

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Figure 3-3. Combinatorial/Active-LOW

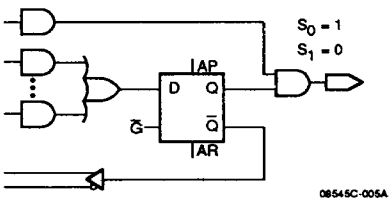

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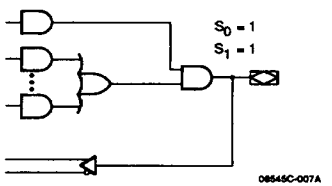
Figure 3-2. Latched/Active-HIGH



LD001530

Figure 3-4. Combinatorial/Active-HIGH

S_1	S_0	Output Configuration
0	0	Latched/Active-LOW
0	1	Latched/Active-HIGH
1	0	Combinatorial/Active-LOW
1	1	Combinatorial/Active-HIGH

0 = Unprogrammed Fuse
1 = Programmed Fuse

4

Feedback

Another feature of the PAL10H20EG8/PAL10020EG8 output macrocell structure is the flexibility of its feedback selection. The feedback can be from either the I/O line or the latched output. The feedback multiplexer is also controlled by the S_1 fuse. The feedback path changes with the output-mode selection. If the output is selected to be latched, the feedback is latched. If the output is combinatorial, the feedback is from the I/O line. This feature enables the designer to optimally use the device to meet precise application requirements. Additionally, it allows the device to perform control tasks, such as arbitration functions, easily.

Output Enable

Each of the eight output logic macrocells of the PAL10H20EG8/PAL10020EG8 contains a dedicated product term for the output-enable function. When this product term is asserted LOW, the output is forced into a LOW state, where it remains until the output-enable product term goes HIGH.

PRESET and RESET

To improve in-system functionality, the PAL10H20EG8/PAL10020EG8 has additional PRESET and RESET product terms. Common asynchronous RESET and PRESET are provided for all the latches of the PAL10H20EG8/PAL10020EG8. When the asynchronous PRESET product term is asserted HIGH the output latches are loaded with a HIGH and when the RESET product term is asserted HIGH the output latches are loaded with a LOW. For the RESET/PRESET to work the latches should be in latched and not transparent mode. These functions are particularly useful for system power-on and reset. The latches automatically reset at power-up.

PRELOAD

To simplify testing, the PAL10H20EG8/PAL10020EG8 is designed with PRELOAD circuitry that provides an easy method for testing logic functionality. PRELOAD allows any arbitrary values to be loaded into the PAL device's output latches.

A typical functional-test sequence would be to verify all possible outputs for the device being tested. To verify these transitions requires the ability to set the latches to an arbitrary "present state" value and to set the device inputs to any arbitrary "present input" value. Once this is done, the latch enable is driven transparent to allow logic to determine the "new state" of the outputs. These outputs can then be checked to validate the design.

Without PRELOAD capability, it is difficult and in some cases impossible to load an arbitrary value into the latches. This can lead to logic verification sequences which are either incomplete or excessively long. With PRELOAD capability, logic verification sequences can be greatly shortened, reducing the

test time and the development costs, and guaranteeing proper in-system operation.

Security Fuse

A security fuse is provided on each PAL10H20EG8/PAL10020EG8 to protect proprietary logic designs. It is programmed at the same time the array is programmed. The security fuse disables the pattern verification circuitry, and is verified by verifying the whole fuse array as if every fuse were programmed. The security fuse also disables preload.

Fabrication

The PAL10H20EG8/PAL10020EG8 is manufactured using Advanced Micro Devices' new oxide-isolation process. This advanced process offers increased density and reduced internal capacitance resulting in the fastest possible programmable logic devices.

The PAL10H20EG8/PAL10020EG8 is fabricated with AMD's fast-programming and highly-reliable fuse technology. Utilizing an easily implemented programming algorithm, these products can be rapidly programmed to any customized pattern.

Testing

The PAL10H20EG8/PAL10020EG8 contains many internal test features, including circuitry and extra fuses which allow AMD to test each part before shipping. This ensures extremely high post-programming functional yields. The test fuses are programmed to assure the ability of each part to perform correct programming. There are extra test words which are preprogrammed during manufacturing and tested to ensure correct logic operation and parametric integrity.

Using the PAL10H20EG8/PAL10020EG8 Device as a State Machine

Latches can be used in the implementation of state machines, but care must be taken in their use. They cannot be treated as if they were registers, which are more common in the TTL PAL devices. Since a latch is a level-sensitive storage device, it is more difficult to control the sequencing of states. In theory, when the gate pin is lowered, the latch can assume a new state. After waiting for the state to stabilize and for the feedback signal to propagate, the new state can be latched. Latching the state delays any further state changes until the next time the gate signal $\overline{G}$ goes LOW.

Latches Are Not Registers

The danger in treating a latch just like a register is that a feedback race condition will be explicitly built into the circuit. Enough setup time must be allowed for latching new data, yet if too much delay is allowed, the transparent latch may actually change state twice before being latched. For example, a divide-by-two counter (Figure 4a) may oscillate until the gate pin is raised if too much setup time is provided. The final state will depend on how fast the output was oscillating (Figure 4b), and will be unpredictable.

Use a Dual-Phase Clock

The usual method of dealing with this problem is to use a dual-phase clock, with two sets of latches. Implementation in the PAL10H20EG8/PAL10020EG8 would require a second device for the opposite phase. The logic must be partitioned such that all latches that are enabled on one phase of the clock feed only latches that are enabled on the opposite phase. This allows operation in a master-slave mode. The implementation can be made by providing one latch merely as a holding element, which can pass the data unchanged to another latch; this is essentially a master-slave register. In such a situation, two latches are needed for each state bit. The divide-by-two counter using a master and a slave is shown in Figure 4c.

If the entire state machine can be partitioned into two groups of state bits such that group 1 states only feed group 2 states and vice versa, then it becomes possible to place logic between the master latch and the slave latch. At that point the terms "master" and "slave" lose significance; each latch may implement a state bit by itself.

Greater System Speed And Efficiency

This kind of arrangement can sometimes be used to obtain a greater overall system speed than would be possible using

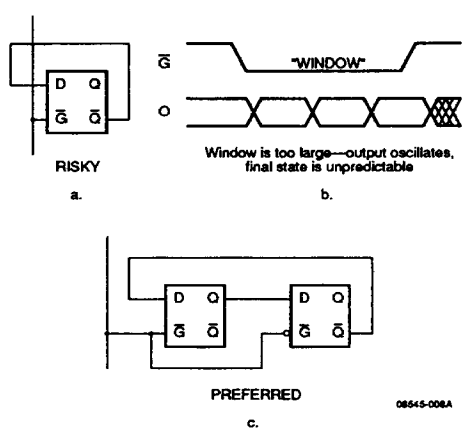
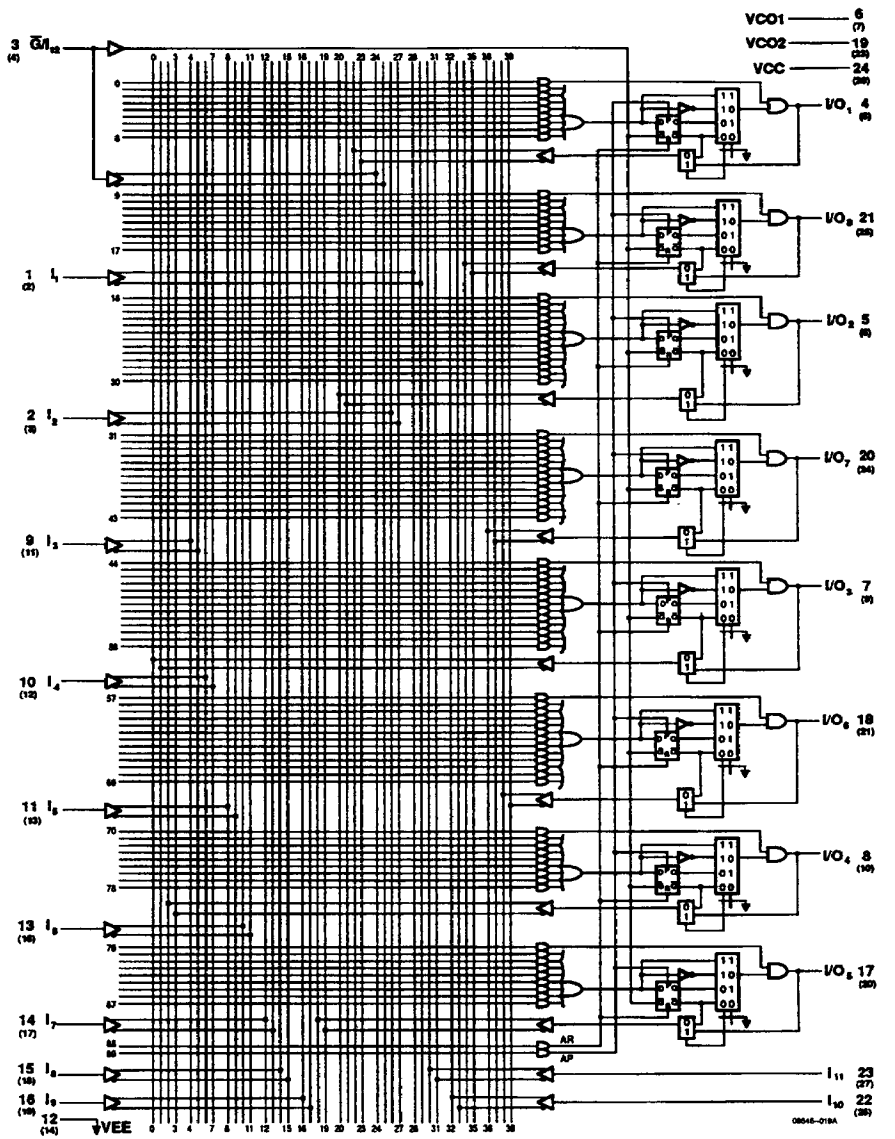


Figure 4. Using a Dual-Phase Clock

registers instead of latches. Since a register is essentially made up of two latches, it can also provide for a more efficient design with latches.



DIP (PLCC) pinouts.

Figure 5. Logic Diagram for PAL10H20EG8/PAL10020EG8

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65°C to +150°C
Supply Voltage (V_{EE})
with Respect to Ground ..... −8 V to 0 V
DC Input Voltage
with Respect to Ground ..... V_{EE} to 0 V
Output Current
-Continuous ..... 35 mA
-Surge ..... 100 mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Commercial (C) Devices — 10KH Devices
Ambient Temperature (T_A) Operating
Air Flow 500 lfpm ..... 0°C to +75°C
Supply Voltage (V_{EE}) ..... −5.46 V to −4.94 V

Commercial (C) Devices — 100K Devices
Ambient Temperature (T_A) Operating
Air Flow 500 lfpm ..... 0°C to +85°C
Supply Voltage (V_{EE}) ..... −4.8 V to −4.2 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over **COMMERCIAL** operating ranges (Notes 1, 2)

PAL10H20EG8 (10KH) Devices

Parameter Symbols	Parameter Description	Test Conditions			Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	$V_{IN} = V_{IH}$ (Max.) or V_{IL} (Min.)	Loading is 50 Ω to −2.0 V	$T_A = 0°C$	−1020	−840	mV
				$T_A = +25°C$	−980	−810	
				$T_A = +75°C$	−920	−735	
V_{OL}	Output LOW Voltage			$T_A = 0°C$	−1950	−1630	mV
				$T_A = +25°C$	−1950	−1630	
				$T_A = +75°C$	−1950	−1600	
V_{IH}	Input HIGH Voltage	Guaranteed Input HIGH Voltage (Note 3)		$T_A = 0°C$	−1170	−840	mV
				$T_A = +25°C$	−1130	−810	
				$T_A = +75°C$	−1070	−735	
V_{IL}	Input LOW Voltage	Guaranteed Input LOW Voltage (Note 3)		$T_A = 0°C$	−1950	−1480	mV
				$T_A = +25°C$	−1950	−1480	
				$T_A = +75°C$	−1950	−1450	
I_{IH}	Input HIGH Current	$V_{IN} = V_{IH}$ (Max.)		$T_A = 0°C$		300	µA
				$T_A = +25°C$		300	
				$T_A = +75°C$		300	
I_{IL}	Input LOW Current	$V_{IN} = V_{IL}$ (Min.)		$T_A = 0°C$	0.5		µA
				$T_A = +25°C$	0.5		
				$T_A = +75°C$	0.3		
I_{EE}	Power Supply Current	All Inputs and Outputs Open		$T_A = 0°C$	−260		mA
				$T_A = +25°C$	−260		
				$T_A = +75°C$	−260		

Notes: 1. Designed to meet specifications shown after thermal equilibrium has been established. Guaranteed with transverse air flow exceeding 500 linear feet per minute.
2. The relative values of the specified conditions and limits will be referenced to an algebraic scale. The extremities of the scale are:
"Max." the value closest to positive infinity.
"Min." the value closest to negative infinity.
3. These are absolute voltages with respect to the device ground pin and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment and fixturing.

DC CHARACTERISTICS over COMMERCIAL operating ranges (Cont'd.) (Notes 1, 2)

PAL10020EG8 (100K) Devices

Parameter Symbols	Parameter Description	Test Conditions			Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	$V_{IN} = V_{IH}$ (Max.) or V_{IL} (Min.)	Loading is 50 Ω to −2.0 V	$V_{EE} = -4.2$ V	−1025	−880	mV
				$V_{EE} = -4.5$ V	−1025	−880	
				$V_{EE} = -4.8$ V	−1035	−880	
V_{OL}	Output LOW Voltage			$V_{EE} = -4.2$ V	−1810	−1605	mV
				$V_{EE} = -4.5$ V	−1810	−1620	
				$V_{EE} = -4.8$ V	−1810	−1620	
V_{IH}	Input HIGH Voltage	Guaranteed Input HIGH Voltage (Note 3)		$V_{EE} = -4.2$ V	−1150	−880	mV
				$V_{EE} = -4.5$ V	−1165	−880	
				$V_{EE} = -4.8$ V	−1165	−880	
V_{IL}	Input LOW Voltage	Guaranteed Input LOW Voltage (Note 3)		$V_{EE} = -4.2$ V	−1810	−1475	mV
				$V_{EE} = -4.5$ V	−1810	−1475	
				$V_{EE} = -4.8$ V	−1810	−1490	
I_{IH}	Input HIGH Current	$V_{IN} = V_{IH}$ (Max.)		$V_{EE} = -4.2$ V		300	µA
				$V_{EE} = -4.5$ V		300	
				$V_{EE} = -4.8$ V		300	
I_{IL}	Input LOW Current	$V_{IN} = V_{IL}$ (Min.)		$V_{EE} = -4.2$ V	0.5		µA
				$V_{EE} = -4.5$ V	0.5		
				$V_{EE} = -4.8$ V	0.5		
I_{EE}	Power Supply Current	All Inputs and Outputs Open		$V_{EE} = -4.2$ V	−285		mA
				$V_{EE} = -4.5$ V	−285		
				$V_{EE} = -4.8$ V	−285		

Notes: 1. Designed to meet specifications shown after thermal equilibrium has been established. Guaranteed with transverse air flow exceeding 500 linear feet per minute.
2. The relative values of the specified conditions and limits will be referenced to an algebraic scale. The extremities of the scale are:
"Max." the value closest to positive infinity.
"Min." the value closest to negative infinity.
3. These are absolute voltages with respect to the device ground pin and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment and fixturing.

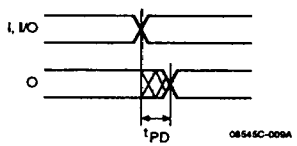
SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Notes 1, 2)

Parameter Symbol	Parameter Description	Min.	Max.	Unit
t_{PD}	Input or Feedback to Output		6	ns
t_S	Input or Feedback Setup Time	4		ns
t_H	Hold Time	0		ns
t_G	Gate to Output or Feedback		4	ns
t_{AR}/t_{AP}	Asynchronous RESET/PRESET to Latched Output		8	ns
t_{ARW}/t_{APW}	Asynchronous RESET/PRESET Width	6		ns
t_{ARR}/t_{APR}	Asynchronous RESET/PRESET Recovery Time	6		ns
t_{WL}	Gate Width LOW	3		ns
t_{EA}	Input to Output Enable		7	ns
t_{ER}	Input to Output Disable		7	ns
t_{RO}	Output Rise Time (20% – 80%)	0.7	2.2	ns
t_{FO}	Output Fall Time (80% – 20%)	0.7	2.2	ns

1. Designed to meet specifications shown after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained.
2. Test conditions: see Setup for Testing Switching Characteristics.

Definitions of Switching Parameters

t_{PD}: Signal propagation delay from an input or an I/O pin through the array to a combinatorial ouput or a latched output while $\overline{G}$ is LOW.



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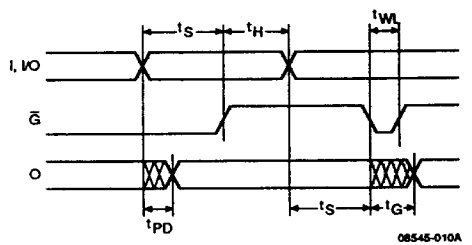
t_S: Time that input data must be valid before $\overline{G}$ goes HIGH in order to latch data.

t_H: Time that input data must be valid after $\overline{G}$ goes HIGH in order to latch data.

t_G: Delay between lowering $\overline{G}$ and data appearing at the output.

Note: In order for a signal to appear at the output at a time t_G after lowering $\overline{G}$, the signal must be set up a time t_S before $\overline{G}$ is lowered. If this amount of time is not allowed, then the output will change at a time t_{PD} after the inputs were changed. The t_S needed is illustrated in the waveforms.



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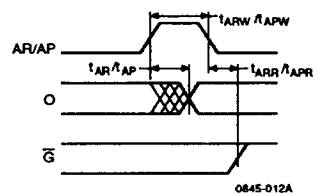
t_{WL}: The minimum gate LOW pulse width needed to latch new data.

t_{AR}/t_{AP}: Delay from an input or I/O pin activating asynchronous reset or preset to data appearing at a latched output.

t_{ARW}/t_{APW}: The minimum input or I/O pin pulse width needed to activate asynchronous reset or preset.

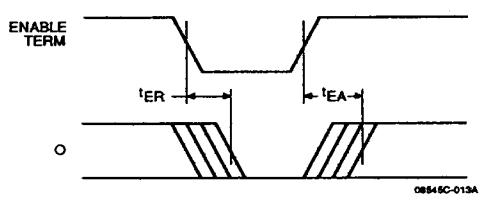
t_{ARR}/t_{APR}: Time that input or I/O pin must inactivate asynchronous reset or preset before $\overline{G}$ goes LOW in order to pass data.



WF027100

t_{EA}: Delay between input or I/O pin activating enable term and data appearing at outputs.

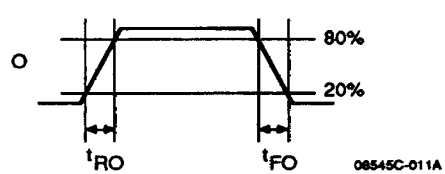
t_{ER}: Delay between input or I/O pin deactivating enable term and outputs going LOW.



WF027110

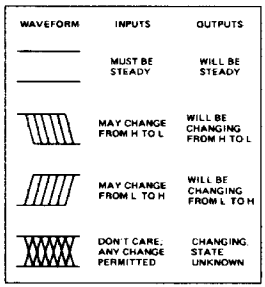
t_{RO}: Time taken for an output signal voltage to swing from 20% to 80% of the full logic swing.

t_{FO}: Time taken for an output signal voltage to swing from 80% to 20% of the full logic swing.



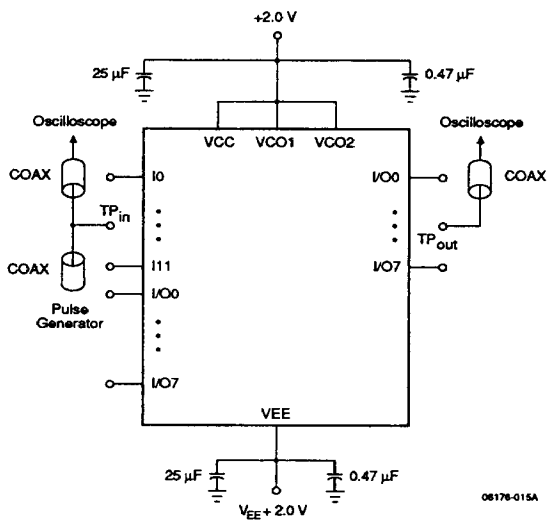
WF025960

KEY TO SWITCHING WAVEFORMS



KS000012

Setup for Testing Switching Characteristics



LS003460

Each oscilloscope channel input should have a 50 Ω termination to ground. Oscilloscope bandwidth should be a least 1 GHz.

The pulse generator should be capable of providing 1.5 ns rise and fall times (20% to 80%).

All input and output cables should be equal lengths of matched 50 Ω coaxial cable. Wire lengths between input (or I/O) pins and TP_{in} or between output pins and TP_{out} should be less than 1/4 in. long. Stubs should be avoided if possible; unavoidable stubs should be less than 2 in. long.

Used inputs that are not switching should be forced to V_{IL} or V_{IH}.

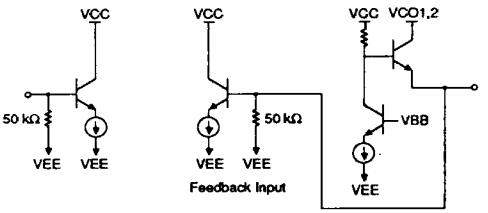
Outputs that are switching but not sensed should be terminated through 50 Ω to ground.

Unused inputs and outputs may be left open.

Note that all voltages are shifted by +2.0 V with respect to normal ECL operating conditions in order to take advantage of the input terminations of the oscilloscope.

Timing thresholds in this configuration are taken to be +0.7 V.

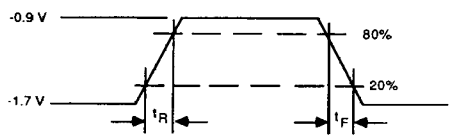
Input and Output Equivalent Schematics



06176C-019A
TC004760

SWITCHING TEST WAVEFORM

INPUT PULSE



06176C-014A
WF023080

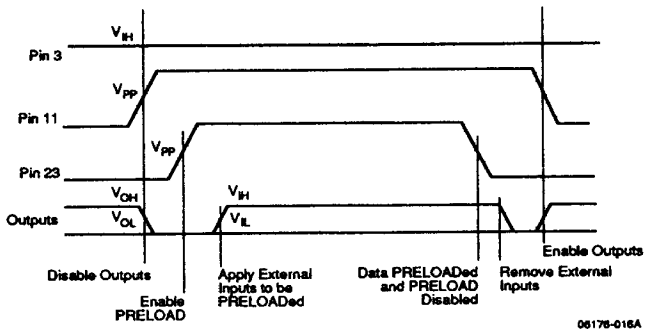
$t_R = t_F = 2.2$ ns Max. for 10KH
$t_R = t_F = 1.0$ ns Max. for 100K

PRELOAD OF LATCHED OUTPUTS

The PAL10H20EG8/PAL10020EG8 latched outputs are provided with circuitry to allow loading each latch to either a HIGH or LOW state. This simplifies testing since any state can be loaded into the latches to control outputs. The pin levels necessary to perform the PRELOAD function are detailed below.

PRELOAD is accessed by applying V_{PP} on pin 23. The data to be preloaded is set on the output pins. Bringing pin 23 back to a logic-LOW level latches the data into the output latches. During PRELOAD the outputs are disabled by a supervoltage on pin 11.

Parameter Symbol	Parameter Description	Min.	Typ.	Max.	Unit
V_{IH}	Input HIGH Level During PRELOAD and Verify	-1.1	-0.9	-0.7	V
V_{IL}	Input LOW Level During PRELOAD and Verify	-1.85	-1.65	-1.45	V
V_{PP}	Voltage Applied to Pins 11 and 23 (DIP)	1.8	2.0	2.2	V

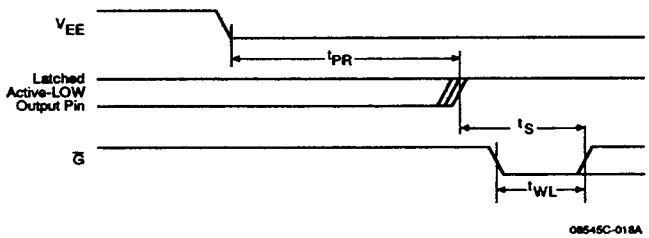


PRELOAD Timing Waveform

POWER-UP RESET

The latches in the PAL10H20EG8/PAL10020EG8 have been designed with the capability to RESET during system power-up. Following power-up, all latches will be LOW. The output state will depend upon the state of the output buffer and the polarity fuse. This feature provides extra flexibility to the designer. A timing diagram and a parameter table are shown below. Due to the asynchronous operation of the power-up RESET and the wide range of ways V_{EE} can fall to steady state, two conditions are required to insure a valid power-up RESET. These conditions are:

1. The V_{EE} fall must be monotonic.
2. Following RESET, the gate pin must not be driven LOW until all applicable input and feedback setup times are met.



Parameter Symbol	Parameter Description	Min.	Typ.	Max.	Unit
t_{PR}	Power-Up RESET Time		600	1000	ns
t_S	Input or Feedback Setup Time	See Switching Characteristics			
t_{WL}	Gate Width LOW				