PERSONAL COMPUTER DATA ACQUISITION A/D CONVERTER

FEATURES

- **Upgrade of Pin-Compatible TC7135, ICL7135, MAX7135 and SI7135**
- **Guaranteed 200 kHz Operation**
- **Single 5V Operation With TC7660**
- **Multiplexed BCD Data Output**
- **UART and Microprocessor Interface**
- **Control Outputs for Auto-Ranging**
- **Input Sensitivity ..... 100 μV**
- **No Sample and Hold Required**

APPLICATIONS

- **Personal Computer Data Acquisition**
- **Scales, Panel Meters, Process Controls**
- **HP-IL Bus Instrumentation**

ORDERING INFORMATION

Part No.	Package	Temperature Range
TC835CBU	64-Pin PQFP	0°C to +70°C
TC835CKW	44-Pin PQFP	0°C to +70°C
TC835CPI	28-Pin Plastic DIP	0°C to +70°C

NOTE: Tape and reel available for 44-pin PQFP packages.

GENERAL DESCRIPTION

The TC835 is a low-power, 4-1/2 digit (0.005% resolution), BCD analog-to-digital converter (ADC) that has been characterized for 200 kHz clock rate operation. The five conversions per second rate is nearly twice as fast as the ICL7135 or TC7135. The TC835 (like the TC7135) does not use the external diode-resistor roll-over error compensation circuits required by the ICL7135.

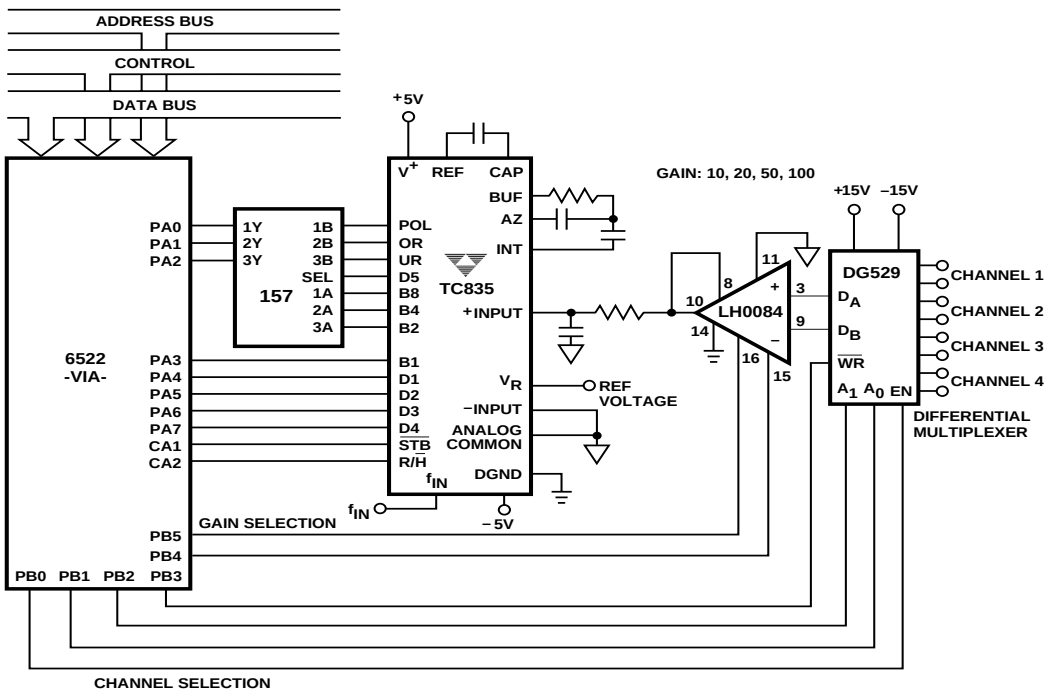
The multiplexed BCD data output is perfect for interfacing to personal computers. The low-cost, greater than 14-bit high-resolution, and 100 μV sensitivity makes the TC835 exceptionally cost-effective.

Microprocessor-based data acquisition systems are supported by the BUSY and $\overline{\text{STROBE}}$ outputs, along with the RUN/$\overline{\text{HOLD}}$ input of the TC835. The overrange, underrange, busy, and run/hold control functions and multiplexed BCD data outputs make the TC835 the ideal converter for μP-based scales and measurement systems and intelligent panel meters.*

The TC835 interfaces with full-function LCD and LED display decoder/drivers. The UNDERRANGE and OVERRANGE outputs may be used to implement an auto-ranging scheme or special display functions.

*See Application Notes 16 and 17 for microprocessor interface techniques.

TYPICAL APPLICATION



TC835-8 11/5/96

TC835

ABSOLUTE MAXIMUM RATINGS* (Note 1)

Positive Supply Voltage ..... +6V
Negative Supply Voltage ..... - 9V
Analog Input Voltage (Pin 9 or 10) ..... V^+ to V^- (Note 2)
Reference Input Voltage (Pin 2) ..... V^+ to V^-
Clock Input Voltage ..... 0V to V^+
Operating Temperature Range ..... 0°C to +70°C
Storage Temperature Range ..... – 65°C to +150°C
Lead Temperature (Soldering, 10 sec) ..... +300°C

Package Power Dissipation ($T_A \leq 70°C$)
28-Pin Plastic DIP 1.14W
44-Pin PQFP 1.00W
64-Pin PFP 1.14W

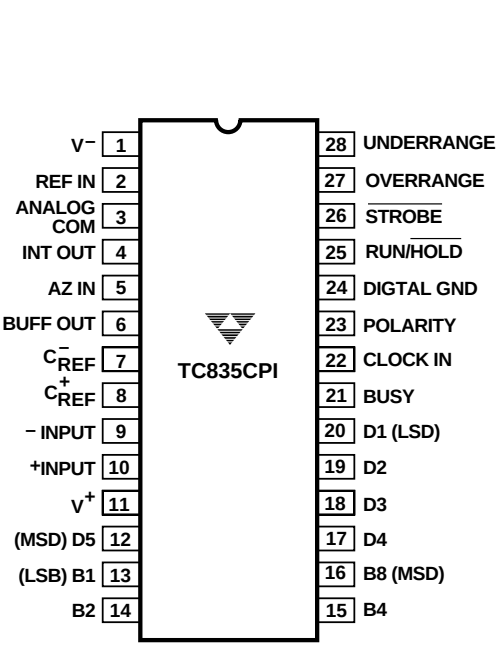
*Static-sensitive device. Unused devices must be stored in conductive material. Protect devices from static discharge and static fields. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to Absolute Maximum Rating Conditions for extended periods may affect device reliability.

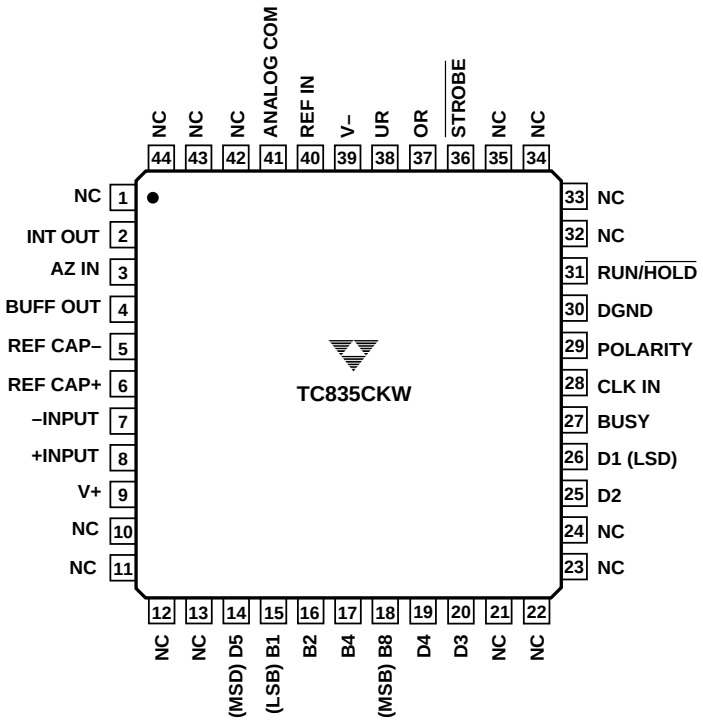
ELECTRICAL CHARACTERISTICS: T_A = +25°C, f_{CLOCK} = 200 kHz, V^+ = +5V, V^- = – 5V, unless otherwise specified.

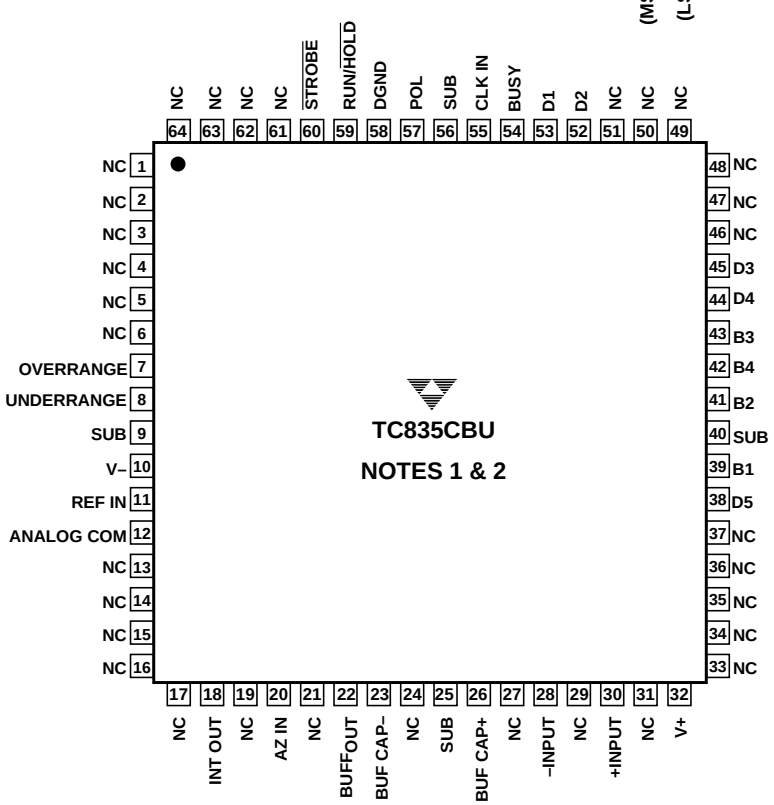
Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Analog						
	Display Reading With Zero Volt Input	Notes 3 and 4	–0.0000	±0.0000	+0.0000	Display Reading
TC_Z	Zero Reading Temperature Coefficient	V_{IN} = 0V Note 5	—	0.5	2	µV/°C
TC_{FS}	Full-Scale Temperature Coefficient	V_{IN} = 2V Notes 5 and 6	—	—	5	ppm/°C
NL	Nonlinearity Error	Note 7	—	0.5	1	Count
DNL	Differential Linearity Error	Note 7	—	0.01	—	LSB
	Display Reading in Ratiometric Operation	$V_{IN} = V_{REF}$ Note 3	+0.9996	+0.9998	+1.0000	Display Reading
±FSE	± Full-Scale Symmetry Error (Roll-Over Error)	$–V_{IN} = +V_{IN}$ Note 8	—	0.5	1	Count
I_{IN}	Input Leakage Current	Note 4	—	1	10	pA
e_N	Noise	Peak-to-Peak Value Not Exceeded 95% of Time	—	15	—	μV_{P-P}
Digital						
I_{IL}	Input Low Current	V_{IN} = 0V	—	10	100	µA
I_{IH}	Input High Current	V_{IN} = +5V	—	0.08	10	µA
V_{OL}	Output Low Voltage	I_{OL} = 1.6 mA	—	0.2	0.4	V
V_{OH}	Output High Voltage B_1, B_2, B_4, B_8, D_1–D_5 Busy, Polarity, Overrange, Underrange, Strobe	 I_{OH} = 1 mA I_{OH} = 10 µA	 2.4 4.9	 4.4 4.99	 5 5	 V V
f_{CLK}	Clock Frequency	Note 10	0	200	1200	kHz
Power Supply						
V^+	Positive Supply Voltage		4	5	6	V
V^-	Negative Supply Voltage		– 3	– 5	– 8	V
I^+	Positive Supply Current	f_{CLK} = 0 Hz	—	1	3	mA
I^-	Negative Supply Current	f_{CLK} = 0 Hz	—	0.7	3	mA
PD	Power Dissipation	f_{CLK} = 0 Hz	—	8.5	30	mW

NOTES:
1. Functional operation is not implied.
2. Limit input current to under 100 µA if input voltages exceed supply voltage.
3. Full-scale voltage = 2V.
4. V_{IN} = 0V.
5. $0°C \leq T_A \leq +70°C$.
6. External reference temperature coefficient less than 0.01 ppm/°C.
7. $– 2V \leq V_{IN} \leq +2V$. Error of reading from best fit straight line.
8. $|V_{IN}| = 1.9959$.
9. Test circuit shown in Figure 1.
10. Specification related to clock frequency range over which the TC835 correctly performs its various functions. Increased errors result at higher operating frequencies.

PIN CONFIGURATIONS







NOTES: 1. NC = No internal connection.
2. Pins 9, 25, 40 and 56 are connected to the die substrate. The potential at these pins is approximately V^+. No external connections should be made.

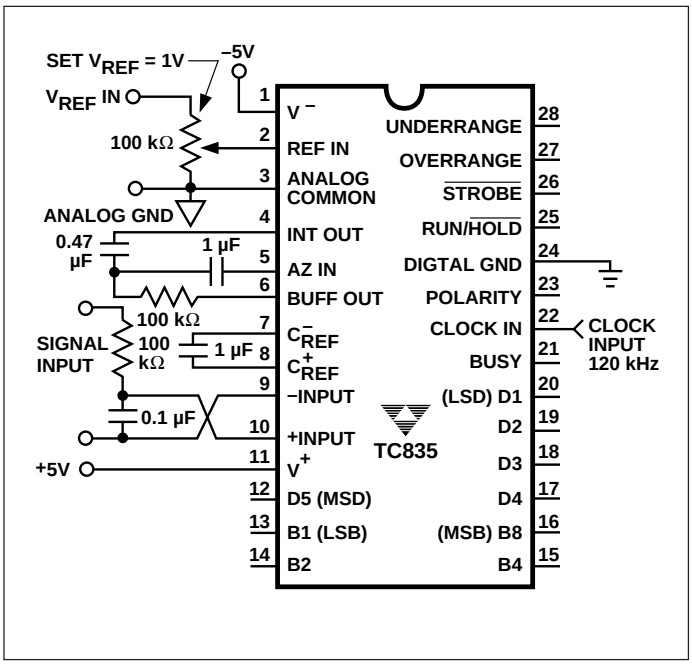


Figure 1. Test Circuit

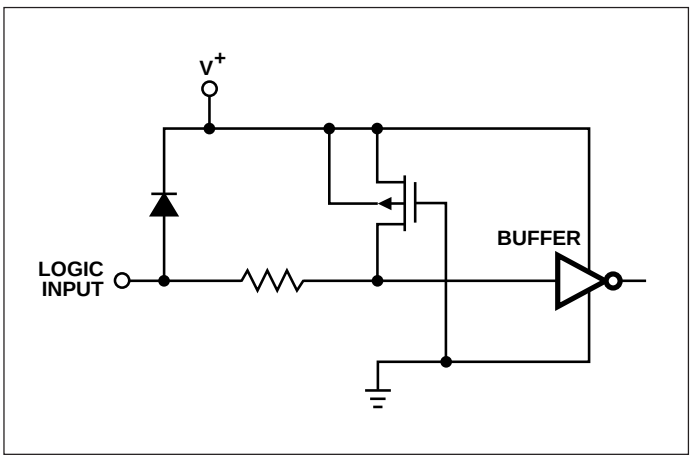


Figure 2. Digital Logic Input

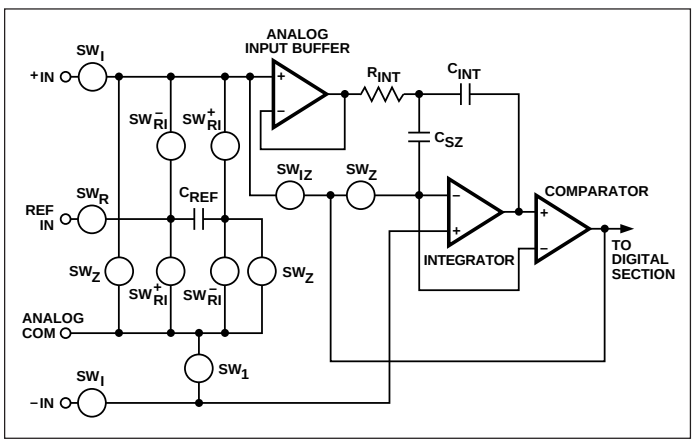


Figure 3A. Analog Circuit Function Diagram

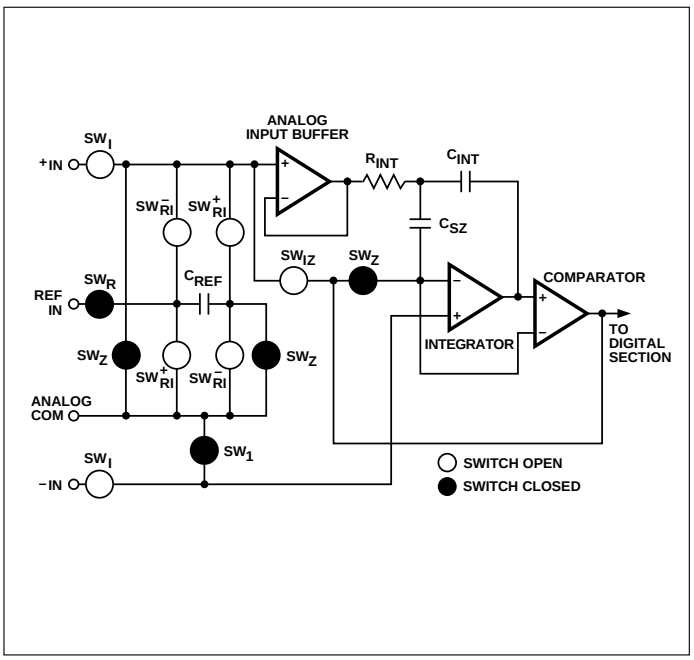


Figure 3B. System Zero Phase

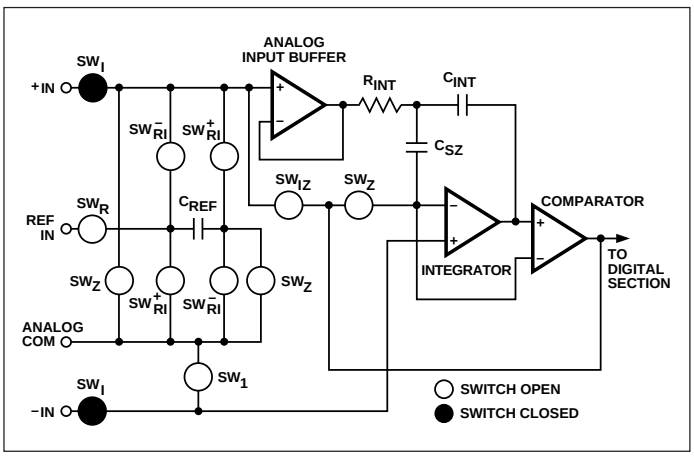


Figure 3C. Input Signal Integration Phase

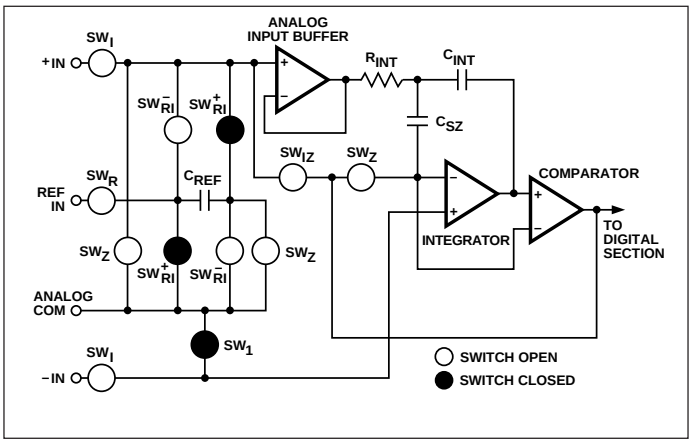


Figure 3D. Reference Voltage Integration Cycle

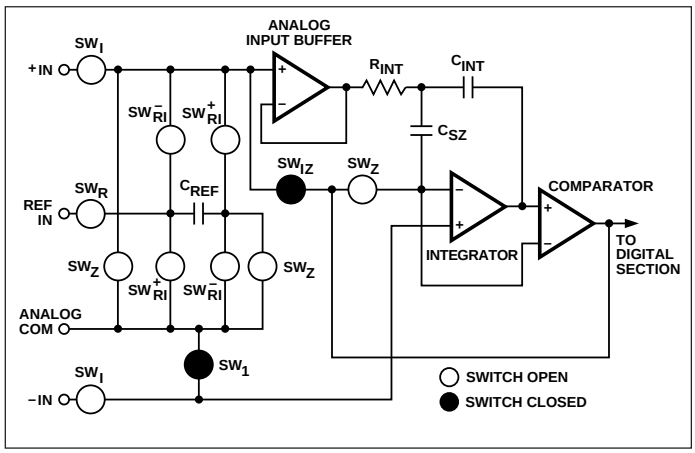


Figure 3E. Integrator Output Zero Phase

GENERAL THEORY OF OPERATION

(All Pin Designations Refer to 28-Pin DIP)

Dual-Slope Conversion Principles

The TC835 is a dual-slope, integrating analog-to-digital converter. An understanding of the dual-slope conversion technique will aid in following the detailed TC835 operational theory.

The conventional dual-slope converter measurement cycle has two distinct phases:

(1) Input signal integration
(2) Reference voltage integration (deintegration)

The input signal being converted is integrated for a fixed time period. Time is measured by counting clock pulses. An opposite polarity constant reference voltage is then integrated until the integrator output voltage returns to zero. The reference integration time is directly proportional to the input signal.

In a simple dual-slope converter, a complete conversion requires the integrator output to "ramp-up" and "ramp-down."

A simple mathematical equation relates the input signal, reference voltage, and integration time:

$$\frac{1}{RC}\int_0^{t_{SI}} V_{IN}(t)\,dt = \frac{V_R\,t_{RI}}{RC},$$

where:

V_R = Reference voltage

t_{SI} = Signal integration time (fixed)

t_{RI} = Reference voltage integration time (variable).

For a constant V_{IN}:

$$V_{IN} = V_R\left[\frac{t_{RI}}{t_{SI}}\right].$$

The dual-slope converter accuracy is unrelated to the integrating resistor and capacitor values, as long as they are stable during a measurement cycle. An inherent benefit is noise immunity. Noise spikes are integrated, or averaged, to zero during the integration periods. Integrating ADCs are immune to the large conversion errors that plague successive approximation converters in high-noise environments. (See Figure 4.)

TC835 Operational Theory

The TC835 incorporates a system zero phase and integrator output voltage zero phase to the normal two-phase dual-slope measurement cycle. Reduced system errors, fewer calibration steps, and a shorter overrange recovery time result.

The TC835 measurement cycle contains four phases:

(1) System zero
(2) Analog input signal integration
(3) Reference voltage integration
(4) Integrator output zero

Internal analog gate status for each phase is shown in Table 1.

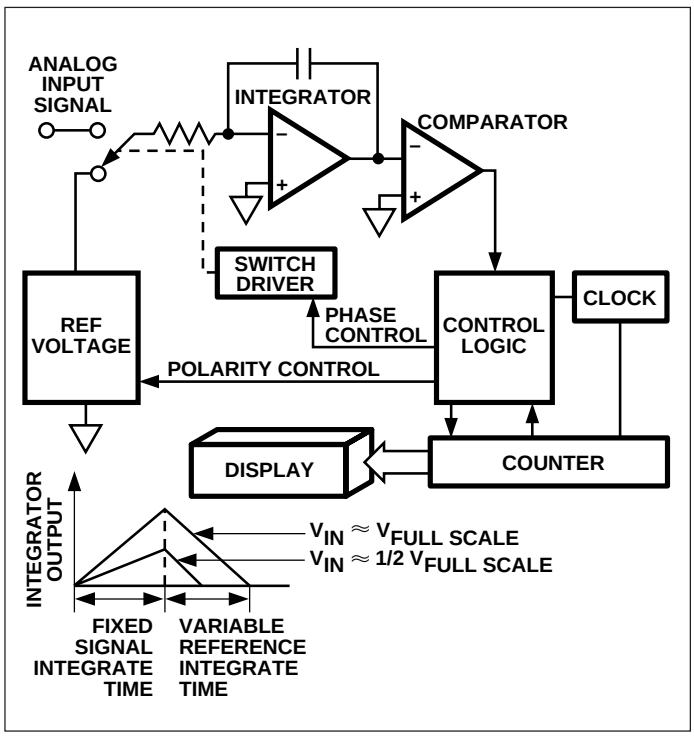


Figure 4. Basic Dual-Slope Converter

Table 1. Internal Analog Gate Status

Conversion Cycle Phase	Internal Analog Gate Status							Reference Schematic
	SW_I	SW_{RI}^+	SW_{RI}^-	SW_Z	SW_R	SW_1	SW_{IZ}	
System Zero				Closed	Closed	Closed		3B
Input Signal Integration	Closed							3C
Reference Voltage Integration		Closed*				Closed		3D
Integrator Output Zero						Closed	Closed	3E

***NOTE:** Assumes a positive polarity input signal. SW_{RI}^- would be closed for a negative input signal.

System Zero (Figure 3B)

During this phase, errors due to buffer, integrator, and comparator offset voltages are compensated for by charging C_{AZ} (auto-zero capacitor) with a compensating error voltage. With a zero input voltage the integrator output will remain at zero.

The external input signal is disconnected from the internal circuitry by opening the two SW_I switches. The internal input points connect to ANALOG COMMON. The reference capacitor charges to the reference voltage potential through SW_R. A feedback loop, closed around the integrator and comparator, charges the C_{AZ} capacitor with a voltage to compensate for buffer amplifier, integrator, and comparator offset voltages.

Analog Input Signal Integration (Figure 3C)

The TC835 integrates the differential voltage between the +INPUT and –INPUT pins. The differential voltage must be within the device common-mode range; - 1V from either supply rail, typically.

The input signal polarity is determined at the end of this phase.

Reference Voltage Integration (Figure 3D)

The previously-charged reference capacitor is connected with the proper polarity to ramp the integrator output back to zero. The digital reading displayed is:

$$\text{Reading} = 10{,}000 \left[\frac{\text{Differential Input}}{V_{REF}}\right].$$

Integrator Output Zero (Figure 3E)

This phase guarantees the integrator output is at 0V when the system zero phase is entered and that the true system offset voltages are compensated for. This phase normally lasts 100 to 200 clock cycles. If an overrange condition exists, the phase is extended to 6200 clock cycles.

Analog Section Functional Description

(In Reference to the 28-Pin Plastic Package)

Differential Inputs
(+INPUT, Pin 10 and –INPUT, Pin 9)

The TC835 operates with differential voltages within the input amplifier common-mode range. The input amplifier common-mode range extends from 0.5V below the positive supply to 1V above the negative supply. Within this common-mode voltage range, an 86 dB common-mode rejection ratio is typical.

The integrator output also follows the common-mode voltage. The integrator output must not be allowed to saturate. A worst-case condition exists, for example, when a large positive common-mode voltage with a near full-scale negative differential input voltage is applied. The negative input signal drives the integrator positive when most of its swing has been used up by the positive common-mode voltage. For these critical applications the integrator swing can be reduced to less than the recommended 4V full-scale swing, with some loss of accuracy. The integrator output can swing within 0.3V of either supply without loss of linearity.

ANALOG COMMON Input (Pin 3)

ANALOG COMMON is used as the –INPUT return during auto-zero and deintegrate. If –INPUT is different from ANALOG COMMON, a common-mode voltage exists in the system. This signal is rejected by the excellent CMRR of the converter. In most applications, –INPUT will be set at a fixed, known voltage (power supply common, for instance). In this application, ANALOG COMMON should be tied to the same point, thus removing the common-mode voltage from the converter. The reference voltage is referenced to ANALOG COMMON.

REFERENCE Voltage Input (REF IN, Pin 2)

The REF IN input must be a positive voltage with respect to ANALOG COMMON. Two reference voltage circuits are shown in Figure 5.

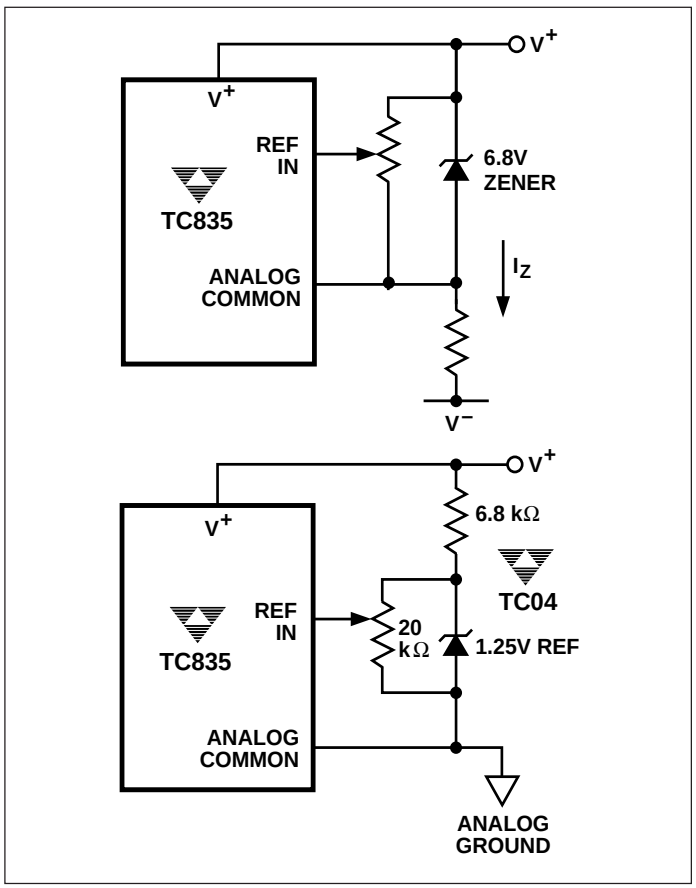


Figure 5. Using an External Reference

Digital Section Functional Description

The major digital subsystems within the TC835 are illustrated in Figure 6, with timing relationships shown in Figure 7. The multiplexed BCD output data can be displayed on LCD or LED display with the TC7211A (LCD) 4-digit display driver.

The digital section is best described through a discussion of the control signals and data outputs.

RUN/$\overline{\text{HOLD}}$ Input (Pin 25)

When left open, this pin assumes a logic "1" level. With a R/$\overline{\text{H}}$ = 1, the TC835 performs conversions continuously, with a new measurement cycle beginning every 40,002 clock pulses.

When R/$\overline{\text{H}}$ changes to a logic "0," the measurement cycle in progress will be completed, and data held and displayed as long as the logic "0" condition exists.

A positive pulse (>300nsec) at R/$\overline{\text{H}}$ initiates a new measurement cycle. The measurement cycle in progress when R/$\overline{\text{H}}$ initially assumed the logic "0" state must be completed before the positive pulse can be recognized as a single conversion run command.

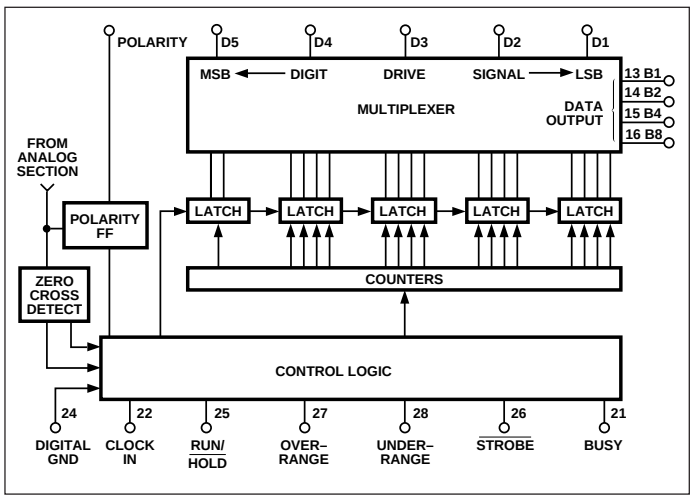


Figure 6. Digital Section Functional Diagram

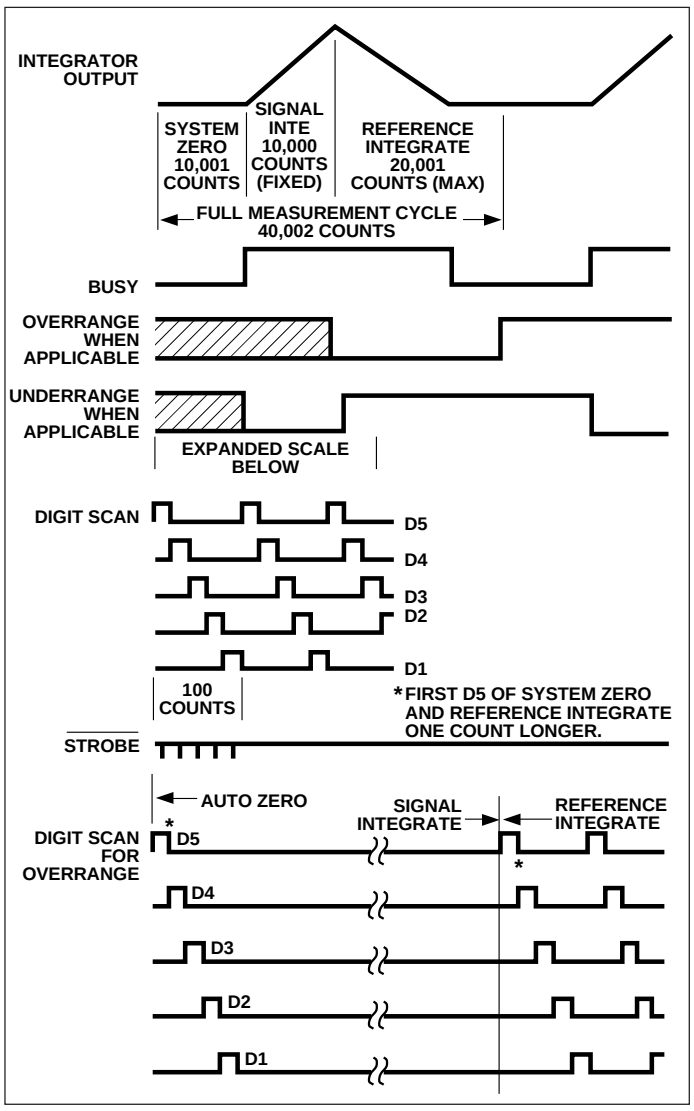


Figure 7. Timing Diagrams for Outputs

TC835

The new measurement cycle begins with a 10,001-count auto-zero phase. At the end of this phase the busy signal goes high.

$\overline{\text{STROBE}}$ Output (Pin 26)

During the measurement cycle, the $\overline{\text{STROBE}}$ control line is pulsed low five times. The five low pulses occur in the center of the digit drive signals (D_1, D_2, D_3, D_5, Figure 8).

D_5 (MSD) goes high for 201 counts when the measurement cycles end. In the center of the D_5 pulse, 101 clock pulses after the end of the measurement cycle, the first $\overline{\text{STROBE}}$ occurs for one-half clock pulse. After the D_5 digit strobe, D_4 goes high for 200 clock pulses. The $\overline{\text{STROBE}}$ goes low 100 clock pulses after D_4 goes high. This continues through the D_1 digit drive pulse.

The digit drive signals will continue to permit display scanning. $\overline{\text{STROBE}}$ pulses are not repeated until a new measurement is completed. The digit drive signals will not continue if the previous signal resulted in an overrange condition.

The active low $\overline{\text{STROBE}}$ pulses aid BCD data transfer to UARTs, processors and external latches. (See Application Note 16.)

BUSY Output (Pin 21)

At the beginning of the signal-integration phase, BUSY goes high and remains high until the first clock pulse after the integrator zero crossing. BUSY returns to the logic "0" state after the measurement cycle ends in an overrange condition. The internal display latches are loaded during the first clock pulse after BUSY, and are latched at the clock pulse end. The BUSY signal does not go high at the beginning of the measurement cycle, which starts with the auto-zero cycle.

OVERRANGE Output (Pin 27)

If the input signal causes the reference voltage integration time to exceed 20,000 clock pulses, the OVERRANGE output is set to a logic "1." The overrange output register is set when BUSY goes low, and is reset at the beginning of the next reference-integration phase.

UNDERRANGE Output (Pin 28)

If the output count is 9% of full scale or less (≤1800 counts), the underrange register bit is set at the end of BUSY. The bit is set low at the next signal-integration phase.

POLARITY Output (Pin 23)

A positive input is registered by a logic "1" polarity signal. The polarity bit is valid at the beginning of reference integrate and remains valid until determined during the next conversion.

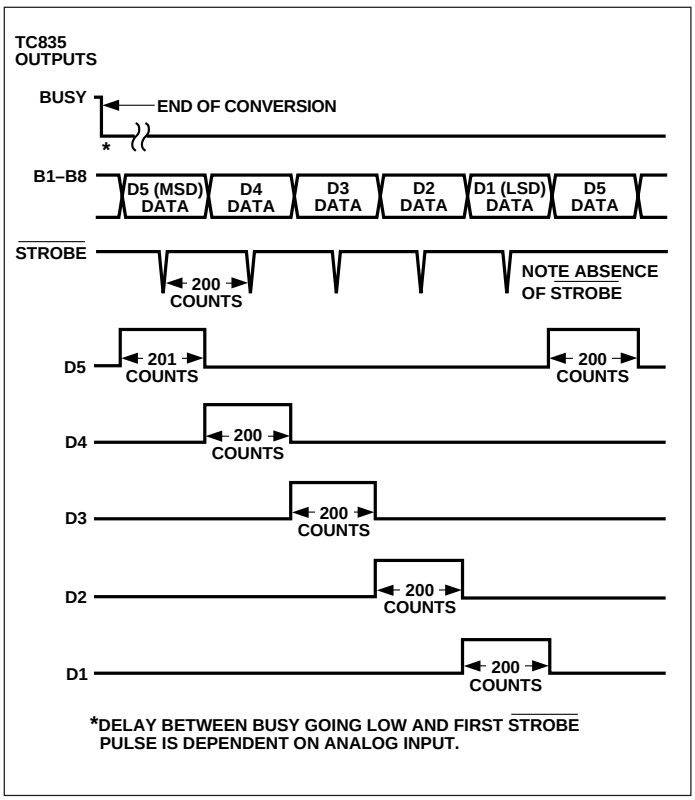


Figure 8. Strobe Signal Pulses Low Five Times per Conversion

The polarity bit is valid even for a zero reading. Signals less than the converter's LSB will have the signal polarity determined correctly. This is useful in null applications.

DIGIT Drive Outputs (Pins 12, 17, 18, 19 and 20)

Digit drive signals are positive-going signals. The scan sequence is D_5 to D_1. All positive pulses are 200 clock pulses wide, except D_5, which is 201 clock pulses wide.

All five digits are scanned continuously, unless an overrange condition occurs. In an overrange condition, all digit drives are held low from the final $\overline{\text{STROBE}}$ pulse until the beginning of the next reference-integrate phase. The scanning sequence is then repeated. This provides a blinking visual display indication.

BCD Data Outputs (Pins 13, 14, 15 and 16)

The binary coded decimal (BCD) bits B_8, B_4, B_2, B_1, are positive-true logic signals. The data bits become active simultaneously with the digit drive signals. In an overrange condition, all data bits are at a logic "0" state.

APPLICATIONS INFORMATION

Component Value Selection

The integrating resistor is determined by the full-scale input voltage and the output current of the buffer used to charge the integrator capacitor. Both the buffer amplifier and the integrator have a class A output stage, with 100 μA of quiescent current. A 20 μA drive current gives negligible linearity errors. Values of 5 μA to 40 μA give good results. The exact value of an integrating resistor for a 20 μA current is easily calculated.

$$R_{INT} = \frac{\text{full-scale voltage}}{20\ \mu A}$$

Integrating Capacitor

The product of integrating resistor and capacitor should be selected to give the maximum voltage swing that ensures the tolerance buildup will not saturate the integrator swing (approximately 0.3V from either supply). For ±5V supplies and ANALOG COMMON tied to supply ground, a ±3.5V to ±4V full-scale integrator swing is adequate. A 0.10 μF to 0.47 μF is recommended. In general, the value of C_{INT} is given by:

$$C_{INT} = \frac{[10{,}000 \times \text{clock period}] \times I_{INT}}{\text{Integrator output voltage swing}}$$

$$= \frac{(10{,}000)\ (\text{clock period})\ (20\ \mu A)}{\text{Integrator output voltage swing}}$$

A very important characteristic of the integrating capacitor is that it has low dielectric absorption to prevent rollover or ratiometric errors. A good test for dielectric absorption is to use the capacitor with the input tied to the reference. This ratiometric condition should read half-scale 0.9999, any deviation is probably due to dielectric absorption. Polypropylene capacitors give undetectable errors at reasonable cost. Polystyrene and polycarbonate capacitors may also be used in less critical applications.

Auto-Zero and Reference Capacitors

The size of the auto-zero capacitor has some influence on the noise of the system. A large capacitor reduces the noise. The reference capacitor should be large enough such that stray capacitance to ground from its nodes is negligible.

The dielectric absorption of the reference capacitor and auto-zero capacitor are only important at power-on, or when the circuit is recovering from an overload. Smaller or cheaper capacitors can be used if accurate readings are not required for the first few seconds of recovery.

Reference Voltage

The analog input required to generate a full-scale output is $V_{IN} = 2\ V_{REF}$.

The stability of the reference voltage is a major factor in the overall absolute accuracy of the converter. For this reason, it is recommended that a high-quality reference be used where high-accuracy absolute measurements are being made. Suitable references are:

Part Type	Manufacturer
TC04A	TelCom Semiconductor
TC9491	TelCom Semiconductor

Conversion Timing

Line Frequency Rejection

A signal integration period at a multiple of the 60 Hz line frequency will maximize 60 Hz "line noise" rejection.

A 200 kHz clock frequency will reject 60 Hz and 400 Hz noise. This corresponds to five readings per second.

Conversion Rate vs Clock Frequency

Oscillator Frequency (kHz)	Conversion Rate (Conv/Sec)
100	2.5
120	3
200	5
300	7.5
400	10
800	20
1200	30

Oscillator Frequency (kHz)	Line Frequency Rejection		
	60 Hz	50 Hz	400 Hz
50.000	•	•	•
53.333	—	—	•
66.667	•	—	•
80.000	—	—	•
83.333	—	•	•
100.000	•	•	•
125.000	—	•	•
133.333	—	—	•
166.667	—	—	•
200.000	•	—	•
250.000	—	•	•

The conversion rate is easily calculated:

$$\text{Conversion Rate (Readings 1/sec)} = \frac{\text{Clock Frequency (Hz)}}{4000}$$

TC835

Power Supplies and Grounds

Power Supplies

The TC835 is designed to work from ±5V supplies. For single +5V operation, a TC7660 can provide a – 5V supply.

Grounding

Systems should use separate digital and analog ground systems to avoid loss of accuracy.

Displays and Driver Circuits

TelCom Semiconductor manufactures two display decoder/driver circuits to interface the TC835 to an LCD or LED display. Each drive has 28 outputs for driving four 7-segment digit displays.

Device	Package	Description
TC7211AIPL	40-Pin Epoxy	4-Digit LCD Driver/Decoder

Several sources exist for LCD and LED display:

Manufacturer	Address	Display Type
Hewlett Packard Components	640 Page Mill Rd. Palo Alto, CA 94304	LED
Litronix, Inc.	19000 Homestead Rd. Cupertino, CA 94010	LED
AND	720 Palomar Ave. Sunnyvale, CA 94086	LCD and LED
Epson America, Inc.	3415 Kanhi Kawa St. Torrance, CA 90505	LCD

High-Speed Operation

The maximum conversion rate of most dual-slope A/D converters is limited by the frequency response of the comparator. The comparator in this circuit follows the integrator ramp with a 3 μsec delay, and at a clock frequency of 200 kHz (5 μsec period), half of the first reference integrate clock period is lost in delay. This means that the meter reading will change from 0 to 1 with a 50 μV input, 1 to 2 with 150 μV, 2 to 3 at 250 μV, etc. This transition at midpoint is considered desirable by most users; however, if the clock frequency is increased appreciably above 200 kHz, the instrument will flash "1" on noise peaks even when the input is shorted.

For many dedicated applications where the input signal is always of one polarity, the delay of the comparator need not be a limitation. Since the nonlinearity and noise do not increase substantially with frequency, clock rates of up to ~1 MHz may be used. For a fixed clock frequency, the extra count or counts caused by comparator delay will be a constant and can be subtracted out digitally.

The clock frequency may be extended above 200 kHz without this error, however, by using a low-value resistor in series with the integrating capacitor. The effect of the resistor is to introduce a small pedestal voltage on to the integrator output at the beginning of the reference integrate phase. By careful selection of the ratio between this resistor and the integrating resistor (a few tens of ohms in the recommended circuit), the comparator delay can be compensated and the maximum clock frequency extended by approximately a factor of 3. At higher frequencies, ringing and second-order breaks will cause significant nonlinearities in the first few counts of the instrument.

The minimum clock frequency is established by leakage on the auto-zero and reference capacitors. With most devices, measurement cycles as long as 10 seconds give no measurable leakage error.

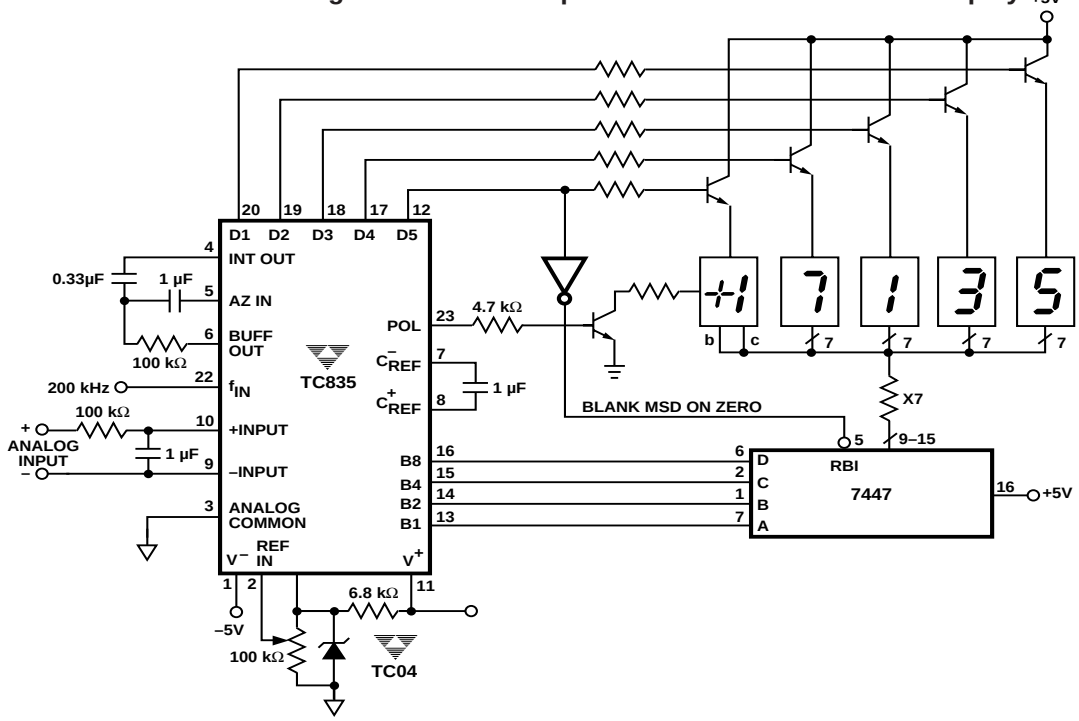
The clock used should be free from significant phase or frequency jitter. Several suitable low-cost oscillators are shown in the applications section. The multiplexed output means that if the display takes significant current from the logic supply, the clock should have good PSRR.

Zero-Crossing Flip-Flop

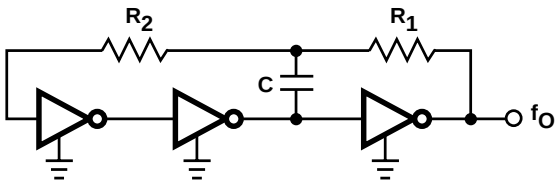
The flip-flop interrogates the data once every clock pulse after the transients of the previous clock pulse and half-clock pulse have died down. False zero-crossings caused by clock pulses are not recognized. Of course, the flip-flop delays the true zero-crossing by up to one count in every instance, and if a correction were not made, the display would always be one count too high. Therefore, the counter is disabled for one clock pulse at the beginning of the reference integrate (deintegrate) phase. This one-count delay compensates for the delay of the zero-crossing flip-flop, and allows the correct number to be latched into the display. Similarly, a one-count delay at the beginning of auto-zero gives an overload display of 0000 instead of 0001. No delay occurs during signal integrate, so that true ratiometric readings result.

TYPICAL APPLICATIONS DIAGRAMS

4-1/2 Digit ADC With Multiplexed Common Anode LED Display



RC Oscillator Circuit



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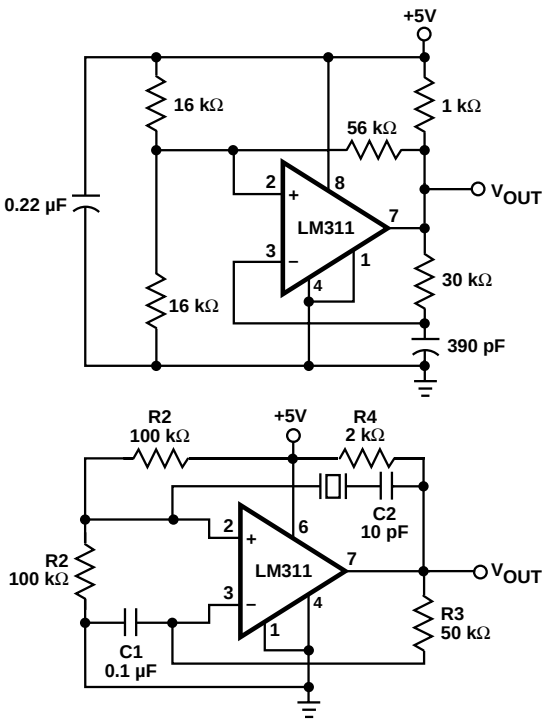
1. $f_O = \frac{1}{2\,C(0.41\,R_P + 0.7\,R_1)}$, $R_P = \frac{R_1\,R_2}{R_1 + R_2}$
   a. If $R_1 = R_2 = R_1$, $f \cong 0.55/RC$
   b. If $R_2 >> R_1$, $f \cong 0.45/R_1C$
   c. If $R_2 << R_1$, $f \cong 0.72/R_1C$
2. Examples:
   a. f = 120 kHz, C = 420 pF
      $R_1 = R_2 \approx 10.9\ k\Omega$
   b. f = 120 kHz, C = 420 pF, $R_2 = 50\ k\Omega$
      $R_1 = 8.93\ k\Omega$
   c. f = 120 kHz, C = 220 pF, $R_2 = 5\ k\Omega$
      $R_1 = 27.3\ k\Omega$

Comparator Clock Circuits



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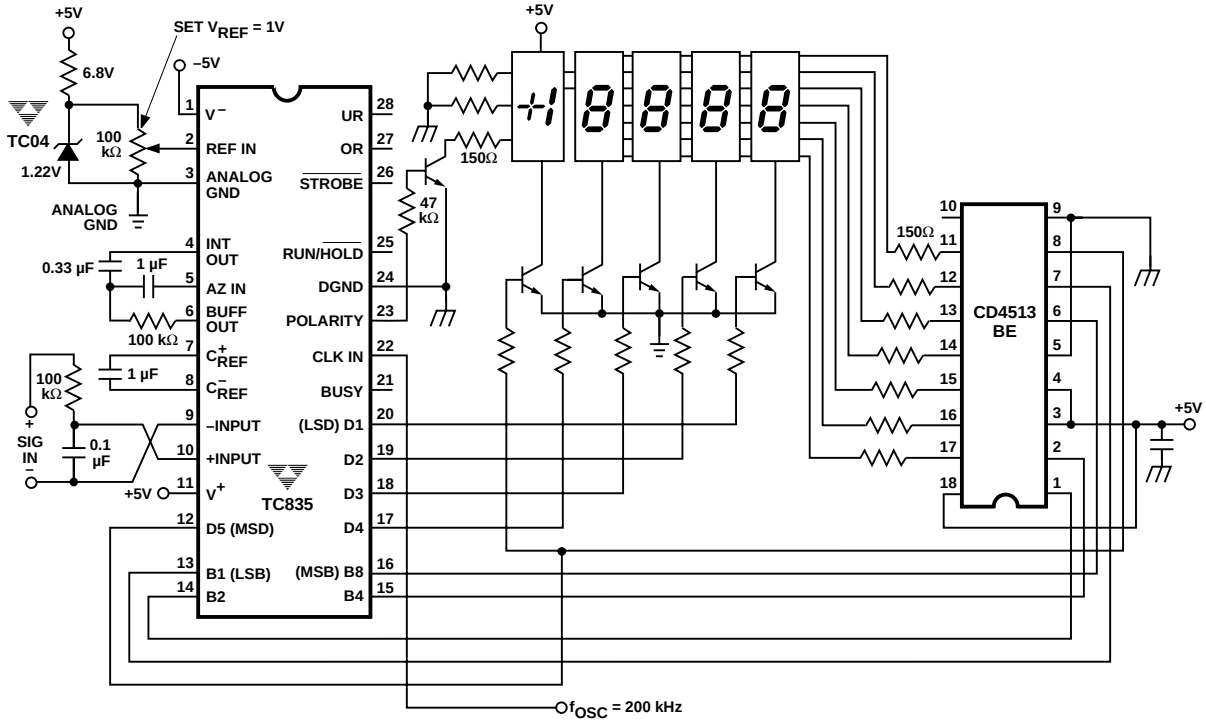
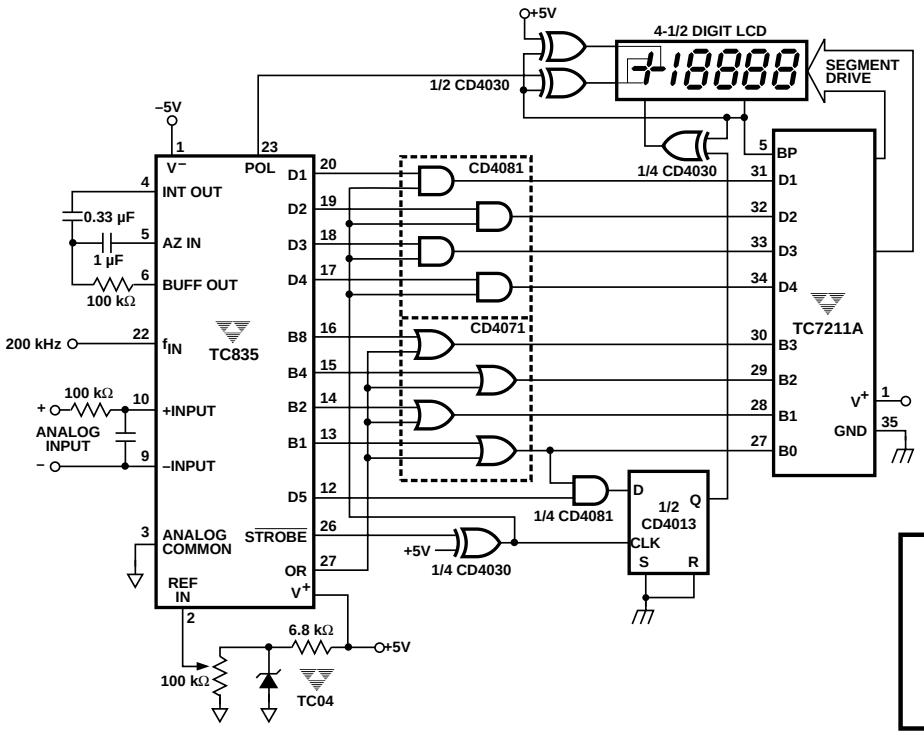
TYPICAL APPLICATIONS DIAGRAMS

4-1/2 Digit ADC with Multiplexed Common Cathode LED Display





Negative Supply Voltage Generator