Winbond Host Interface
SD/SDIO/MMC
Memory Card Bridge
W86L488

W86L488 Data Sheet Revision History

	Pages	Dates	Version	Version on Web	Main Contents
1		Aug. 2002	0.50		First published.
2		Dec. 2002	0.60		Add QFN package.
3	P6, P8, P10, P11, P24, P25, P26, P41, P42, P43, P44, P45, P46	May 21, 2003	0.70		1. Modify pin function of CLK, ACLK, BCLK, XASN, XDRQN, 2. Revised function description of Data Access Request & Interrupt. 3. Revised Reference Schematic
4					
5					
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LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Winbond customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Winbond for any damages resulting from such improper use or sales.

Winbond Electronics Corp.

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1. GENERAL DESCRIPTION

The W86L488 is a SD/SDIO/MMC interface bridge between microprocessor and SD/SDIO/MMC device. The data width of microprocessor is 8 or 16-bits. W86L488 supports synchronous or asynchronous type of host interface. It also supports DMA and Interrupt type of transfer mode to improve data transfer performance. The signals on the SD bus are captured or driven by W86L488. W86L488 is monitored and controlled by microprocessor via internal registers. W86L488 fits for most of IA devices, such as PDA, Cellular Phone, DSC, and MP3 player.

2. FEATURES

- Compliant with SD spec. Version 1.01. (Support SDIO)
- Compliant with MMC spec. Version 3.2.
- Simultaneously access two ports of SD/SDIO/MMC supported. (W86L488AY only)
- Support physical layer commands of SD/SDIO/MMC interface.
- Support SD/MMC and SPI mode for SD/SDIO/MMC interface.
- Support Keitaide-Music MMC card commands in SPI mode.
- Support SDIO interrupt and bus suspend/resume operation.
- Built-in 128 bytes data buffer for data transmit (send/receive).
- Support two types of Host microprocessor Interface access – synchronous and asynchronous.
- DMA and Interrupt transfer mode supported.
- Host microprocessor Interface support (Such as: Motorola's Dragon Ball series;Intel's Strong ARM, ARM series; Hitachi's SH2 series; Fujisui's FR30)
- Support 8/16 bits data bus of Microprocessor I/F.
- Built-in 3.58 to 25MHz crystal driver circuit, support external oscillator or crystal clock.
- Operation voltage: 2.7~3.6V for SD/SDIO/MMC, 2.5/3.3V for Host CPU interface.
- 48/64-pin QFN package.

Ordering Information

Part Number	Description	Package Type	Production Flow
W86L488Y	1Port SD/SDIO	48-PIN QFN	Commercial, 0°C to +70°C
W86L488AY	2Port SD/SDIO	64-PIN QFN	Commercial, 0°C to +70°C

3. PIN CONFIGURATIONS

3.1 W86L488Y Pin Configuration

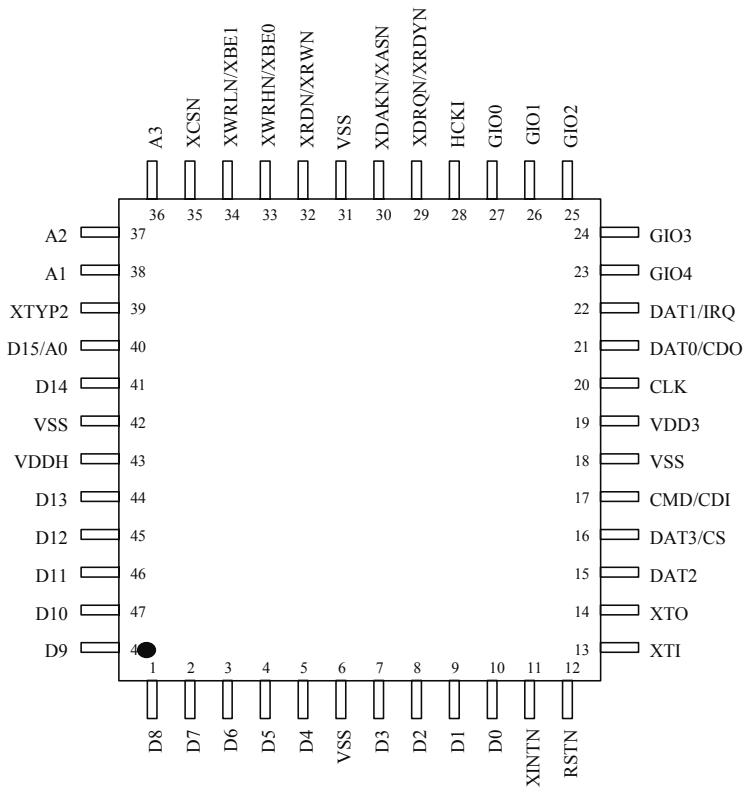


Fig. 3-1 W86L488Y Pin Assignment (48-pin QFN).

3.2 W86L488AY Pin Configuration

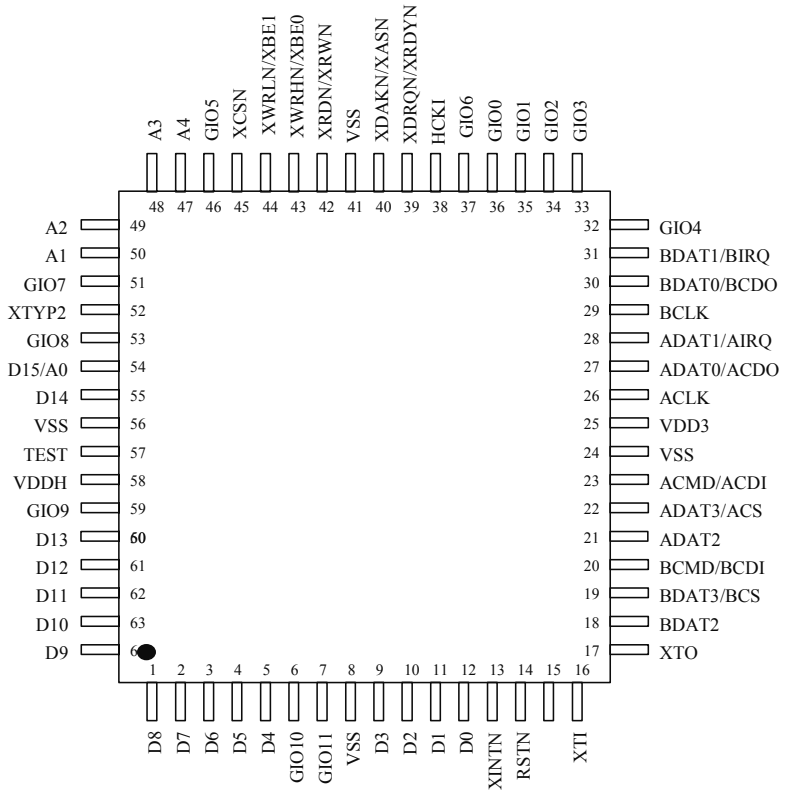


Fig. 3-2 W86L488AY Pin Assignment (64-pin QFN).

4. PIN DESCRIPTIONS

4.1 W86L488Y Pin Descriptions

Pin	Name	Type	Description
SD/SDIO/MMC Interface (VDD3 powered):			
21	DAT0/CDO	DO/DI	SD/MMC mode: Data line bit 0 signal for SD/SDIO card, data signal for MMC card. SPI mode: Card data output in SPI mode.
22	DAT1/IRQ	DO/DI	SD/MMC mode: Data line bit 1 signal for SD/SDIO card or interrupt request for SDIO. SPI mode: No use.
15	DAT2	DO/DI	SD/MMC mode: Data line bit 2 signal for SD/SDIO card or read wait for SDIO. SPI mode: No use.
16	DAT3/CS	DO/DI	SD/MMC mode: Data line bit 3 or Card detect for SD/SDIO card. SPI mode: Card select.
17	CMD/CDI	DO/DI	SD/MMC mode: Command response for SD/SDIO card or MMC card. SPI mode: Card data input. This pin will tri-state when the command is not driven.
20	CLK	DO	Clock output signal for SD/SDIO card or MMC card. This pin will stay at high or low when card clock is not needed depends on the state of CKDH bit setting.

4.1 W86L488Y Pin Descriptions, continued

Pin	Name	Type	Description
Crystal Driver (VDD3 powered):			
13	XTI	DI	Clock driver input signal, may be used as external clock input.
14	XTO	DO	Clock driver output signal.
Host Interface Signal (VDDH powered):			
28	HCKI	DI	Host clock input.
35	XCSN	DI	Chip select input pin, active low.
36:38	A[3:1]	DI	Address input pins.
40	D15/A0	DI/DO	Data bus D15 pin, D[15:8] is the high byte of the data bus, D15 also used as A0 when 8-bit CPU data size. In 8-bit mode, internal register high byte (D15:8) will accessed at data bus [7:0] when A0 = 1, low byte (D7:0) will accessed at data bus [7:0] when A0 = 0.
41	D14	DI/DO	Data bus D14 pin.
44:48	D[13:9]	DI/DO	Data bus D[13:9] pins.
1:5	D[8:4]	DI/DO	Data bus D[8:4] pins, D[7:0] is the low byte of the data bus.
7:10	D[3:0]	DI/DO	Data bus D[3:0] pins.
33	XWRHN/ XBE0	DI	Type 1: High byte (D15 to D8) write control pin, active low. Type 2: High byte (D15 to D8) data valid pin, active low.
34	XWRLN/ XBE1	DI	Type 1: Low byte (D7 to D0) write control pin, active low. Type 2: Low byte (D7 to D0) data valid pin, active low.
11	XINTN	DO	Interrupt request pin, active low.

4.1 W86L488Y Pin Descriptions, continued

Pin	Name	Type	Description
32	XRDN/ XRWN	DI	Type 1: Read control pin, active low. Type 2: Read write control pin, 1: read 0: write
30	XASN	DI	Type 1: None. Type 2: Bus access cycle start pin, active low.
29	XDRQN/ XRDYN	DO	Type 1: Data Access request pin, active low. Type 2: Bus cycle complete pin, active low.
39	XTYP2	DI	Host interface type 2 select pin, 0: type 1 mode. 1: type 2 mode.
General I/O Port Signal (VDD3 powered)::			
27:23	GIO[0:4]	DI/DO	5-bit general input output port signals. GIO0 pin can be used as dedicate card insert detect. Input and active low in default.
Other Signal (VDDH powered):			
12	RSTN	DI	Reset input, hardware reset input, active low.

4.1 W86L488Y Pin Descriptions, continued

Pin	Name	Type	Description
Power:			
19	VDD3	DP	Power supply 3.3V.
43	VDDH	DP	Power supply 2.5V or 3.3V for Host I/F. *1
6,18, 31,42	VSS x4	DP	Ground (4 pins).

Type: DP is Power, DI is Digital Input, DO is Digital Output.

Note*1: When Host I/F voltage is 2.5V, VDDH connects to 2.5V.

When Host I/F voltage is 3.3V, VDDH connects to 3.3V.

4.2 W86L488AY Pin Descriptions

Pin	Name	Type	Description
SD/SDIO/MMC Interface (VDD3 powered):			
27 30	ADAT0/ACDO BDAT0/BCDO	DO/DI	SD/MMC mode: Data line bit 0 signal for SD/SDIO card, data signal for MMC card. SPI mode: Card data output in SPI mode.
28 31	ADAT1/AIRQ BDAT1/BIRQ	DO/DI	SD/MMC mode: Data line bit 1 signal for SD/SDIO card or interrupt request for SDIO. SPI mode: No use.
21 18	ADAT2 BDAT2	DO/DI	SD/MMC mode: Data line bit 2 signal for SD/SDIO card or read wait for SDIO. SPI mode: No use.

4.2 W86L488AY Pin Descriptions, continued

Pin	Name	Type	Description
22 19	ADAT3/ACS BDAT3/BCS	DO/DI	SD/MMC mode: Data line bit 3 or Card detect for SD/SDIO card. SPI mode: Card select.
23 20	ACMD/ACDI BCMD/BCDI	DO/DI	SD/MMC mode: Command response for SD/SDIO card or MMC card. SPI mode: Card data input. This pin will tri-state when the command is not driven.
26 29	ACLK BCLK	DO	Clock output signal for SD/SDIO card or MMC card. This pin will stay at high or low when card clock is not needed depends on the state of CKDH bit setting.
Crystal Driver (VDD3 powered):			
16	XTI	DI	Clock driver input signal, may be used as external clock input.
17	XTO	DO	Clock driver output signal.
Host Interface Signal (VDDH powered):			
38	HCKI	DI	Host clock input.
45	XCSN	DI	Chip select input pin, active low.
47:50	A[4:1]	DI	Address input pins.
54	D15/A0	DI/DO	Data bus D15 pin, D[15:8] is the high byte of the data bus, D15 also used as A0 when 8-bit CPU data size. In 8-bit mode, internal register high byte (D15:8) will accessed at data bus [7:0] when A0 = 1, low byte (D7:0) will accessed at data bus [7:0] when A0 = 0.
55	D14	DI/DO	Data bus D14 pin.
60:64	D[13:9]	DI/DO	Data bus D[13:9] pins.
1:5	D[8:4]	DI/DO	Data bus D[8:4] pins, D[7:0] is the low byte of the data bus.
9:12	D[3:0]	DI/DO	Data bus D[3:0] pins.

4.2 W86L488AY Pin Descriptions, continued

Pin	Name	Type	Description
43	XWRHN/ XBE0	DI	Type 1: High byte (D15 to D8) write control pin, active low. Type 2: High byte (D15 to D8) data valid pin, active low.
44	XWRLN/ XBE1	DI	Type 1: Low byte (D7 to D0) write control pin, active low. Type 2: Low byte (D7 to D0) data valid pin, active low.
42	XRDN/ XRWN	DI	Type 1: Read control pin, active low. Type 2: Read write control pin, 1: read 0: write
13	XINTN	DO	Interrupt request pin,active low.
40	XASN	DI	Type 1: None. Type 2: Bus access cycle start pin, active low.
39	XDRQN/ XRDYN	DO	Type 1: Data Access request pin, active low. Type 2: Bus cycle complete pin, active low.
52	XTYP2	DI	Host interface type 2 select pin, 0: type 1 mode. 1: type 2 mode.

4.2 W86L488AY Pin Descriptions, continued

Pin	Name	Type	Description
General I/O Port Signal:			
46, 32:36	GIO[5:0]	DI/DO	6-bit general input output port signals of port A. GIO0 pin can be used as dedicate card insert detection of port A. Input and active low in default (GIO[4:0] powered by VDD3, GIO5 powered by VDDH).
7, 6, 59, 53, 51,37	GIO[11:6]	DI/DO	6-bit general input output port signals of port B. GIO6 pin can be used as dedicate card insert detection of port B. Input, active low in default (GIO6 powered by VDD3, GIO[11:7] powered by VDDH).
Other Signal (VDDH powered):			
14	RSTN	DI	Reset input, hardware-reset input, active low.
57	TEST	DI	Test input, must connected to VSS.
Power:			
25	VDD3	DP	Power supply 3.3V.
58	VDDH	DP	Power supply 2.5V or 3.3V for Host I/F. *2
8, 24, 41, 56	VSS x4	DP	Ground (4 pins).

Type: DP is Power, DI is Digital Input, DO is Digital Output.

Note*2: When Host I/F voltage is 2.5V, VDDH connects to 2.5V.

When Host I/F voltage is 3.3V, VDDH connects to 3.3V.

5. BLOCK DIAGRAM

5.1 W86L488Y Block Diagram

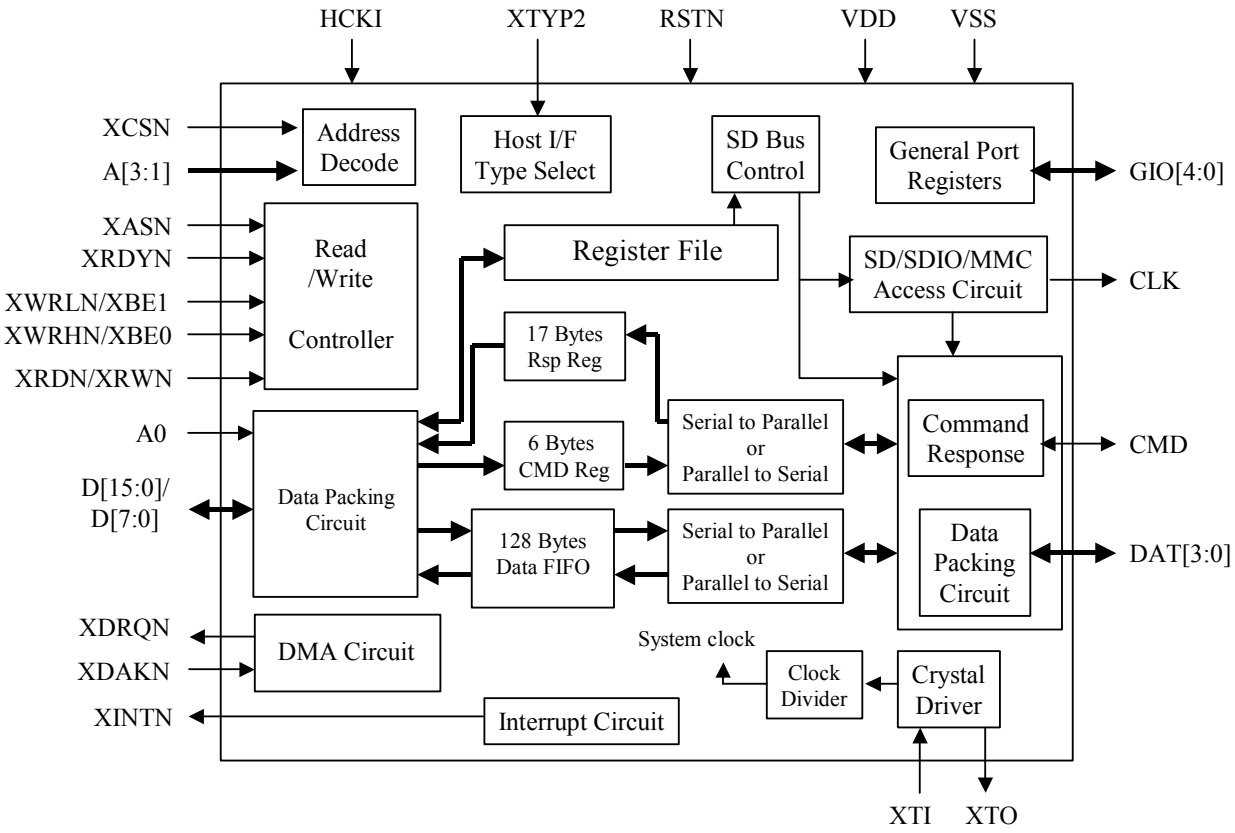


Fig. 5-1 Block Diagram of W86L488Y.

5.2 W86L488AY Block Diagram

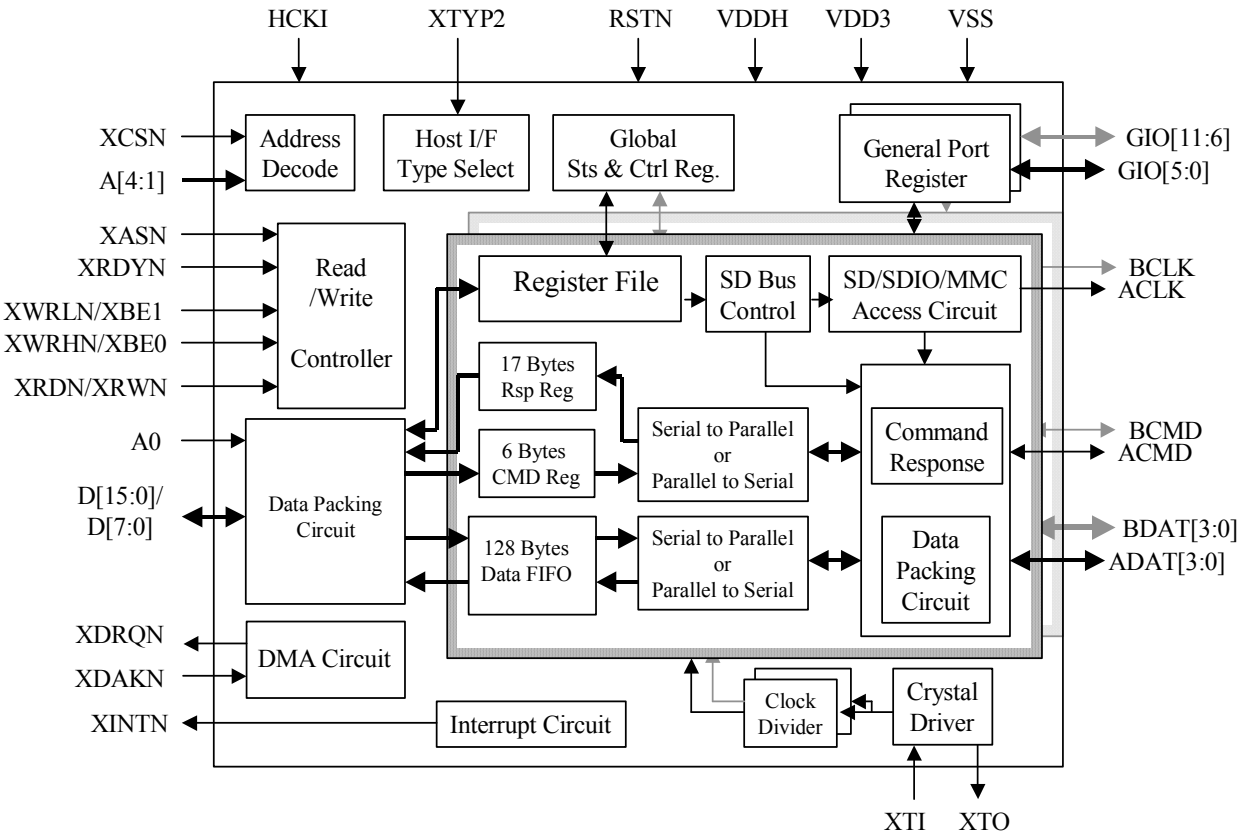


Fig. 5-2 Block Diagram of W86L488AY.

6. REGISTER

The registers in the W86L488Y/AY are direct access registers and indirect access registers. The direct access registers and indirect access registers are listed as follows:

6.1 W86L488Y Register

Addr A[3:1]	Register Name (note 1)	Content (note 2)															
		Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Direct Access Registers:																	
000	Command Pipe Reg. (WO) Response Reg. (RO)	Command pipe registers / Response registers															
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
001	Status Reg. (RO)	Status								-	-	-	-	-	-	-	-
		0	0	0	0	1	0	0	0								
001	Control Reg. (bit 8 WO, R/W)	-	-	-	-	-	-	-	Control								
									0	0	0	0	0	0	0	0	1
010	Receive Data Buffer (R/O)	Receive data buffer															
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
010	Transmit Data Buffer (WO)	Transmit data buffer															
		X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
011	Interrupt Status Reg. (RO)	Interrupt status								-	-	-	-	-	-	-	-
		0	0	0	0	0	0	0	0								
011	Interrupt Enable Reg. (R/W)	-	-	-	-	-	-	-	-	Interrupt enable							
										0	0	0	0	0	1	1	0
100	General I/O Port Data Reg. (R/W)	GIO data								-	-	-	-	-	-	-	-
		0	0	0	X	X	X	X	X								
100	General I/O Port Control Reg. (R/W)	-	-	-	-	-	-	-	-	GIO control							
										0	0	0	0	0	0	0	0
101	General IP Interrupt Status Reg. (RC)	GIO interrupt status								-	-	-	-	-	-	-	-
		0	0	0	0	0	0	0	0								
101	General IP	-	-	-	-	-	-	-	-	GIO interrupt enable							

	Interrupt Enable Reg. (R/W)									0	0	0	0	0	0	0	0
110	Index Address Reg. (R/W)	-	-	-	-	-	-	-	-				Index address				
										0	0	0	0	0	0	0	0
111	Index Data Register	Index data register															
		X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
Indirect Access Registers:																	
0000	Extend Status Reg. (RO)	Extend status								-	-	-	-	-	-	-	-
		0	0	0	0	0	X	-	-								
0000	Setting Reg. (R/W)	-	-	-	-	-	-	Setting register									
								0	0	0	1	0	0	0	0	0	1
0001	SDIO Bus Function Reg. (RO)	M_Fn				S_Fn				-	-	-	-	-	-	-	-
		1	1	1	1	1	1	1	1								
0001	SDIO Bus Control Reg. (bit[7:6] RO, R/W)	-	-	-	-	-	-	-	-	SDIO bus control							
										0	0	0	0	0	0	0	0
0010	Master Data Format Register (R/W)			-	-	Data length (master)											
		0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
0011	Master Block Count Register (R/W)		-	-	-	-	-	-	Block count (master)								
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
0100	Slave Data Format Register (R/W)			-	-	Data length (slave)											
		0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
0101	Slave Block Count Register (R/W)		-	-	-	-	-	-	Block count (slave)								
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
0110	Nac Time-out Register (R/W)	Nac time out register															
		0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
0111	Error Status Reg. (RO)	Error status										-	-	-	-	-	-
		0	0	0	0	0	0	0	0	0	0						
1000	Buffer Service Length Register (RO)	Blv	Buffer service length							-	-	-	-	-	-	-	-
		0	0	0	0	0	0	0	0								
1000	Ready & Data	-	-	-	-	-	-	-	-	F	-	-	-	-	-	-	d8

	Size Register (R/W)									0	0	0	0	0	0	0	0
1001	Test Register (R/W)	Test register															
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1010	ID Code Register (RO)	ID Code register															
		0	1	0	0	1	0	0	0	1	0	0	0	1	1	0	0

Note 1: R/W means the register can be read and write.

RO means the register is read only.

RC means the register is read only and read clear.

WO means the register is write only.

Note 2: The data bit in the content is the initial value during hardware reset.

0: the bit value is 0.

1: the bit value is 1.

X: the bit value is unknow.

-: Undefined bit in the register and the value will read 0.

6.2 W86L488AY Register

Addr A[4:1]	Register Name (note 1)	Content (note 2)															
		Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Global Registers:																	
1000	Global Status Reg. (RO)	Global status register															
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1001	Global Control Reg. (bit[9:8] RO,R/W)	Global control register															
		0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0
1010	Ready & Data Size Register (R/W)	-	-	-	-	-	-	-	-	F	-	-	-	-	-	-	d8
										0	0	0	0	0	0	0	0
Direct Access Registers:																	
0000	Command Pipe Reg. (WO) Response Reg. (RO)	Command pipe registers / Response registers															
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0001	Status Reg. (RO)	Status								-	-	-	-	-	-	-	-
		0	0	0	0	1	0	0	0								
0001	Control Reg. (bit 8 WO, R/W)	-	-	-	-	-	-	-	Control								
									0	1/1	0	0	0	0	0	0	1
0010	Receive Data Buffer (R/O)	Receive data buffer															
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0010	Transmit Data Buffer (WO)	Transmit data buffer															
		X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
0011	Interrupt Status Reg. (RO)	Interrupt status								-	-	-	-	-	-	-	-
		0	0	0	0	0	0	0	0								
0011	Interrupt Enable Reg. (R/W)	-	-	-	-	-	-	-	-	Interrupt enable							
										0	0	0	0	0	1	1	0
0100	General I/O Port Data Reg. (R/W)	GIO data								-	-	-	-	-	-	-	-
		0	0	X	X	X	X	X	X								
0100	General I/O Port Control Reg. (R/W)	-	-	-	-	-	-	-	-			GIO control					
										0	0	0	0	0	0	0	0

0101	General IP Interrupt Status Reg. (RC)			GIO interrupt status						-	-	-	-	-	-	-	-
		0	0	0	0	0	0	0	0								
0101	General IP Interrupt Enable Reg. (R/W)	-	-	-	-	-	-	-	-			GIO interrupt enable					
										0	0	0	0	0	0	0	0
0110	Index Address Reg. (R/W)	-	-	-	-	-	-	-	-				Index address				
										0	0	0	0	0	0	0	0
0111	Index Data Register	Index data register															
		X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
Indirect Access Registers:																	
0000	Extend Status Reg. (RO)	Extend status								-	-	-	-	-	-	-	-
		0	0	0	0	0	X	-	-								
0000	Setting Reg. (R/W)	-	-	-	-	-	-	Setting register									
								0	0	0	1	0	0	0	0	0	1
0001	SDIO Bus Function Reg. (RO)	M_Fn				S_Fn				-	-	-	-	-	-	-	-
		1	1	1	1	1	1	1	1								
0001	SDIO Bus Control Reg. (bit[7:6] RO, R/W)	-	-	-	-	-	-	-	-	SDIO bus control							
										0	0	0	0	0	0	0	0
0010	Master Data Format Register (R/W)			-	-	Data length (master)											
		0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
0011	Master Block Count Register (R/W)		-	-	-	-	-	-	Block count (master)								
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
0100	Slave Data Format Register (R/W)			-	-	Data length (slave)											
		0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
0101	Slave Block Count Register (R/W)		-	-	-	-	-	-	Block count (slave)								
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
0110	Nac Time-out Register (R/W)	Nac time out register															
		0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
0111	Error Status Reg. (RO)	Error status										-	-	-	-	-	-
		0	0	0	0	0	0	0	0	0	0						

1000	Buffer Service Length Register (RO)	Blv	Buffer service length							-	-	-	-	-	-	-	-
		0	0	0	0	0	0	0	0								
1000	Ready & Data Size Register (RO)	-	-	-	-	-	-	-	-	F	-	-	-	-	-	-	d8
										0	0	0	0	0	0	0	0
1001	Test Register (R/W)	Test register															
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1010	ID Code Register (RO)	ID Code register															
		0	1	0	0	1	0	0	0	1	0	0	0	1	1	0	0

Note 1: R/W means the register can be read and write.

RO means the register is read only.

RC means the register is read only and read clear.

WO means the register is write only.

Note 2: The data bit in the content is the initial value during hardware reset.

0: the bit value is 0.

1: the bit value is 1.

X: the bit value is unknow.

-: Undefined bit in the register and the value will read 0.

7. FUCNTIONAL DESCRIPTION

7.1 Host Interface

The Host interface type may be type 1 or type 2 and the data size of the data bus may be 16-bit or 8-bit.

Host Interface Type 1:

The Host interface type 1 is selected when XTYP2 pin is low. Figure 7-1 shows the timing of 16-bit CPU read and write in type 1. Figure 7-2 is the timing of 16-bit CPU write high byte and write low byte. Figure 7-3 and 7-4 show the timing of CPU 8-bit data bus read and write in type 1.

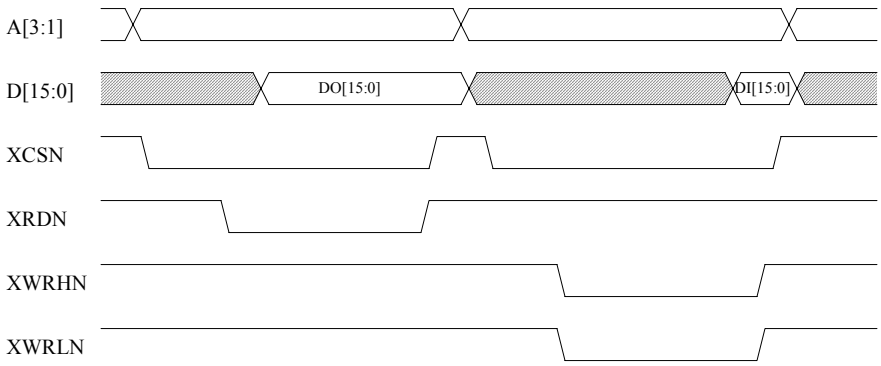


Fig. 7-1 16-bit Read and Write Access in Host I/F Type 1.

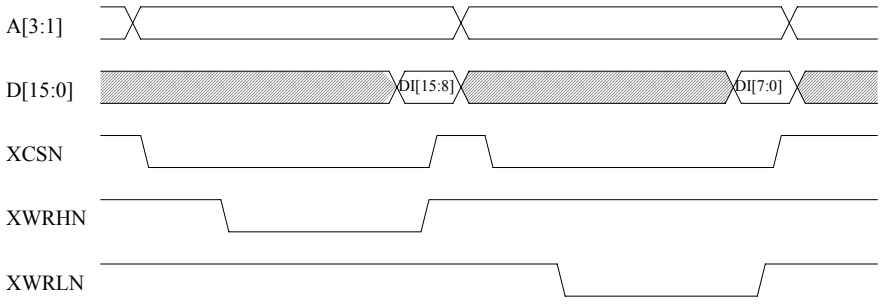


Fig. 7-2 High Byte and Low Byte Write Access in Host I/F Type 1.

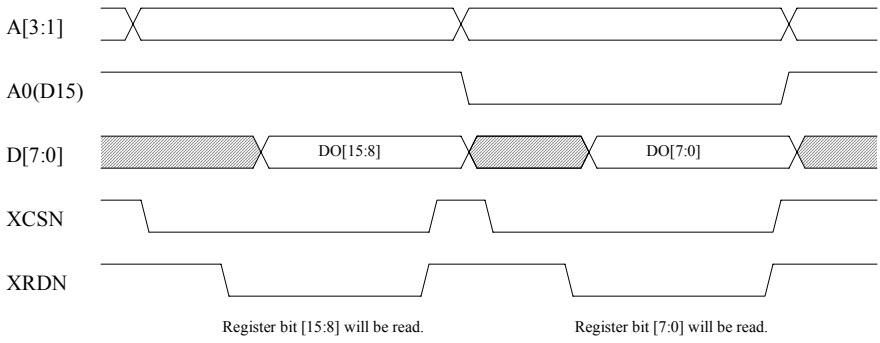


Fig. 7-3 CPU 8-bit Data Bus Read Access in Host I/F Type 1.

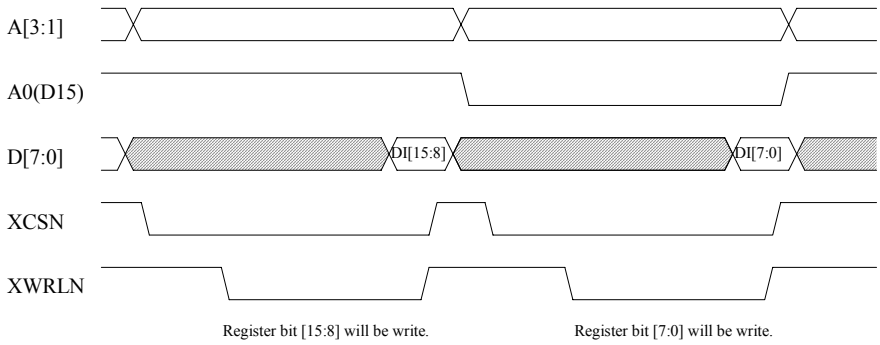


Fig. 7-4 CPU 8-bit Data Bus Write Access in Host I/F Type 1.

Host Interface Type 2:

The Host interface type 2 is selected when XTYP2 pin is high. The data size of the CPU data bus may be 16-bit or 8-bit and the access cycle may be in 3-cycle or 2-cycle. Figure 7-5 shows the timing of CPU read write in type 2 and the access cycle is 3-cycle access, figure 7-6 shows the timing of CPU read write in type 2 and the access cycle is 2-cycle access.

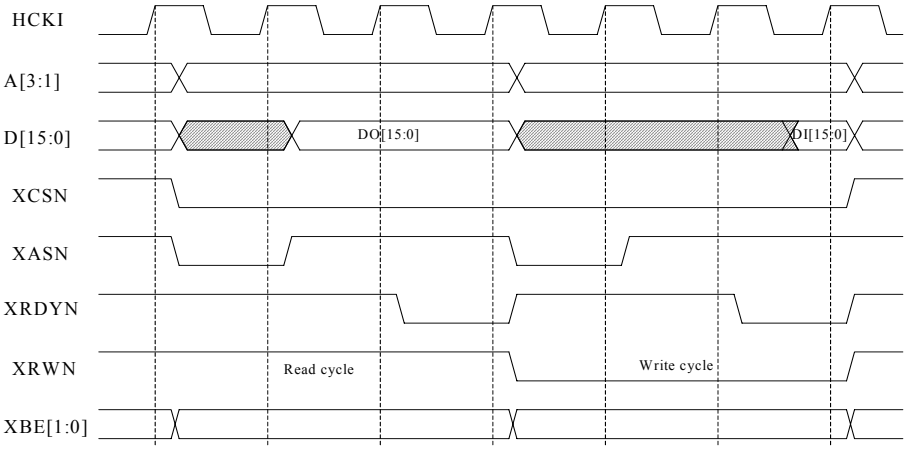


Fig. 7-5 Read and Write Timing in Host I/F Type 2, 3-Cycle Access.

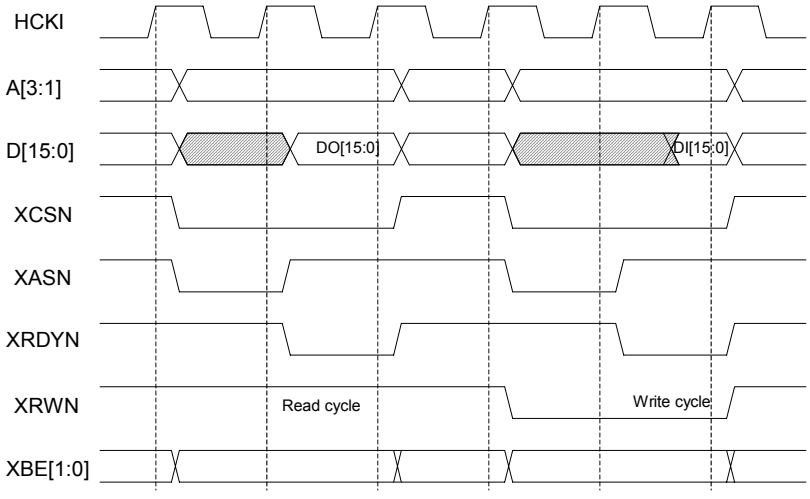


Fig. 7-6 Read and Write Timing in Host I/F Type 2, 2-Cycle Access.

Data Access Request:

Data access request XDRQN is used to notify the Host that the Host should write data to the transmit data buffer or read data from the receive data buffer in data write to the card or data read from the card. The Data access request action also effective when Host interface type 2 is selected.

During data transmit to the card, the XDRQN will active if the data write command has been transfer to the card and the transmit data buffer have not enough data to transmit to the card. The XDRQN will not active if the transmit data buffer have enough data to transmit to the card. The last byte of the data should placed at bit [15:8] if the data length is odd byte and CPU data size is 16-bit.

During data receive from the card, the XDRQN will active if the data read command has been transfer to the card and the data have been received in the receive data buffer. The XDRQN will not active if the data read command has been executed completedly and the receive data buffer is read out. The last byte of the data is located at bit [7:0] if the data length is odd byte and CPU data size is 16-bit.

There are two types of data access request waveform, one is single access mode and the other is burst access mode. Single access mode is configured if DABST = low, XDRQN will inactive after each access receive or transmit data buffer, the XDRQN will re-active after four clock later. Figure 7-7 shows the waveform of Host access receive data buffer in single access mode (DABST = low). Burst access mode is configured if DABST = high, XDRQN will hold at active state until the data has been transferred completedly. The Host can access receive or transmit data buffer with higher speed continuously and regardless of the system clock. Figure 7-8 is the waveform of Host access transmit data buffer in burst mode (DABST = high).

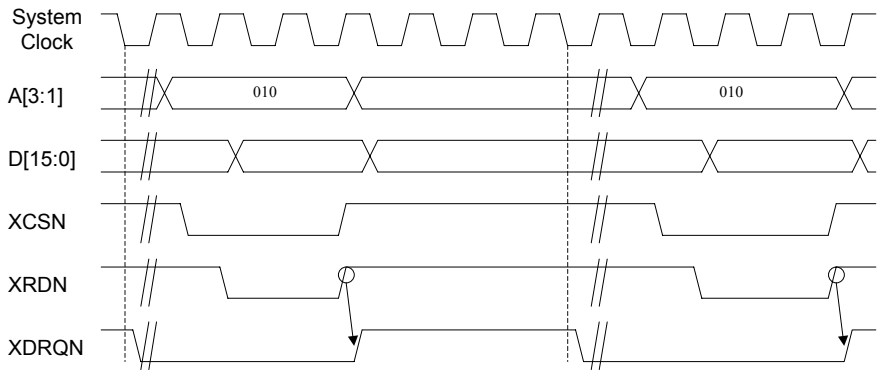


Fig. 7-7 Host Read Receive Data Buffer in Single Access Mode (DABST = low).

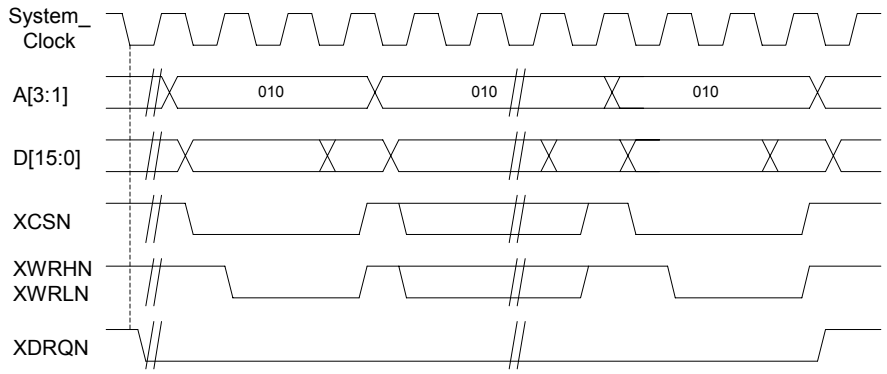


Fig. 7-8 Host Write Transmit Data Buffer in Burst Access Mode (DABST = high).

Interrupt:

The XINTN pin is used to notify Host that something happens or error occurs. The INT bit of status register can be read and check repeatedly if the Host cannot accept XINTN pin. XINTN will active (low) at the falling edge of system clock if any bit in the interrupt register is high, XINTN pin will return to high when write high to the related bit of the interrupt status register except DRQ interrupt in, the XINTN pin will go low again at four system clock cycles later if any other interrupt event is still pending.

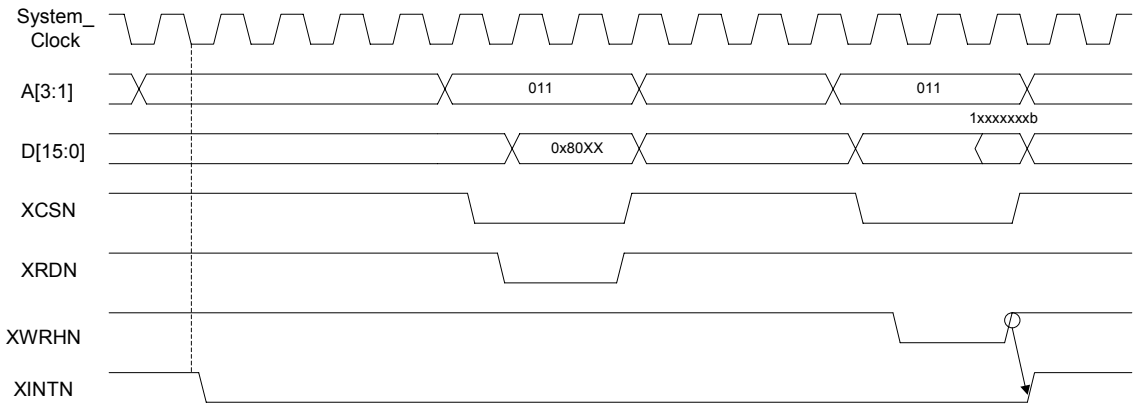


Fig. 7-9 Timing of Interrupt in.

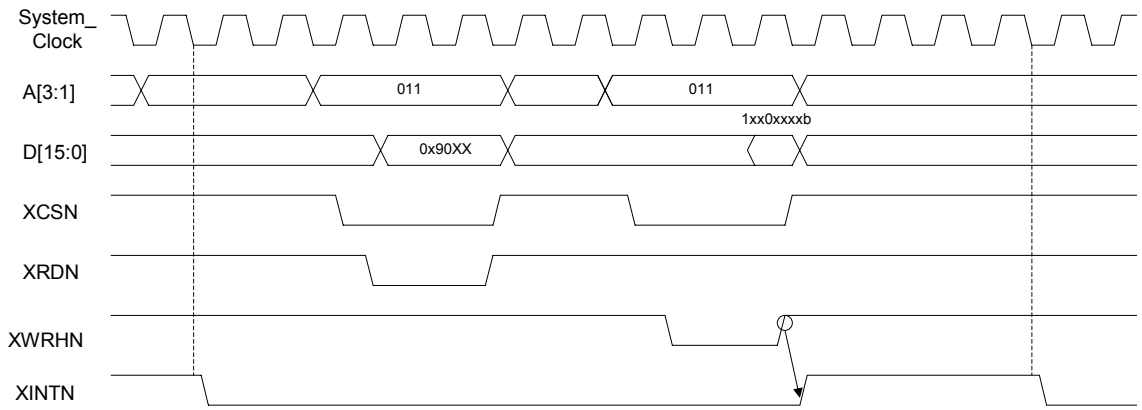


Fig. 7-10 Timing of Interrupt in (XINTN pin goes to low again).

7.2 Card Inserting and Removing

There are two method for Host to detect SD/SDIO or MMC card inserting or removing through W86L488, the first method is detected by CD/DAT3 pin, the second method is a dedicate switch on the SD/MMC slot can be connected to the GIO0 pin and set GIO0 to input direction. These two methods can be performed even if the W86L488 is in power down state.

Method 1, CD/DAT3 as card detection:

The CD/DAT3 of SD bus can be used as card detection if no data transfer on the DAT3, if SIEN bit of the control register is low and CD_IE and INT_E on the interrupt enable register are all high, card inserting or removing will generate interrupt. Host must read the interrupt status register and re-check the card state by read the CD bit on the extend status register. This detection method will not effective when wide bus on the SD bus is transfer. MMC card may not support this detection method.

Method 2, GIO0, GIP6 as card detection (inserting):

Some SD/MMC slot support external switch for card existing detection, the switch will on when SD/SDIO or MMC card is exist. GIO0 and GIP6 with a pull high resister can be used as card detection of port A and port B. In port A the Host can disable the GOEN0 bit on the general I/O port control register and enable the GIT_EN0 bit on the general I/O port interrupt enable register and enable GIT_IE and INT_E bits on the interrupt enable register. SD or MMC card inserting or removing will change the switch state then change the state of GIO0 pin and then generate interrupt to the Host. Host may re-check the card state by read the GIN0 bit on the general I/O port data register. The card insert status of port A and port B also can be read in the global status and control register.

Figure 7-10 shows the waveform of GIO0 and GIOx when card insert and remove if GIO0 as card insert and GIOx as write protect input.

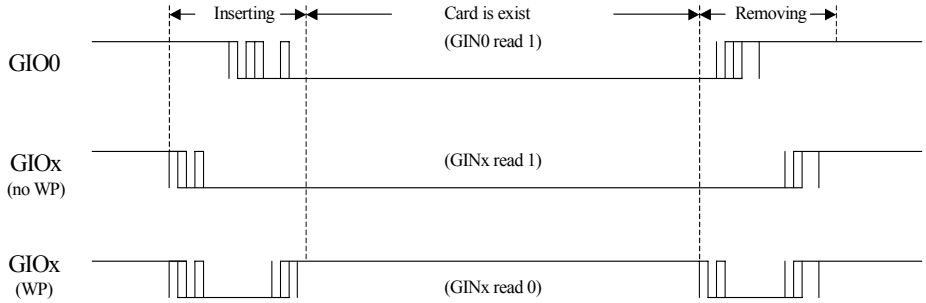


Fig. 7-10 Card Insert use GIO0 and Write Protect use GIOx.

7.3 Reset Action

Hardware Reset:

Hardware reset is performed by setting RSTN pin to low state for at least 1uS. The CPU data size will set to 16-bit default, all the registers will set to default value. The receive and transmit data buffer will be cleared, all the internal logic will be reset to initial state.

Software Reset:

Software reset is executed by write the RST bit of the control register to 1, all the internal logic will be reset to initial state and receive and transmit data buffer will be cleared, but the content of registers are not affected. In W86L488AY, the port A and port B will reset at the same time if global software reset in the global control register is set.

Data Buffer Reset:

Data buffer reset is used to reset the receive data buffer and transmit data buffer simutaneously, the serial interface command will affected if the data receive or transmit command is progressing. Internal logic state and the content of registers are not affected.

7.4 Clock Source

The clock source of W86L488 is the waveform of XTO pin, if crystal is connected, the frequency may be from 3.58MHz to 25MHz, if the clock source is from external clock, XTI may be used as clock input and the maximum frequency is 25MHz. In W86L488AY, the clock driver will disabled when port A and port B are power down or global power down in the global control register is set.

8. ELECTRICAL CHARACTERISTICS

8.1 Absolute Maximum Ratings*

	Parameter	Symbol	Rating	Units
1	Supply Voltage with respect to V_{VSS}	V_{VDD}	-0.3 to 6	V
2	Current at any pin other than supplies		0 to 10	mA
3	Storage Temperature	T_{st}	-65 to 150	°C

* Exceeding these values may cause permanent damage.

8.2 Recommended Operating Conditions

	Characteristics	Symbol	Rating	Unit
1	Host I/F Operation Voltage (referenced to VSS pin).	V_{VDDH}	2.5 to 3.6	V
2	Operation Voltage (referenced to VSS pin).	V_{VDD3}	3.0 to 3.6	V
3	Operation Voltage (referenced to VSS pin) (Note)	V_{VDD3}	2.7to 3.0	V
4	Clock Frequency at XTI pin	f_{XTL}	25	MHz
5	Operation Temperature	T_{op}	0 to 70	°C

Note: Clock frequency not guaranteed up to 25MHz.

8.3 Power Supply Characteristics

(Measurement VDD3+ VDDH at VDD3 = VDDH)

	Parameter	Condition	Symbol	Min	Typ‡	Max	Units	Test
1	Standby Supply Current	Power Supply	I_Q		2	20	uA	Test 1
2	Operating Supply Current (Single port)	(V_{VDD} = 3.3V)	I_{VDD}		14	22	mA	Test 2
3	Operating Supply Current (Dual port)		I_{VDD}		24	36	mA	Test 2
4	Operating Supply Current (Single port)	(V_{VDD} = 3.3V)	I_{VDD}		13		mA	Test 3
5	Operating Supply Current (Dual port)		I_{VDD}		23		mA	Test 3

‡: Typical figure are at V_{DIVDD} = 3.3V and temperature = 25 °C and are for design aid only, not guaranteed and not subject to production testing.

Test 1: All input pins are V_{VDD} or V_{VSS}, configured as power down mode, output without loading and no clock input on the XTI and HCKI pins.

Test 2: 25 MHz external clock input on the XTI pin, output without loading.

Test 3: 25 MHz crystal connected at XTI and XTO pins, output without loading.

8.4 Digital Characteristics

	Parameter	Condition	Symbol	Min.	Typ‡	Max.	Units	Notes
1	Output High Voltage	2mA load	V_{OH}	0.9			VDD	1
2	Output Low Voltage	2mA sink	V_{OL}			0.1	VDD	1
3	Output High Voltage at SD4 output	3mA load	V_{OH}	0.9			VDD	
4	Output Low Voltage at SD4 output	3mA sink	V_{OL}			0.1	VDD	
5	High Level Input Voltage		V_{IH}	0.7			VDD	
6	Low Level Input Voltage		V_{IL}			0.3	VDD	
7	Input Current		Iin			1	uA	
8	Input Capacitance		Cin		10		pF	

‡: Typical figure are at V_{DVDD} = 3.3V and temperature = 25°C and are for design aid only, not guaranteed and not subject to production testing.

Note: All output pins except SD4 output.

8.5 Timing Characteristics

	Parameter	Symbol	Min.	Typ.	Max.	Units	Notes
Clock (figure 8-1)							
1	XTI	fXTI	1	-	20	MHz	1
2	XTI high pulse width	$tXTI_{wh}$	10	-	-	nS	1
3	XTI low pulse width	$tXTI_{wl}$	10	-	-	nS	1
4	XTI rise time	$tXTI_{r}$	-	-	5	nS	1
5	XTI fall time	$tXTI_{f}$	-	-	5	nS	1
6	XTO delay time	$tXTO_{d}$	-	-	5	nS	2
7	XTI crystal driver	fXTI	3.58	-	25	MHz	3
8	HCLK frequency	fHCLK	1	-	40	MHz	
9	HCLK high pulse width	$tHCLK_{wh}$	10	-	-	nS	
10	HCLK low pulse width	$tHCLK_{wl}$	10	-	-	nS	
11	HCLK rise time	$tHCLK_{l}$	-	-	5	nS	
12	HCLK fall time	$tHCLK_{f}$	-	-	5	nS	

8.5. Timing Characteristics, continued

	Parameter	Symbol	Min	Typ	Max	Units	Notes
Reset							
1	RSTN	tRST	4	-	-	cycle	
Host Interface at Type 1 (figure 8-2, 8-3)							
1	Access time	t_{acc}	100	-	-	nS	4
2	Address setup time	tA_{su}	10	-	-	nS	
3	Address hold time	tA_{h}	5	-	-	nS	
4	D[15:0] output delay time	tD_{od}	-	-	30	nS	5,6
5	D[15:0] output hold time	tD_{oh}	10	-	-	nS	5,7
6	D[15:0] input setup time	tD_{su}	10	-	-	nS	8
7	D[15:0] input hold time	tD_{h}	5	-	-	nS	9
8	DMA request delay time	$tDRQ_{d}$	-	-	20	nS	2
9	DMA request hold time	$tDRQ_{h}$	5	-	20	nS	2
Host Interface at Type 2 (figure 8-5)							
1	Input signals setup time	$tIF2_{su}$	10	-	-	nS	10
2	Input signals hold time	$tIF2_{h}$	5	-	-	nS	10
3	Address setup time	$tA2_{su}$	10	-	-	nS	
4	Address hold time	$tA2_{h}$	5	-	-	nS	
5	XRDYN delay time	$tRDY_{d}$	-	-	20	nS	2
6	XRDYN hold time	$tRDY_{h}$	5	-	-	nS	2
7	D[15:0] output delay time	tD_{od}	-	-	30	nS	5
8	D[15:0] output hold time	tD_{oh}	10	-	-	nS	5
9	D[15:0] input setup time	tD_{su}	10	-	-	nS	
10	D[15:0] input hold time	tD_{h}	5	-	-	nS	
Interrupt (figure 8-4)							
1	Interrupt delay time	$tINT_{d}$	-	-	20	nS	
2	Interrupt hold time	$TINT_{h}$	5	-	20	nS	

8.5. Timing Characteristics, continued

Parameter		Symbol	Min.	Typ.	Max.	Units	Notes
Serial Interface Signals (figure 8-6, 8-7, 8-8, 8-9)							
1	SD3 output delay	$tSD3_d$	5	-	15	nS	2
2	SD3 input setup time	$tSD3D_{su}$	10	-	-	nS	
3	SD3 input hold time	$tSD3_h$	5	-	-	nS	
4	SD1,SD2,SD5,SD6 output delay time	$tSDn_d^*$	-	-	30	nS	2
5	SD1,SD2,SD5,SD6 input setup time	$tSDn_{su}$	10	-	-	nS	
6	SD1,SD2,SD5,SD6 input hold time	$tSDn_h$	5	-	-	nS	

Notes:

1. External clock input.
2. 20 pF output loading.
3. Crystal driver.
4. Minimum active pulse width of (XCSN and XRDN) or (XCSN and XWRHN and XWRLN).
5. : 40 pF output loading.
6. From the last active signal of XCSN or XRDN.
7. From the first in-active signal of XCSN or XRDN.
8. To the first in-active signal of XCSN, XWRHN or XWRLN, XWRHN or XWRLN related to the D[15:8] or D[7:0].
9. From the first in-active signal of XCSN, XWRHN or XWRLN, XWRHN or XWRLN related to the D[15:8] or D[7:0].
10. XCSN, XASN, XRWN and XBE[1:0] signals.

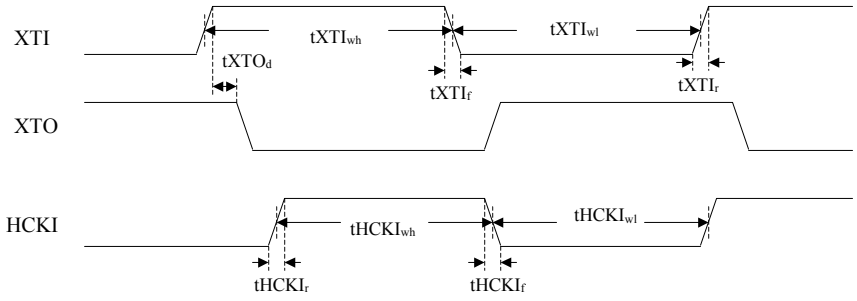


Fig. 8-1 Timing Characteristic of XTI, XTO and HCKI.

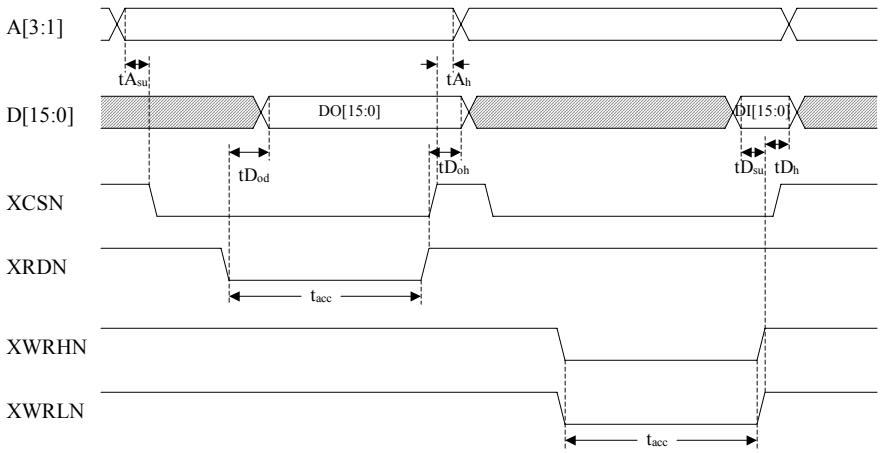


Fig. 8-2 Host Access Timing Characteristic in Host I/F Type 1.

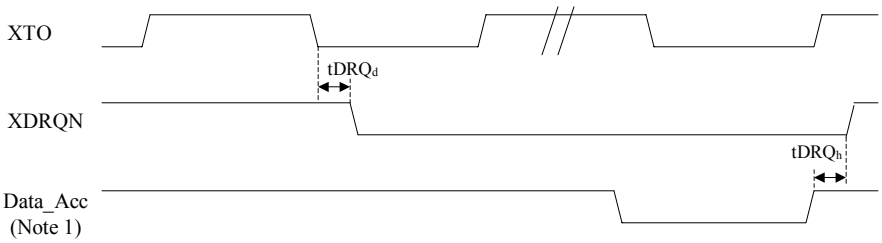


Fig. 8-3 Data Access Request Timing Characteristic.

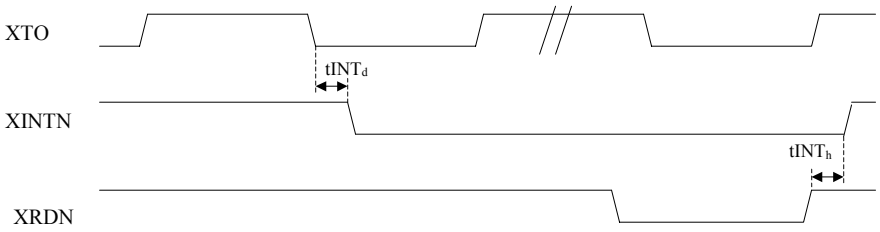


Fig. 8-4 Interrupt Timing Characteristic.

Note 1: May be XRDN or XWRHN or XWRLN signals when DABST = low.

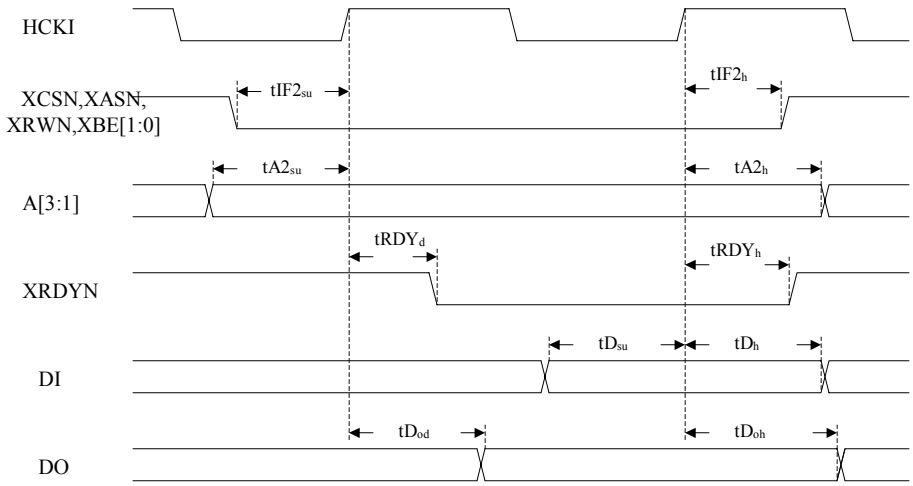


Fig. 8-5 Host Interface Type 2 Timing Characteristic.

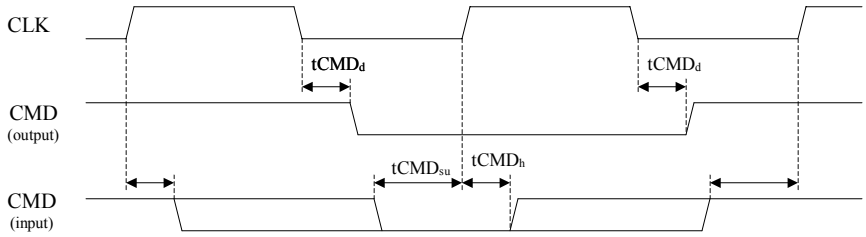


Fig. 8-6 Serial Interface CMD Timing Characteristic (SD Mode).

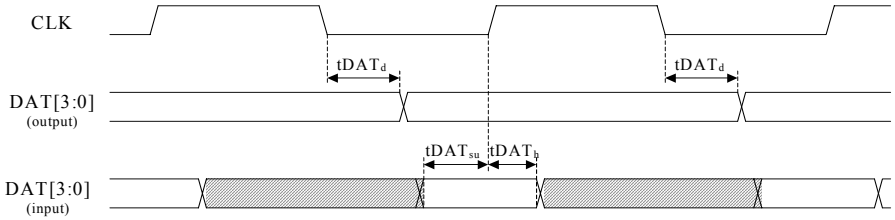


Fig. 8-7 Serial Interface DAT[3:0] Timing Characteristic (SD Mode).

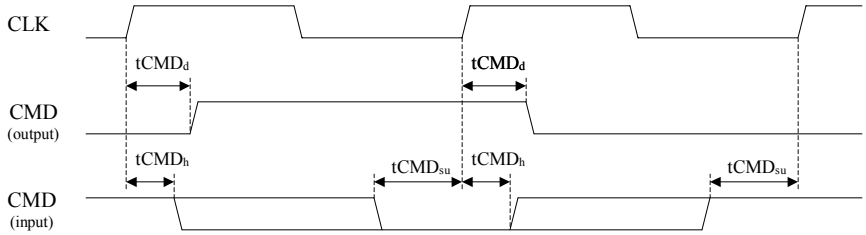


Fig. 8-8 Serial Interface CMD Timing Characteristic (MMC Mode).

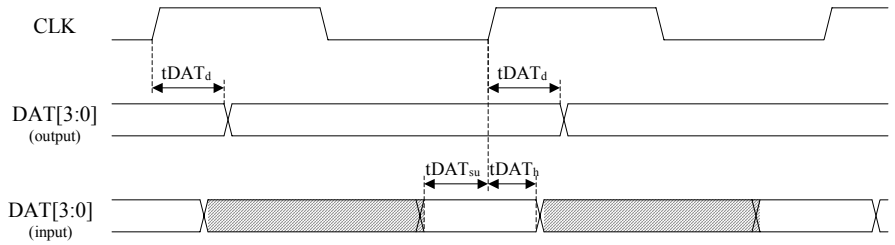


Fig. 8-9 Serial Interface DAT[3:0] Timing Characteristic (MMC Mode).

9. HOW TO READ THE TOP MARKING

The top marking of W86L488Y

1st line: Winbond logo and SMART@IO Mark

2nd line: Part number of W86L488Y

3rd line: Tracking code 220 A A 01A SA

312: packages made in '03, week 12

A: assembly house ID; A means ASE, O means OSE, G means GR

A: IC revision; A means version A, B means version B

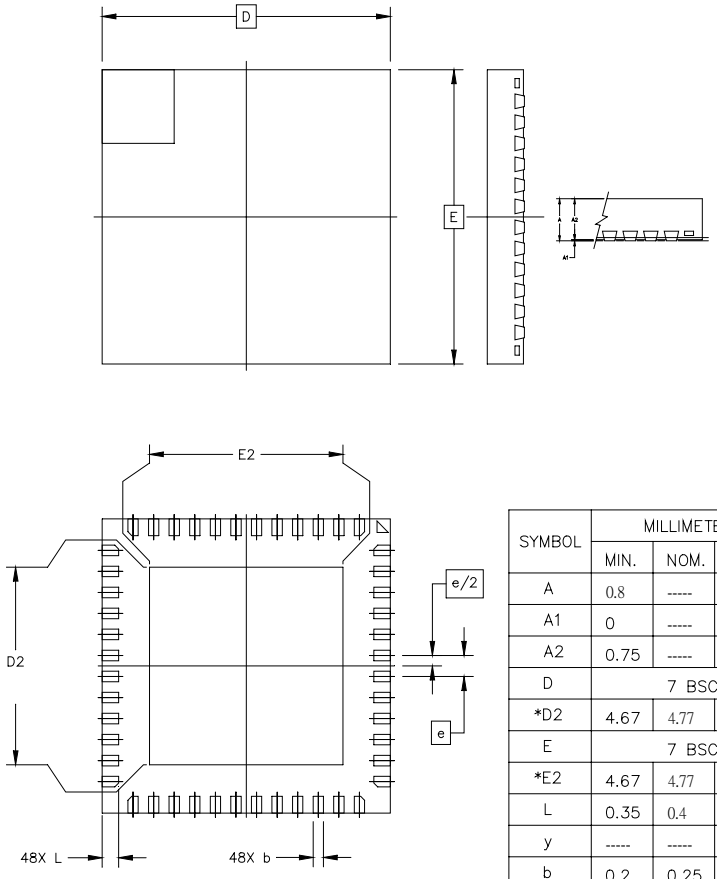
01C: for internal use

SA: for internal use

10. PACKAGE DIMENSIONS

10.1 W86L488Y Package Dimensions

48- QFN

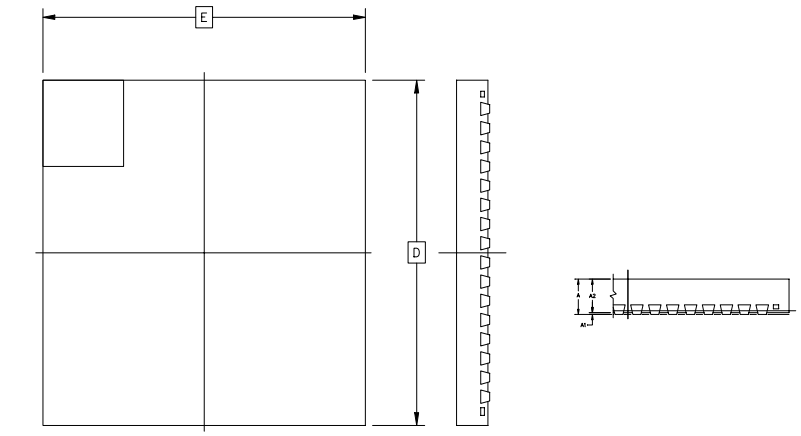


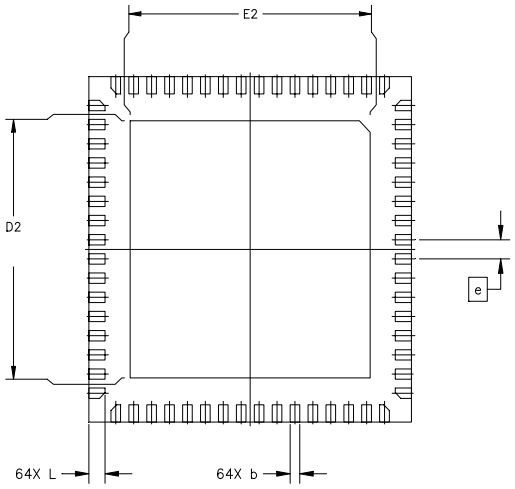
SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.8	-----	1	0.031	-----	0.039
A1	0	-----	0.05	0	-----	0.002
A2	0.75	-----	1	0.03	-----	0.039
D	7 BSC			0.2756 BSC		
*D2	4.67	4.77	4.87	0.1839	0.1878	0.1917
E	7 BSC			0.2756 BSC		
*E2	4.67	4.77	4.87	0.1839	0.1878	0.1917
L	0.35	0.4	0.45	0.0138	0.0157	0.0178
y	-----	-----	0.10	-----	-----	0.004
b	0.2	0.25	0.3	0.0079	0.0098	0.0118
e	0.5 BSC			0.0197 BSC		

*D2,*E2 : By die size difference.

10.2 10.2 W86L488AY Package Dimensions

64- QFN



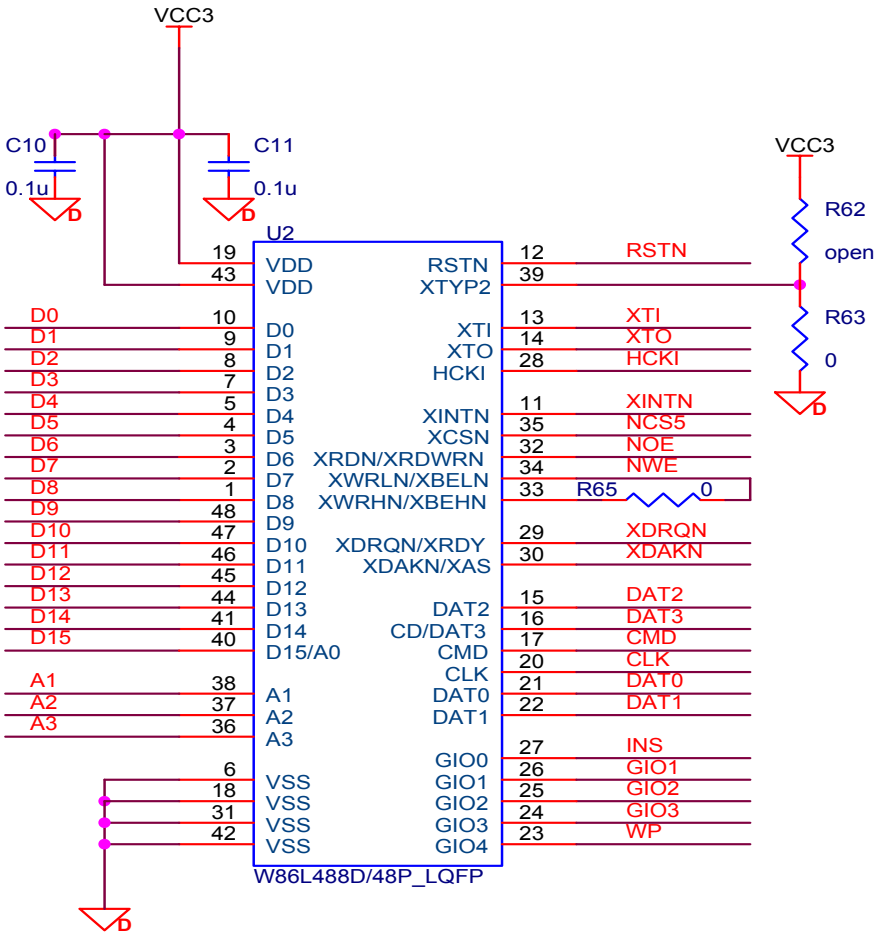


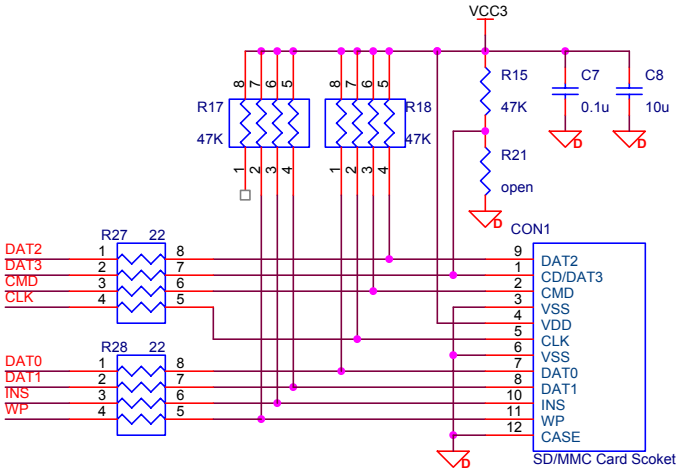
SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.8	-----	1	0.031	-----	0.039
A1	0	-----	0.025	0	-----	0.001
A2	0.75	-----	1	0.03	-----	0.039
D	9 BSC			0.3543 BSC		
*D2	6.55	-----	6.85	0.2579	-----	0.2697
E	9 BSC			0.3543 BSC		
*E2	6.55	-----	6.85	0.2579	-----	0.2697
L	0.3	0.4	0.5	0.0118	0.0157	0.0197
y	-----	-----	0.10	-----	-----	0.004
b	0.17	0.25	0.27	0.0067	0.0098	0.0106
e	0.5 BSC			0.0197 BSC		

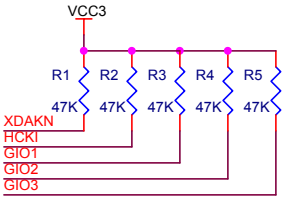
*D2,*E2 : By die size difference.

11. REFERENCE SCHEMATIC

11.1 W86L488Y Reference Schematic




VCC3
R15
47K
C7
0.1u
C8
10u
R17
47K
R18
47K
R21
open
CON1
R27 22
R28 22
DAT2
DAT3
CMD
CLK
DAT0
DAT1
INS
WP
DAT2
CD/DAT3
CMD
VSS
VDD
CLK
VSS
DAT0
DAT1
INS
WP
CASE
SD/MMC Card Scoket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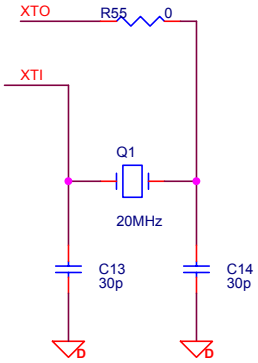
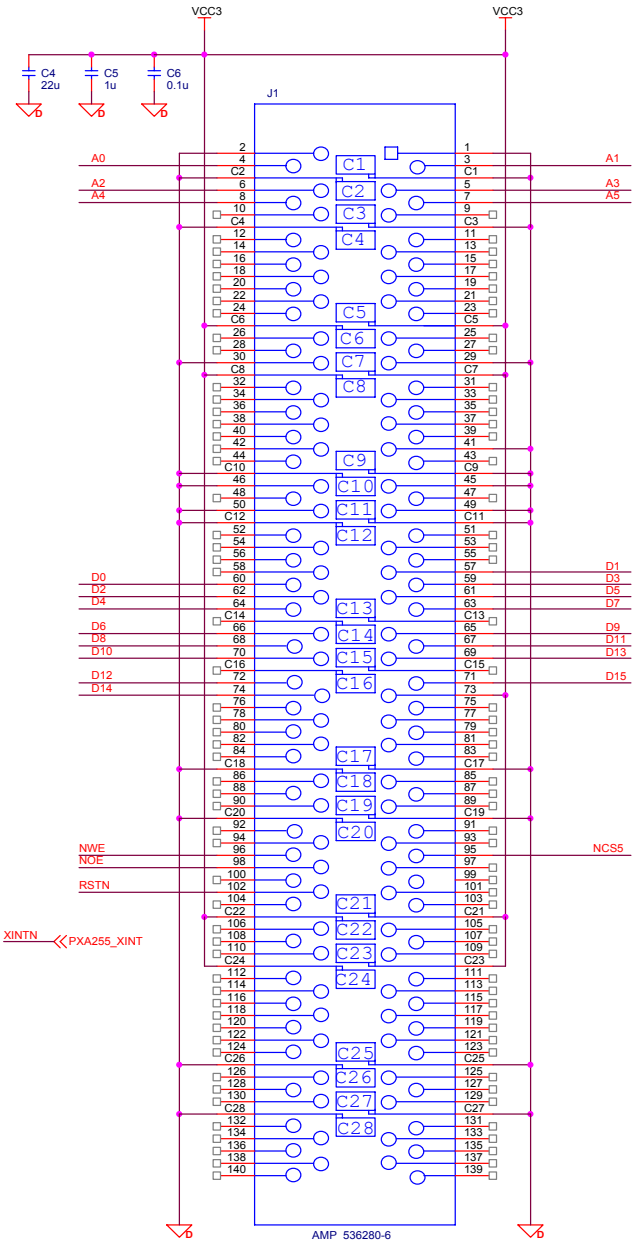
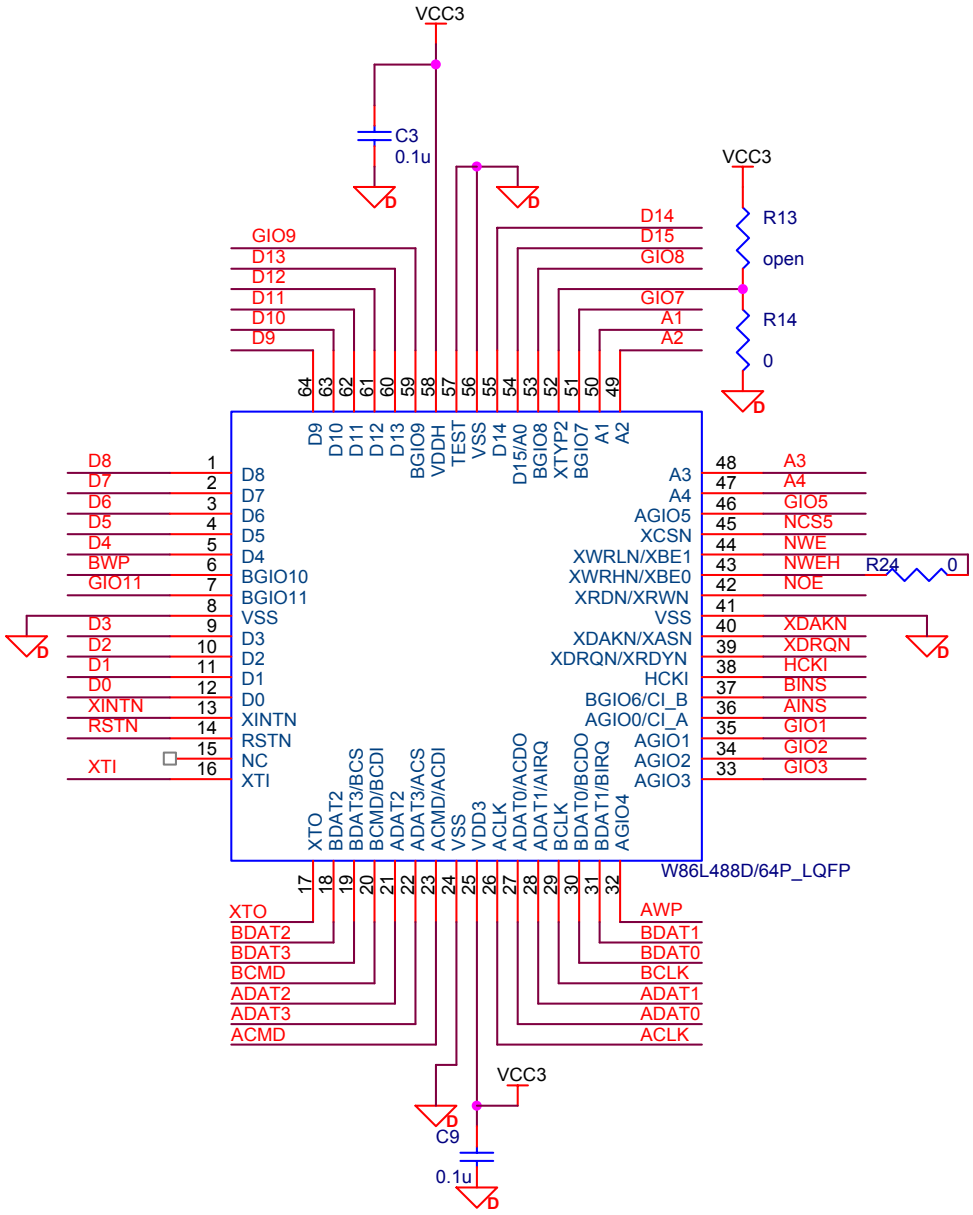
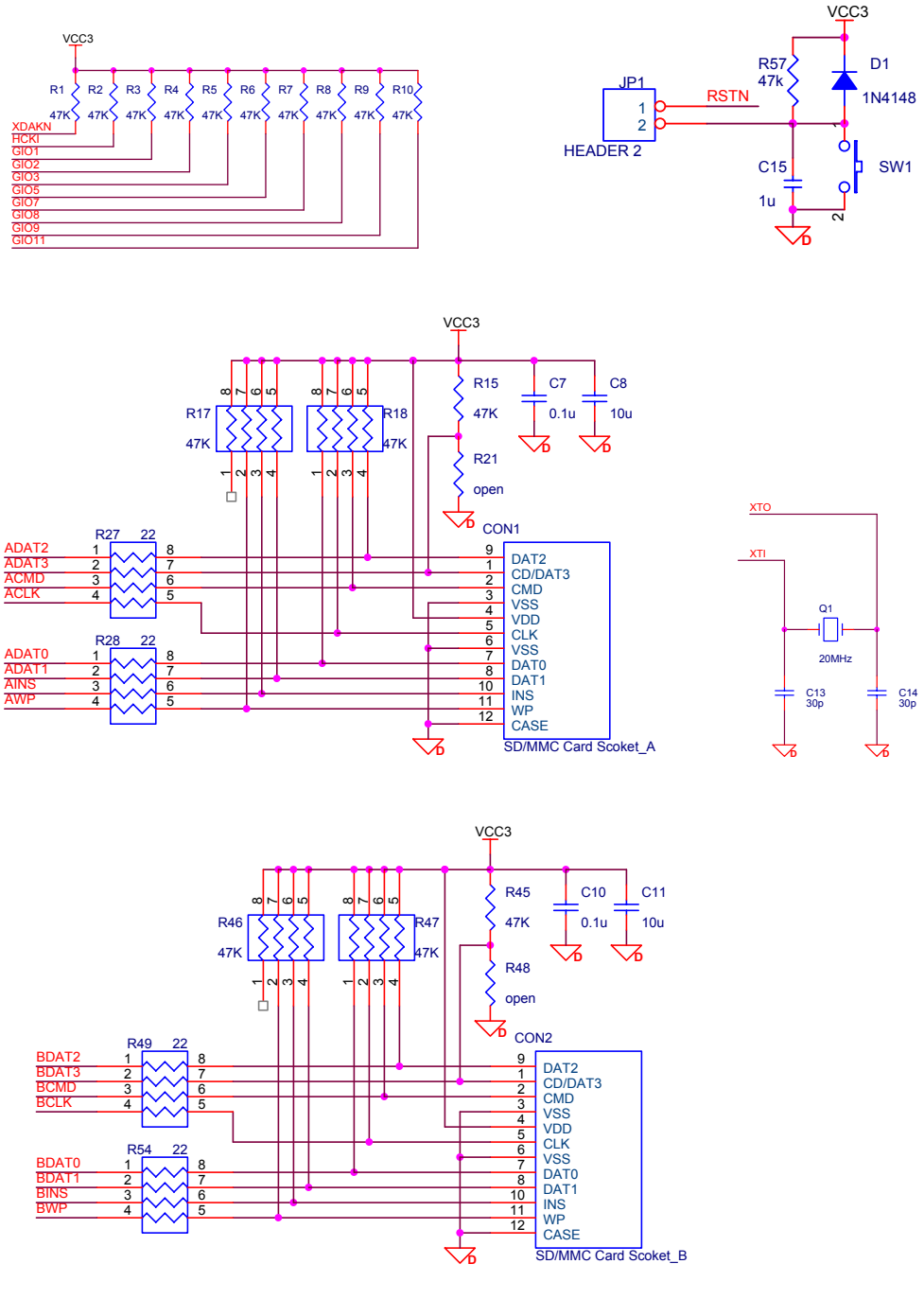
R1
R2
R3
R4
R5
47K
XDAKN
HCKI
GIO1
GIO2
GIO3


XTO
R55
0
XTI
Q1
20MHz
C13
30p
C14
30p


VCC3
VCC3
C4
22u
C5
1u
C6
0.1u
J1
A0
A1
A2
A3
A4
A5
D0
D1
D2
D3
D4
D5
D6
D7
D8
D9
D10
D11
D12
D13
D14
D15
NWE
NOE
NCS5
RSTN
XINTN
PXA255_XINT
AMP 536280-6

11.2 W86L488AY Reference Schematic

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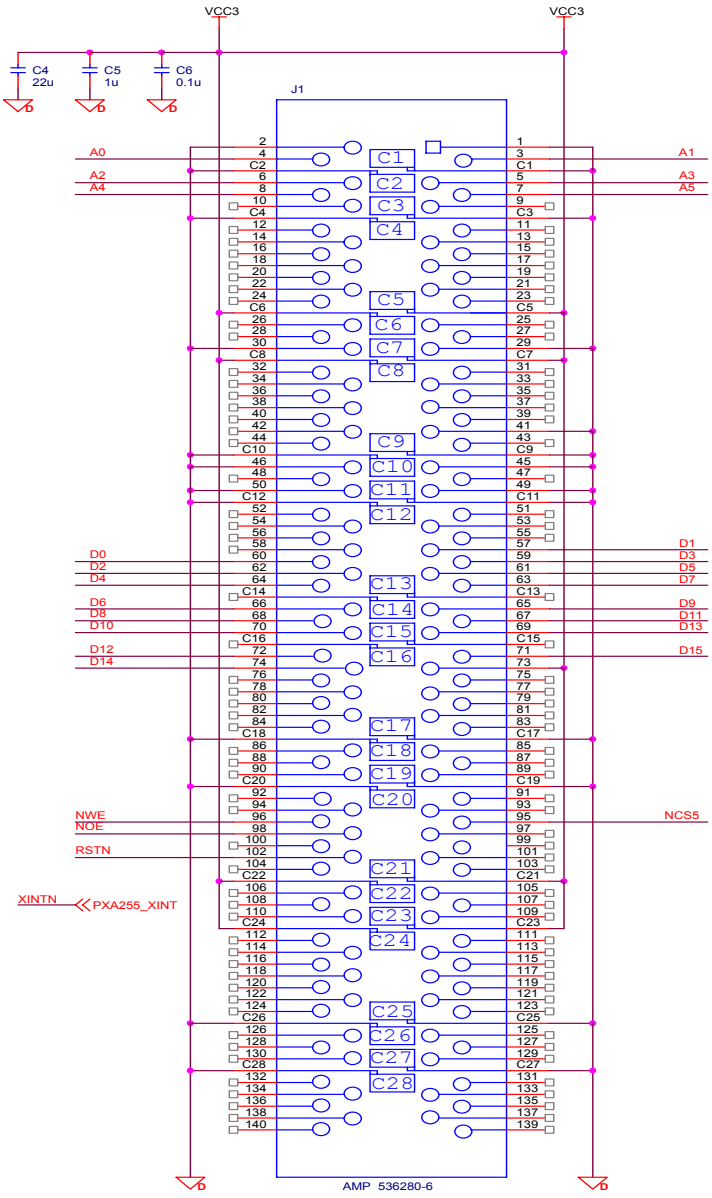
R1 47K
R2 47K
R3 47K
R4 47K
R5 47K
R6 47K
R7 47K
R8 47K
R9 47K
R10 47K
XDAKN
HCK1
GIO1
GIO2
GIO3
GIO5
GIO7
GIO8
GIO9
GIO11
JP1
HEADER 2
RSTN
R57 47k
D1
1N4148
C15 1u
SW1
R17 47K
R18 47K
R15 47K
C7 0.1u
C8 10u
R21 open
CON1
R27 22
R28 22
ADAT2
ADAT3
ACMD
ACLK
ADAT0
ADAT1
AINS
AWP
DAT2
CD/DAT3
CMD
VSS
VDD
CLK
VSS
DAT0
DAT1
INS
WP
CASE
SD/MMC Card Scoket_A
XTO
XTI
Q1
20MHz
C13 30p
C14 30p
R46 47K
R47 47K
R45 47K
C10 0.1u
C11 10u
R48 open
CON2
R49 22
R54 22
BDAT2
BDAT3
BCMD
BCLK
BDAT0
BDAT1
BINS
BWP
SD/MMC Card Scoket_B


VCC3
VCC3
C4
22u
C5
1u
C6
0.1u
J1
A0
A2
A4
A1
A3
A5
D0
D2
D4
D6
D8
D10
D12
D14
D1
D3
D5
D7
D9
D11
D13
D15
NWE
NOE
RSTN
NCS5
XINTN
PXA255_XINT
AMP 536280-6

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