
HN62448 Series

524288-word × 16-bit/1048576-word × 8-bit CMOS
Mask Programmable ROM

HITACHI

ADE-203-397B (Z)
Rev. 2.0
Oct. 2, 1996

Description

The Hitachi HN62448 is a 8-Mbit CMOS mask-programmable ROM organized either as 524288-words by 16-bits or as 1048576-words by 8-bits. And a high speed access of 100/120 ns is the most suitable to the system using a high speed microcomputer by 16 bits.

Features

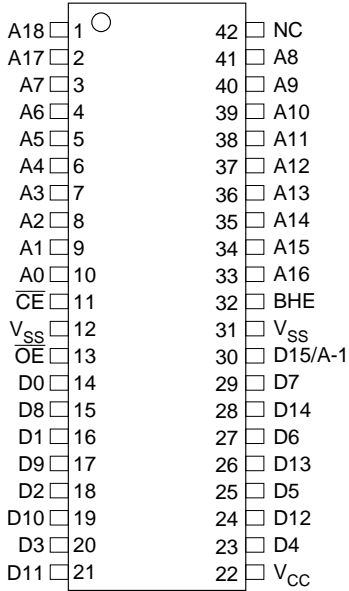
- Single 5 V power supply
- Access time:
 - Normal access time: 100/120 ns (max)
- Low power dissipation
 - Active: 300 mW (typ)
 - Standby: 5 μ W (typ)
- Byte-wide or word-wide data organization with BHE
- Three-state data output for wired or-tying
- Directly TTL compatible (All input and output)

Ordering Information

Type No.	Access time	Package
HN62448P-10	100 ns	600mil 42-pin plastic DIP (DP-42)
HN62448P-12	120 ns	
HN62448FB-10	100 ns	44-pin plastic SOP (FP-44D)
HN62448FB-12	120 ns	
HN62448TT-10	100 ns	44-pin plastic TSOP II (TTP-44D)
HN62448TT-12	120 ns	

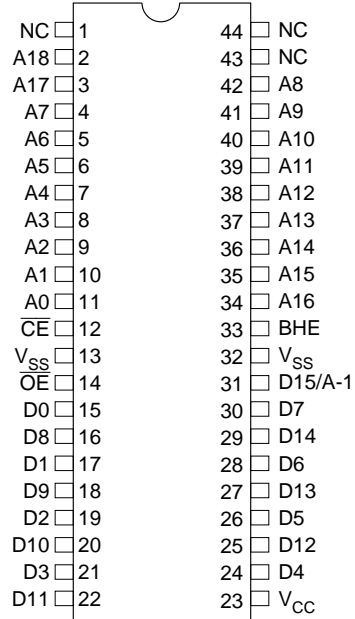
Pin Arrangement

HN62448P Series



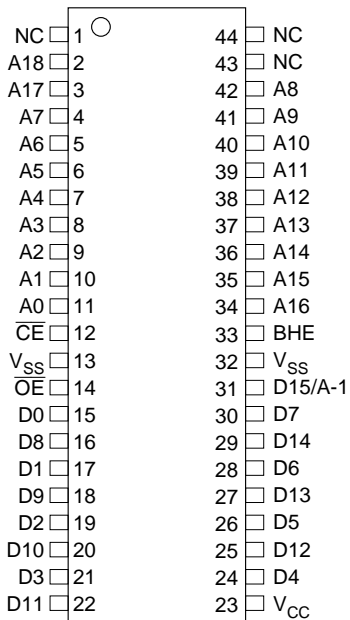
(Top View)

HN62448FB Series



(Top View)

HN62448TT Series

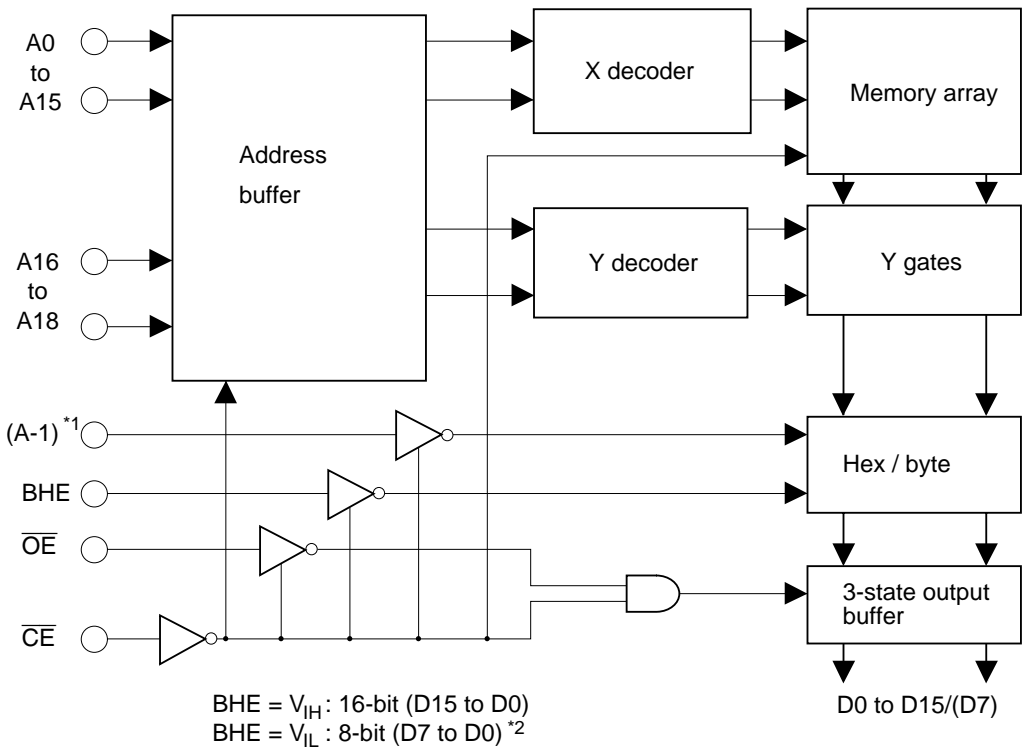


(Top View)

Pin Description

Pin name	Function
A0 to A18	Address input
D0 to D14	Data output
D15/A-1	Data output/address input
\overline{OE}	Output enable
\overline{CE}	Chip enable
BHE	Byte/word selection
V_{CC}	Power supply
V_{SS}	Ground
NC	No connection

Block Diagram



- Note: 1. A-1 is least significant address.
 2. When BHE is 'low', D14 to D8 go to the high impedance state.

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit	Note
Supply voltage	V_{CC}	-0.3 to +7.0	V	1
All input and output voltage	V_{in}, V_{out}	-0.3 to $V_{CC} + 0.3$	V	1
Operating temperature range	T_{opr}	0 to 70	°C	
Storage temperature range	T_{stg}	-55 to +125	°C	
Temperature under bias	T_{bias}	-20 to +85	°C	

Note: 1. With respect to V_{SS} .

Recommended DC Operating Conditions ($T_a = 0$ to $+70^\circ\text{C}$)

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input voltage	V_{IH}	2.2	—	$V_{CC} + 0.3$	V
	V_{IL}	-0.3	—	0.8	V

DC Characteristics ($V_{CC} = 5\text{ V} \pm 10\%$, $V_{SS} = 0\text{ V}$, $T_a = 0$ to $+70^\circ\text{C}$)

Parameter		Symbol	Min	Max	Unit	Test conditions
Supply current	Active	I_{CC}	—	100/80	mA	$V_{CC} = 5.5\text{ V}$, $I_{DOUT} = 0\text{ mA}$, $t_{RC} = 100/120\text{ ns}$
	Standby	I_{SB1}	—	30	μA	$V_{CC} = 5.5\text{ V}$, $\overline{CE} \geq V_{CC} - 0.2\text{ V}$
	Standby	I_{SB2}	—	3	mA	$V_{CC} = 5.5\text{ V}$, $\overline{CE} \geq 2.2\text{ V}$
Input leakage current		$ I_{IL} $	—	10	μA	$V_{in} = 0$ to V_{CC}
Output leakage current		$ I_{OL} $	—	10	μA	$\overline{CE} = 2.2\text{ V}$, $V_{OUT} = 0$ to V_{CC}
Output voltage		V_{OH}	2.4	—	V	$I_{OH} = -205\text{ }\mu\text{A}$
		V_{OL}	—	0.4	V	$I_{OL} = 1.6\text{ mA}$

Capacitance ($V_{CC} = 5\text{ V} \pm 10\%$, $V_{SS} = 0\text{ V}$, $T_a = 25^\circ\text{C}$, $V_{in} = 0\text{ V}$, $f = 1\text{ MHz}$)

Parameter	Symbol	Min	Max	Unit
Input capacitance*1	C_{in}	—	15	pF
Output capacitance*1	C_{out}	—	15	pF

Note: 1. This parameter is periodically sampled and not 100% tested.

AC Characteristics ($V_{CC} = 5\text{ V} \pm 10\%$, $V_{SS} = 0\text{ V}$, $T_a = 0\text{ to } +70^\circ\text{C}$)

Test Condition

- Output load: 1TTL gate + $C_L = 100\text{ pF}$ (including scope & jig)
- Input pulse levels: 0.45 to 2.8 V
- Input and output timing reference levels: 1.5V
- Input rise and fall time: 5 ns

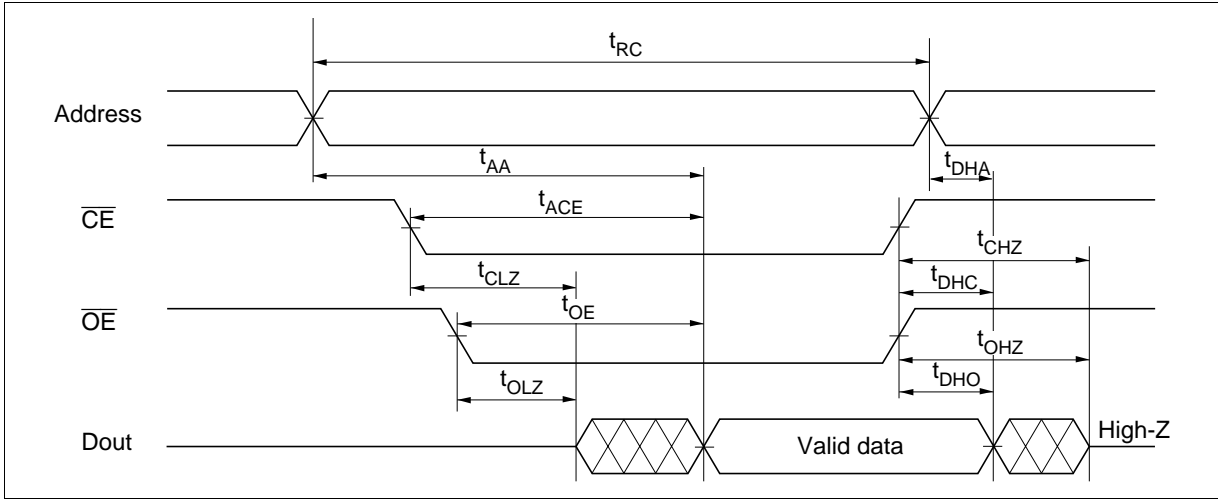
Read Cycle

Parameter	Symbol	HN62448-10		HN62448-12		Unit	Note
		Min	Max	Min	Max		
Read cycle time	t_{RC}	100	—	120	—	ns	
Address access time	t_{AA}	—	100	—	120	ns	3
\overline{CE} access time	t_{ACE}	—	100	—	120	ns	3
\overline{OE} access time	t_{OE}	—	40	—	50	ns	3
BHE access time	t_{BHE}	—	100	—	120	ns	
Output hold time from address change	t_{DHA}	0	—	0	—	ns	2
Output hold time from \overline{CE}	t_{DHC}	0	—	0	—	ns	2
Output hold time from \overline{OE}	t_{DHO}	0	—	0	—	ns	2
Output hold time from BHE	t_{DHB}	0	—	0	—	ns	
\overline{CE} to output in high-Z	t_{CHZ}	—	40	—	40	ns	1
\overline{OE} to output in high-Z	t_{OHZ}	—	40	—	40	ns	1
BHE to output in high-Z	t_{BHZ}	—	40	—	40	ns	1
\overline{CE} to output in low-Z	t_{CLZ}	5	—	5	—	ns	4
\overline{OE} to output in low-Z	t_{OLZ}	5	—	5	—	ns	4
BHE to output in low-Z	t_{BLZ}	5	—	5	—	ns	

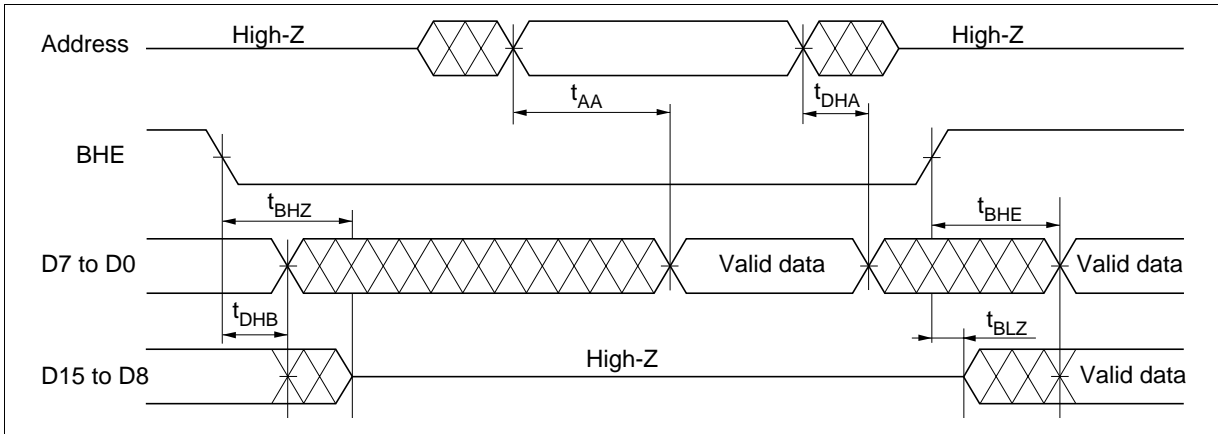
- Note:
1. t_{CHZ} , t_{OHZ} and t_{BHZ} are defined as the time at which the output achieves the open circuit conditions and are not referred to output voltage levels.
 2. t_{DHA} , t_{DHC} , t_{DHO} : Determined by faster.
 3. t_{AA} , t_{ACE} , t_{OE} : Determined by slower.
 4. t_{CLZ} , t_{OLZ} : Determined by slower.
 5. \overline{CE} and \overline{OE} are enable A18 to A0 are valid.
 6. D15/A-1 pin is in the output state when BHE is high, \overline{CE} and \overline{OE} are enable. Therefore, the input signals of opposite phase to the output must not be applied to them.
 7. This device is used ATD (Address Transient Detector). Therefore, transfer either \overline{CE} or address (A2 to A18) after power up to 4.5 V.

Timing Waveforms

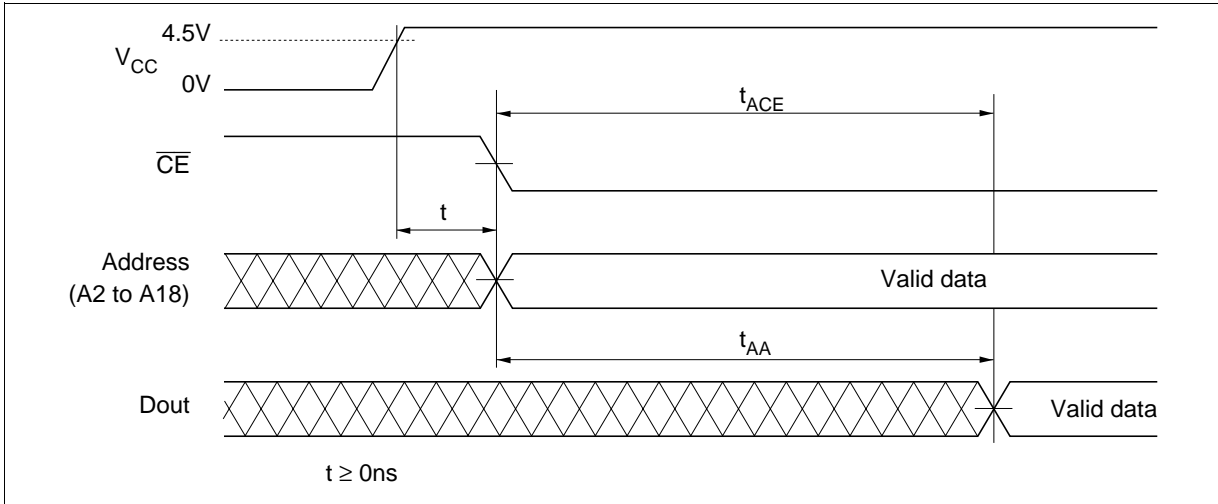
Word Mode (BHE = 'V_{IH}') or Byte Mode (BHE = 'V_{IL}')*2,3,4



Word Mode, Byte Mode Switch*5, 6



Power Up Sequence*7

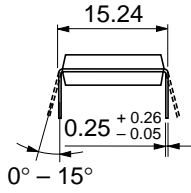
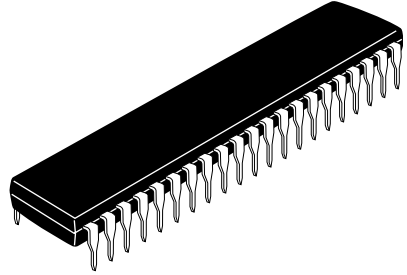
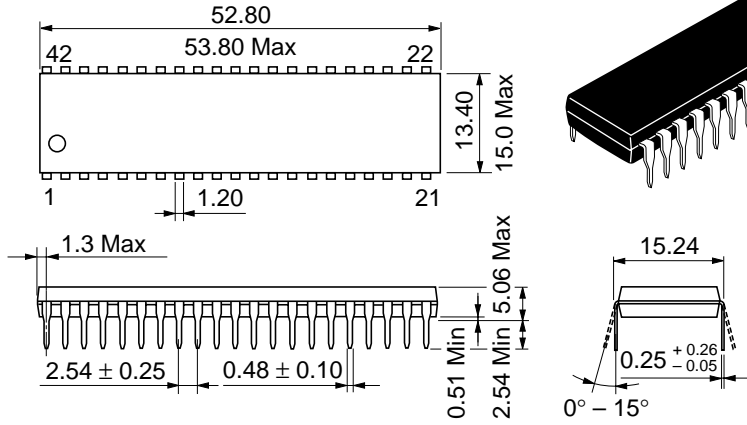


HN62448 Series

Package Dimensions

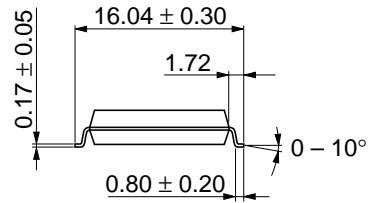
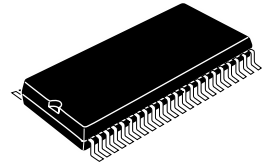
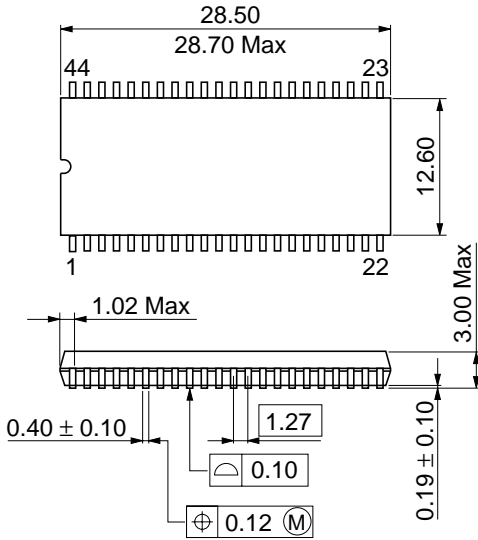
HN62448P Series (DP-42)

Unit: mm



HN62448FB Series (FP-44D)

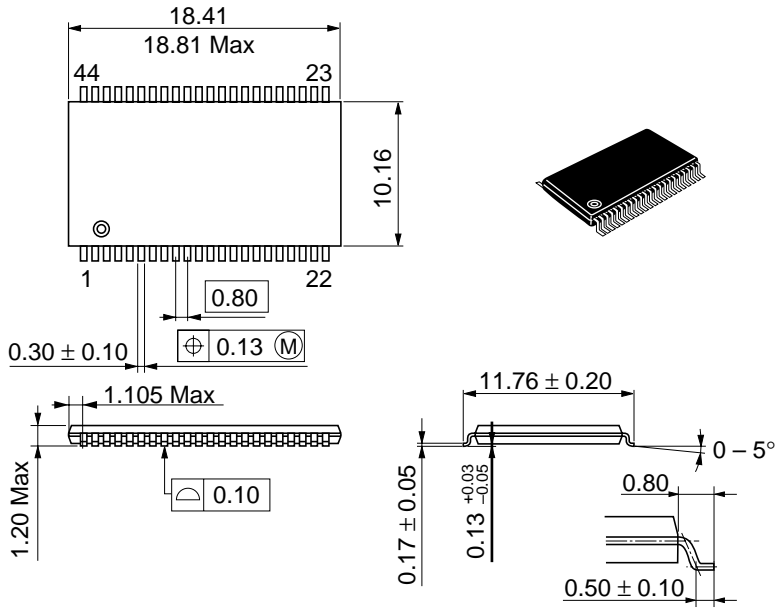
Unit: mm



Package Dimensions (cont.)

HN62448TT Series (TTP-44D)

Unit: mm



When using this document, keep the following in mind:

1. This document may, wholly or partially, be subject to change without notice.
2. All rights are reserved: No one is permitted to reproduce or duplicate, in any form, the whole or part of this document without Hitachi's permission.
3. Hitachi will not be held responsible for any damage to the user that may result from accidents or any other reasons during operation of the user's unit according to this document.
4. Circuitry and other examples described herein are meant merely to indicate the characteristics and performance of Hitachi's semiconductor products. Hitachi assumes no responsibility for any intellectual property claims or other problems that may result from applications based on the examples described herein.
5. No license is granted by implication or otherwise under any patents or other rights of any third party or Hitachi, Ltd.
6. **MEDICAL APPLICATIONS:** Hitachi's products are not authorized for use in **MEDICAL APPLICATIONS** without the written consent of the appropriate officer of Hitachi's sales company. Such use includes, but is not limited to, use in life support systems. Buyers of Hitachi's products are requested to notify the relevant Hitachi sales offices when planning to use the products in **MEDICAL APPLICATIONS**.

HITACHI

Hitachi, Ltd.

Semiconductor & IC Div.
Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100, Japan
Tel: Tokyo (03) 3270-2111
Fax: (03) 3270-5109

For further information write to:

Hitachi America, Ltd.
Semiconductor & IC Div.
2000 Sierra Point Parkway
Brisbane, CA. 94005-1835
U S A
Tel: 415-589-8300
Fax: 415-583-4207

Hitachi Europe GmbH
Electronic Components Group
Continental Europe
Dornacher Straße 3
D-85622 Feldkirchen
München
Tel: 089-9 91 80-0
Fax: 089-9 29 30 00

Hitachi Europe Ltd.
Electronic Components Div.
Northern Europe Headquarters
Whitebrook Park
Lower Cookham Road
Maidenhead
Berkshire SL6 8YA
United Kingdom
Tel: 0628-585000
Fax: 0628-778322

Hitachi Asia Pte. Ltd.
16 Collyer Quay #20-00
Hitachi Tower
Singapore 0104
Tel: 535-2100
Fax: 535-1533

Hitachi Asia (Hong Kong) Ltd.
Unit 706, North Tower,
World Finance Centre,
Harbour City, Canton Road
Tsim Sha Tsui, Kowloon
Hong Kong
Tel: 27359218
Fax: 27306071

Revision Record

Rev.	Date	Contents of Modification	Drawn by	Approved by
1.0	Jun. 13, 1995	Initial issue	T. Kawajiri	H. Moriuchi
2.0	Oct. 2, 1996	Change of format AC Characteristics Input pulse levels: 0.45 to 2.4 V to 0.45 to 2.8 V		
