Siliconix incorporated

SMM20N50

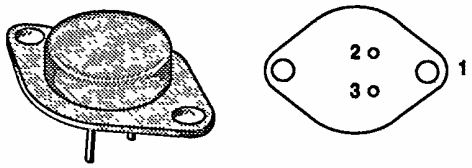
T-39-15

N-Channel Enhancement Mode Transistor

PRODUCT SUMMARY

$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ (Ω)	I_D (A)
500	0.30	20

TO-204AE (TO-3) BOTTOM VIEW



1 DRAIN (CASE)
2 GATE
3 SOURCE

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNITS
Drain-Source Voltage		V_{DS}	500	V
Gate-Source Voltage		V_{GS}	±20	
Continuous Drain Current	T_C = 25°C	I_D	20	A
	T_C = 100°C		12.5	
Pulsed Drain Current[1]		I_{DM}	80	
Avalanche Current (See Figure 9)		I_A	20	
Power Dissipation	T_C = 25°C	P_D	250	W
	T_C = 100°C		100	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	−55 to 150	°C
Lead Temperature ($^1/_{16}$" from case for 10 sec.)		T_L	300	

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THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNITS
Junction-to-Case	R_{thJC}		0.50	K/W
Junction-to-Ambient	R_{thJA}		30	
Case-to-Sink	R_{thCS}	0.1		

[1]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, Figure 11).

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ELECTRICAL CHARACTERISTICS (T_J = 25°C Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	TYP	LIMITS MIN	LIMITS MAX	UNIT
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 µA		500		V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 1000 µA		2.0	4.0	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = $V_{(BR)DSS}$, V_{GS} = 0 V			250	µA
		V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 0 V, T_J = 125°C			1000	
On-State Drain Current[1]	$I_{D(ON)}$	V_{DS} = 10 V, V_{GS} = 10 V		20		A
Drain-Source On-State Resistance[1]	$r_{DS(ON)}$	V_{GS} = 10 V, I_D = 10 A	0.26		0.30	Ω
		V_{GS} = 10 V, I_D = 10 A, T_J = 125°C	0.52		0.70	
Forward Transconductance[1]	g_{fs}	V_{DS} = 15 V, I_D = 10 A	11	8.0		S
DYNAMIC						
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	3800			pF
Output Capacitance	C_{oss}		750			
Reverse Transfer Capacitance	C_{rss}		350			
Total Gate Charge[2]	Q_g	V_{DS} = 0.5 x $V_{(BR)DSS}$, V_{GS} = 10 V, I_D = 20 A	105	80	140	nC
Gate-Source Charge[2]	Q_{gs}		18	10	25	
Gate-Drain Charge[2]	Q_{gd}		60	40	80	
Turn-On Delay Time[2]	$t_{d(on)}$	V_{DD} = 250 V, R_L = 25 Ω I_D ≅ 10 A, V_{GEN} = 10 V, R_G = 4.7 Ω	34		45	ns
Rise Time[2]	t_r		57		70	
Turn-Off Delay Time[2]	$t_{d(off)}$		120		150	
Fall Time[2]	t_f		62		75	
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (T_C = 25°C)						
Continuous Current	I_S				20	A
Pulsed Current[3]	I_{SM}				110	
Forward Voltage[1]	V_{SD}	I_F = I_S, V_{GS} = 0 V			1.6	V
Reverse Recovery Time	t_{rr}	I_F = I_S, dI_F/dt = 100 A/µs	300		650	ns
Reverse Recovery Charge	Q_{rr}		2.0			µC

[1]Pulse test: Pulse Width ≤ 300 µseo, Duty Cycle ≤ 2%.
[2]Independent of operating temperature.
[3]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, Figure 11).

TYPICAL CHARACTERISTICS (25°C Unless Otherwise Specified)

T-39-15

Figure 1. Output Characteristics

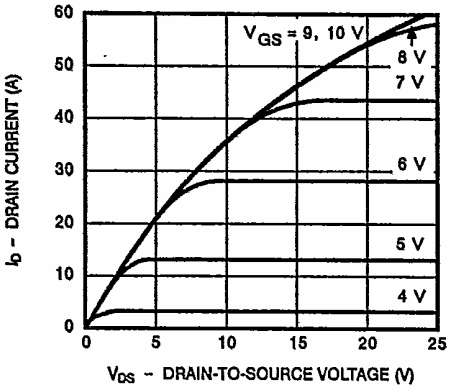


Figure 2. Transfer Characteristics

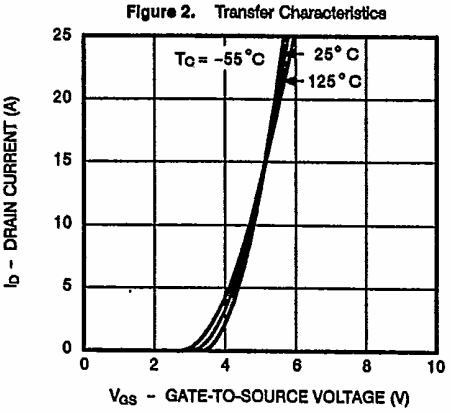


Figure 3. Transconductance

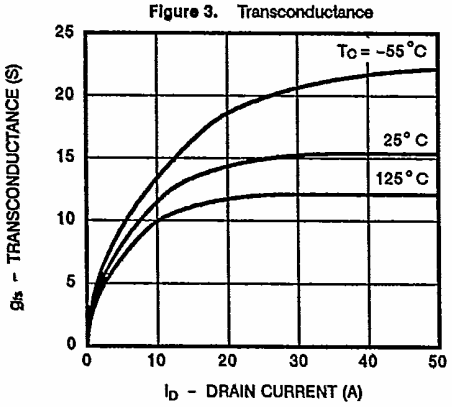


Figure 4. On-Resistance

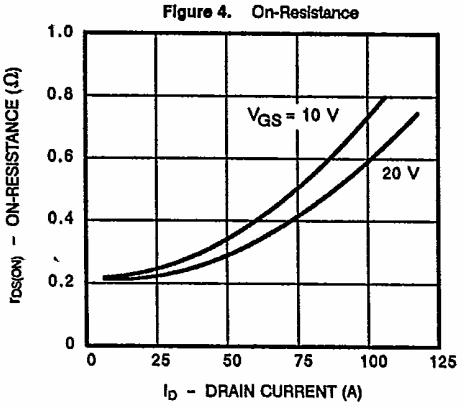


Figure 5. Capacitance

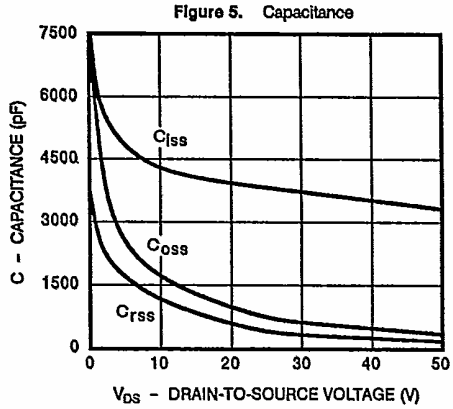
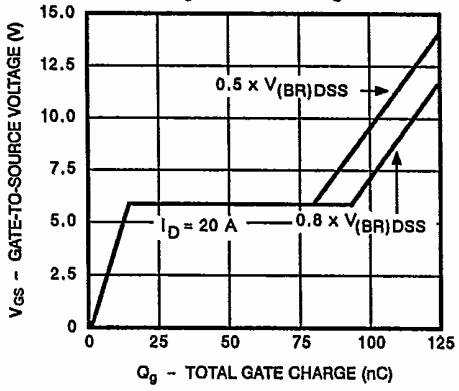


Figure 6. Gate Charge



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TYPICAL CHARACTERISTICS (Cont'd)

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Figure 7. On-Resistance vs. Junction Temperature

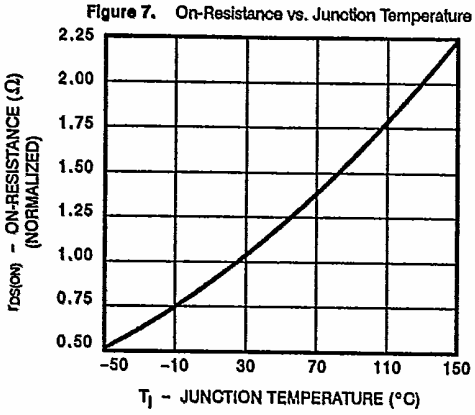
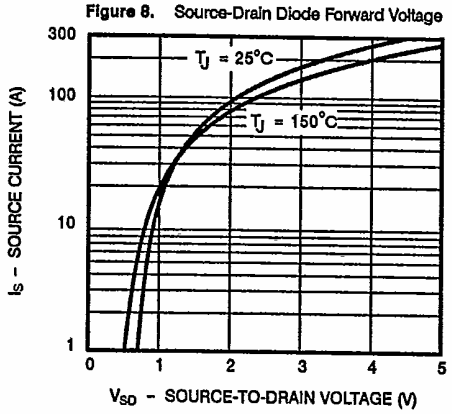


Figure 8. Source-Drain Diode Forward Voltage



THERMAL RATINGS

Figure 9. Maximum Avalanche and Drain Current vs. Case Temperature

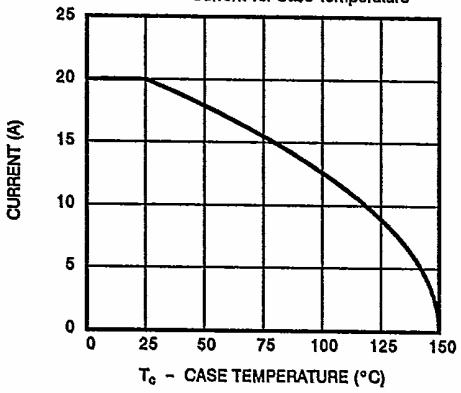
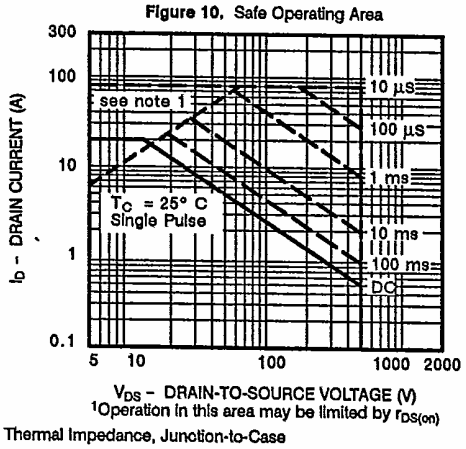


Figure 10. Safe Operating Area



[1]Operation in this area may be limited by $r_{DS(on)}$

Figure 11. Normalized Effective Transient Thermal Impedance, Junction-to-Case