μPD449
2,048 x 8-BIT STATIC CMOS RAM

Revision 4

Description

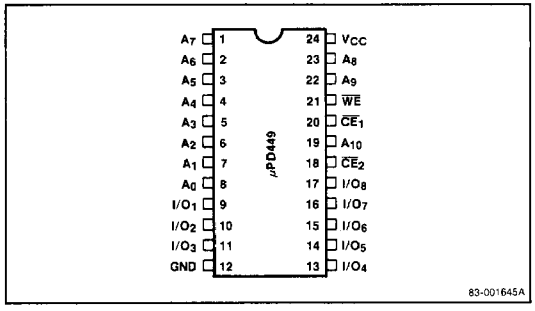
The μPD449 is a high-speed, low-power, 2048-word by 8-bit static CMOS RAM fabricated with advanced silicon-gate CMOS technology. A unique circuitry technique makes the μPD449 a very low operating power device which requires no clock or refreshing to operate. Since the device has two chip enable inputs, it is suited for battery backup applications. Minimum standby power current is drawn by this device when $\overline{CE}_1$ or $\overline{CE}_2$ equals V_{CC} independently of the other input levels. Data retention is guaranteed at a power supply voltage as low as 2 V.

The μPD449 has a standard 24-pin dual-in-line package and is plug-in compatible with 16K EPROMs.

Features

- ☐ Single +5 V supply
- ☐ Fully static operation — no clock or refreshing required
- ☐ TTL compatible — all inputs and outputs
- ☐ Common I/O using three-state output
- ☐ Two chip enable inputs for battery backup application
- ☐ Max access/min cycle times down to 150 ns
- ☐ Low power dissipation,
  - — Active: 38 mA max
  - — Standby: 10 μA max
- ☐ Data retention voltage: 2 V min
- ☐ Operating temperature range: −40 to +85°C
- ☐ Standard 24-pin plastic package
- ☐ Plug-in compatible with 16K EPROMs
- ☐ L version
  - — Standby current 1.0 μA max at 60°C for battery backup operation

Pin Configuration



Pin Identification

No.	Symbol	Function
1-8, 19, 22, 23	A_0-A_{10}	Address input
9-11, 13-17	I/O_1-I/O_8	Data input/output
20, 18	$\overline{CE}_1$, $\overline{CE}_2$	Chip enable input
21	$\overline{WE}$	Write enable input
24	V_{CC}	Power (+5 V)
12	GND	GND

Performance Ranges

Device	Access Time (Max)	Cycle Time (Min)	Power Supply (Max)	
			Active	Standby
μPD449C-3	150 ns	150 ns	38 mA	(Note 1)
μPD449C-2	200 ns	200 ns	30 mA	(Note 1)
μPD449C-1	250 ns	250 ns	26 mA	(Note 1)
μPD449C	450 ns	450 ns	18 mA	(Note 1)

Note:
(1) μPD449C-L/-1L/-2L/-3L
T_A = 25°C, 0.2 μA
T_A = 60°C, 1.0 μA
T_A = 85°C, 10 μA
μPD449C/-1/-2/-3
T_A = 25°C, 1.0 μA
T_A = 60°C, 5.0 μA
T_A = 85°C, 10 μA

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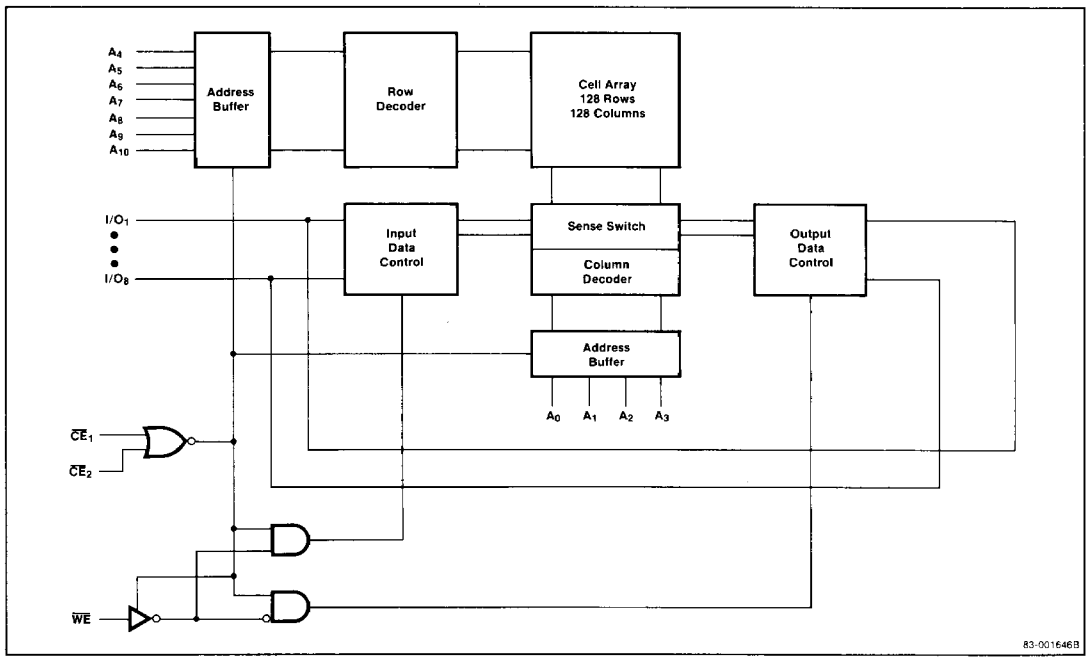
Block Diagram



Absolute Maximum Ratings

Power supply voltage, V_{CC}	7.0 V
Input voltage, V_{IN}	−0.3 to V_{CC} + 0.3 V
Output voltage, V_{OUT}	−0.3 to V_{CC} + 0.3 V
Operating temperature, T_{OPR}	−40 to +85°C
Storage temperature, T_{STG}	−55 to +125°C

Comment: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of the specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Capacitance

T_A = 25°C, f = 1 MHz

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input capacitance	C_{IN}			6	pF	V_{IN} = 0 V
Input/output capacitance	$C_{I/O}$			8	pF	$V_{I/O}$ = 0 V

Recommended DC Operating Conditions

T_A = −40 to +85°C

Parameter	Symbol	Limits Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input voltage low	V_{IL}	−0.3		0.8	V
Input voltage high	V_{IH}	2.2		V_{CC} + 0.3	V

Truth Table

$\overline{CE_1}$	$\overline{CE_2}$	$\overline{WE}$	MODE	I/O	I_{CC}
X	H	X	Not selected	Hi-Z	Standby
H	X	X	Not selected	Hi-Z	Standby
L	L	H	Read	D_{OUT}	Active
L	L	L	Write	D_{IN}	Active

AC Test Conditions

Input pulse levels	0.8 to 2.2 V
Input pulse rise and fall time	10 ns
Timing reference levels	1.5 V
Output load	1 TTL +100 pF

DC Characteristics

$T_A = -40$ to $+85°C$, $V_{CC} = 5\,V \pm 10\%$

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input leakage current	I_{LI}			1	μA	$V_{IN} = 0$ V to V_{CC}
I/O leakage current	I_{LO}			1	μA	$V_{I/O} = 0$ V to V_{CC}, $\overline{CE_1}$ or $\overline{CE_2} = V_{IH}$ or $\overline{WE} = V_{IL}$
Operating supply current	I_{CCA1}		(1)	(1)	mA	$\overline{CE_1}$ and $\overline{CE_2} = V_{IL}$, $I_{I/O} = 0$, min cycle
Operating supply current	I_{CCA2}		5	10	mA	$\overline{CE_1}$ and $\overline{CE_2} = V_{IL}$, $I_{I/O} = 0$ DC current
Standby supply current	I_{SB}		0.02	(2)	μA	$\overline{CE_1}$ or $\overline{CE_2} \geq V_{CC} - 0.2$ V, other $\overline{CE}$ input ≤ 0.2 V or $\geq V_{CC} - 0.2$ V, $V_{IN} = 0$ V to V_{CC}

DC Characteristics (cont)

$T_A = -40$ to $+85°C$, $V_{CC} = 5\,V \pm 10\%$

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Output voltage low	V_{OL}			0.4	V	$I_{OL} = 2.0$ mA
Output voltage high	V_{OH}	2.4			V	$I_{OH} = -1.0$ mA

Notes:

(1) μPD449C-3/3L, 25 mA typ, 38 mA max
μPD449C-2/2L, 20 mA typ, 30 mA max
μPD449C-1/1L, 18 mA typ, 26 mA max
μPD449C/-L, 12 mA typ, 18 mA max

(2) μPD449C-L/-1L/-2L/-3L
$T_A = 25°C$, 0.2 μA max
$T_A = 60°C$, 1.0 μA max
$T_A = 85°C$, 10 μA max
μPD449C/-1/-2/-3
$T_A = 25°C$, 1.0 μA max
$T_A = 60°C$, 5.0 μA max
$T_A = 85°C$, 10 μA max

AC Characteristics

$T_A = -40$ to $+85°C$, $V_{CC} = 5\,V \pm 10\%$

Parameter	Symbol	μPD449-3 Min	μPD449-3 Max	μPD449-2 Min	μPD449-2 Max	μPD449-1 Min	μPD449-1 Max	μPD449 Min	μPD449 Max	Unit
Read Cycle										
Read cycle time	t_{RC}	150		200		250		450		ns
Address access time	t_A		150		200		250		450	ns
Chip enable ($\overline{CE_1}$) to output valid	t_{CO1}		150		200		250		450	ns
Chip enable ($\overline{CE_2}$) to output valid	t_{CO2}		150		200		250		450	ns
Output hold from address change	t_{OH}	15		15		15		15		ns
Chip enable ($\overline{CE_1}$) to output in Lo-Z	t_{LZ1}	5		5		5		5		ns
Chip enable ($\overline{CE_2}$) to output in Lo-Z	t_{LZ2}	5		5		5		5		ns
Chip enable ($\overline{CE_1}$) to output in Hi-Z	t_{HZ1}		50		60		80		100	ns
Chip enable ($\overline{CE_2}$) to output in Hi-Z	t_{HZ2}		50		60		80		100	ns
Write Cycle										
Write cycle time	t_{WC}	150		200		250		450		ns
Chip enable ($\overline{CE_1}$) to end of write	t_{CW1}	120		150		180		210		ns
Chip enable ($\overline{CE_2}$) to end of write	t_{CW2}	120		150		180		210		ns
Address setup time	t_{AW}	0		0		0		0		ns
Write pulse width	t_{WP}	90		120		150		180		ns
Write recovery time	t_{WR}	0		0		0		0		ns
Data valid to end of write	t_{DW}	50		60		80		100		ns
Data hold time	t_{DH}	0		0		0		0		ns
Write enable to output in Hi-Z	t_{WZ}		50		60		80		100	ns
Output active from end of write	t_{OW}	10		10		10		10		ns

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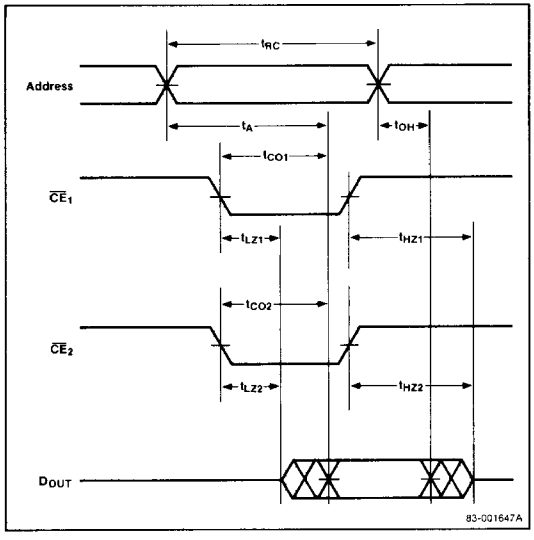
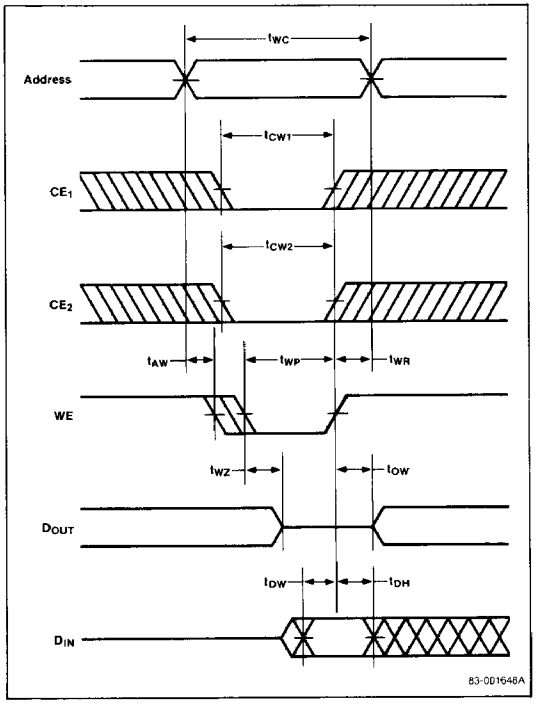
Timing Waveforms

Read Cycle (Address Access)



Write Cycle (Address Access)



Low V_{CC} Data Retention Characteristics

$T_A = -40$ to $+85°C$

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Data retention supply voltage	V_{CCDR}	2.0			V	$V_{IN}=0$ V to V_{CC}, $\overline{CE}_1$ or $\overline{CE}_2=V_{CC}$
Data retention supply current	I_{CCDR}		0.01	(1)	μA	$V_{IN}=0$ V to V_{CC}, $\overline{CE}_1$ or $\overline{CE}_2=V_{CC}$, other $\overline{CE}$ input = 0 V or V_{CC}, $V_{IN}=0$ V to V_{CC}, $V_{CC}=3.0$ V
Chip deselection to data retention mode	t_{CDR}	0			ns	
Operation recovery time	t_R	t_{RC}			ns	

Note:

(1) μPD449C-L/-1L/-2L/-3L
- $T_A = 25°C$, 0.2 μA max
- $T_A = 60°C$, 1.0 μA max
- $T_A = 85°C$, 10 μA max

μPD449C/-1/-2/-3
- $T_A = 25°C$, 1.0 μA max
- $T_A = 60°C$, 5.0 μA max
- $T_A = 85°C$, 10 μA max

Data Retention Timing Chart