

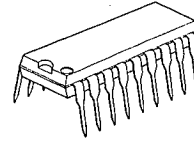
FDD READ AMPLIFIER SYSTEM

■ GENERAL DESCRIPTION

The NJM3470/3470A are monolithic read amplifier systems for obtaining digital signal from floppy disk storage.

The NJM3470/3470A are designed to get pulse output signal produced by the magnetic head amp of the input signal. They contain amplifiers, peak detector, and pulse shape circuit. They are classified two ranks by peak shift characteristic; NJM3470(5%), NJM3470A(2%)

■ PACKAGE OUTLINE

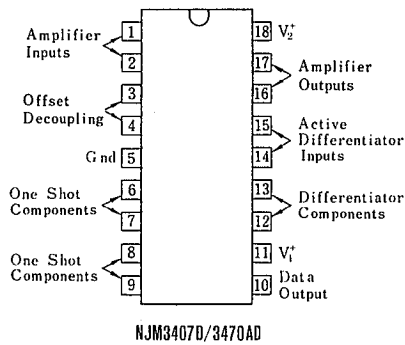


NJM3470D/3470AD

■ FEATURES

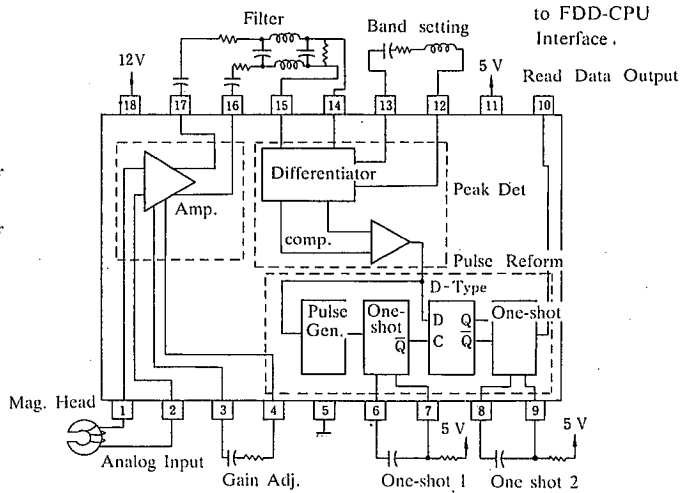
- Gain Adjustable
- Wide Bandwidth (5MHz min. @ -3dB)
- Peak Shift (A-rank : 2%max.)
- Package Outline DIP18
- Bipolar Technology

■ PIN CONFIGURATION



NJM3470D/3470AD

■ BLOCK DIAGRAM



NJM3470 BLOCK DIAGRAM and STANDARD OUTPUT CIRCUIT

■ ABSOLUTE MAXIMUM RATINGS

(Ta=25°C)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage I (Pin 11)	V <sup>+</sup> <sub>1</sub>	7	V
Supply Voltage II (Pin 18)	V <sup>+</sup> <sub>2</sub>	16	V
Input Voltage (Pin 1-2)	V <sub>IN</sub>	-0.2~7.0	V
Output Voltage (Pin 10)	V <sub>O</sub>	-0.2~7.0	V
Operating Temperature Range	T <sub>opr</sub>	-20~75	°C
Storage Temperature Range	T <sub>stg</sub>	-40~125	°C

## ■ ELECTRICAL CHARACTERISTICS

( $T_a=25^\circ\text{C}$ ,  $V^+=5\text{V}$ ,  $V^+=12\text{V}$ ) note: ( ) apply to A-rank.

### Amplifier Block

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Differential Voltage Gain	$A_{VD}$	$f=200\text{kHz}$ , $V_{ID}=5.0\text{mVrms}$	80 (100)	100 (110)	120 (120)	V/V
Input Bias Current	$I_B$		—	-10	-25	$\mu\text{A}$
Input Common Mode Range	$V_{ICM}$	THD=5%	-0.1	—	1.0	V
Differential Input Voltage Range	$V_{ID}$	THD=5%	—	—	25	mV <sub>P-P</sub>
Output Voltage Swing Differential	$V_{OD}$		3.0	4.0	—	V <sub>P-P</sub>
Output Source Current	$I_{SOURCE}$		—	8.0	—	mA
Output Sink Current	$I_{SINK}$		2.8	4.0	—	mA
Small Signal Input Resistance	$r_i$		100	250	—	k $\Omega$
Small Signal Output Resistance	$r_o$		—	15	—	$\Omega$
Bandwidth, -3.0dB	BW	$V_{ID}=2.0\text{mVrms}$	5.0	—	—	MHz
Common Mode Rejection Ratio	CMR	$f=100\text{kHz}$ , $A_{VD}=40\text{dB}$ , $V_{in}=200\text{mV}_{P-P}$	50	—	—	dB
Supply Voltage Rejection Ratio ( $V_1^+$ )	$SVR_1$	$A_{VD}=40\text{dB}$ , $4.75\leq V_1^+\leq 5.25\text{V}$	50	—	—	dB
Supply Voltage Rejection Ratio ( $V_2^+$ )	$SVR_2$	$A_{VD}=40\text{dB}$ , $10\leq V_2^+\leq 14\text{V}$	60	—	—	dB
Differential Output Offset	$V_{DO}$	$V_{ID}=V_{IN}=0\text{V}$	—	—	0.4	V
Common Mode Output Offset	$V_{CO}$	$V_{ID}=V_{IN}=0\text{V}$	—	3.0	—	V
Equivalent Input Noise Voltage	$e_n$	BW=10Hz~1.0MHz	—	15	—	$\mu\text{Vrms}$

### Peak Detector Block

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Differentiator Output Sink Current	$I_{OD}$	$V_{OD}=5\text{V}$	1.0	1.4	—	mA
Peak Shift	PS	$f=250\text{kHz}$ , $V_{ID}=1.0\text{V}_{P-P}$ , $i_{cap}=500\mu\text{A}$ $PS=t_{PS1}-t_{PS2}/2(t_{PS1}+t_{PS2})\times 100$	—	—	5.0 (2.0)	%
Differentiator Input Resistance, Differential	$r_{ID}$		—	30	—	k $\Omega$
Differentiator Output Resistance, Differential	$r_{OD}$		—	40	—	$\Omega$

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### Logic Block

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Timing Accuracy (mono #1)	$E_{t1}$	$t_1=1.0\mu\text{S}=0.625R_1C_1+200\text{nS}$ $R_1=6.4\text{k}\Omega$ $C_1=200\text{pF}$ (accuracy: $R_1$ , $C_1$ ) $1.5\text{k}\Omega\leq R_1\leq 10\text{k}\Omega$ $150\text{pF}\leq C_1\leq 680\text{pF}$	85	—	115	%
Timing Accuracy (mono #2)	$t_2$		150	—	1000	nS
Timing Accuracy (mono #2)	$E_{t2}$	$t_2=200\text{nS}=0.625R_2C_2$ $R_2=1.6\text{k}\Omega$ $C_2=200\text{pF}$ (accuracy: $R_2$ , $C_2$ ) $1.5\text{k}\Omega\leq R_2\leq 10\text{k}\Omega$ $100\text{pF}$ $C_2$ 800pF	85	—	115	%

## MEMO

[CAUTION]

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