DESCRIPTION

The 7560 group is the 8-bit microcomputer based on the 740 family core technology.
The 7560 group has the LCD drive control circuit, an 8-channel A-D/D-A converter, UART and PWM as additional functions.
The various microcomputers in the 7560 group include variations of internal memory size and packaging. For details, refer to the section on part numbering.
For details on availability of microcomputers in the 7560 Group, refer the section on group expansion.

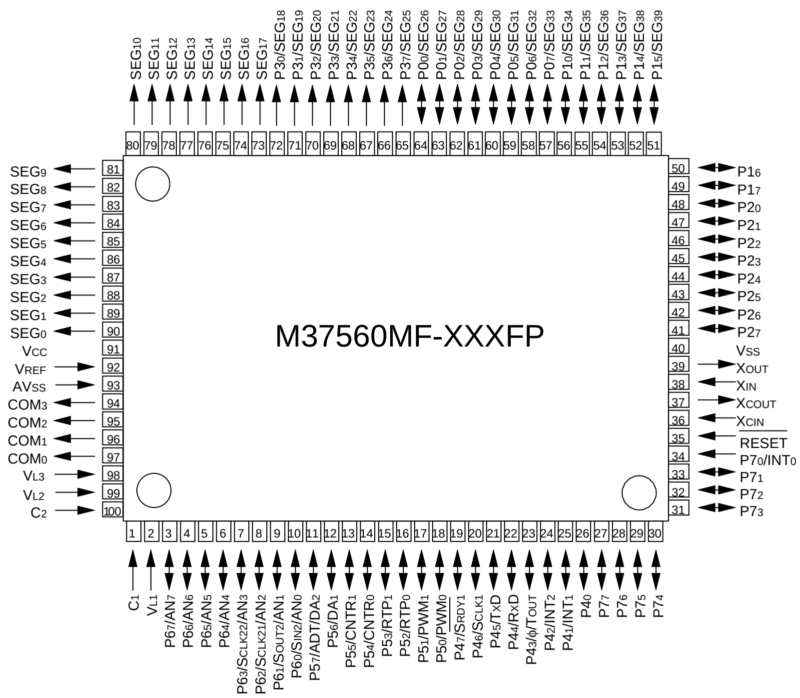
FEATURES

- Basic machine-language instructions 71
- The minimum instruction execution time .... 0.5 µs (at 8 MHz oscillation frequency)
- Memory size
  ROM .... 32 K to 60 K bytes
  RAM .... 1024 to 2560 bytes
- Programmable input/output ports 55
- Software pull-up resistors .... Built-in
- Output ports 8
- Input ports 1
- Interrupts .... 17 sources, 16 vectors (includes key input interrupt)
- Timers .... 8-bit × 3, 16-bit × 2
- Serial I/O1 .... 8-bit × 1 (UART or Clock-synchronous)
- Serial I/O2 .... 8-bit × 1 (Clock-synchronous)
- PWM output .... 8-bit × 1
- A-D converter .... 8-bit × 8 channels
- D-A converter .... 8-bit × 2 channels
- LCD drive control circuit
  Bias 1/2, 1/3
  Duty 1/2, 1/3, 1/4
  Common output 4
  Segment output 40
- 2 Clock generating circuits
  (connect to external ceramic resonator or quartz-crystal oscillator)
- Watchdog timer .... 14-bit × 1
- Power source voltage .... 2.2 to 5.5 V
- Power dissipation
  In high-speed mode .... 40 mW
  (at 8 MHz oscillation frequency, at 5 V power source voltage)
  In low-speed mode .... 60 µW
  (at 32 kHz oscillation frequency, at 3 V power source voltage)
- Operating temperature range .... – 20 to 85°C

APPLICATIONS

Camera, household appliances, consumer electronics, etc.

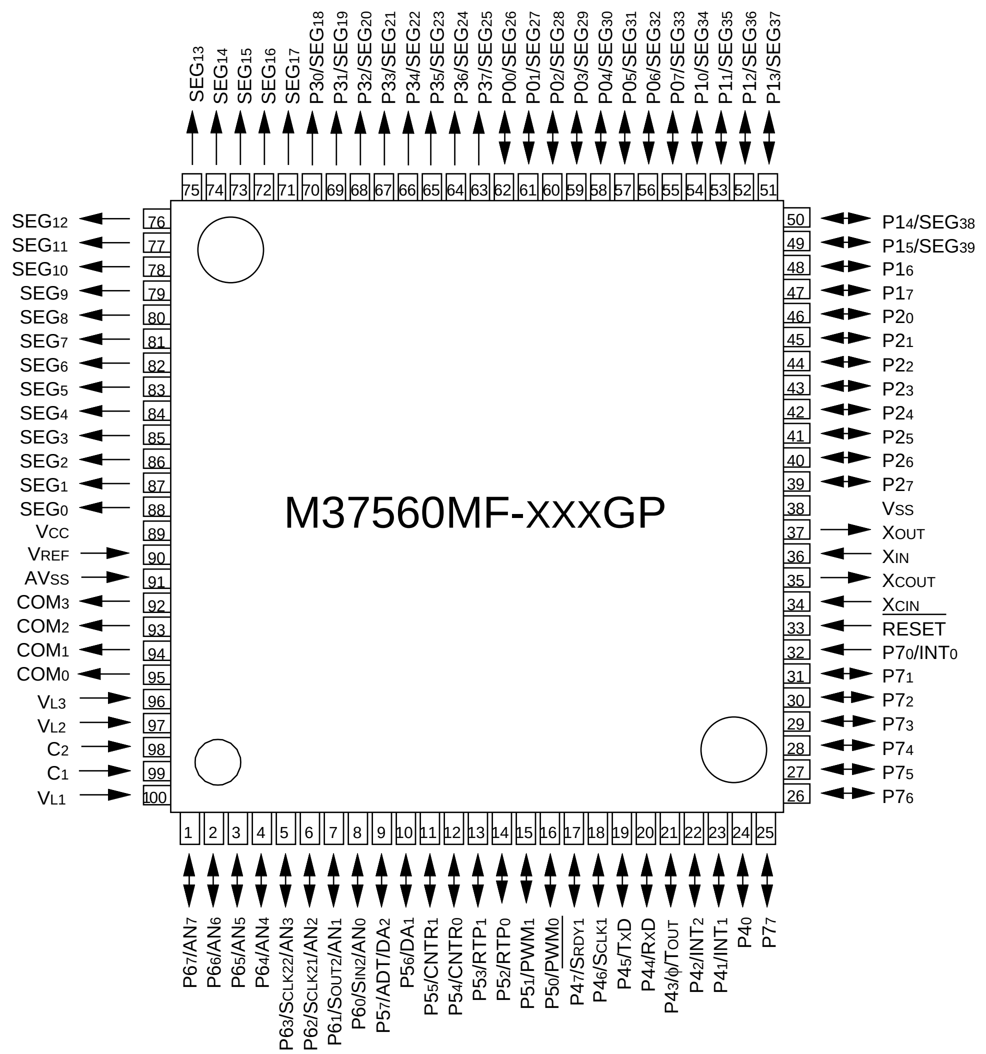
PIN CONFIGURATION (TOP VIEW)



Package type : 100P6S-A

Fig. 1 Pin configuration of M37560MF-XXXFP

PIN CONFIGURATION (TOP VIEW)



Package type : 100P6Q-A

Fig. 2 Pin configuration of M37560MF-XXXGP

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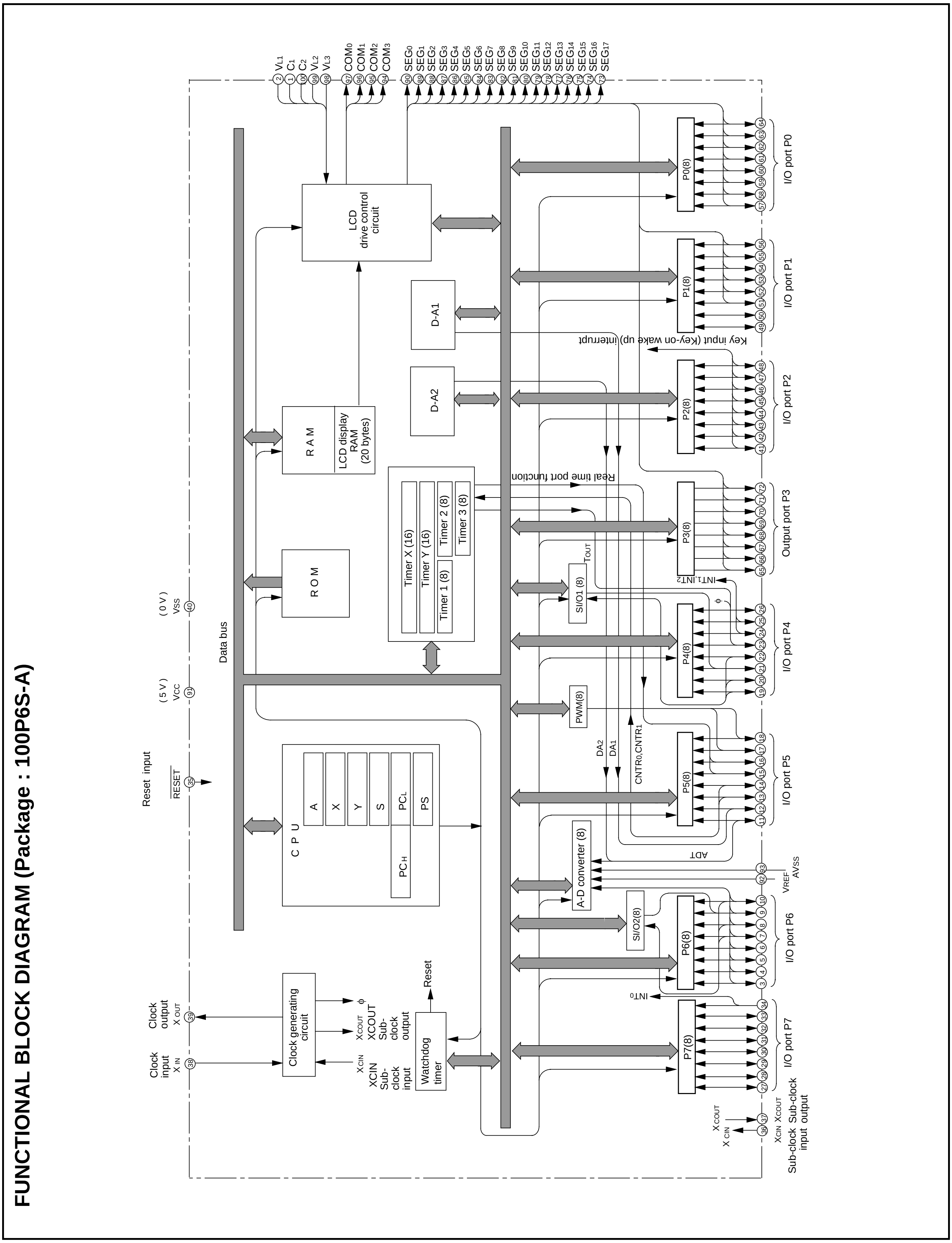


Fig. 3 Functional block diagram

PIN DESCRIPTION

Table 1 Pin description (1)

Pin	Name	Function	Function except a port function
V_{CC}, V_{SS}	Power source	•Apply voltage of 2.2 V to 5.5 V to V_{CC}, and 0 V to V_{SS}.	
V_{REF}	Analog reference voltage	•Reference voltage input pin for A-D converter.	
AV_{SS}	Analog power source	•GND input pin for A-D converter. •Connect to V_{SS}.	
$\overline{RESET}$	Reset input	•Reset input pin for active "L".	
X_{IN}	Clock input	•Input and output pins for the main clock generating circuit. •Connect a ceramic resonator or a quartz-crystal oscillator between the X_{IN} and X_{OUT} pins to set the oscillation frequency. •If an external clock is used, connect the clock source to the X_{IN} pin and leave the X_{OUT} pin open. A feedback resistor is built-in.	
X_{OUT}	Clock output		
V_{L1}–V_{L3}	LCD power source	•Input $0 \leq V_{L1} \leq V_{L2} \leq V_{L3}$ voltage. •Input 0 – V_{L3} voltage to LCD. ($0 \leq V_{L1} \leq V_{L2} \leq V_{L3}$ when a voltage is multiplied.)	
C_1, C_2	Charge-pump capacitor pin	•External capacitor pins for a voltage multiplier (3 times) of LCD contorl.	
COM_0–COM_3	Common output	•LCD common output pins. •COM_2 and COM_3 are not used at 1/2 duty ratio. •COM_3 is not used at 1/3 duty ratio.	
SEG_0–SEG_{17}	Segment output	•LCD segment output pins.	
$P0_0/SEG_{26}$–$P0_7/SEG_{33}$	I/O port P0	•8-bit I/O port. •CMOS compatible input level. •CMOS 3-state output structure. •Pull-up control is enabled. •I/O direction register allows each 8-bit pin to be programmed as either input or output.	•LCD segment output pins
$P1_0/SEG_{34}$–$P1_5/SEG_{39}$	I/O port P1	•6-bit I/O port with same function as port P0. •CMOS compatible input level. •CMOS 3-state output structure. •Pull-up control is enabled. •I/O direction register allows each 6-bit pin to be programmed as either input or output.	
$P1_6$, $P1_7$		•2-bit I/O port. •CMOS compatible input level. •CMOS 3-state output structure. •I/O direction register allows each pin to be individually programmred as either input or output. •Pull-up control is enabled.	
$P2_0$ – $P2_7$	I/O port P2	•8-bit I/O port with same function as $P1_6$ and $P1_7$. •CMOS compatible input level. •CMOS 3-state output structure. •Pull-up control is enabled.	•Key input (key-on wake-up) interrupt input pins
$P3_0/SEG_{18}$ – $P3_7/SEG_{25}$	Output port P3	•8-bit output port with same function as port P0. •CMOS 3-state output structure. •Port output control is enabled.	•LCD segment output pins

Table 2 Pin description (2)

Pin	Name	Function	Function except a port function
$P4_0$	I/O port P4	•1-bit I/O port with same function as $P1_6$ and $P1_7$. •CMOS compatible input level. •N-channel open-drain output structure.	
$P4_1/INT_1$, $P4_2/INT_2$		•7-bit I/O port with same function as $P1_6$ and $P1_7$. •CMOS compatible input level. •CMOS 3-state output structure. •Pull-up control is enabled.	•Interrupt input pins
$P4_3/\phi/T_{OUT}$			•ϕ clock output pin •Timer 2 output pin
$P4_4/R_XD$, $P4_5/T_XD$, $P4_6/\overline{S_{CLK1}}$, $P4_7/\overline{S_{RDY1}}$			•Serial I/O1 I/O pins
$P5_0/PWM_0$, $P5_1/PWM_1$	I/O port P5	•8-bit I/O port with same function as $P1_6$ and $P1_7$. •CMOS compatible input level. •CMOS 3-state output structure. •Pull-up control is enabled.	•PWM function pins
$P5_2/RTP_0$, $P5_3/RTP_1$			•Real time port function pins
$P5_4/CNTR_0$, $P5_5/CNTR_1$			•Timer X, Y function pins
$P5_6/DA_1$, $P5_7/ADT/DA_2$			•D-A conversion output pins
$P6_0/AN_0/S_{IN2}$, $P6_1/AN_1/S_{OUT2}$, $P6_2/AN_2/S_{CLK21}$, $P6_3/AN_3/S_{CLK22}$	I/O port P6	•8-bit I/O port with same function as $P1_6$ and $P1_7$. •CMOS compatible input level. •CMOS 3-state output structure. •Pull-up control is enabled.	•A-D conversion input pins •Serial I/O2 I/O pins
$P6_4/AN_4$– $P6_7/AN_7$			•A-D conversion input pins
$P7_0/INT_0$	Input port P7	•1-bit input port.	•Interrupt input pin
$P7_1$–$P7_7$	I/O port P7	•7-bit I/O port with same function as $P1_6$ and $P1_7$. •CMOS compatible input level. •N-channel open-drain output structure.	
X_{COUT}	Sub-clock output	•Sub-clock generating circuit I/O pins. (Connect a resonator. External clock cannot be used.)	
X_{CIN}	Sub-clock input		

PART NUMBERING

Product M37560 **M** **F** – **XXX** **FP**

Package type
FP : 100P6S-A package
GP : 100P6Q-A package

ROM number

ROM/PROM size
1 : 4096 bytes
2 : 8192 bytes
3 : 12288 bytes
4 : 16384 bytes
5 : 20480 bytes
6 : 24576 bytes
7 : 28672 bytes
8 : 32768 bytes
9 : 36864 bytes
A : 40960 bytes
B : 45056 bytes
C : 49152 bytes
D : 53248 bytes
E : 57344 bytes
F : 61440 bytes

The first 128 bytes and the last 2 bytes of ROM are reserved areas ; they cannot be used.

Memory type
M : Mask ROM version

Fig. 4 Part numbering

GROUP EXPANSION

Mitsubishi plans to expand the 7560 group as follows.

Memory Type

Support for mask ROM version.

Memory Size

ROM size .... 32 K to 60 K bytes
RAM size .... 1024 to 2560 bytes

Packages

100P6Q-A .... 0.5 mm-pitch plastic molded QFP
100P6S-A .... 0.65 mm-pitch plastic molded QFP

Memory Expansion Plan

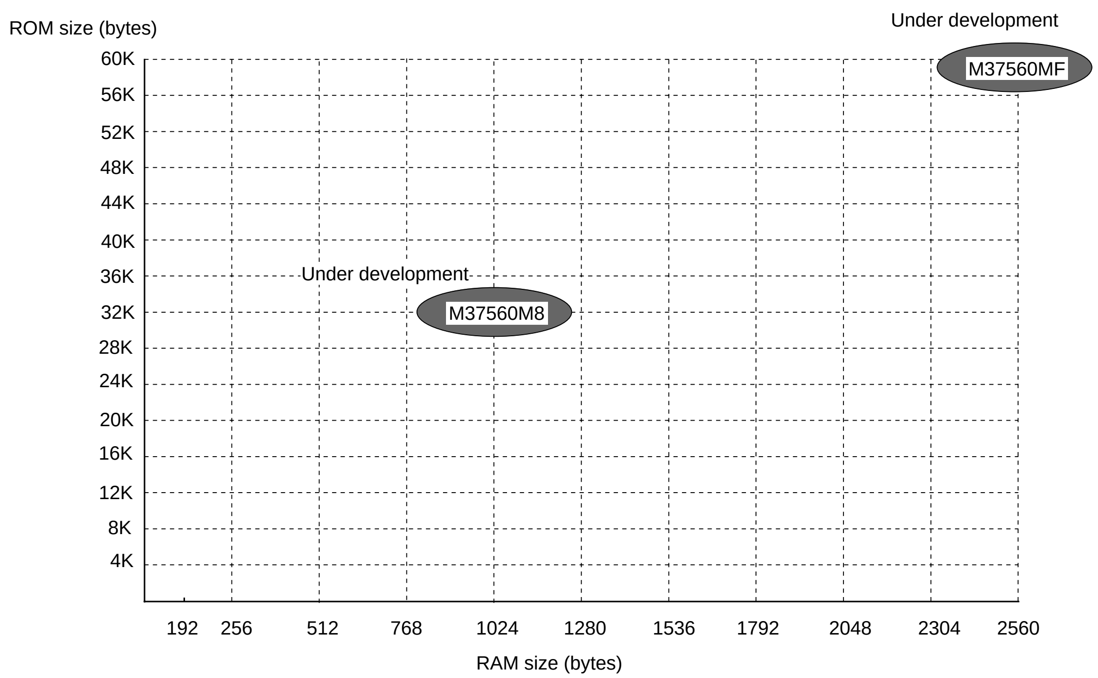


Fig. 5 Memory expansion plan

Currently products are listed below.

Table 3. List of products **As of Mar. 2001**

Product	ROM size (bytes) ROM size for User in ( )	RAM size (bytes)	Package	Remarks
M37560M8-XXXFP	32768 (32638)	1024	100P6S-A	Mask ROM version
M37560M8-XXXGP			100P6Q-A	Mask ROM version
M37560MF-XXXFP	61440 (61310)	2560	100P6S-A	Mask ROM version
M37560MF-XXXGP			100P6Q-A	Mask ROM version

FUNCTIONAL DESCRIPTION
CENTRAL PROCESSING UNIT (CPU)

The 7560 group uses the standard 740 family instruction set. Refer to the table of 740 family addressing modes and machine instructions or the 740 Family Software Manual for details on the instruction set.
Machine-resident 740 family instructions are as follows:
The FST and SLW instruction cannot be used.
The STP, WIT, MUL, and DIV instruction can be used.

[Accumulator (A)]

The accumulator is an 8-bit register. Data operations such as data transfer, etc., are executed mainly through the accumulator.

[Index Register X (X)]

The index register X is an 8-bit register. In the index addressing modes, the value of the OPERAND is added to the contents of register X and specifies the real address.

[Index Register Y (Y)]

The index register Y is an 8-bit register. In partial instruction, the value of the OPERAND is added to the contents of register Y and specifies the real address.

[Stack Pointer (S)]

The stack pointer is an 8-bit register used during subroutine calls and interrupts. This register indicates start address of stored area (stack) for storing registers during subroutine calls and interrupts.
The low-order 8 bits of the stack address are determined by the contents of the stack pointer. The high-order 8 bits of the stack address are determined by the stack page selection bit. If the stack page selection bit is “0” , the high-order 8 bits becomes “00_{16}”. If the stack page selection bit is “1”, the high-order 8 bits becomes “01_{16}”.
The operations of pushing register contents onto the stack and popping them from the stack are shown in Figure 7.
Store registers other than those described in Figure 7 with program when the user needs them during interrupts or subroutine calls.

[Program Counter (PC)]

The program counter is a 16-bit counter consisting of two 8-bit registers PC_H and PC_L. It is used to indicate the address of the next instruction to be executed.

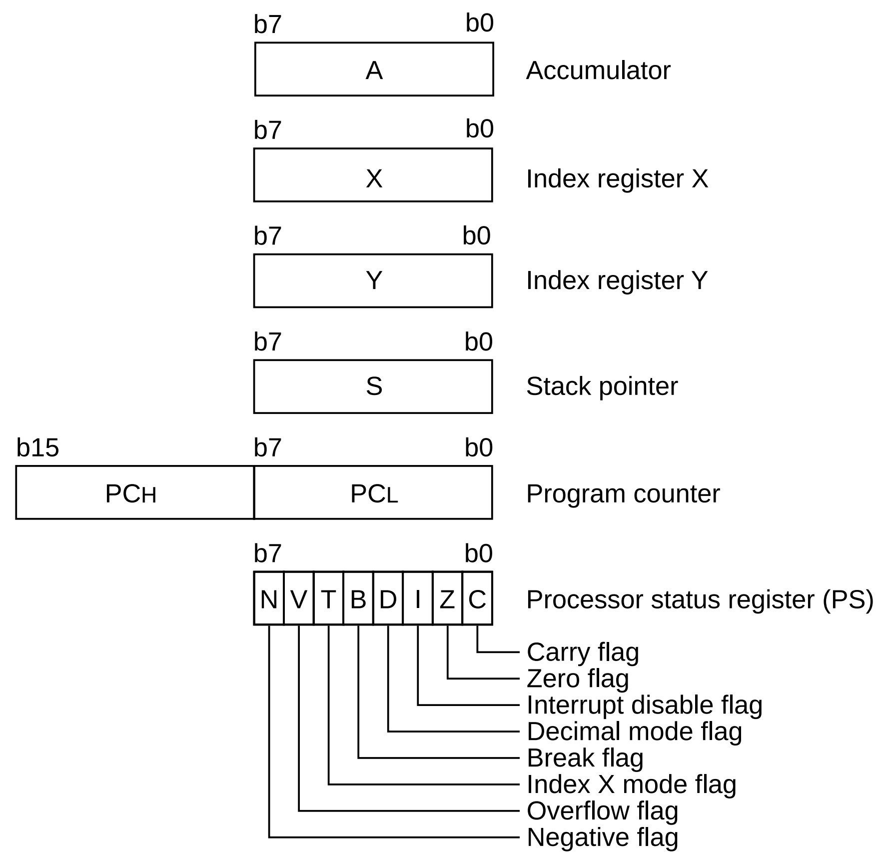


Fig. 6 740 Family CPU register structure

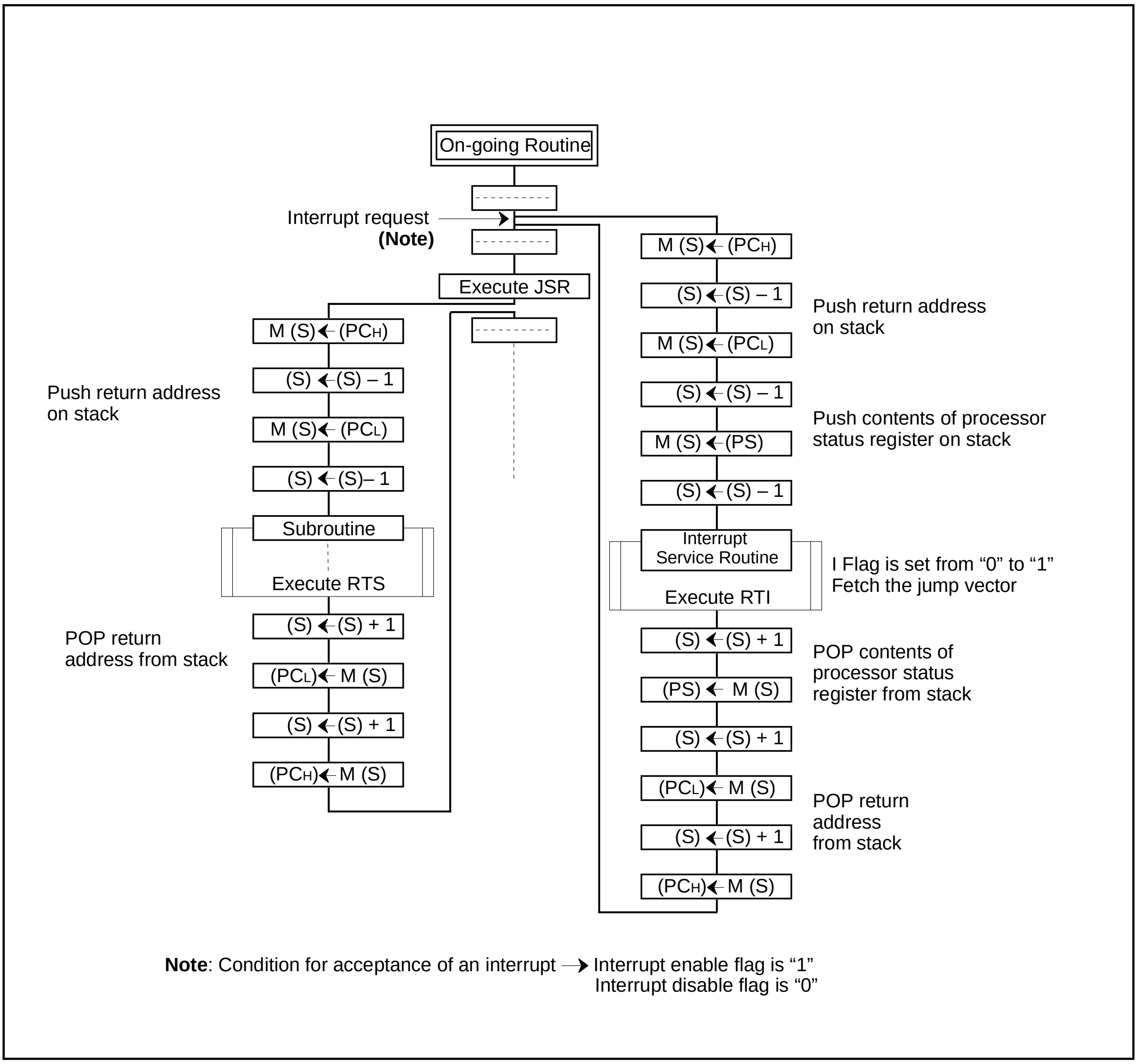


Fig. 7 Register push and pop at interrupt generation and subroutine call

Table 4 Push and pop instructions of accumulator or processor status register

	Push instruction to stack	Pop instruction from stack
Accumulator	PHA	PLA
Processor status register	PHP	PLP

[Processor status register (PS)]

The processor status register is an 8-bit register consisting of 5 flags which indicate the status of the processor after an arithmetic operation and 3 flags which decide MCU operation. Branch operations can be performed by testing the Carry (C) flag , Zero (Z) flag, Overflow (V) flag, or the Negative (N) flag. In decimal mode, the Z, V, N flags are not valid.

- Bit 0: Carry flag (C)
  The C flag contains a carry or borrow generated by the arithmetic logic unit (ALU) immediately after an arithmetic operation. It can also be changed by a shift or rotate instruction.
- Bit 1: Zero flag (Z)
  The Z flag is set if the result of an immediate arithmetic operation or a data transfer is “0”, and cleared if the result is anything other than “0”.
- Bit 2: Interrupt disable flag (I)
  The I flag disables all interrupts except for the interrupt generated by the BRK instruction.
  Interrupts are disabled when the I flag is “1”.
- Bit 3: Decimal mode flag (D)
  The D flag determines whether additions and subtractions are executed in binary or decimal. Binary arithmetic is executed when this flag is “0”; decimal arithmetic is executed when it is “1”.
  Decimal correction is automatic in decimal mode. Only the ADC and SBC instructions can be used for decimal aritmetic.
- Bit 4: Break flag (B)
  The B flag is used to indicate that the current interrupt was generated by the BRK instruction. The BRK flag in the processor status register is always “0”. When the BRK instruction is used to generate an interrupt, the processor status register is pushed onto the stack with the break flag set to “1”.
- Bit 5: Index X mode flag (T)
  When the T flag is “0”, arithmetic operations are performed between accumulator and memory. When the T flag is “1”, direct arithmetic operations and direct data transfers are enabled between memory locations.
- Bit 6: Overflow flag (V)
  The V flag is used during the addition or subtraction of one byte of signed data. It is set if the result exceeds +127 to -128. When the BIT instruction is executed, bit 6 of the memory location operated on by the BIT instruction is stored in the overflow flag.
- Bit 7: Negative flag (N)
  The N flag is set if the result of an arithmetic operation or data transfer is negative. When the BIT instruction is executed, bit 7 of the memory location operated on by the BIT instruction is stored in the negative flag.

Table 5 Set and clear instructions of each bit of processor status register

	C flag	Z flag	I flag	D flag	B flag	T flag	V flag	N flag
Set instruction	SEC	–	SEI	SED	–	SET	–	–
Clear instruction	CLC	–	CLI	CLD	–	CLT	CLV	–

[CPU Mode Register (CPUM)] 003B16

The CPU mode register contains the stack page selection bit and the internal system clock selection bit.
The CPU mode register is allocated at address 003B16.

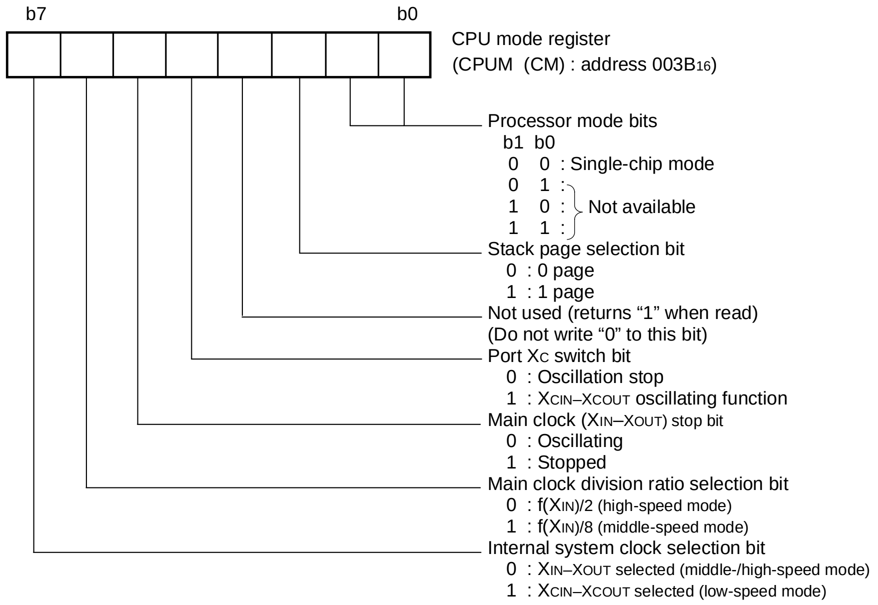


Fig. 8 Structure of CPU mode register

MEMORY
Special Function Register (SFR) Area
The Special Function Register area in the zero page contains control registers such as I/O ports and timers.

RAM
RAM is used for data storage and for stack area of subroutine calls and interrupts.

ROM
The first 128 bytes and the last 2 bytes of ROM are reserved for device testing and the rest is user area for storing programs.

Interrupt Vector Area
The interrupt vector area contains reset and interrupt vectors.

Zero Page
The 256 bytes from addresses 0000_{16} to $00FF_{16}$ are called the zero page area. The internal RAM and the special function registers (SFR) are allocated to this area.
The zero page addressing mode can be used to specify memory and register addresses in the zero page area. Access to this area with only 2 bytes is possible in the zero page addressing mode.

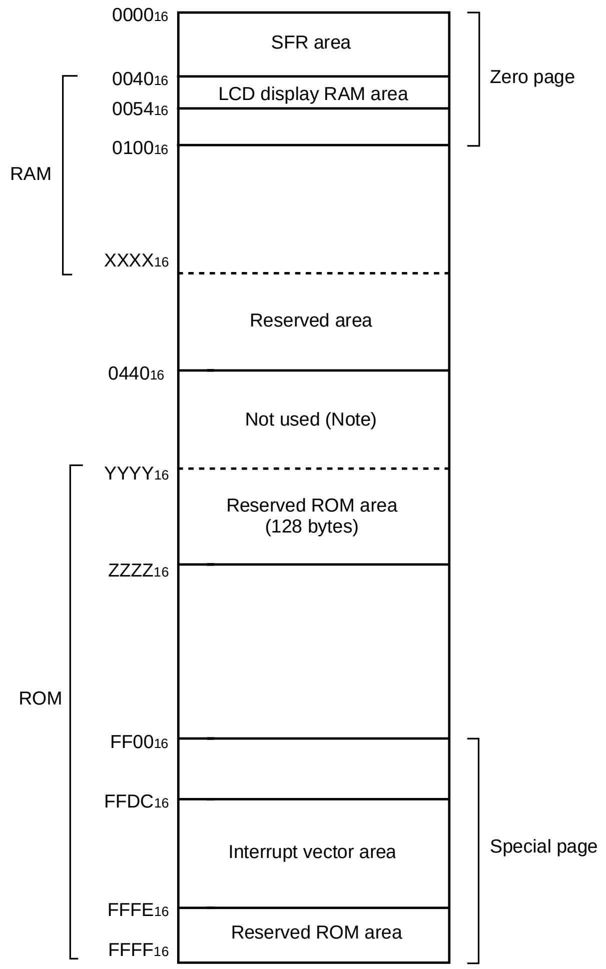
Special Page
The 256 bytes from addresses $FF00_{16}$ to $FFFF_{16}$ are called the special page area. The special page addressing mode can be used to specify memory addresses in the special page area. Access to this area with only 2 bytes is possible in the special page addressing mode.

RAM area

RAM size (bytes)	Address $XXXX_{16}$
192	$00FF_{16}$
256	$013F_{16}$
384	$01BF_{16}$
512	$023F_{16}$
640	$02BF_{16}$
768	$033F_{16}$
896	$03BF_{16}$
1024	$043F_{16}$
1536	$063F_{16}$
2048	$083F_{16}$
2560	$0A3F_{16}$

ROM area

ROM size (bytes)	Address $YYYY_{16}$	Address $ZZZZ_{16}$
4096	$F000_{16}$	$F080_{16}$
8192	$E000_{16}$	$E080_{16}$
12288	$D000_{16}$	$D080_{16}$
16384	$C000_{16}$	$C080_{16}$
20480	$B000_{16}$	$B080_{16}$
24576	$A000_{16}$	$A080_{16}$
28672	9000_{16}	9080_{16}
32768	8000_{16}	8080_{16}
36864	7000_{16}	7080_{16}
40960	6000_{16}	6080_{16}
45056	5000_{16}	5080_{16}
49152	4000_{16}	4080_{16}
53248	3000_{16}	3080_{16}
57344	2000_{16}	2080_{16}
61440	1000_{16}	1080_{16}



Note: When RAM area exceeds 1024 bytes, the areas shown the table are used.

Fig. 9 Memory map diagram

0000_{16}	Port P0 (P0)	0020_{16}	Timer X (low) (TXL)
0001_{16}	Port P0 direction register (P0D)	0021_{16}	Timer X (high) (TXH)
0002_{16}	Port P1 (P1)	0022_{16}	Timer Y (low) (TYL)
0003_{16}	Port P1 direction register (P1D)	0023_{16}	Timer Y (high) (TYH)
0004_{16}	Port P2 (P2)	0024_{16}	Timer 1 (T1)
0005_{16}	Port P2 direction register (P2D)	0025_{16}	Timer 2 (T2)
0006_{16}	Port P3 (P3)	0026_{16}	Timer 3 (T3)
0007_{16}	Port P3 output control register (P3C)	0027_{16}	Timer X mode register (TXM)
0008_{16}	Port P4 (P4)	0028_{16}	Timer Y mode register (TYM)
0009_{16}	Port P4 direction register (P4D)	0029_{16}	Timer 123 mode register (T123M)
$000A_{16}$	Port P5 (P5)	$002A_{16}$	T_{OUT}/ϕ output control register (CKOUT)
$000B_{16}$	Port P5 direction register (P5D)	$002B_{16}$	PWM control register (PWMCON)
$000C_{16}$	Port P6 (P6)	$002C_{16}$	PWM prescaler (PREPWM)
$000D_{16}$	Port P6 direction register (P6D)	$002D_{16}$	PWM register (PWM)
$000E_{16}$	Port P7 (P7)	$002E_{16}$	Reserved area
$000F_{16}$	Port P7 direction register (P7D)	$002F_{16}$	Reserved area
0010_{16}		0030_{16}	Reserved area
0011_{16}		0031_{16}	Reserved area
0012_{16}		0032_{16}	D-A1 conversion register (DA1)
0013_{16}		0033_{16}	D-A2 conversion register (DA2)
0014_{16}	Reserved area	0034_{16}	A-D control register (ADCON)
0015_{16}	Key input control register (KIC)	0035_{16}	A-D conversion register (AD)
0016_{16}	PULL register A (PULLA)	0036_{16}	D-A control register (DACON)
0017_{16}	PULL register B (PULLB)	0037_{16}	Watchdog timer control register (WDTCON)
0018_{16}	Transmit/Receive buffer register(TB/RB)	0038_{16}	Segment output enable register (SEG)
0019_{16}	Serial I/O1 status register (SIO1STS)	0039_{16}	LCD mode register (LM)
$001A_{16}$	Serial I/O1 control register (SIO1CON)	$003A_{16}$	Interrupt edge selection register (INTEDGE)
$001B_{16}$	UART control register (UARTCON)	$003B_{16}$	CPU mode register (CPUM)
$001C_{16}$	Baud rate generator (BRG)	$003C_{16}$	Interrupt request register 1(IREQ1)
$001D_{16}$	Serial I/O2 control register (SIO2CON)	$003D_{16}$	Interrupt request register 2(IREQ2)
$001E_{16}$	Reserved area	$003E_{16}$	Interrupt control register 1(ICON1)
$001F_{16}$	Serial I/O2 register (SIO2)	$003F_{16}$	Interrupt control register 2(ICON2)

Fig. 10 Memory map of special function register (SFR)

I/O PORTS

Direction Registers

The I/O ports (ports P0, P1, P2, P4, P5, P6, $P7_1$–$P7_7$) have direction registers which determine the input/output direction of each individual pin. (Ports $P0_0$–$P0_7$ are shared with bit 0 of the port P0 direction register, and ports $P1_0$–$P1_5$ shared with bit 0 of the port P1 direction register.) Each bit in a direction register corresponds to one pin, and each pin can be set to be input port or output port. When “0” is written to the bit corresponding to a pin, that pin becomes an input pin. When “1” is written to that bit, that pin becomes an output pin.

If data is read from a pin set to output, the value of the port output latch is read, not the value of the pin itself. Pins set to input are floating. If a pin set to input is written to, only the port output latch is written to and the pin remains floating.

Port P3 Output Control Register

Bit 0 of the port P3 output control register (address 0007_{16}) enables control of the output of ports $P3_0$–$P3_7$.

When the bit is set to “1”, the port output function is valid.

When resetting, bit 0 of the port P3 output control register is set to “0” (the port output function is invalid) and pulled up.

Pull-up Control

By setting the PULL register A (address 0016_{16}) or the PULL register B (address 0017_{16}), ports P0 to P2, P4 to P6 can control pull-up with a program.

However, the contents of PULL register A and PULL register B do not affect ports programmed as the output ports.

The PULL register A setting is invalid for pins set to segment output with the segment output enable register.

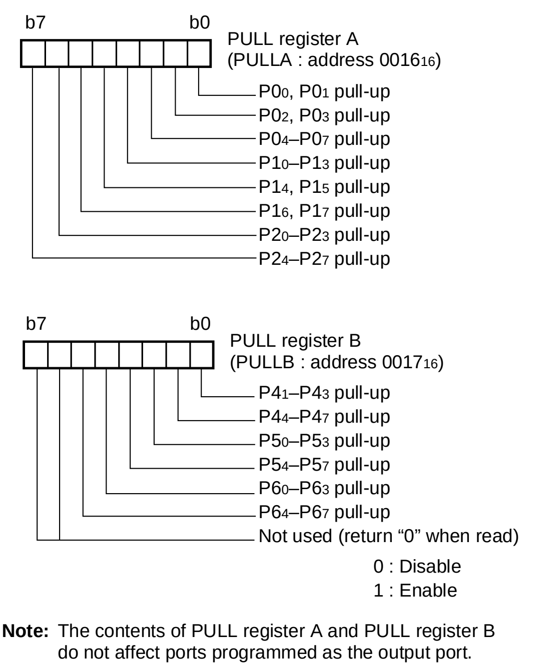


Fig. 11 Structure of PULL register A and PULL register B

Table 6 List of I/O port function (1)

Pin	Name	Input/Output	I/O Format	Non-Port Function	Related SFRs	Diagram No.
P0$_0$/SEG$_{26}$– P0$_7$/SEG$_{33}$	Port P0	Input/output, byte unit	CMOS compatible input level CMOS 3-state output	LCD segment output	PULL register A Segment output enable register	(1) (2)
P1$_0$/SEG$_{34}$– P1$_5$/SEG$_{39}$	Port P1	Input/output, 6-bit unit	CMOS compatible input level CMOS 3-state output	LCD segment output	PULL register A Segment output enable register	(1) (2)
P1$_6$, P1$_7$		Input/output, individual bits	CMOS compatible input level CMOS 3-state output		PULL register A	(4)
P2$_0$–P2$_7$	Port P2	Input/output, individual bits	CMOS compatible input level CMOS 3-state output	Key input (key-on wake-up) interrupt input	PULL register A Interrupt control register2 Key input control register	
P3$_0$/SEG$_{18}$– P3$_7$/SEG$_{25}$	Port P3	Output	CMOS 3-state output	LCD segment output	Segment output enable register P3 output enable register	(3)
P4$_0$	Port P4	Input/output, individual bits	CMOS compatible input level N-channel open-drain output			(13)
P4$_1$/INT$_1$, P4$_2$/INT$_2$			CMOS compatible input level CMOS 3-state output	External interrupt input	Interrupt edge selection register	(4)
P4$_3$/ϕ/TOUT				Timer output ϕ output	PULL register B Timer 123 mode register TOUT/ϕ output control register	(12)
P4$_4$/RxD, P4$_5$/TxD, P4$_6$/SCLK1, P4$_7$/$\overline{\text{SRDY1}}$				Serial I/O1 function I/O	PULL register B Serial I/O1 control register Serial I/O1 status register UART control register	(5) (6) (7) (8)
P5$_0$/PWM$_0$, P5$_1$/PWM$_1$	Port P5	Input/output, individual bits	CMOS compatible input level CMOS 3-state output	PWM output	PULL register B PWM control register	(10)
P5$_2$/RTP$_0$, P5$_3$/RTP$_1$				Real time port function output	PULL register B Timer X mode register	(9)
P5$_4$/CNTR$_0$				Timer X function I/O	PULL register B Timer X mode register	(11)
P5$_5$/CNTR$_1$				Timer Y function input	PULL register B Timer Y mode register	(14)
P5$_6$/DA$_1$				DA$_1$ output	PULL register B D-A control register	(15)
P5$_7$/ADT/ DA$_2$				DA$_2$ output A-D trigger input	PULL register B D-A control register A-D control register	(15)

Table 7 List of I/O port function (2)

Pin	Name	Input/Output	I/O Format	Non-Port Function	Related SFRs	Diagram No.
P6$_0$/S$_{IN2}$/AN$_0$	Port P6	Input/ output, individual bits	CMOS compatible input level CMOS 3-state output	A-D conversion input Serial I/O2 function I/O	PULL register B A-D control register Serial I/O2 control register	(17)
P6$_1$/S$_{OUT2}$/ AN$_1$						(18)
P6$_2$/S$_{CLK21}$/ AN$_2$						(19)
P6$_3$/S$_{CLK22}$ / AN$_3$						(20)
P6$_4$/AN$_4$– P6$_7$/AN$_7$				A-D conversion input	A-D control register PULL register B	(16)
P7$_0$/INT$_0$	Port P7	Input	CMOS compatible input level	External interrupt input	Interrupt edge selection register	(23)
P7$_1$–P7$_7$		Input/ output, individual bits	CMOS compatible input level N-channel open-drain output			(13)
COM$_0$–COM$_3$	Common	Output	LCD common output		LCD mode register	(21)
SEG$_0$–SEG$_{17}$	Segment	Output	LCD segment output			(22)

Notes1: How to use double-function ports as function I/O ports, refer to the applicable sections.

2: Make sure that the input level at each pin is either 0 V or V_{CC} during execution of the STP instruction. When an input level is at an intermediate potential, a current will flow V_{CC} to V_{SS} through the input-stage gate.

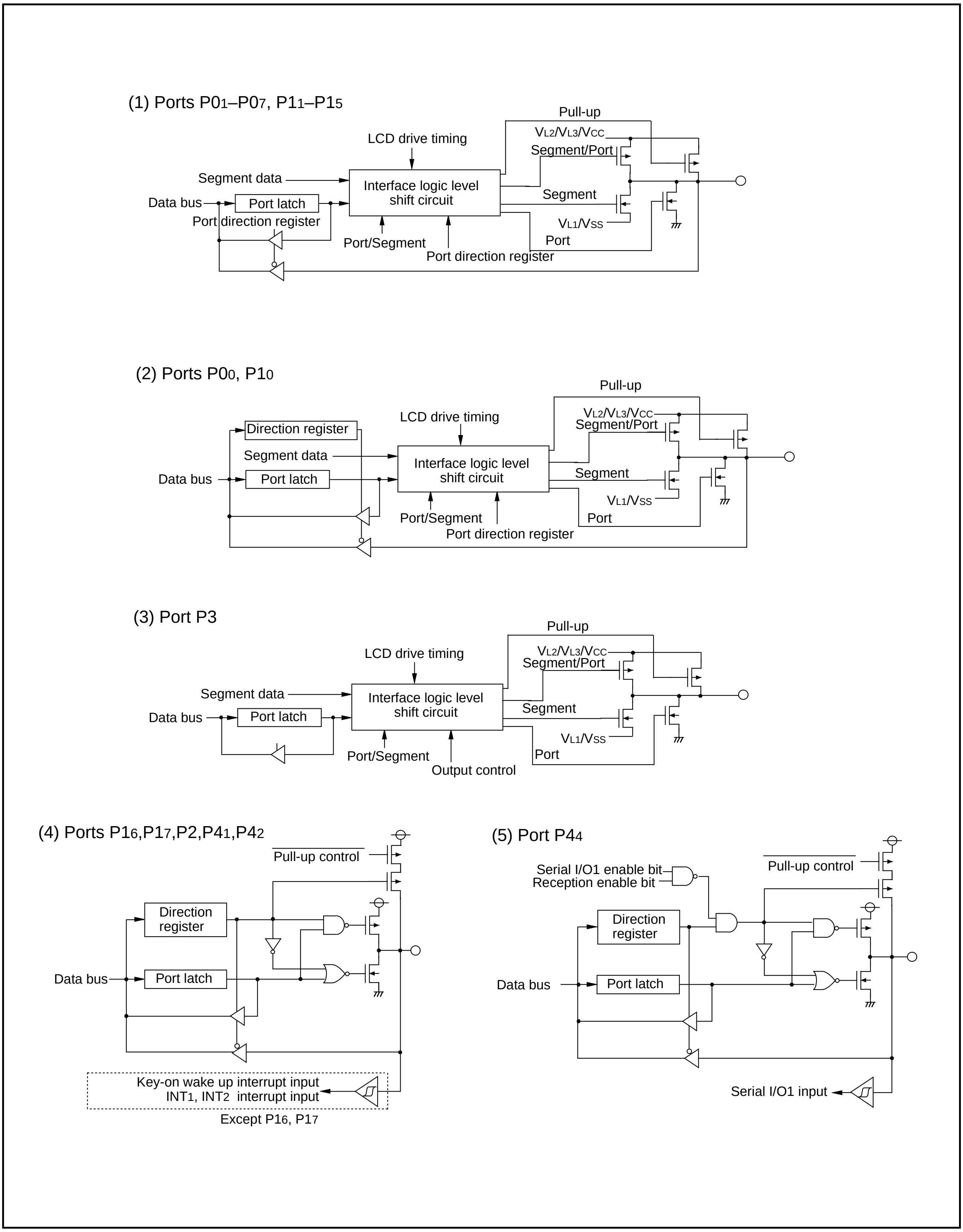


Fig. 12 Port block diagram (1)

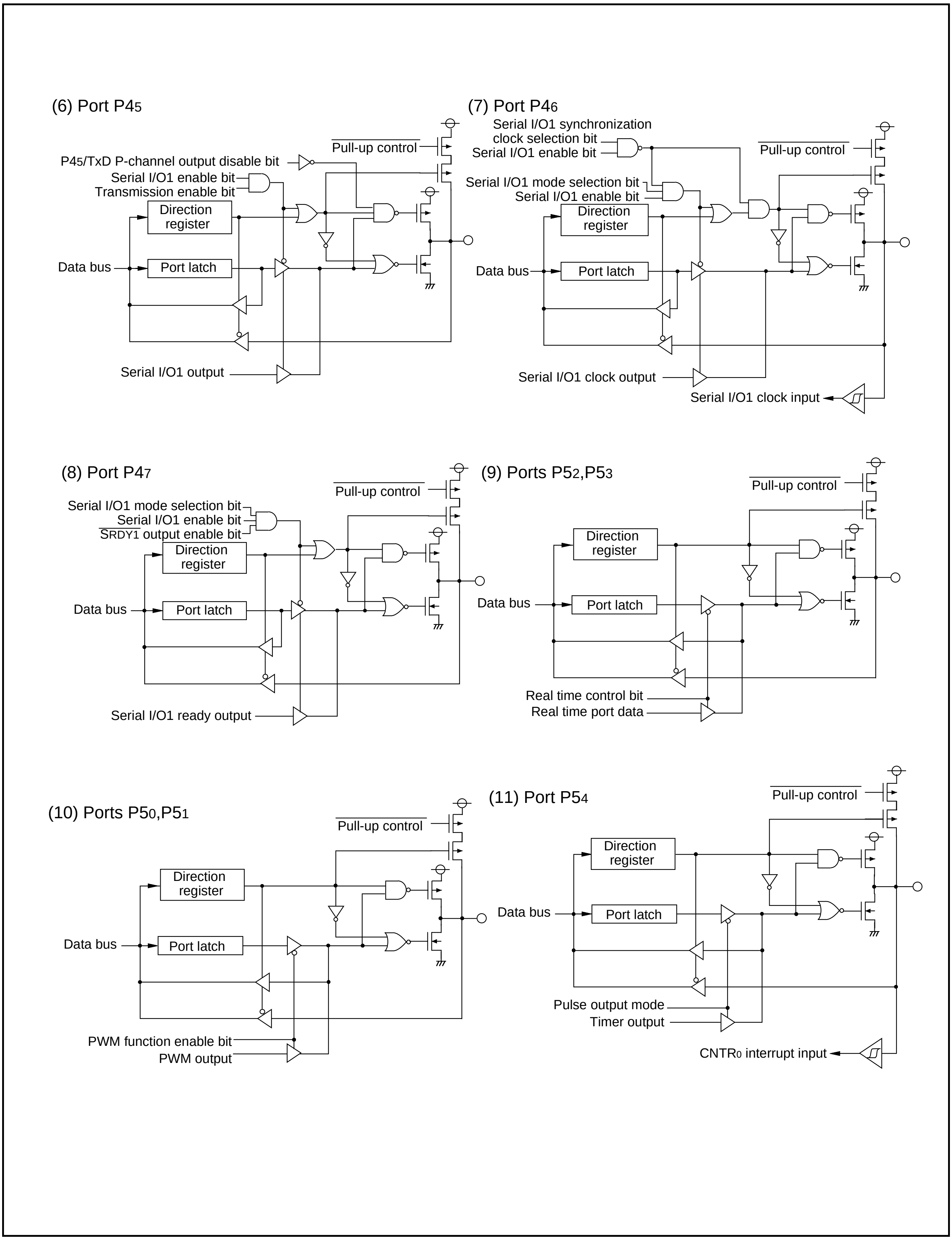


Fig. 13 Port block diagram (2)

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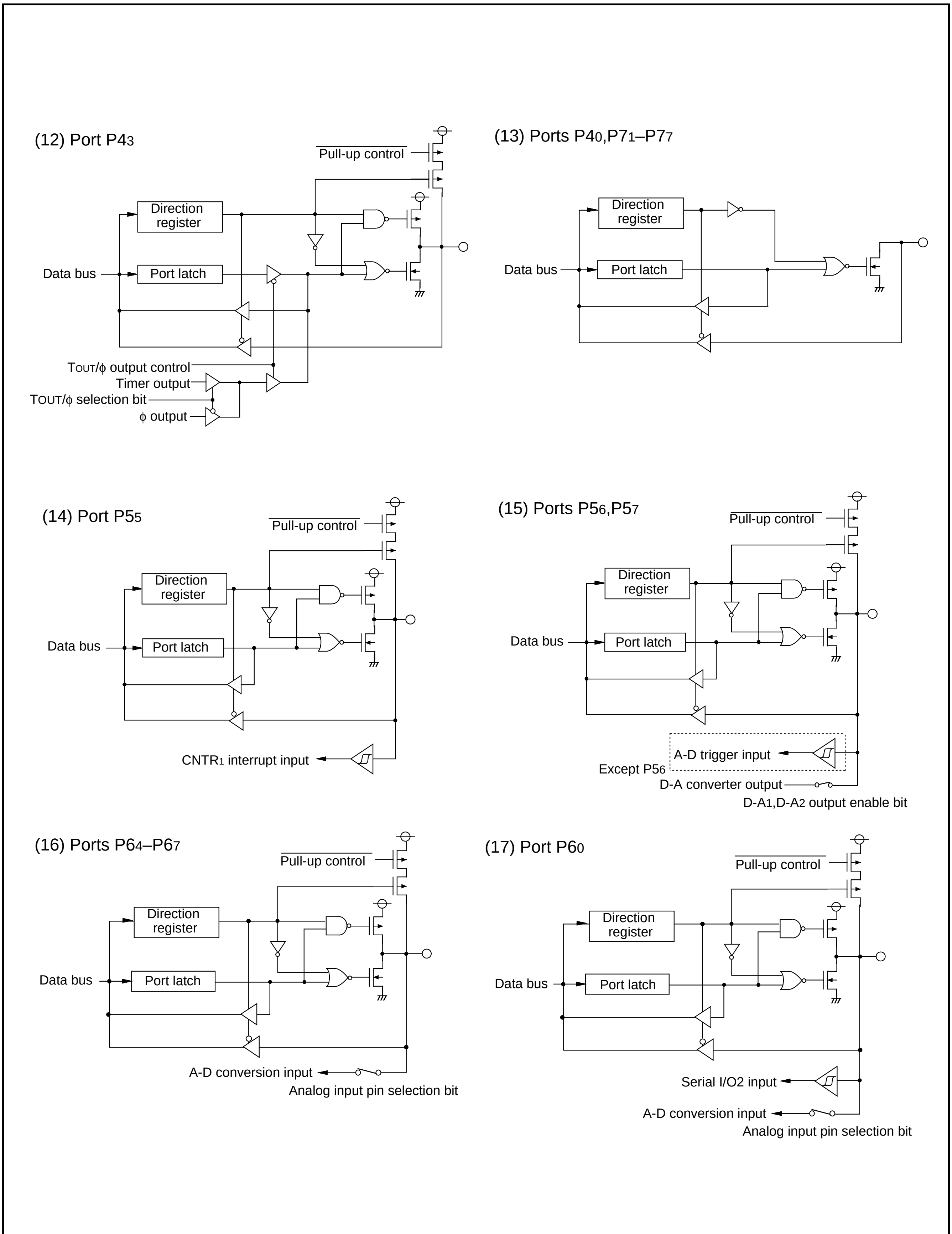


Fig. 14 Port block diagram (3)

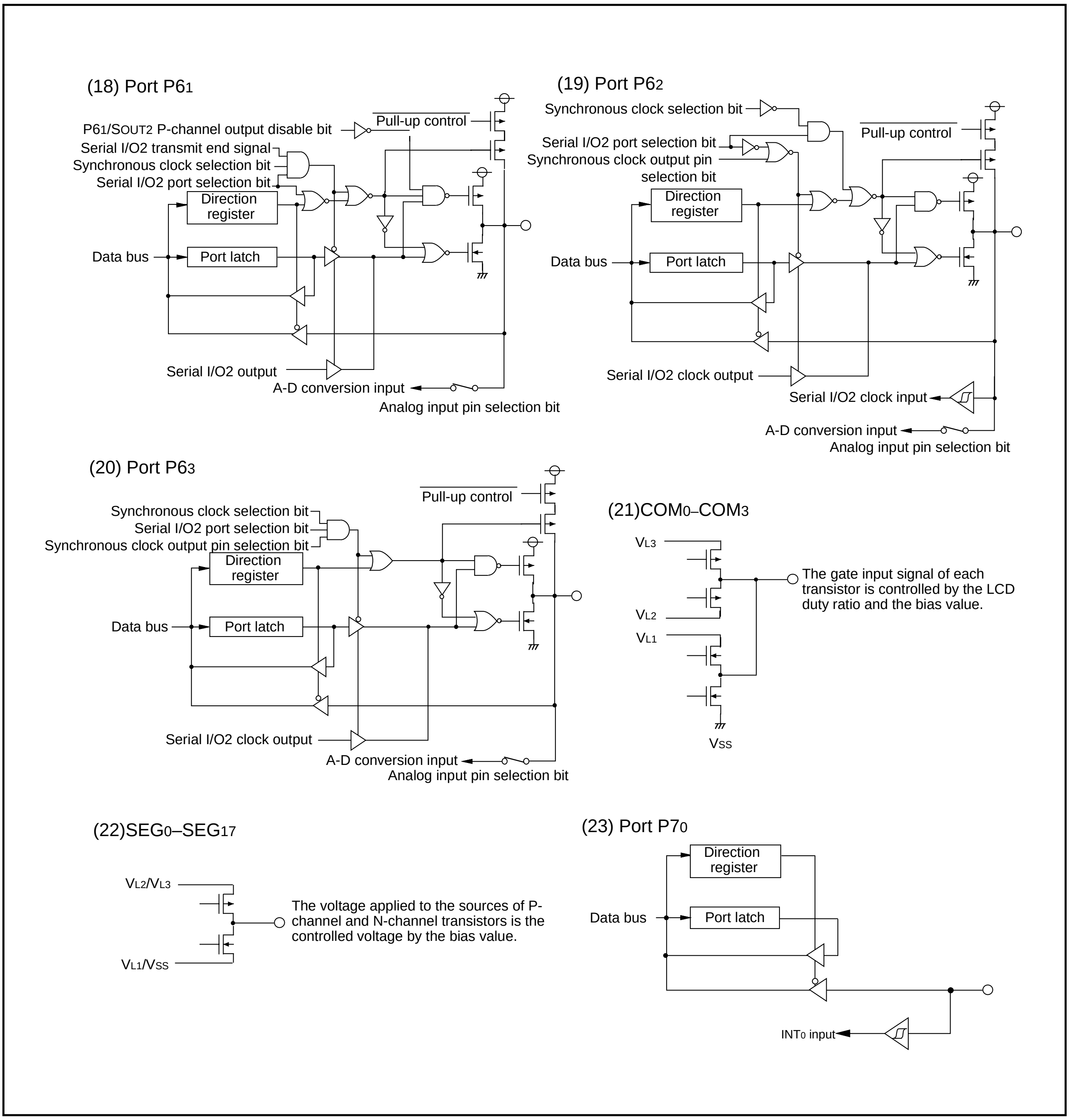


Fig. 15 Port block diagram (4)

INTERRUPTS

Interrupts occur by seventeen sources: seven external, nine internal, and one software.

Interrupt Control

Each interrupt is controlled by an interrupt request bit, an interrupt enable bit, and the interrupt disable flag except for the software interrupt set by the BRK instruction. An interrupt occurs if the corresponding interrupt request and enable bits are “1” and the interrupt disable flag is “0”.
Interrupt enable bits can be set or cleared by software.
Interrupt request bits can be cleared by software, but cannot be set by software.
The BRK instruction cannot be disabled with any flag or bit. The I flag disables all interrupts except the BRK instruction interrupt.
When several interrupts occur at the same time, the interrupts are received according to priority.

Interrupt Operation

By acceptance of an interrupt, the following operations are automatically performed:

1. The contents of the program counter and the processor status register are automatically pushed onto the stack.
2. The interrupt disable flag is set and the corresponding interrupt request bit is cleared.
3. The interrupt jump destination address is read from the vector table into the program counter.

Table 8 Interrupt vector addresses and priority

Interrupt Source	Priority	Vector Addresses **(Note 1)**		Interrupt Request Generating Conditions	Remarks
		High	Low		
Reset **(Note 2)**	1	$FFFD_{16}$	$FFFC_{16}$	At reset	Non-maskable
INT_0	2	$FFFB_{16}$	$FFFA_{16}$	At detection of either rising or falling edge of INT_0 input	External interrupt (active edge selectable)
INT_1	3	$FFF9_{16}$	$FFF8_{16}$	At detection of either rising or falling edge of INT_1 input	External interrupt (active edge selectable)
Serial I/O1 reception	4	$FFF7_{16}$	$FFF6_{16}$	At completion of serial I/O1 data reception	Valid when serial I/O1 is selected
Serial I/O1 transmission	5	$FFF5_{16}$	$FFF4_{16}$	At completion of serial I/O1 transmit shift or when transmission buffer is empty	Valid when serial I/O1 is selected
Timer X	6	$FFF3_{16}$	$FFF2_{16}$	At timer X underflow	
Timer Y	7	$FFF1_{16}$	$FFF0_{16}$	At timer Y underflow	
Timer 2	8	$FFEF_{16}$	$FFEE_{16}$	At timer 2 underflow	
Timer 3	9	$FFED_{16}$	$FFEC_{16}$	At timer 3 underflow	
$CNTR_0$	10	$FFEB_{16}$	$FFEA_{16}$	At detection of either rising or falling edge of $CNTR_0$ input	External interrupt (active edge selectable)
$CNTR_1$	11	$FFE9_{16}$	$FFE8_{16}$	At detection of either rising or falling edge of $CNTR_1$ input	External interrupt (active edge selectable)
Timer 1	12	$FFE7_{16}$	$FFE6_{16}$	At timer 1 underflow	
INT_2	13	$FFE5_{16}$	$FFE4_{16}$	At detection of either rising or falling edge of INT_2 input	External interrupt (active edge selectable)
Serial I/O2	14	$FFE3_{16}$	$FFE2_{16}$	At completion of serial I/O2 data transmission or reception	Valid when serial I/O2 is selected
Key input (Key-on wake-up)	15	$FFE1_{16}$	$FFE0_{16}$	At falling of conjunction of input level for port P2 (at input mode)	External interrupt (valid at falling)
ADT	16	$FFDF_{16}$	$FFDE_{16}$	At falling edge of ADT input	Valid when ADT interrupt is selected External interrupt (valid at falling)
A-D conversion				At completion of A-D conversion	Valid when A-D interrupt is selected
BRK instruction	17	$FFDD_{16}$	$FFDC_{16}$	At BRK instruction execution	Non-maskable software interrupt

Notes1: Vector addresses contain interrupt jump destination addresses.
2: Reset function in the same way as an interrupt with the highest priority.

■Notes on interrupts

When setting the followings, the interrupt request bit may be set to "1".

•When setting external interrupt active edge
Related register: Interrupt edge selection register (address $3A_{16}$)
Timer X mode register (address 27_{16})
Timer Y mode register (address 28_{16})

•When switching interrupt sources of an interrupt vector address where two or more interrupt sources are allocated
Related register: Interrupt source selection bit of A-D control regsiter (bit 6 of address 34_{16})

When not requiring for the interrupt occurrence synchronous with these setting, take the following sequence.

①Set the corresponding interrupt enable bit to "0" (disabled).
②Set the interrupt edge select bit (polarity switch bit) or the interrupt source select bit to "1".
③Set the corresponding interrupt request bit to "0" after 1 or more instructions have been executed.
④Set the corresponding interrupt enable bit to "1" (enabled).

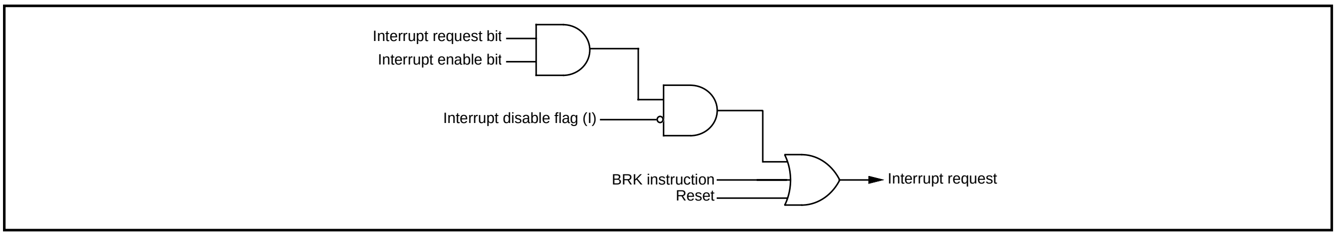


Fig. 16 Interrupt control

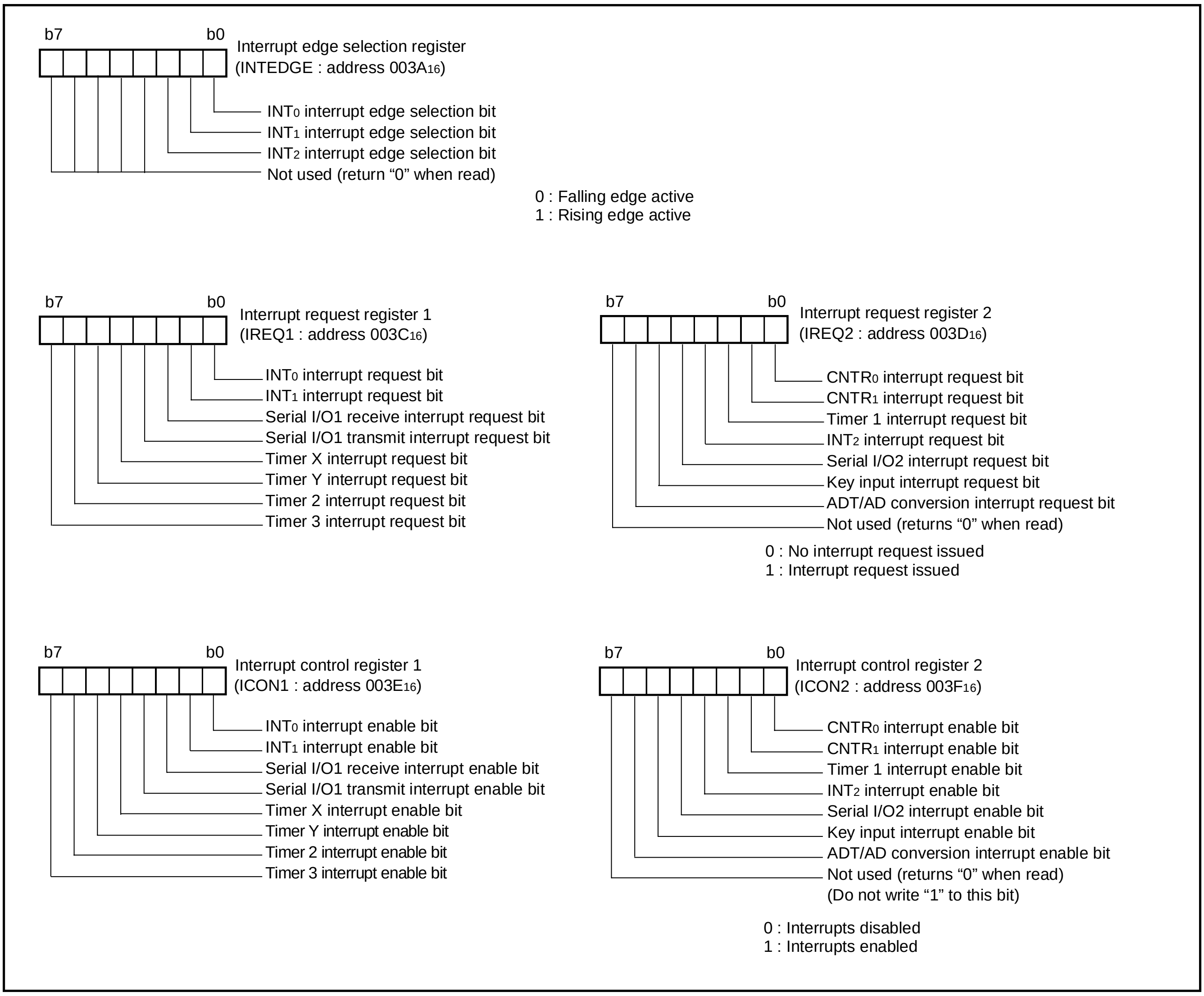


Fig. 17 Structure of interrupt-related registers

Key Input Interrupt (Key-on Wake Up)

A Key-on wake up interrupt request is generated by applying "L" level voltage to any pin of port P2 that have been set to input mode. In other words, it is generated when AND of input level goes from "1" to "0". An example of using a key input interrupt is shown in Figure 18, where an interrupt request is generated by pressing one of the keys consisted as an active-low key matrix which inputs to ports P2$_0$–P2$_3$.

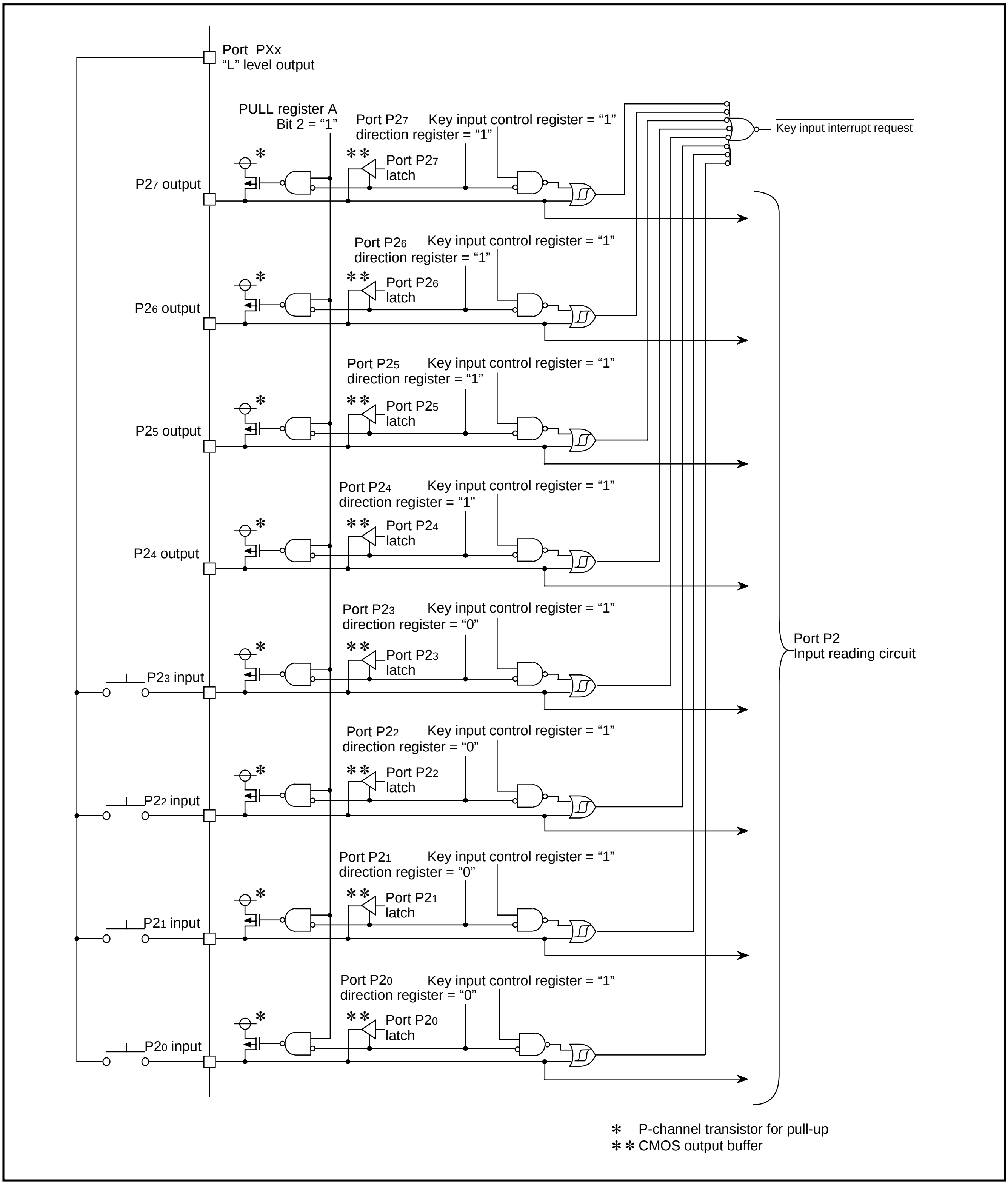


Fig. 18 Connection example when using key input control register, key input interrupt and port P2 block diagram

TIMERS

The 7560 group has five timers: timer X, timer Y, timer 1, timer 2, and timer 3. Timer X and timer Y are 16-bit timers, and timer 1, timer 2, and timer 3 are 8-bit timers.

All timers are down count timers. When the timer reaches "00_{16}", an underflow occurs at the next count pulse and the corresponding timer latch is reloaded into the timer and the count is continued. When a timer underflows, the interrupt request bit corresponding to that timer is set to "1".

Read and write operation on 16-bit timer must be performed for both high- and low-order bytes. When reading a 16-bit timer, read the high-order byte first. When writing to a 16-bit timer, write the low-order byte first. The 16-bit timer cannot perform the correct operation when reading during the write operation, or when writing during the read operation.

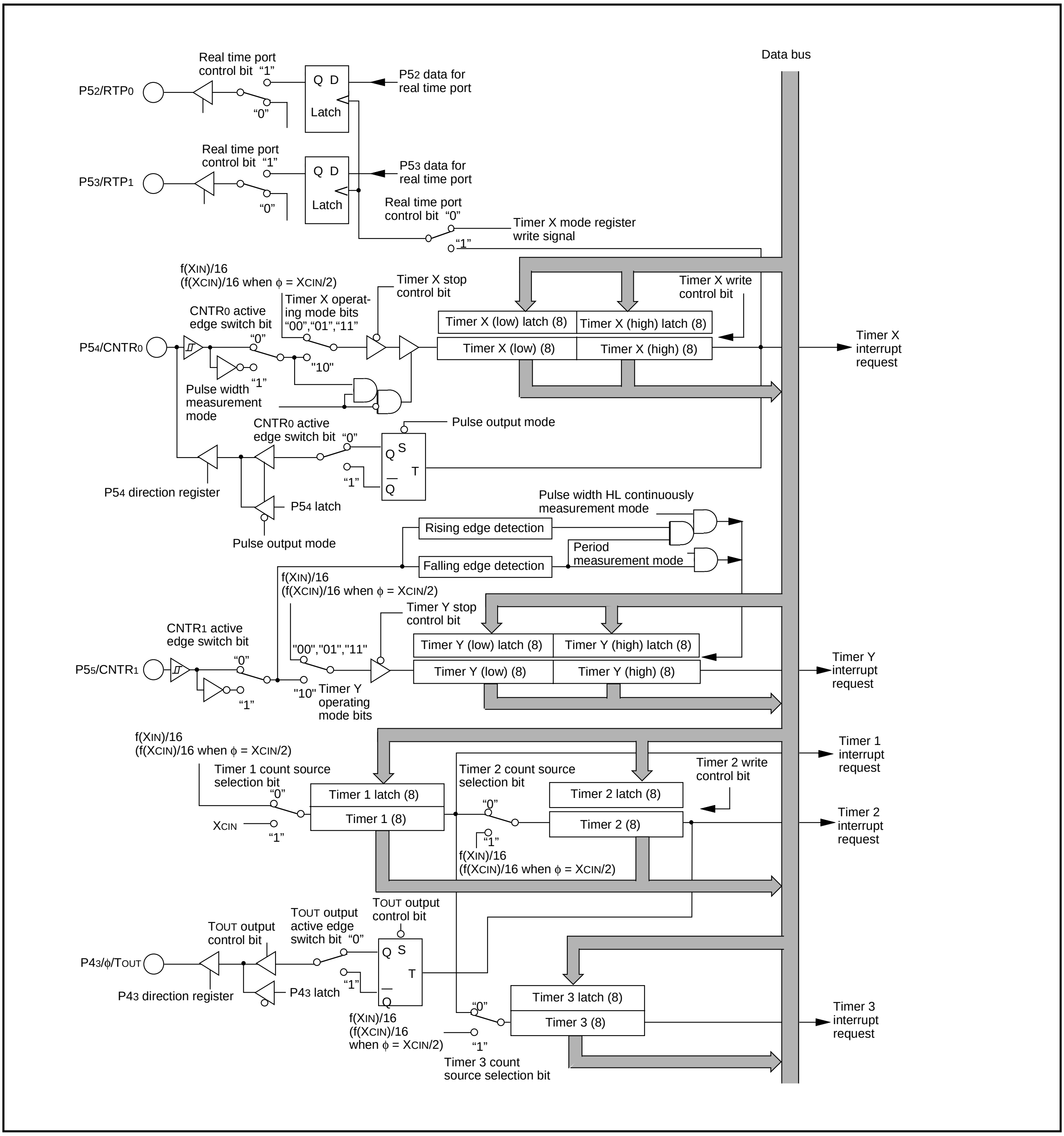


Fig. 19 Timer block diagram

Timer X

Timer X is a 16-bit timer that can be selected in one of four modes and can be controlled the timer X write and the real time port by setting the timer X mode register.

(1) Timer mode

The timer counts $f(X_{IN})/16$ (or $f(X_{CIN})/16$ in low-speed mode).

(2) Pulse output mode

Each time the timer underflows, a signal output from the $CNTR_0$ pin is inverted. Except for this, the operation in pulse output mode is the same as in timer mode. When using a timer in this mode, set the corresponding port $P5_4$ direction register to output mode.

(3) Event counter mode

The timer counts signals input through the $CNTR_0$ pin.
Except for this, the operation in event counter mode is the same as in timer mode. When using a timer in this mode, set the corresponding port $P5_4$ direction register to input mode.

(4) Pulse width measurement mode

The count source is $f(X_{IN})/16$ (or $f(X_{CIN})/16$ in low-speed mode). If $CNTR_0$ active edge switch bit is “0”, the timer counts while the input signal of $CNTR_0$ pin is at “H”. If it is “1”, the timer counts while the input signal of $CNTR_0$ pin is at “L”. When using a timer in this mode, set the corresponding port $P5_4$ direction register to input mode.

●Timer X Write Control

If the timer X write control bit is “0”, when the value is written in the address of timer X, the value is loaded in the timer X and the latch at the same time.
If the timer X write control bit is “1”, when the value is written in the address of timer X, the value is loaded only in the latch. The value in the latch is loaded in timer X after timer X underflows.
If the value is written in latch only, unexpected value may be set in the high-order counter when the writing in high-order latch and the underflow of timer X are performed at the same timing.

●Real Time Port Control

While the real time port function is valid, data for the real time port are output from ports $P5_2$ and $P5_3$ each time the timer X underflows. (However, if the real time port control bit is changed from “0” to “1” after set of the real time port data, data are output independent of the timer X operation.) If the data for the real time port is changed while the real time port function is valid, the changed data are output at the next underflow of timer X.
Before using this function, set the corresponding port direction registers to output mode.

■Note on $CNTR_0$ interrupt active edge selection

$CNTR_0$ interrupt active edge depends on the $CNTR_0$ active edge switch bit.

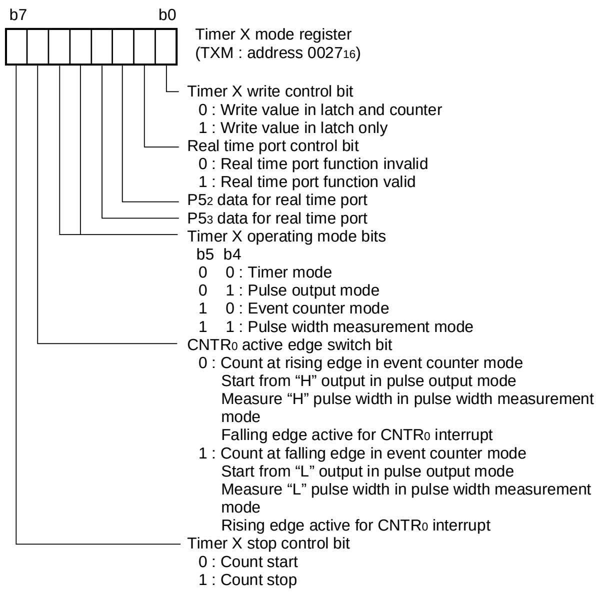


Fig. 20 Structure of timer X mode register

Timer Y

Timer Y is a 16-bit timer that can be selected in one of four modes.

(1) Timer mode

The timer counts $f(X_{IN})/16$ (or $f(X_{CIN})/16$ in low-speed mode).

(2) Period measurement mode

$CNTR_1$ interrupt request is generated at rising/falling edge of $CNTR_1$ pin input signal. Simultaneously, the value in timer Y latch is reloaded in timer Y and timer Y continues counting down. Except for the above-mentioned, the operation in period measurement mode is the same as in timer mode.
The timer value just before the reloading at rising/falling of $CNTR_1$ pin input signal is retained until the timer Y is read once after the reload.
The rising/falling timing of $CNTR_1$ pin input signal is found by $CNTR_1$ interrupt. When using a timer in this mode, set the corresponding port $P5_5$ direction register to input mode.

(3) Event counter mode

The timer counts signals input through the $CNTR_1$ pin.
Except for this, the operation in event counter mode is the same as in timer mode. When using a timer in this mode, set the corresponding port $P5_5$ direction register to input mode.

(4) Pulse width HL continuously measurement mode

$CNTR_1$ interrupt request is generated at both rising and falling edges of $CNTR_1$ pin input signal. Except for this, the operation in pulse width HL continuously measurement mode is the same as in period measurement mode. When using a timer in this mode, set the corresponding port $P5_5$ direction register to input mode.

■Note on $CNTR_1$ interrupt active edge selection

$CNTR_1$ interrupt active edge depends on the $CNTR_1$ active edge switch bit. However, in pulse width HL continuously measurement mode, $CNTR_1$ interrupt request is generated at both rising and falling edges of $CNTR_1$ pin input signal regardless of the setting of $CNTR_1$ active edge switch bit.

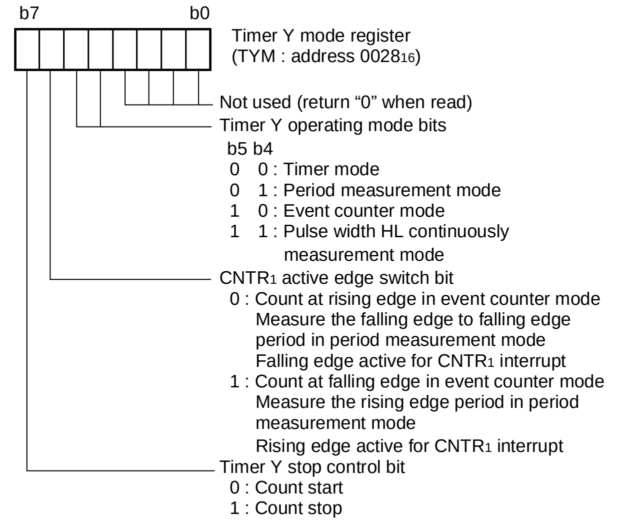


Fig. 21 Structure of timer Y mode register

Timer 1, Timer 2, Timer 3

Timer 1, timer 2, and timer 3 are 8-bit timers. The count source for each timer can be selected by timer 123 mode register. The timer latch value is not affected by a change of the count source. However, because changing the count source may cause an inadvertent count down of the timer. Therefore, rewrite the value of timer whenever the count source is changed.

●Timer 2 Write Control

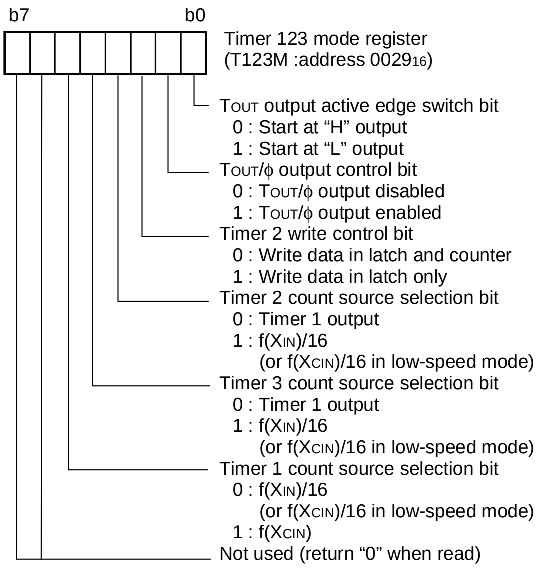
If the timer 2 write control bit is "0", when the value is written in the address of timer 2, the value is loaded in the timer 2 and the latch at the same time.
If the timer 2 write control bit is "1", when the value is written in the address of timer 2, the value is loaded only in the latch. The value in the latch is loaded in timer 2 after timer 2 underflows.

●Timer 2 Output Control

When the timer 2 (T_{OUT}) is output enabled, an inversion signal from pin T_{OUT} is output each time timer 2 underflows.
In this case, set the port $P5_6$ shared with the port T_{OUT} to the output mode.

■Note on Timer 1 to Timer 3

When the count source of timers 1 to 3 is changed, the timer counting value may be changed large because a thin pulse is generated in count input of timer. If timer 1 output is selected as the count source of timer 2 or timer 3, when timer 1 is written, the counting value of timer 2 or timer 3 may be changed large because a thin pulse is generated in timer 1 output.
Therefore, set the value of timer in the order of timer 1, timer 2 and timer 3 after the count source selection of timer 1 to 3.



Note: Internal clock ϕ is f(X_{CIN})/2 in the low-speed mode.

Fig. 22 Structure of timer 123 mode register

SERIAL I/O

Serial I/O1

Serial I/O1 can be used as either clock synchronous or asynchronous (UART) serial I/O. A dedicated timer (baud rate generator) is also provided for baud rate generation.

(1) Clock Synchronous Serial I/O Mode

Clock synchronous serial I/O mode can be selected by setting the mode selection bit of the serial I/O1 control register to “1”.

For clock synchronous serial I/O1, the transmitter and the receiver must use the same clock. If an internal clock is used, transfer is started by a write signal to the TB/RB (address 0018_{16}).

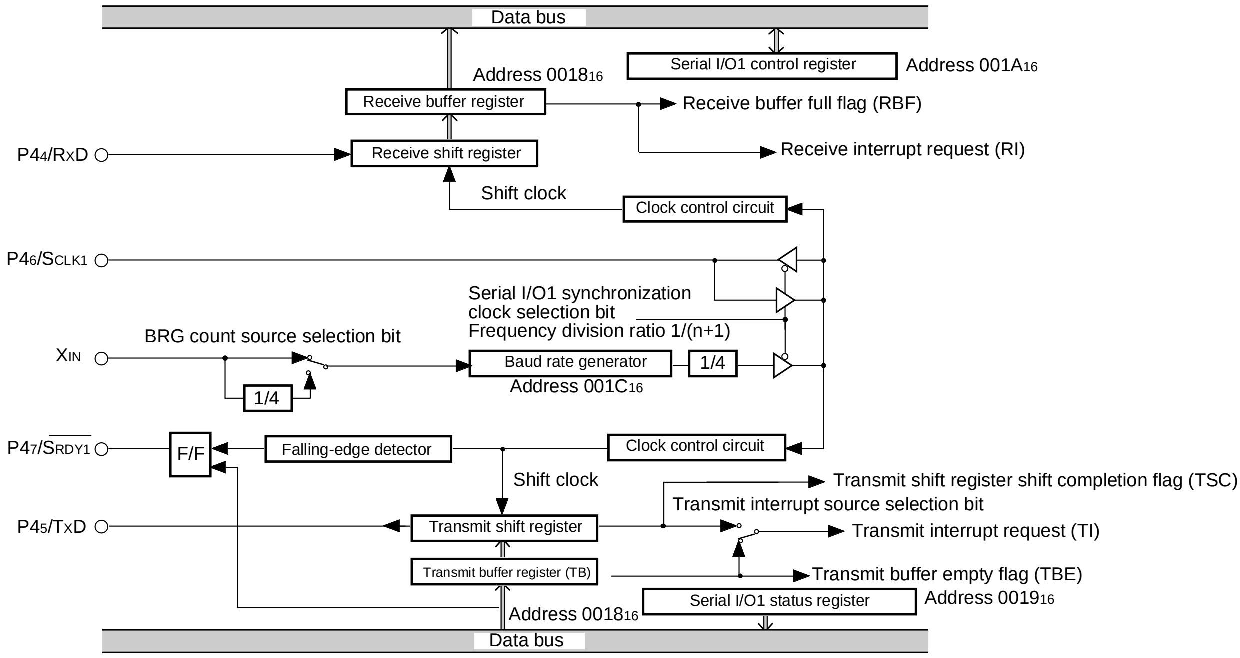
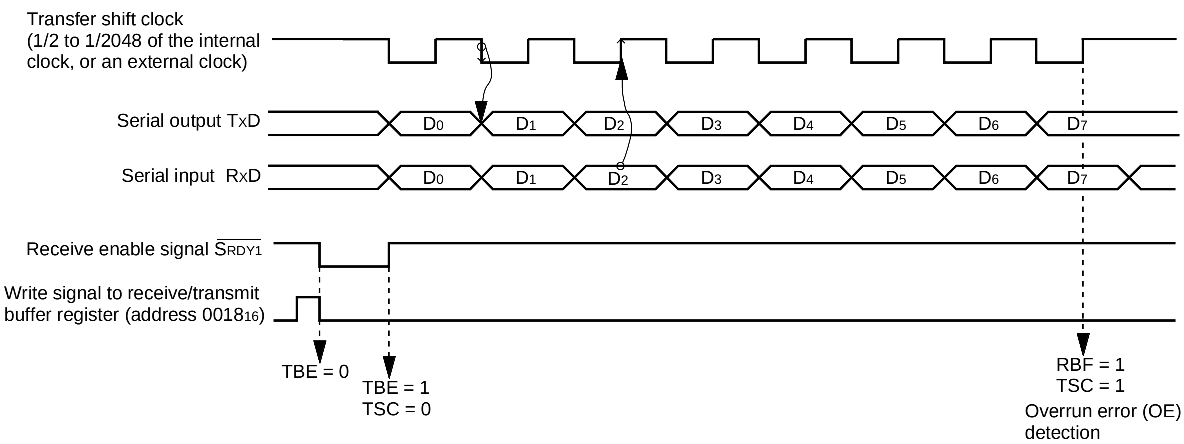


Fig. 23 Block diagram of clock synchronous serial I/O1



Notes
1 : The transmit interrupt (TI) can be generated either when the transmit buffer register has emptied (TBE = 1) or after the transmit shift operation has ended (TSC=1), by setting the transmit interrupt source selection bit (TIC) of the serial I/O1 control register.
2 : If data is written to the transmit buffer register when TSC=0, the transmit clock is generated continuously and serial data is output continuously from the TxD pin.
3 : The receive interrupt (RI) is set when the receive buffer full flag (RBF) becomes “1” .

Fig. 24 Operation of clock synchronous serial I/O1 function

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(2) Asynchronous Serial I/O (UART) Mode

Clock asynchronous serial I/O mode (UART) can be selected by clearing the serial I/O mode selection bit of the serial I/O1 control register to "0".
Eight serial data transfer formats can be selected, and the transfer formats used by a transmitter and receiver must be identical.
The transmit and receive shift registers each have a buffer register, but the two buffers have the same address in memory. Since the shift register cannot be written to or read from directly, transmit data is written to the transmit buffer, and receive data is read from the receive buffer.
The transmit buffer can also hold the next data to be transmitted, and the receive buffer register can hold a character while the next character is being received.

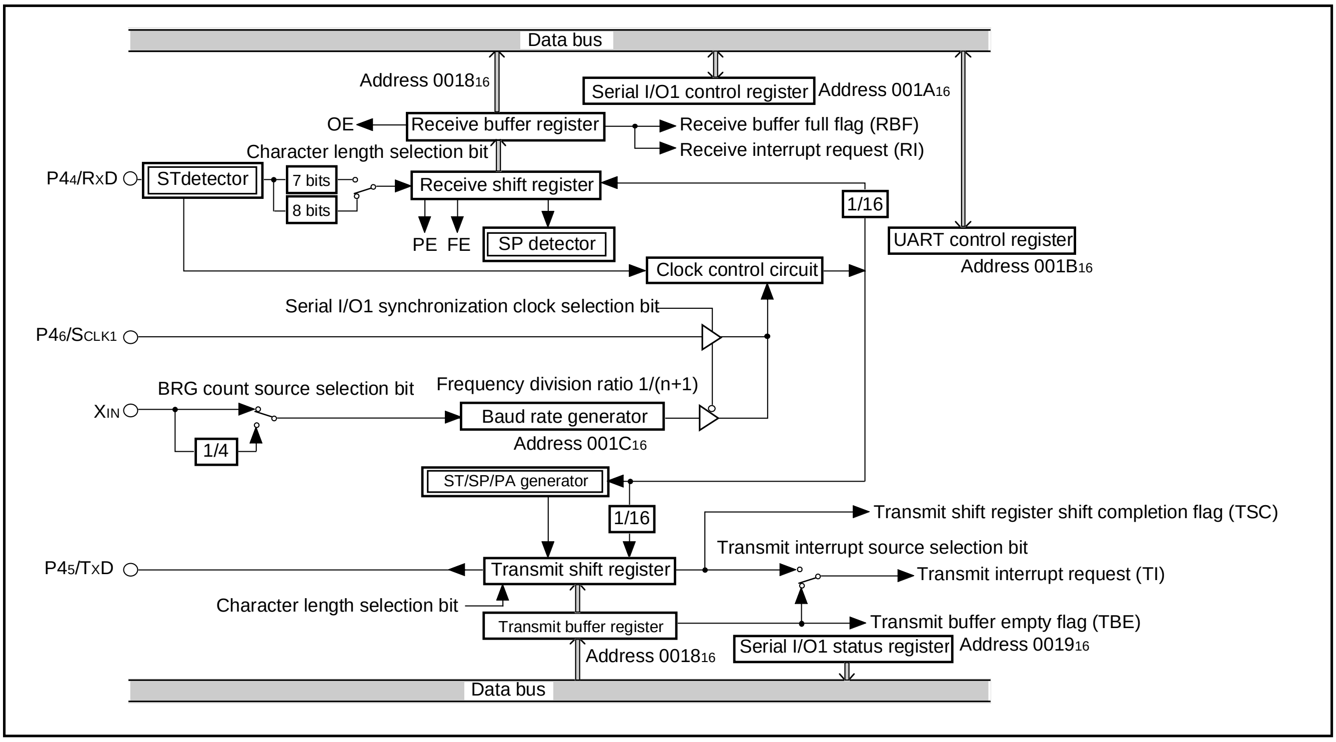
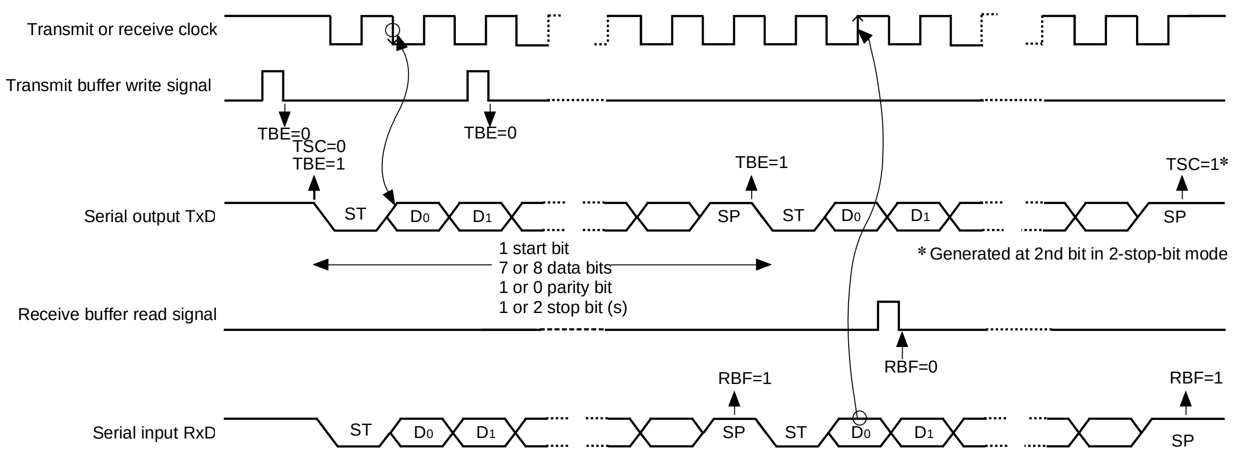


Fig. 25 Block diagram of UART serial I/O1



Notes
1 : Error flag detection occurs at the same time that the RBF flag becomes "1" (at 1st stop bit, during reception).
2 : The transmit interrupt (TI) can be generated to occur when either the TBE or TSC flag becomes "1", depending on the setting of the transmit interrupt source selection bit (TIC) of the serial I/O1 control register.
3 : The receive interrupt (RI) is set when the RBF flag becomes "1".

Fig. 26 Operation of UART serial I/O1 function

[Transmit Buffer/Receive Buffer Register (TB/RB)] 0018_{16}

The transmit buffer register and the receive buffer register are located at the same address. The transmit buffer register is write-only and the receive buffer register is read-only. If a character bit length is 7 bits, the MSB of data stored in the receive buffer register is “0”.

[Serial I/O1 Status Register (SIO1STS)] 0019_{16}

The read-only serial I/O1 status register consists of seven flags (bits 0 to 6) which indicate the operating status of the serial I/O1 function and various errors.
Three of the flags (bits 4 to 6) are valid only in UART mode.
The receive buffer full flag (bit 1) is cleared to “0” when the receive buffer is read.
If there is an error, it is detected at the same time that data is transferred from the receive shift register to the receive buffer register, and the receive buffer full flag is set. A write to the serial I/O1 status register clears all the error flags OE, PE, FE, and SE (bit 3 to bit 6, respectively). Writing “0” to the serial I/O1 enable bit SIOE (bit 7 of the Serial I/O1 Control Register) also clears all the status flags, including the error flags.
All bits of the serial I/O1 status register are initialized to “0” at reset, but if the transmit enable bit (bit 4) of the serial I/O1 control register has been set to “1”, the transmit shift register shift completion flag (bit 2) and the transmit buffer empty flag (bit 0) become “1”.

[Serial I/O1 Control Register (SIO1CON)] $001A_{16}$

The serial I/O1 control register contains eight control bits for the serial I/O1 function.

[UART Control Register (UARTCON)] $001B_{16}$

The UART control register consists of four control bits (bits 0 to 3) which are valid when asynchronous serial I/O is selected and set the data format of an data transfer. One bit in this register (bit 4) is always valid and sets the output structure of the $P4_5/T_XD$ pin.

[Baud Rate Generator (BRG)] $001C_{16}$

The baud rate generator determines the baud rate for serial transfer.
The baud rate generator divides the frequency of the count source by 1/(n + 1), where n is the value written to the baud rate generator.

■Notes on serial I/O

When setting the transmit enable bit to “1”, the serial I/O1 transmit interrupt request bit is automatically set to “1”. When not requiring the interrupt occurrence synchronous with the transmission enalbed, take the following sequence.
①Set the serial I/O1 transmit interrupt enable bit to “0” (disabled).
②Set the transmit enable bit to “1”.
③Set the serial I/O1 transmit interrupt request bit to “0” after 1 or more instructions have been executed.
④Set the serial I/O1 transmit interrupt enable bit to “1” (enabled).

Serial I/O1 status register (SIO1STS : address 0019_{16}) (b7 … b0)

- b0: Transmit buffer empty flag (TBE)
  0: Buffer full
  1: Buffer empty
- b1: Receive buffer full flag (RBF)
  0: Buffer empty
  1: Buffer full
- b2: Transmit shift register shift completion flag (TSC)
  0: Transmit shift in progress
  1: Transmit shift completed
- b3: Overrun error flag (OE)
  0: No error
  1: Overrun error
- b4: Parity error flag (PE)
  0: No error
  1: Parity error
- b5: Framing error flag (FE)
  0: No error
  1: Framing error
- b6: Summing error flag (SE)
  0: (OE) U (PE) U (FE) =0
  1: (OE) U (PE) U (FE) =1
- b7: Not used (returns “1” when read)

UART control register (UARTCON : address $001B_{16}$) (b7 … b0)

- b0: Character length selection bit (CHAS)
  0: 8 bits
  1: 7 bits
- b1: Parity enable bit (PARE)
  0: Parity checking disabled
  1: Parity checking enabled
- b2: Parity selection bit (PARS)
  0: Even parity
  1: Odd parity
- b3: Stop bit length selection bit (STPS)
  0: 1 stop bit
  1: 2 stop bits
- b4: $P4_5/T_XD$ P-channel output disable bit (POFF)
  0: CMOS output (in output mode)
  1: N-channel open-drain output (in output mode)
- b5–b7: Not used (return “1” when read)

Serial I/O1 control register (SIO1CON : address $001A_{16}$) (b7 … b0)

- b0: BRG count source selection bit (CSS)
  0: $f(X_{IN})$
  1: $f(X_{IN})/4$
- b1: Serial I/O1 synchronization clock selection bit (SCS)
  0: BRG output divided by 4 when clock synchronous serial I/O is selected.
  BRG output divided by 16 when UART is selected.
  1: External clock input when clock synchronous serial I/O is selected.
  External clock input divided by 16 when UART is selected.
- b2: $\overline{S_{RDY1}}$ output enable bit (SRDY)
  0: $P4_7$ pin operates as ordinary I/O pin
  1: $P4_7$ pin operates as $\overline{S_{RDY1}}$ output pin
- b3: Transmit interrupt source selection bit (TIC)
  0: Interrupt when transmit buffer has emptied
  1: Interrupt when transmit shift operation is completed
- b4: Transmit enable bit (TE)
  0: Transmit disabled
  1: Transmit enabled
- b5: Receive enable bit (RE)
  0: Receive disabled
  1: Receive enabled
- b6: Serial I/O1 mode selection bit (SIOM)
  0: Asynchronous serial I/O (UART)
  1: Clock synchronous serial I/O
- b7: Serial I/O1 enable bit (SIOE)
  0: Serial I/O1 disabled
  (pins $P4_4$–$P4_7$ operate as ordinary I/O pins)
  1: Serial I/O1 enabled
  (pins $P4_4$–$P4_7$ operate as serial I/O pins)

Fig. 27 Structure of serial I/O1 control registers

Serial I/O2

The serial I/O2 function can be used only for clock synchronous serial I/O.
For clock synchronous serial I/O2, the transmitter and the receiver must use the same clock. When the internal clock is used, transfer is started by a write signal to the serial I/O2 register.
When an internal clock is selected as the synchronous clock of the serial I/O2, either P62 or P63 can be selected as an output pin of the synchronous clock. In this case, the pin that is not selected as an output pin of the synchronous clock functions as a port.

[Serial I/O2 Control Register (SIO2CON)] 001D16

The serial I/O2 control register contains 8 bits which control various serial I/O2 functions.

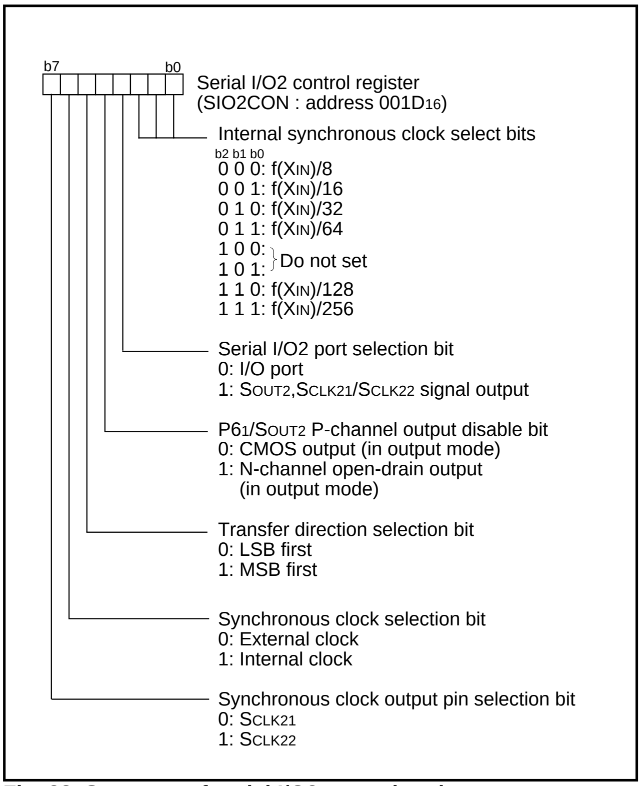


Fig. 28 Structure of serial I/O2 control register

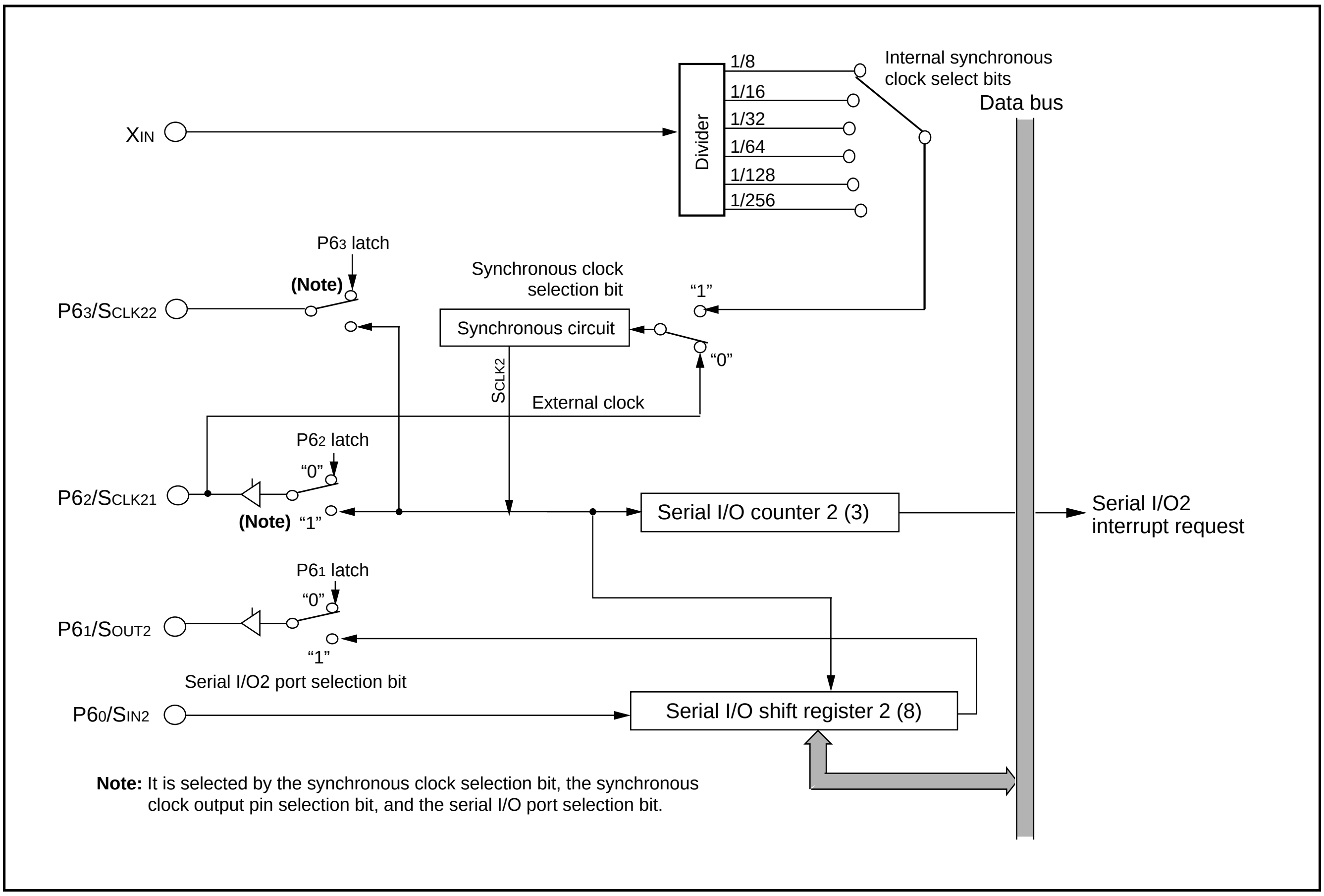
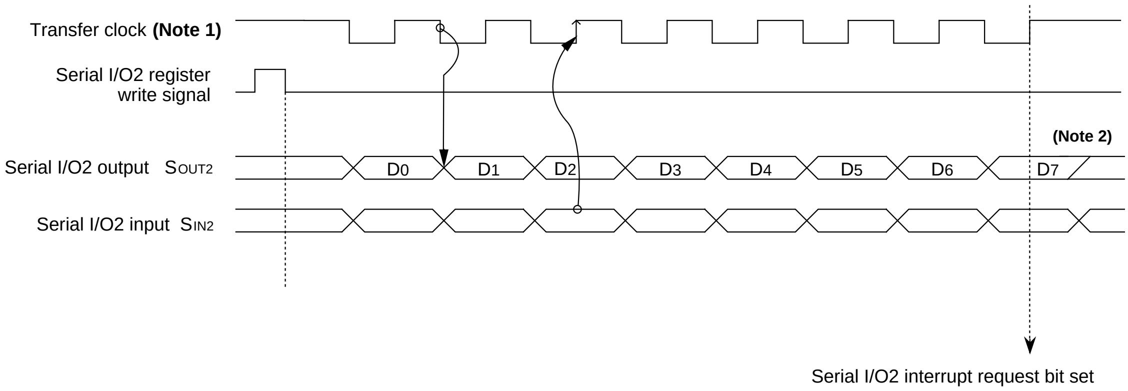


Fig. 29 Block diagram of serial I/O2 function



Notes 1: When the internal clock is selected as the transfer clock, the divide ratio can be selected by setting bits 0 to 2 of the serial I/O2 control register.
2: When the internal clock is selected as the transfer clock, the SOUT2 pin goes to high impedance after transfer completion. When the external clock is selected as the transfer clock, a content of the serial I/O shift register is continued to shift during inputting a transfer clock. The SOUT2 pin does not go to high impedance after transfer completion.

Fig. 30 Timing of serial I/O2 function

PULSE WIDTH MODULATION (PWM)

The 7560 group has a PWM function with an 8-bit resolution, based on a signal that is the clock input X_{IN} or that clock input divided by 2.

Data Setting

The PWM output pin also functions as ports $P5_0$ and $P5_1$. Set the PWM period by the PWM prescaler, and set the period during which the output pulse is an "H" by the PWM register.

If PWM count source is $f(X_{IN})$ and the value in the PWM prescaler is n and the value in the PWM register is m (where n = 0 to 255 and m = 0 to 255) :

PWM period = $255 \times (n+1)/f(X_{IN})$
= $31.875 \times (n+1)$ µs (when $f(X_{IN})$ = 8 MHz)

Output pulse "H" period = PWM period $\times$ m/255
= $0.125 \times (n+1) \times m$ µs
(when $f(X_{IN})$ = 8 MHz)

PWM Operation

When at least either bit 1 (PWM_0 function enable bit) or bit 2 (PWM_1 function enable bit) of the PWM control register is set to "1", operation starts by initializing the PWM output circuit, and pulses are output starting at an "H". When one PWM output is enabled and that the other PWM output is enabled, PWM output which is enabled to output later starts pulse output from halfway.

When the PWM register or PWM prescaler is updated during PWM output, the pulses will change in the cycle after the one in which the change was made.

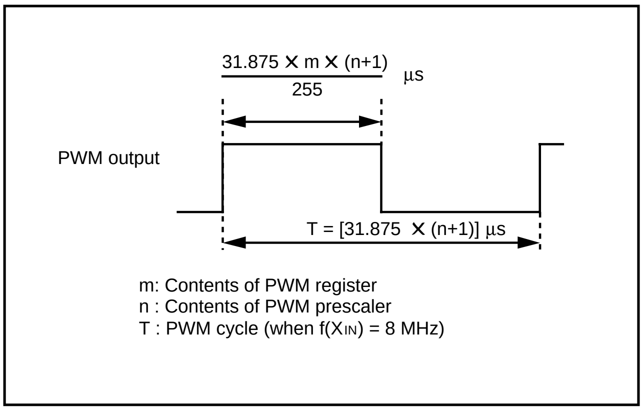


Fig. 31 Timing of PWM cycle

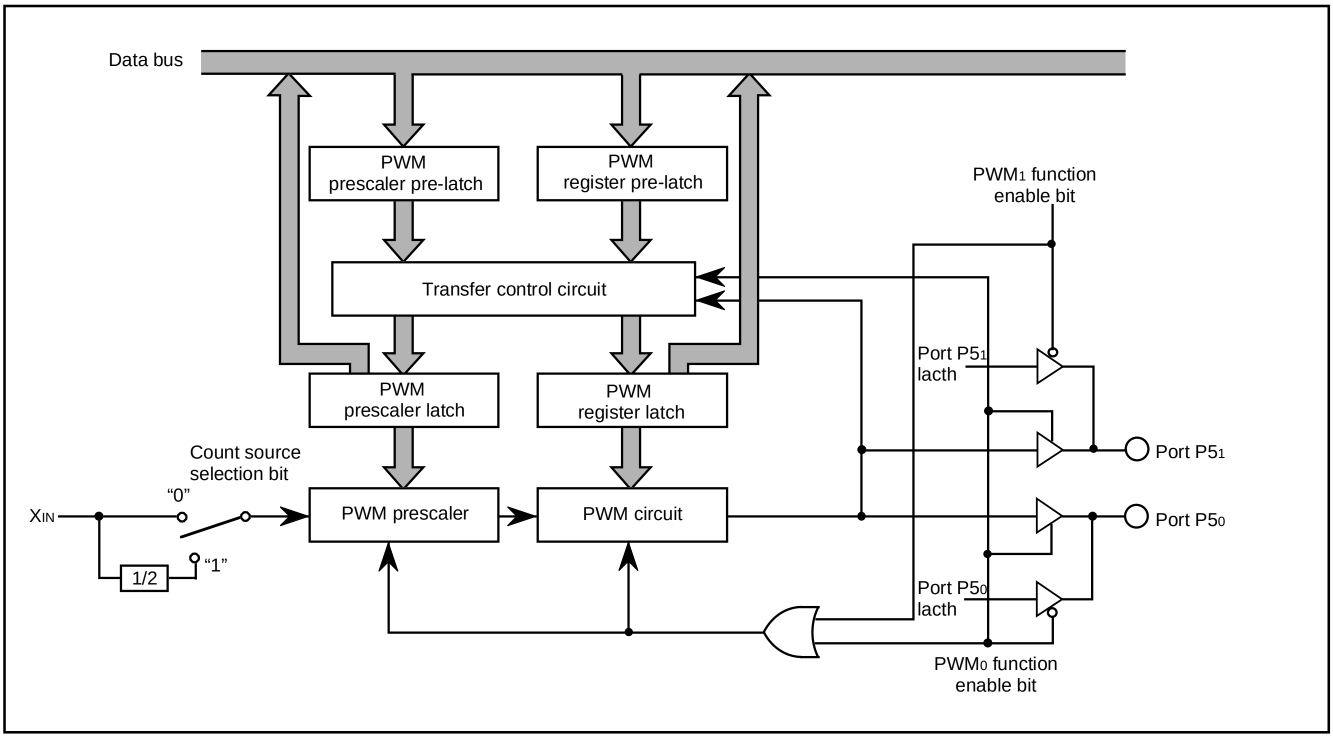


Fig. 32 Block diagram of PWM function

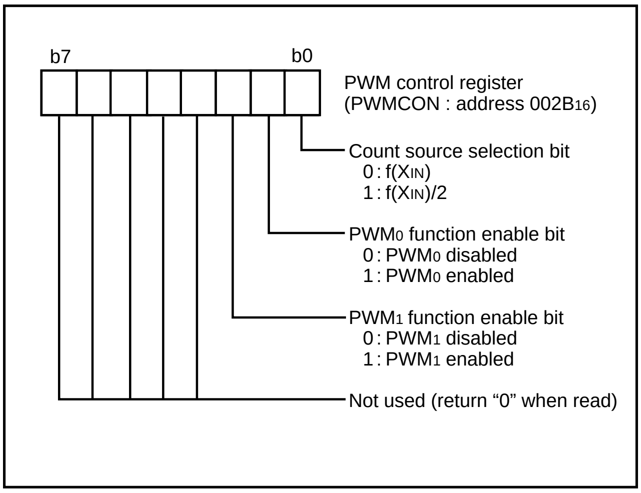


Fig. 33 Structure of PWM control register

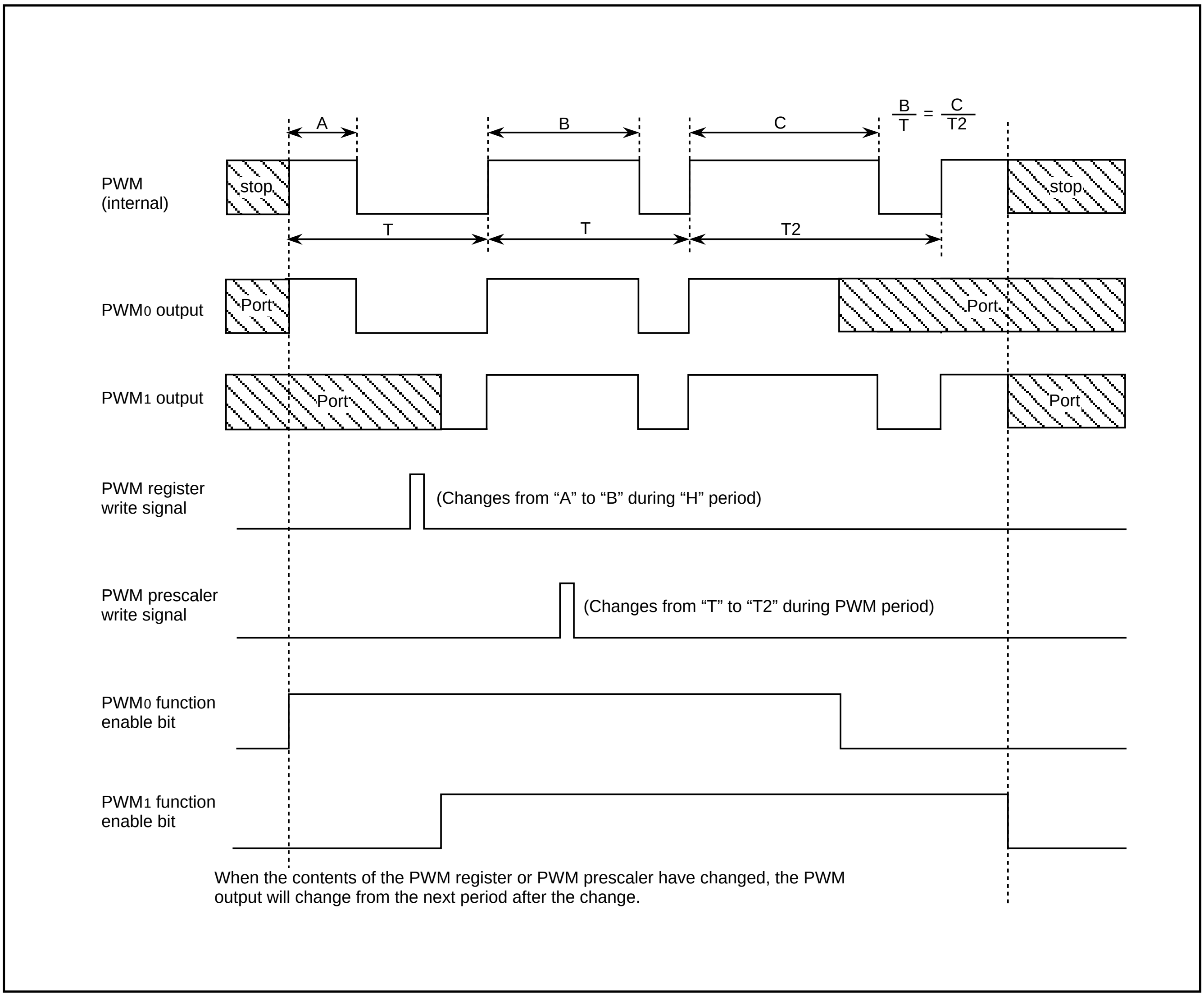


Fig. 34 PWM output timing when PWM register or PWM prescaler is changed

A-D CONVERTER

The functional blocks of the A-D converter are described below.

[A-D Conversion Register (AD)] 0035_{16}

The A-D conversion register is a read-only register that contains the result of an A-D conversion. When reading this register during an A-D conversion, the previous conversion result is read.

[A-D Control Register (ADCON)] 0034_{16}

The A-D control register controls the A-D conversion process. Bits 0 to 2 of this register select specific analog input pins. Bit 3 signals the completion of an A-D conversion. The value of this bit remains at “0” during an A-D conversion, then changes to “1” when the A-D conversion is completed. Writing “0” to this bit starts the A-D conversion. Bit 4 controls the transistor which breaks the through current of the resistor ladder. When bit 5, which is the AD external trigger valid bit, is set to “1”, this bit enables A-D conversion even by a falling edge of an ADT input. Set ports which share with ADT pins to input when using an A-D external trigger.

Comparison Voltage Generator

The comparison voltage generator divides the voltage between AV_{SS} and V_{REF} by 256, and outputs the divided voltages.

Channel Selector

The channel selector selects one of the input ports $P6_7/AN_7$–$P6_0/AN_0$.

Comparator and Control Circuit

The comparator and control circuit compare an analog input voltage with the comparison voltage and store the result in the A-D conversion register. When an A-D conversion is completed, the control circuit sets the AD conversion completion bit and the AD interrupt request bit to “1”.

Note that the comparator is constructed linked to a capacitor, so set $f(X_{IN})$ to at least 500kHz during A-D conversion.

Use the clock divided from the main clock X_{IN} as the internal clock ϕ.

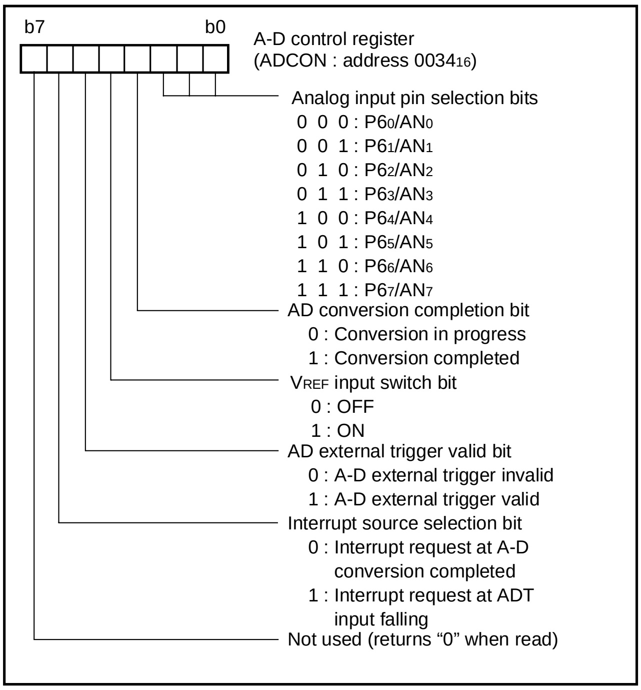


Fig. 35 Structure of A-D control register

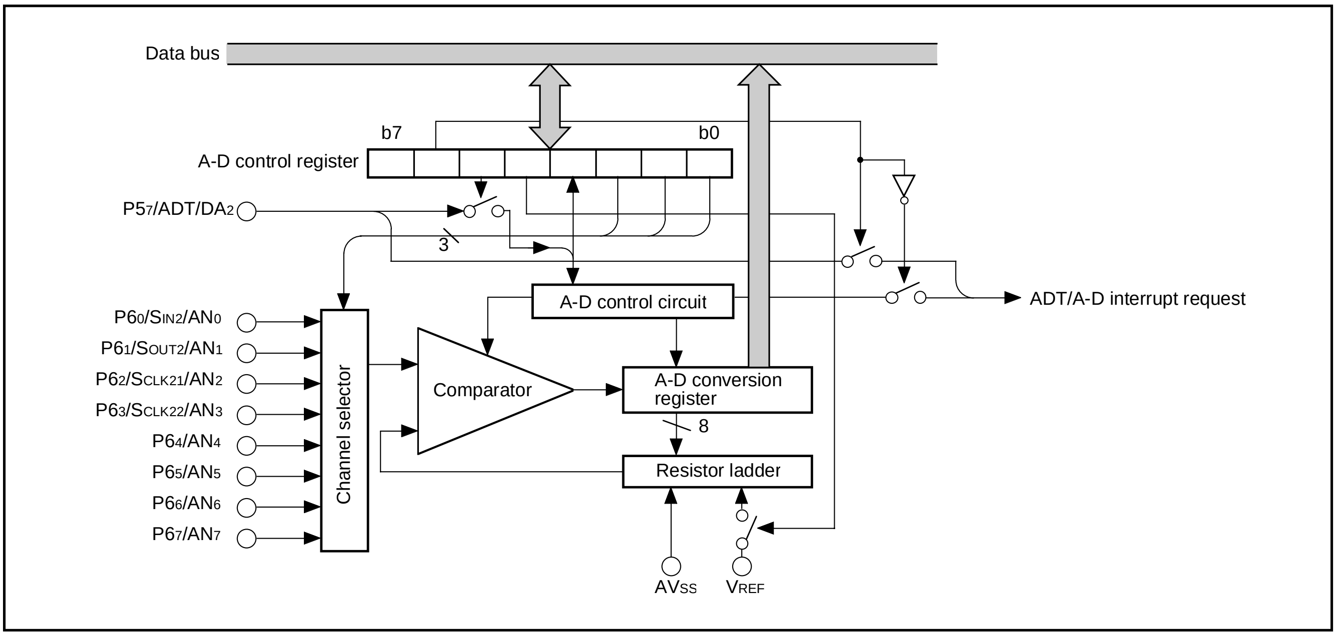


Fig. 36 A-D converter block diagram

D-A Converter

The 7560 group has an on-chip D-A converter with 8-bit resolution and 2 channels (DAi (i=1, 2)). After the DA_1 selection bit or DA_2 selection bit is set to “0”, the D-A converter is performed by setting the value in the D-A conversion register. The result of D-A converter is output from DAi pin. When using the D-A converter, the corresponding port direction register bit ($P5_6/DA_1$, $P5_7/DA_2$) should be set to “0” (input status) and the pull-up resistor should be in the OFF state.

The output analog voltage V is determined by the value n (base 10) in the D-A conversion register as follows:

$V = V_{REF} \times n/256$ (n=0 to 255)
Where V_{REF} is the reference voltage.

At reset, the D-A conversion registers are cleared to “00_{16}”, the DAi output enable bits are cleared to “0”, and DAi pin goes to high impedance state. The DA output is not buffered, so connect an external buffer when driving a low-impedance load.

■ **Note on applied voltage to V_{REF} pin**

When the $P5_6/DA_1$ pin and $P5_7/DA_2$ pin are used as I/O ports, be sure to apply Vcc level to V_{REF} pin.
When these pins are used as D-A conversion output pins, the Vcc level is recommended for the applied voltage to V_{REF} pin.
When the voltage below Vcc level is applied, the D-A conversion accuracy may be worse.

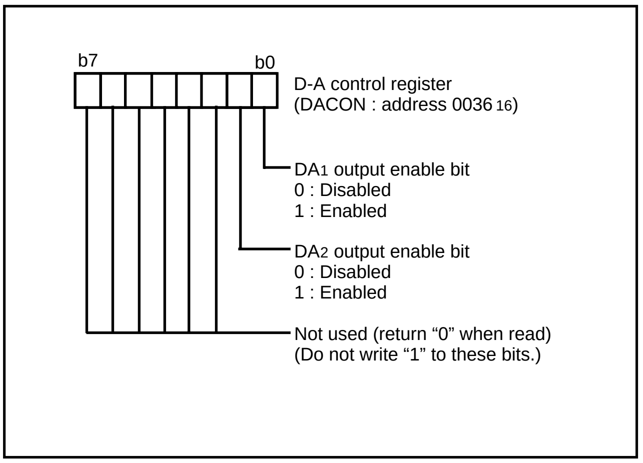


Fig. 37 Structure of D-A control register

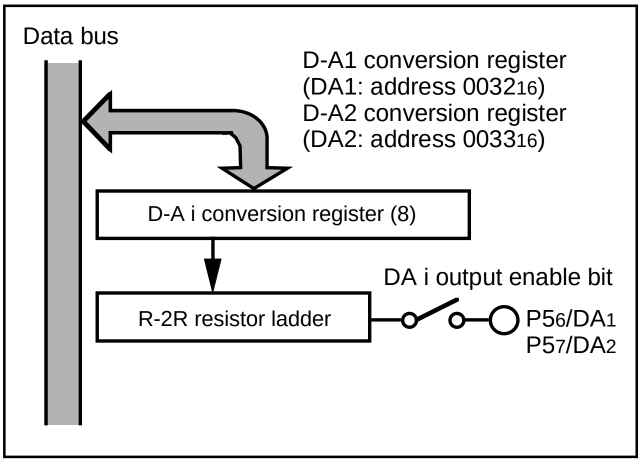


Fig. 38 Block diagram of D-A converter

LCD DRIVE CONTROL CIRCUIT

The 7560 group has the built-in Liquid Crystal Display (LCD) drive control circuit consisting of the following.

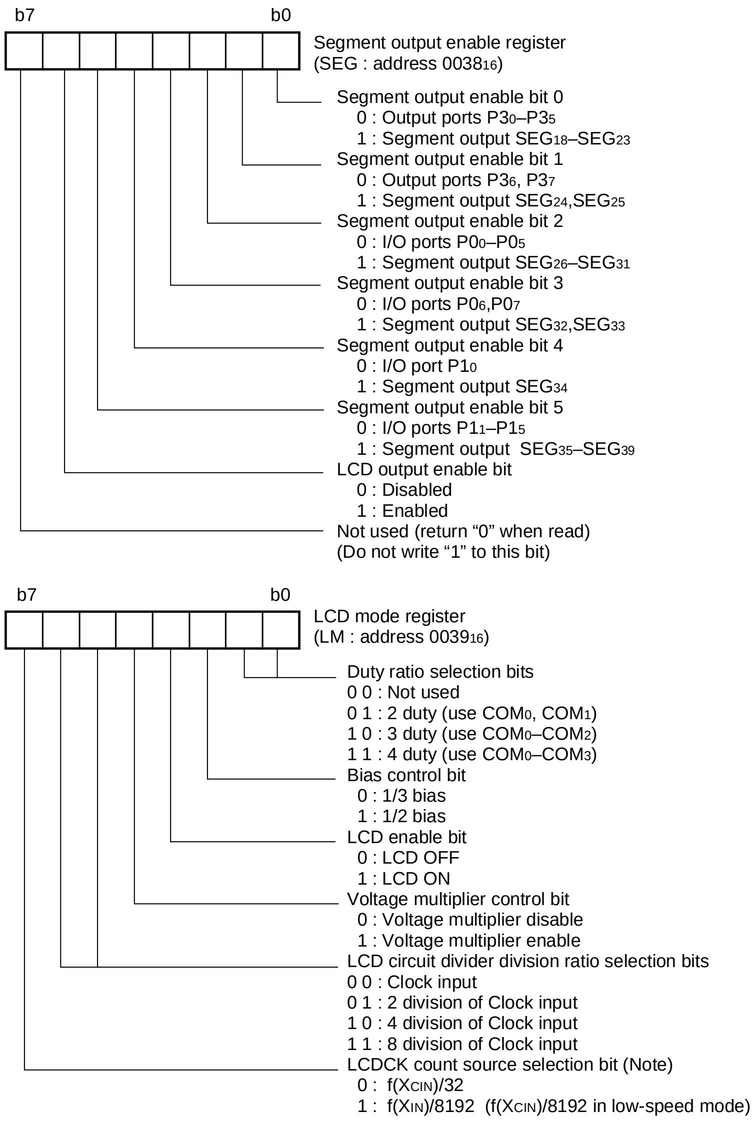
- LCD display RAM
- Segment output enable register
- LCD mode register
- Voltage multiplier
- Selector
- Timing controller
- Common driver
- Segment driver
- Bias control circuit

A maximum of 40 segment output pins and 4 common output pins can be used.

Up to 160 pixels can be controlled for LCD display. When the LCD enable bit is set to “1” after data is set in the LCD mode register, the segment output enable register and the LCD display RAM, the LCD drive control circuit starts reading the display data automatically, performs the bias control and the duty ratio control, and displays the data on the LCD panel.

Table 9. Maximum number of display pixels at each duty ratio

Duty ratio	Maximum number of display pixel
2	80 dots or 8 segment LCD 10 digits
3	120 dots or 8 segment LCD 15 digits
4	160 dots or 8 segment LCD 20 digits



Note : LCDCK is a clock for a LCD timing controller.

Fig. 39 Structure of segment output enable register and LCD mode register

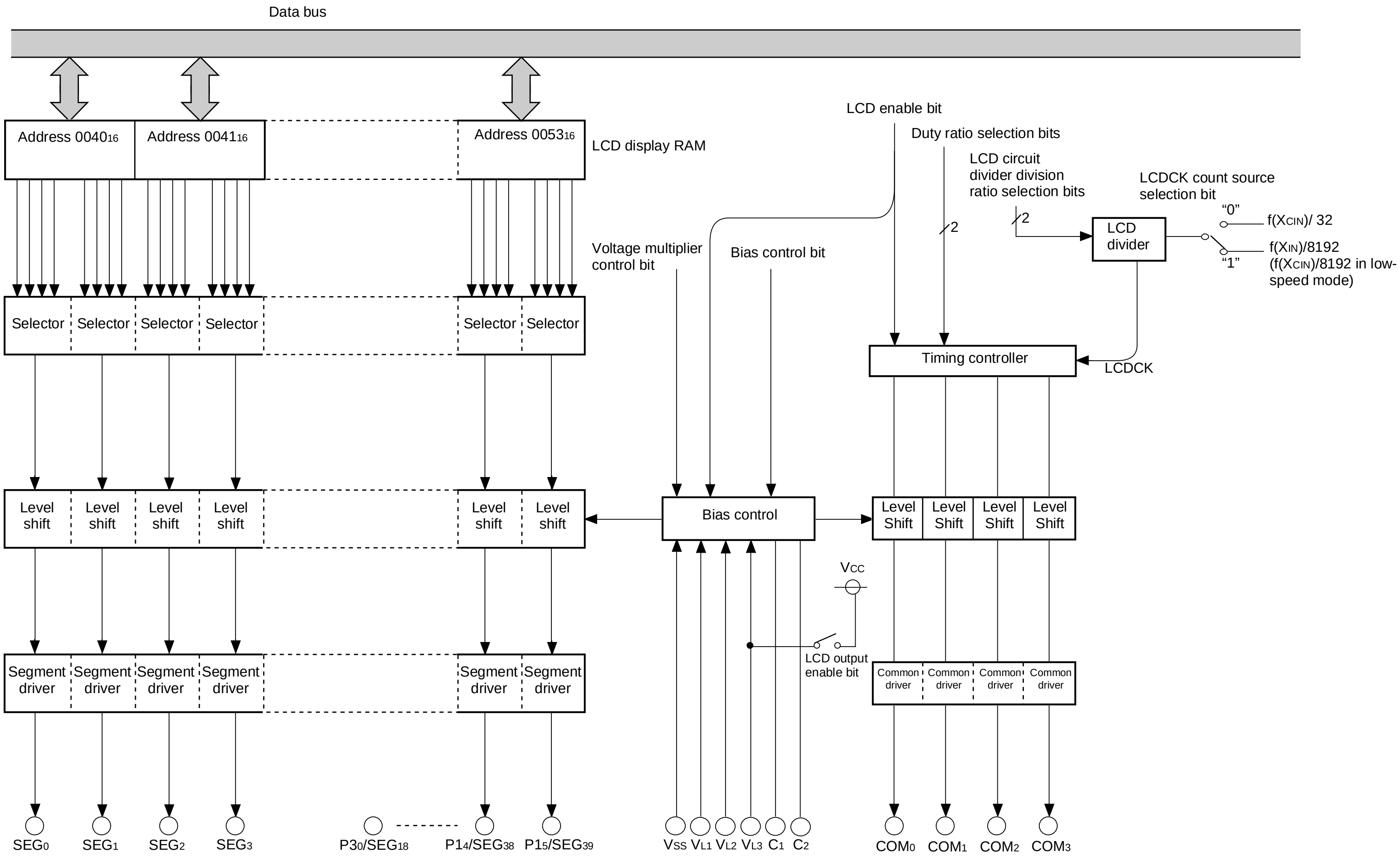


Fig. 40 Block diagram of LCD controller/driver

Voltage Multiplier (3 Times)

The voltage multiplier performs threefold boosting. This circuit inputs a reference voltage for boosting from LCD power input pin V_{L1}. (However, when using a 1/2 bias, connect V_{L1} and V_{L2} and apply voltage by external resistor division.)

Set each bit of the segment output enable register and the LCD mode register in the following order for operating the voltage multiplier.

1. Set the segment output enable bits (bits 0 to 5) of the segment output enable register to “0” or “1.”
2. Set the duty ratio selection bits (bits 0 and 1), the bias control bit (bit 2), the LCD circuit divider division ratio selection bits (bits 5 and 6), and the LCDCK count source selection bit (bit 7) of the LCD mode register to “0” or “1.”
3. Set the LCD output enable bit (bit 6) of the segment output enable register to “1.”
4. Set the voltage multiplier control bit (bit 4) of the LCD mode register to “1.”

When voltage is input to the V_{L1} pin during operating the voltage multiplier, voltage that is twice as large as V_{L1} occurs at the V_{L2} pin, and voltage that is three times as large as V_{L1} occurs at the V_{L3} pin.

When using the voltage multiplier, apply 1.3 V ≤ Voltage ≤ 2.1 V to the V_{L1} pin.

When not using the voltage multiplier,apply proper voltage to the LCD power input pins (V_{L1}–V_{L3}). Then set the LCD output enable bit to “1.”

When the LCD output enable bit is set to “0,” the V_{CC} voltage is applied to the V_{L3} pin inside of this microcomputer.

The voltage multiplier control bit (bit 4 of the LCD mode register) controls the voltage multiplier.

Bias Control and Applied Voltage to LCD Power Input Pins

To the LCD power input pins (V_{L1}–V_{L3}), apply the voltage shown in Table 10 according to the bias value.

Select a bias value by the bias control bit (bit 2 of the LCD mode register).

Table 10. Bias control and applied voltage to V_{L1}–V_{L3}

Bias value	Voltage value
1/3 bias	$V_{L3}=V_{LCD}$ $V_{L2}=2/3\ V_{LCD}$ $V_{L1}=1/3\ V_{LCD}$
1/2 bias	$V_{L3}=V_{LCD}$ $V_{L2}=V_{L1}=1/2\ V_{LCD}$

Note : V_{LCD} is the maximum value of supplied voltage for the LCD panel.

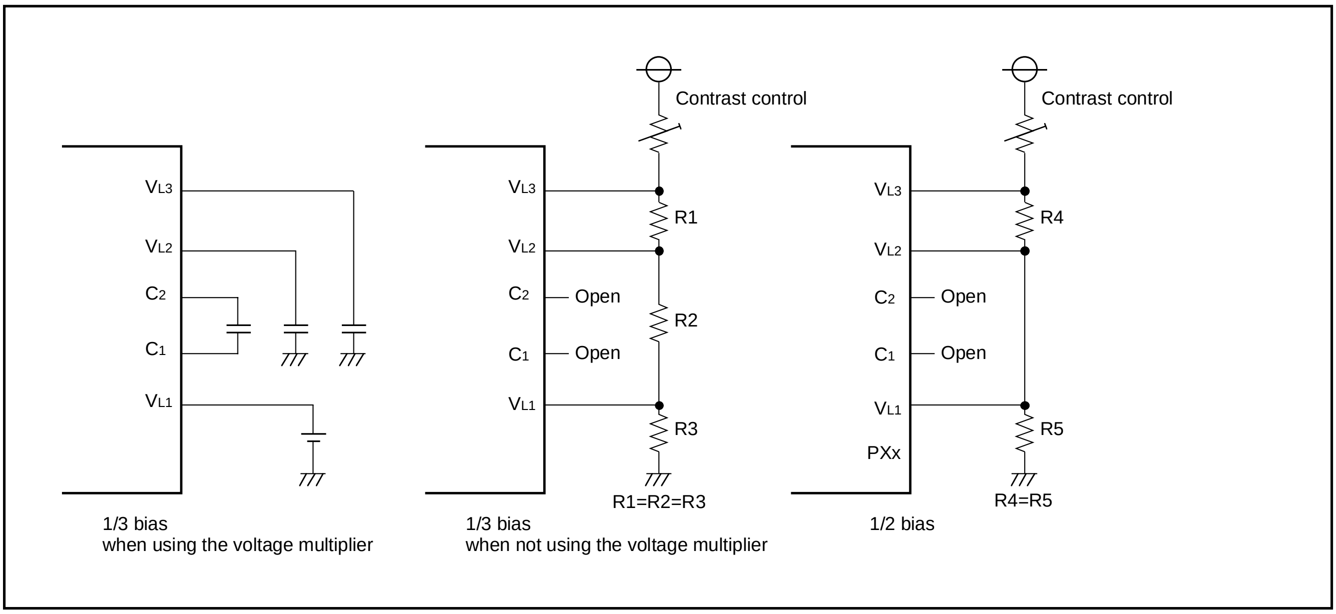


Fig. 41 Example of circuit at each bias

Common Pin and Duty Ratio Control

The common pins (COM_0–COM_3) to be used are determined by duty ratio.
Select duty ratio by the duty ratio selection bits (bits 0 and 1 of the LCD mode register).
When releasing from reset, the V_{CC} (V_{L3}) voltage is output from the common pins.

Table 11. Duty ratio control and common pins used

Duty ratio	Duty ratio selection bits		Common pins used
	Bit 1	Bit 0	
2	0	1	COM_0, COM_1 (Note 1)
3	1	0	COM_0–COM_2 (Note 2)
4	1	1	COM_0–COM_3

Notes 1: COM_2 and COM_3 are open.
2: COM_3 is open.

Segment Signal Output Pin

Segment signal output pins are classified into the segment-only pins (SEG_0–SEG_{17}), the segment/output port pins (SEG_{18}–SEG_{25}), and the segment/I/O port pins (SEG_{26}–SEG_{39}).
Segment signals are output according to the bit data of the LCD RAM corresponding to the duty ratio. After reset release, a V_{CC} (=V_{L3}) voltage is output to the segment-only pins and the segment/output port pins are the high impedance condition and pulled up to V_{CC} (=V_{L3}) voltage.
Also, the segment/I/O port pins(SEG_{26}–SEG_{39}) are set to input ports, and V_{CC} (=V_{L3}) is applied to them by pull-up resistor.

LCD Display RAM

Address 0040_{16} to 0053_{16} is the designated RAM for the LCD display. When “1” are written to these addresses, the corresponding segments of the LCD display panel are turned on.

LCD Drive Timing

The LCDCK timing frequency (LCD drive timing) is generated internally and the frame frequency can be determined with the following equation;

$$f(LCDCK) = \frac{\text{(frequency of count source for LCDCK)}}{\text{(divider division ratio for LCD)}}$$

$$\text{Frame frequency} = \frac{f(LCDCK)}{\text{duty ratio}}$$

Address \ Bit	7	6	5	4	3	2	1	0
	COM_3	COM_2	COM_1	COM_0	COM_3	COM_2	COM_1	COM_0
0040_{16}	SEG_1				SEG_0			
0041_{16}	SEG_3				SEG_2			
0042_{16}	SEG_5				SEG_4			
0043_{16}	SEG_7				SEG_6			
0044_{16}	SEG_9				SEG_8			
0045_{16}	SEG_{11}				SEG_{10}			
0046_{16}	SEG_{13}				SEG_{12}			
0047_{16}	SEG_{15}				SEG_{14}			
0048_{16}	SEG_{17}				SEG_{16}			
0049_{16}	SEG_{19}				SEG_{18}			
$004A_{16}$	SEG_{21}				SEG_{20}			
$004B_{16}$	SEG_{23}				SEG_{22}			
$004C_{16}$	SEG_{25}				SEG_{24}			
$004D_{16}$	SEG_{27}				SEG_{26}			
$004E_{16}$	SEG_{29}				SEG_{28}			
$004F_{16}$	SEG_{31}				SEG_{30}			
0050_{16}	SEG_{33}				SEG_{32}			
0051_{16}	SEG_{35}				SEG_{34}			
0052_{16}	SEG_{37}				SEG_{36}			
0053_{16}	SEG_{39}				SEG_{38}			

Fig. 42 LCD display RAM map

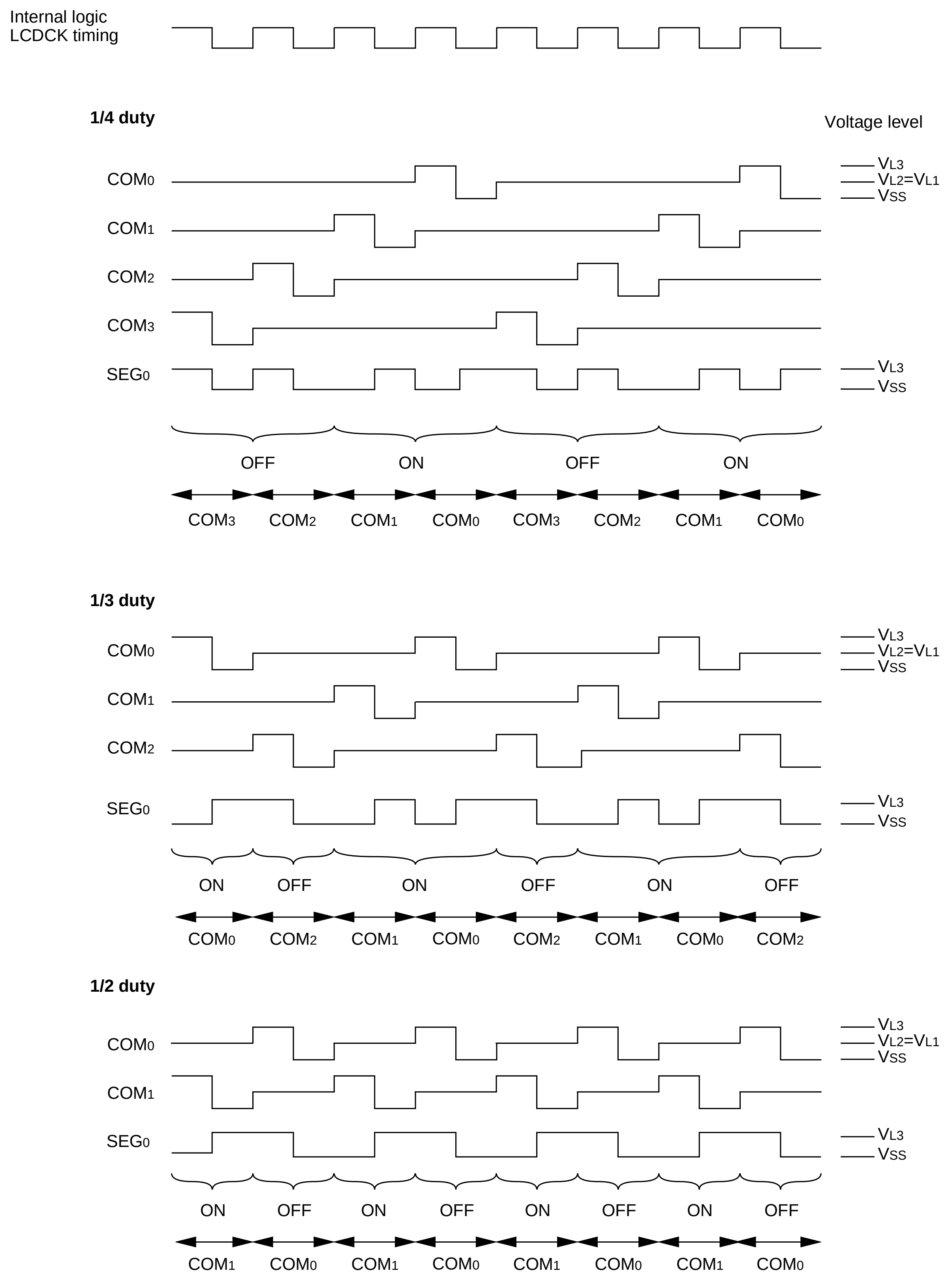


Fig. 43 LCD drive waveform (1/2 bias)

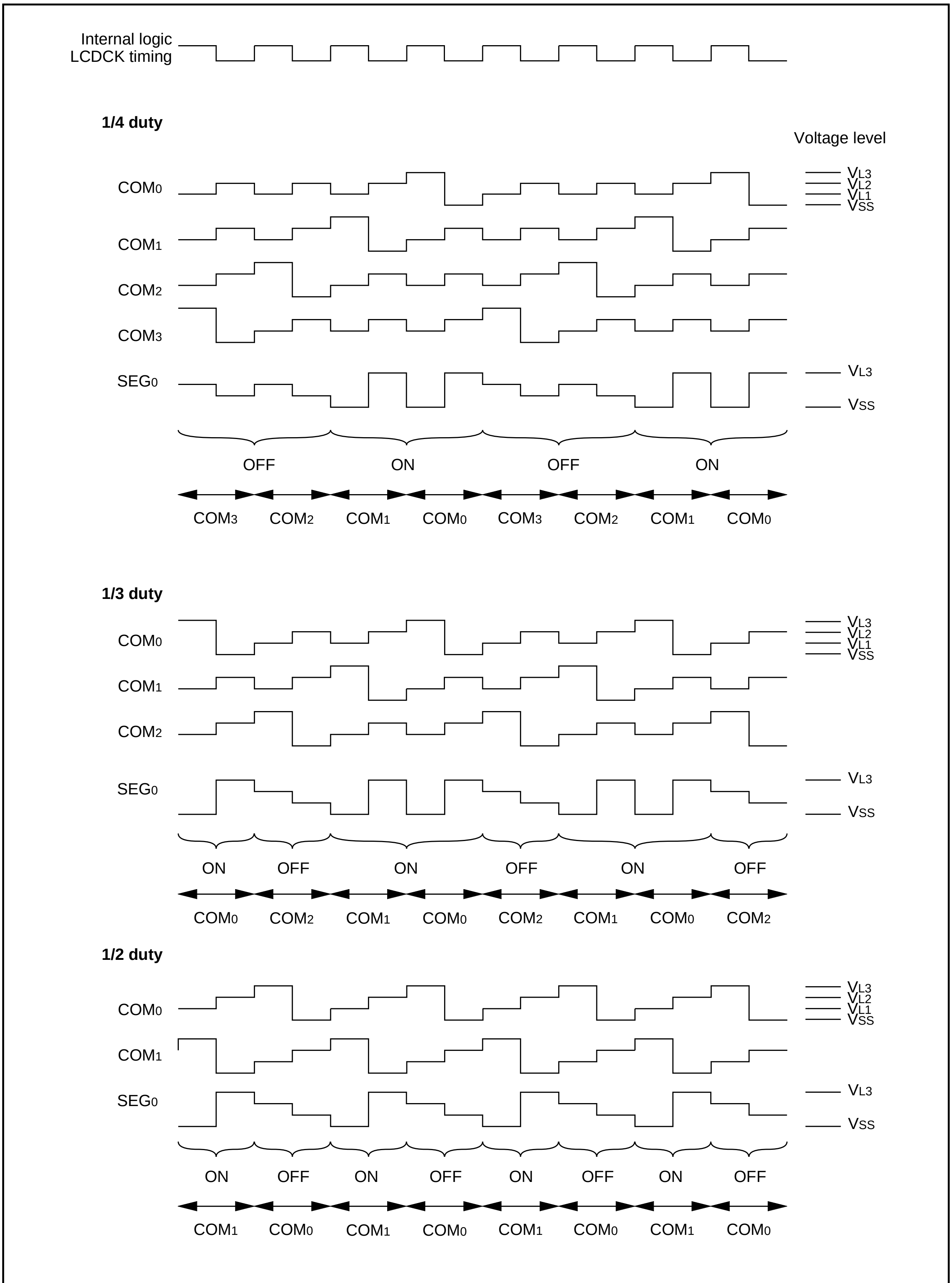


Fig. 44 LCD drive waveform (1/3 bias)

Watchdog Timer

The watchdog timer gives a mean of returning to the reset status when a program cannot run on a normal loop (for example, because of a software runaway).

The watchdog timer consists of an 8-bit watchdog timer L and a 6-bit watchdog timer H. At reset or writing to the watchdog timer control register (address 0037_{16}), the watchdog timer is set to "$3FFF_{16}$." When any data is not written to the watchdog timer control register (address 0037_{16}) after reset, the watchdog timer is in stop state. The watchdog timer starts to count down from "$3FFF_{16}$" by writing an optional value into the watchdog timer control register (address 0037_{16}) and an internal reset occurs at an underflow. Accordingly, programming is usually performed so that writing to the watchdog timer control register (address 0037_{16}) may be started before an underflow. The watchdog timer does not function when an optional value has not been written to the watchdog timer control register (address 0037_{16}). When address 0037_{16} is read, the following values are read:

- value of high-order 6-bit counter
- value of STP instruction disable bit
- value of count source selection bit.

When bit 6 of the watchdog timer control register (address 0037_{16}) is set to "0," the STP instruction is valid. The STP instruction is disabled by rewriting this bit to "1." At this time, if the STP instruction is executed, it is processed as an undefined instruction, so that a reset occurs inside.

This bit cannot be rewritten to "0" by programming. This bit is "0" immediately after reset.

The count source of the watchdog timer becomes the system clock ϕ divided by 8. The detection time in this case is set to 8.19 s at $f(X_{CIN})$ = 32 kHz and 32.768 ms at $f(X_{IN})$ = 8 MHz.

However, count source of high-order 6-bit timer can be connected to a signal divided system clock by 8 directly by writing the bit 7 of the watchdog timer control register (address 0037_{16}) to "1." The detection time in this case is set to 32 ms at $f(X_{CIN})$ = 32 kHz and 128 µs at $f(X_{IN})$ = 8 MHz. There is no difference in the detection time between the middle-speed mode and the high-speed mode.

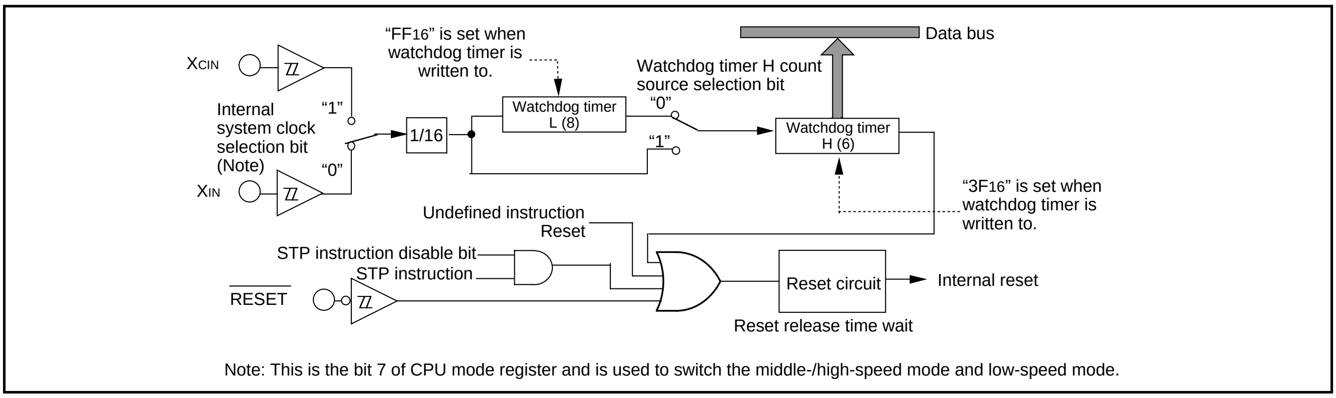


Fig. 45 Block diagram of watchdog timer

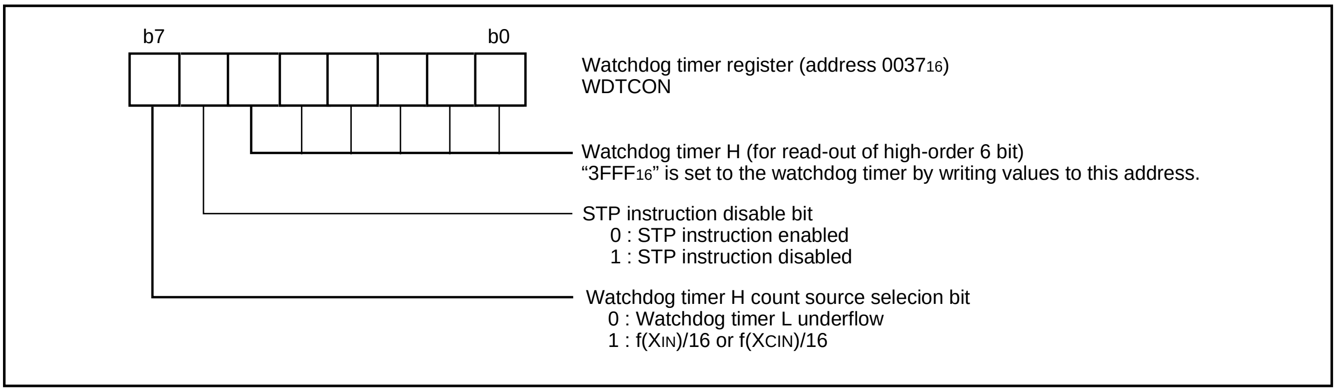


Fig. 46 Structure of watchdog timer control register

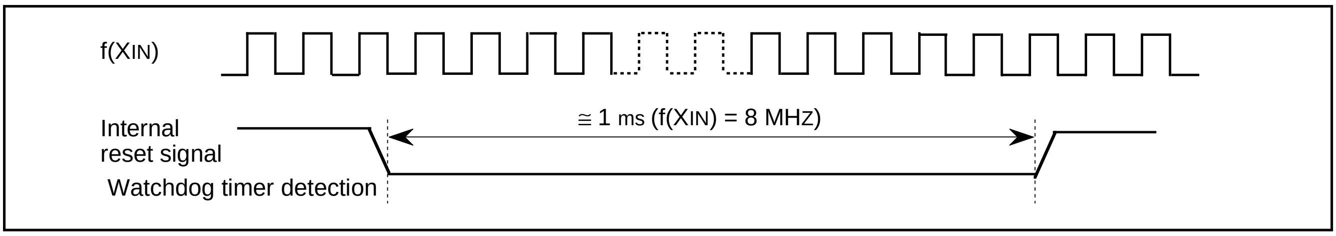


Fig. 47 Timing of reset output

TOUT/ϕ CLOCK OUTPUT FUNCTION

The internal system clock ϕ or timer 2 divided by 2 (TOUT output) can be output from port P4$_3$ by setting the TOUT/ϕ output control bit (bit 1) of the timer 123 mode register and the TOUT/ϕ output control register. Set bit 3 of the port P4 direction register to “1” when outputting the clock.

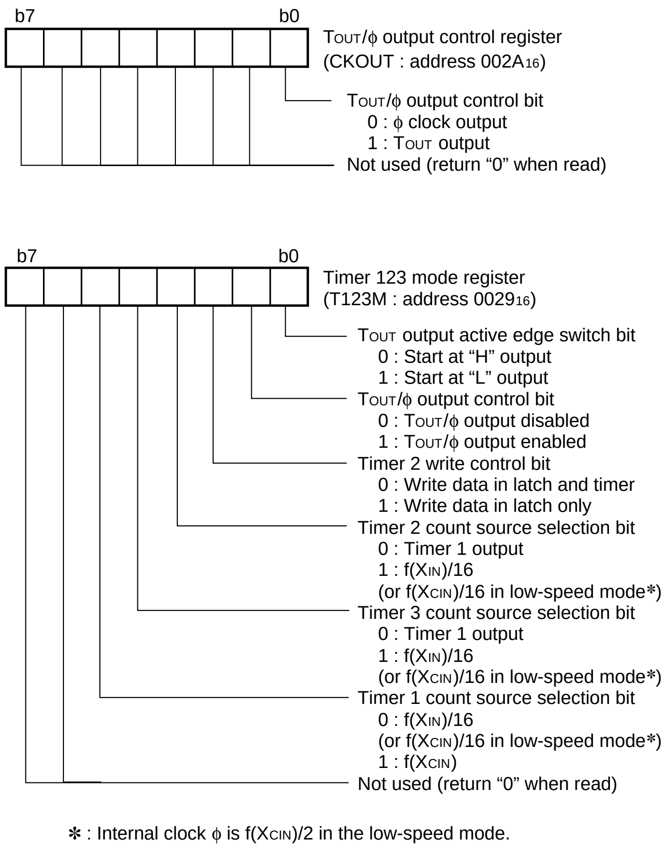


Fig. 48 Structure of TOUT/ϕ output-related register

RESET CIRCUIT

To reset the microcomputer, $\overline{\text{RESET}}$ pin should be held at an “L” level for 2 µs or more. Then the $\overline{\text{RESET}}$ pin is returned to an “H” level (the power source voltage should be between VCC(min.) and 5.5 V, and the quartz-crystal oscillator should be stable), reset is released. After the reset is completed, the program starts from the address contained in address $FFFD_{16}$ (high-order byte) and address $FFFC_{16}$ (low-order byte). Make sure that the reset input voltage is less than 0.2 VCC for VCC of VCC (min.).

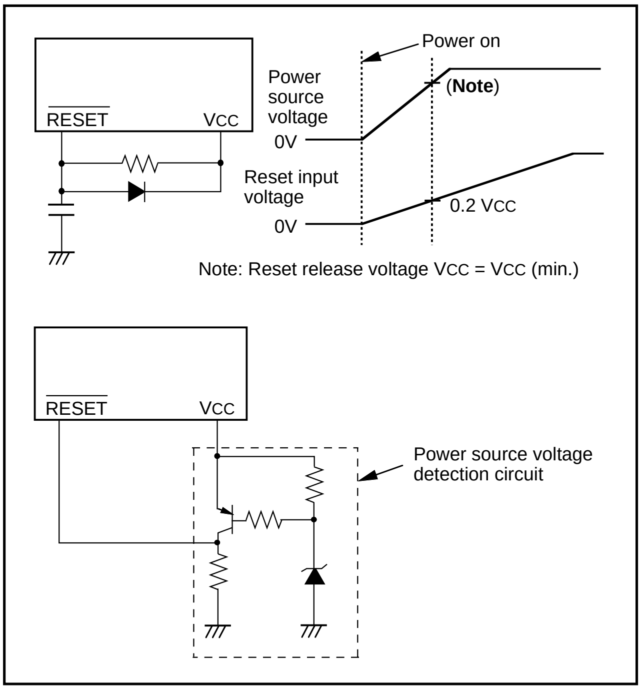


Fig. 49 Example of reset circuit

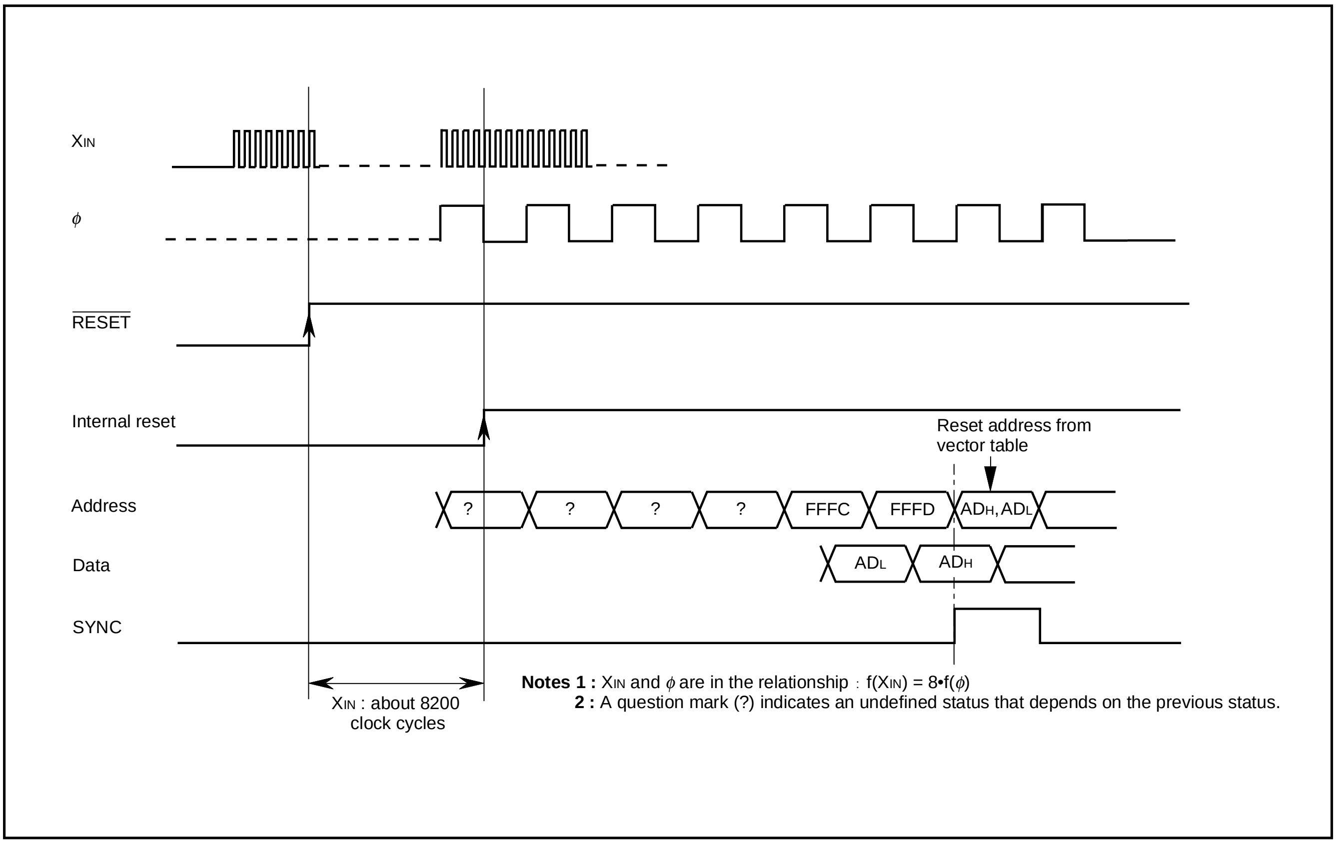


Fig. 50 Reset Sequence

		Address	Register contents
(1)	Port P0 direction register	0001_{16}	00_{16}
(2)	Port P1 direction register	0003_{16}	00_{16}
(3)	Port P2 direction register	0005_{16}	00_{16}
(4)	Port P3 output control register	0007_{16}	00_{16}
(5)	Port P4 direction register	0009_{16}	00_{16}
(6)	Port P5 direction register	$000B_{16}$	00_{16}
(7)	Port P6 direction register	$000D_{16}$	00_{16}
(8)	Port P7 direction register	$000F_{16}$	00_{16}
(9)	Key input control register	0015_{16}	00_{16}
(10)	PULL register A	0016_{16}	$3F_{16}$
(11)	PULL register B	0017_{16}	00_{16}
(12)	Serial I/O1 status register	0019_{16}	1 0 0 0 0 0 0 0
(13)	Serial I/O1 control register	$001A_{16}$	00_{16}
(14)	UART control register	$001B_{16}$	1 1 1 0 0 0 0 0
(15)	Serial I/O2 control register	$001D_{16}$	00_{16}
(16)	Timer X (low)	0020_{16}	FF_{16}
(17)	Timer X (high)	0021_{16}	FF_{16}
(18)	Timer Y (low)	0022_{16}	FF_{16}
(19)	Timer Y (high)	0023_{16}	FF_{16}
(20)	Timer 1	0024_{16}	FF_{16}
(21)	Timer 2	0025_{16}	01_{16}
(22)	Timer 3	0026_{16}	FF_{16}
(23)	Timer X mode register	0027_{16}	00_{16}
(24)	Timer Y mode register	0028_{16}	00_{16}
(25)	Timer 123 mode register	0029_{16}	00_{16}
(26)	T_{OUT}/φ output control register	$002A_{16}$	00_{16}
(27)	PWM control register	$002B_{16}$	00_{16}
(28)	D-A1 conversion register	0032_{16}	00_{16}
(29)	D-A2 conversion register	0033_{16}	00_{16}
(30)	A-D control register	0034_{16}	0 0 0 0 1 0 0 0
(31)	D-A control register	0036_{16}	00_{16}
(32)	Watchdog timer control register	0037_{16}	0 0 1 1 1 1 1 1
(33)	Segment output enable register	0038_{16}	00_{16}
(34)	LCD mode register	0039_{16}	00_{16}
(35)	Interrupt edge selection register	$003A_{16}$	00_{16}
(36)	CPU mode register	$003B_{16}$	0 1 0 0 1 0 0 0
(37)	Interrupt request register 1	$003C_{16}$	00_{16}
(38)	Interrupt request register 2	$003D_{16}$	00_{16}
(39)	Interrupt control register 1	$003E_{16}$	00_{16}
(40)	Interrupt control register 2	$003F_{16}$	00_{16}
(41)	Processor status register	(PS)	✕ ✕ ✕ ✕ ✕ 1 ✕ ✕
(42)	Program counter	(PC_H)	Contents of address $FFFD_{16}$
		(PC_L)	Contents of address $FFFC_{16}$
(43)	Watchdog timer (high-order)		$3F_{16}$
(44)	Watchdog timer (low-order)		FF_{16}

Note: The contents of all other registers and RAM are undefined after reset, so they must be initialized by software.
✕ : Undefined

Fig. 51 Internal state of microcomputer immediately after reset

CLOCK GENERATING CIRCUIT

The 7560 group has two built-in oscillation circuits. An oscillation circuit can be formed by connecting a resonator between X_{IN} and X_{OUT} (X_{CIN} and X_{COUT}). Use the circuit constants in accordance with the resonator manufacturer's recommended values. No external resistor is needed between X_{IN} and X_{OUT} since a feed-back resistor exists on-chip. However, an external feed-back resistor is needed between X_{CIN} and X_{COUT}.
To supply a clock signal externally, input it to the X_{IN} pin and make the X_{OUT} pin open. The sub-clock X_{CIN}-X_{COUT} oscillation circuit cannot directly input clocks that are externally generated. Accordingly, be sure to cause an external resonator to oscillate.
Immediately after poweron, only the X_{IN} oscillation circuit starts oscillating, and X_{CIN} and X_{COUT} pins go to high-impedance state.

Frequency Control
(1) Middle-speed mode

The internal clock ϕ is the frequency of X_{IN} divided by 8.
After reset, this mode is selected.

(2)High-speed mode

The internal clock ϕ is half the frequency of X_{IN}.

(3) Low-speed mode

- The internal clock ϕ is half the frequency of X_{CIN}.
- A low-power consumption operation can be realized by stopping the main clock X_{IN} in this mode. To stop the main clock, set bit 5 of the CPU mode register to “1”.
  When the main clock X_{IN} is restarted, set enough time for oscillation to stabilize by programming.

Note: If you switch the mode between middle/high-speed and low-speed, stabilize both X_{IN} and X_{CIN} oscillations. The sufficient time is required for the sub-clock to stabilize, especially immediately after power-on and at returning from stop mode. When switching the mode between middle/high-speed and low-speed, set the frequency in the condition that $f(X_{IN}) > 3 \cdot f(X_{CIN})$.

Oscillation Control
(1) Stop mode

If the STP instruction is executed, the internal clock ϕ stops at an “H” level, and X_{IN} and X_{CIN} oscillators stop. Timer 1 is set to “FF_{16}” and timer 2 is set to “01_{16}”.
Either X_{IN} or X_{CIN} divided by 16 is input to timer 1 as count source, and the output of timer 1 is connected to timer 2.
The bits of the timer 123 mode register except bit 4 are cleared to “0”. Set the timer 1 and timer 2 interrupt enable bits to disabled (“0”) before executing the STP instruction.
Oscillator restarts at reset or when an external interrupt is received, but the internal clock ϕ is not supplied to the CPU until timer 2 underflows. This allows time for the clock circuit oscillation to stabilize when a ceramic resonator is used.

(2) Wait mode

If the WIT instruction is executed, the internal clock ϕ stops at an “H” level. The states of X_{IN} and X_{CIN} are the same as the state before the executing the WIT instruction. The internal clock restarts at reset or when an interrupt is received. Since the oscillator does not stop, normal operation can be started immediately after the clock is restarted.

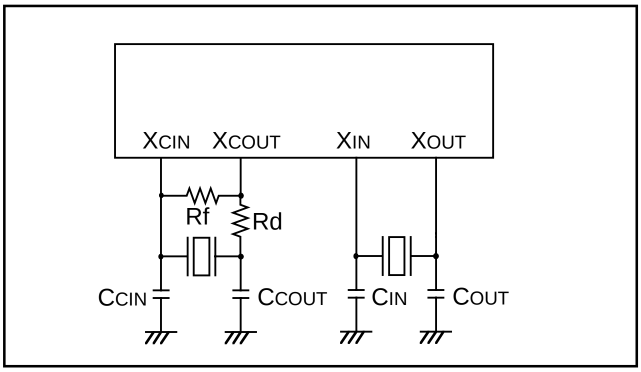


Fig. 52 Ceramic resonator circuit

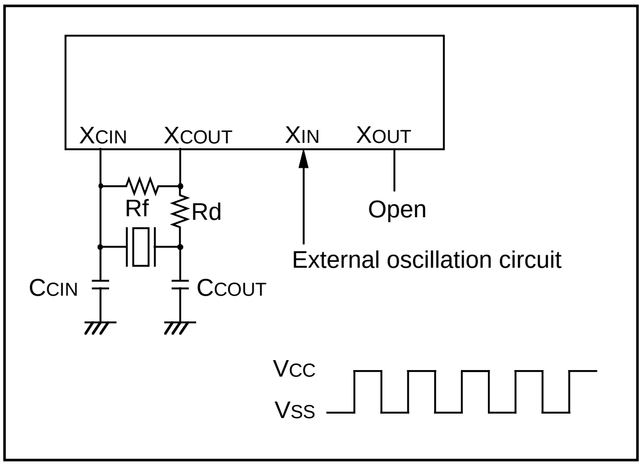
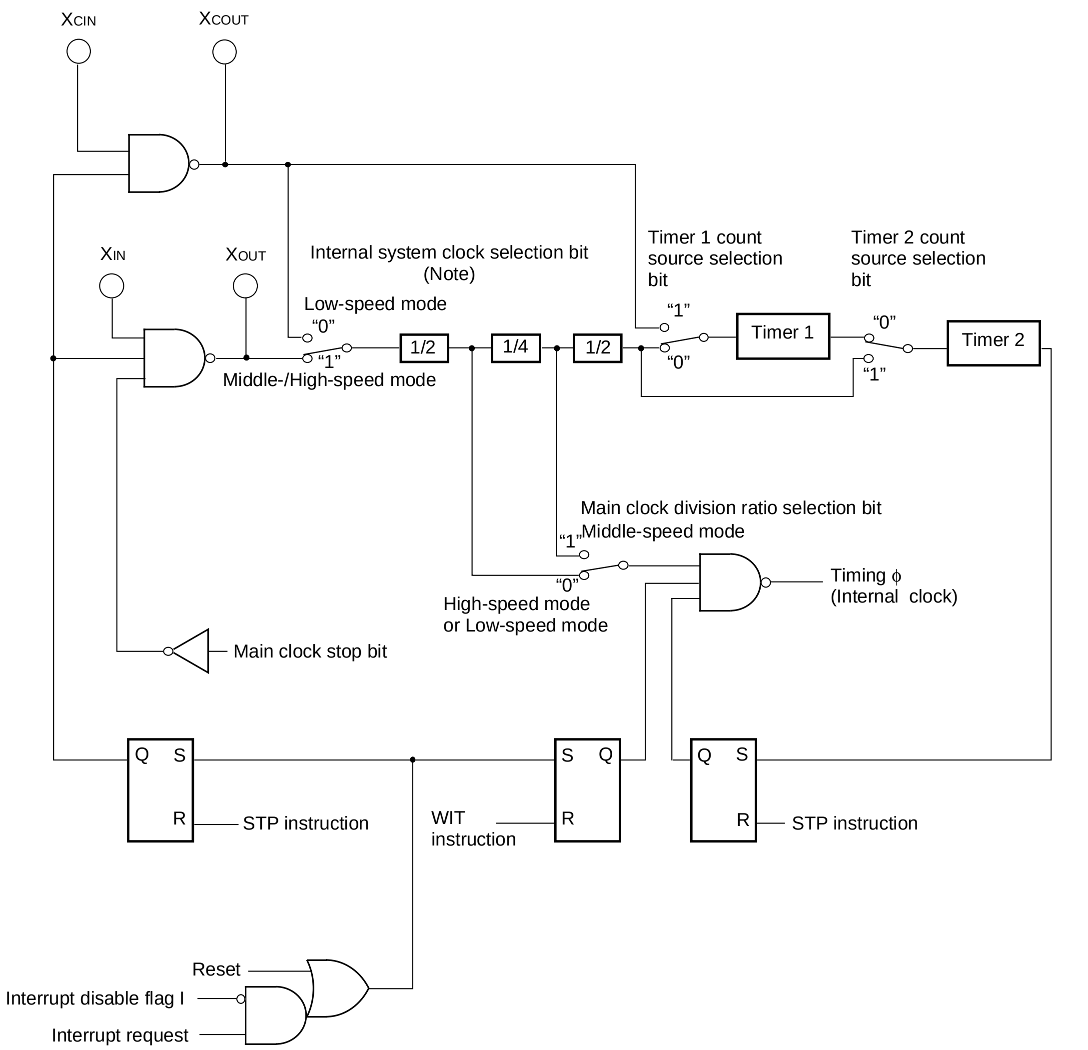
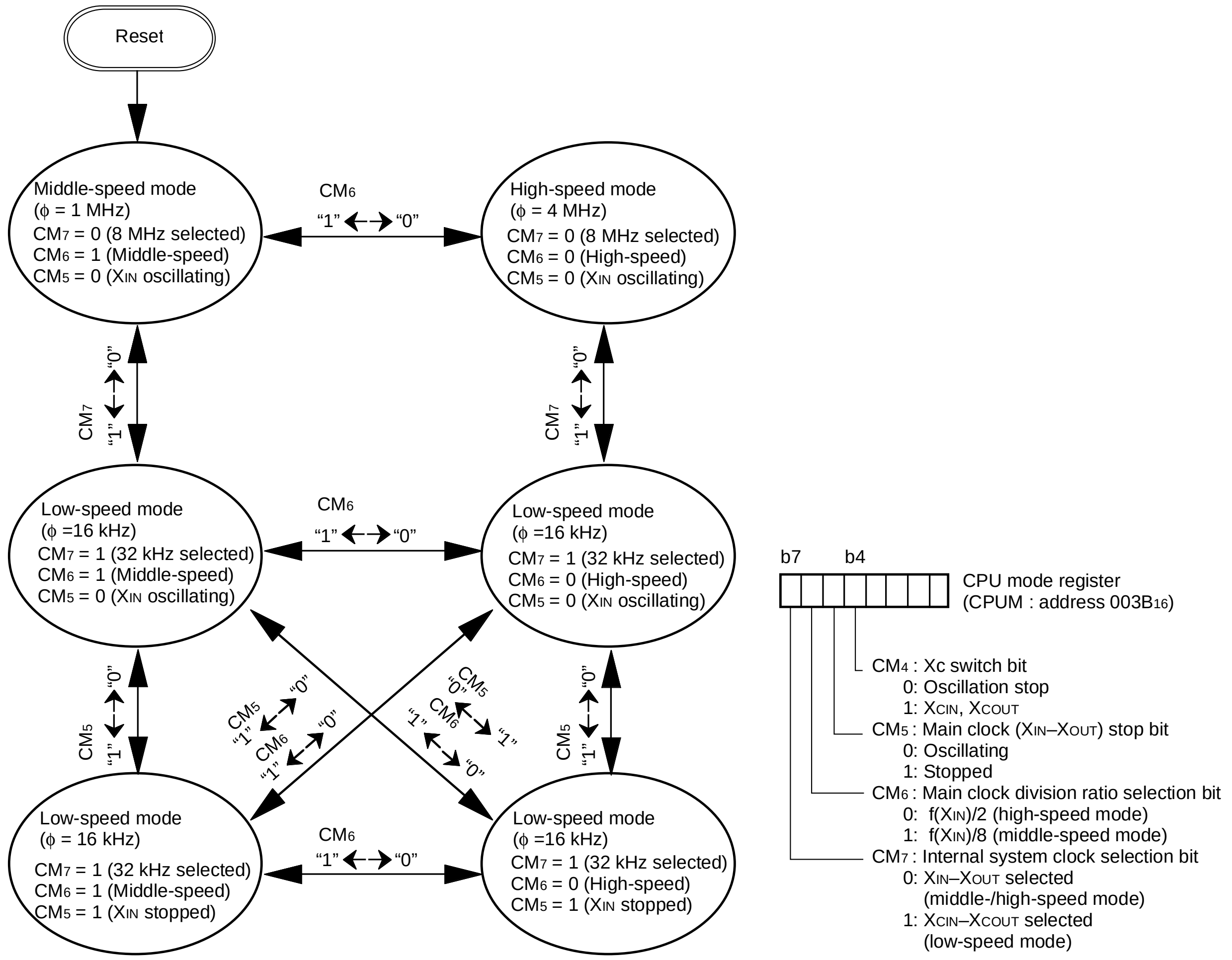


Fig. 53 External clock input circuit



Note: When using the low-speed mode, set the XC switch bit to "1".

Fig. 54 Clock generating circuit block diagram



Notes

1: Switch the mode by the arrows shown between the mode blocks. (Do not switch between the mode directly without an arrow.)
2: The all modes can be switched to the stop mode or the wait mode and returned to the source mode when the stop mode or the wait mode is ended.
3: Timer and LCD operate in the wait mode.
4: When the stop mode is ended, a delay time can be set by timer 1 and timer 2 in middle-/high-speed mode.
5: When the stop mode is ended, a delay time in low-speed mode can be set as well.
6: Wait until oscillation stabilizes after oscillating the main clock X_{IN} before the switching from the low-speed mode to middle-/high-speed mode.
7: The example assumes that 8 MHz is being applied to the X_{IN} pin and 32 kHz to the X_{CIN} pin. φ indicates the internal clock.

Fig. 55 State transitions of system clock

NOTES ON PROGRAMMING

Processor Status Register

The contents of the processor status register (PS) after a reset are undefined, except for the interrupt disable flag (I) which is “1”. After a reset, initialize flags which affect program execution.
In particular, it is essential to initialize the index X mode (T) and the decimal mode (D) flags because of their effect on calculations.

Interrupt

The contents of the interrupt request bits do not change immediately after they have been written. After writing to an interrupt request register, execute at least one instruction before performing a BBC or BBS instruction.

Decimal Calculations

To calculate in decimal notation, set the decimal mode flag (D) to “1”, then execute an ADC or SBC instruction. Only the ADC and SBC instructions yield proper decimal results. After executing an ADC or SBC instruction, execute at least one instruction before executing a SEC, CLC, or CLD instruction.

In decimal mode, the values of the negative (N), overflow (V), and zero (Z) flags are invalid.

Timers

If a value n (between 0 and 255) is written to a timer latch, the frequency division ratio is 1/(n + 1).

Multiplication and Division Instructions

The index mode (T) and the decimal mode (D) flags do not affect the MUL and DIV instruction.
The execution of these instructions does not change the contents of the processor status register.

Ports

The contents of the port direction registers cannot be read.
The following cannot be used:

- The data transfer instruction (LDA, etc.)
- The operation instruction when the index X mode flag (T) is “1”
- The addressing mode which uses the value of a direction register as an index
- The bit-test instruction (BBC or BBS, etc.) to a direction register
- The read-modify-write instruction (ROR, CLB, or SEB, etc.) to a direction register

Use instructions such as LDM and STA, etc., to set the port direction registers.

Serial I/O

In clock synchronous serial I/O, if the receive side is using an external clock and it is to output the $\overline{S_{RDY}}$ signal, set the transmit enable bit, the receive enable bit, and the $\overline{S_{RDY}}$ output enable bit to “1”.
Serial I/O1 continues to output the final bit from the T_XD pin after transmission is completed.
In serial I/O2, the S_{OUT2} pin goes to high impedance state after transmission is completed.

A-D Converter

The comparator uses internal capacitors whose charge will be lost if the clock frequency is too low.
Make sure that $f(X_{IN})$ is at least 500kHz during an A-D conversion.
Do not execute the STP or WIT instruction during an A-D conversion.

Instruction Execution Time

The instruction execution time is obtained by multiplying the frequency of the internal clock ϕ by the number of cycles needed to execute an instruction.
The number of cycles required to execute an instruction is shown in the list of machine instructions.
The frequency of the internal clock ϕ is half of the X_{IN} frequency.

DATA REQUIRED FOR MASK ORDERS

The following are necessary when ordering a mask ROM production:

1. Mask ROM Order Confirmation Form*
2. Mark Specification Form*
3. Data to be written to ROM, in EPROM form (three identical copies) or one floppy disk.

*For the mask ROM confirmation and the mark specifications, refer to the “Mitsubishi MCU Technical Information” Homepage (http://www.infomicom.mesc.co.jp/indexe.htm).

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

Table 12 Absolute maximum ratings

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Power source voltage	All voltages are based on V_{SS}. Output transistors are cut off.	–0.3 to 6.5	V
V_I	Input voltage $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P4_0$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$		–0.3 to V_{CC} +0.3	V
V_I	Input voltage $P7_0$–$P7_7$		–0.3 to V_{CC} +0.3	V
V_I	Input voltage V_{L1}		–0.3 to V_{L2}	V
V_I	Input voltage V_{L2}		V_{L1} to V_{L3}	V
V_I	Input voltage V_{L3}		V_{L2} to 6.5	V
V_I	Input voltage C_1, C_2		–0.3 to 6.5	V
V_I	Input voltage $\overline{RESET}$, X_{IN}		–0.3 to V_{CC} +0.3	V
V_O	Output voltage C_1, C_2		–0.3 to 6.5	V
V_O	Output voltage $P0_0$–$P0_7$, $P1_0$–$P1_5$, $P3_0$–$P3_7$	At output port	–0.3 to V_{CC}	V
		At segment output	–0.3 to V_{L3}	V
V_O	Output voltage $P1_6$, $P1_7$, $P2_0$–$P2_7$, $P4_0$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$, $P7_1$–$P7_7$		–0.3 to V_{CC} +0.3	V
V_O	Output voltage V_{L3}		–0.3 to 6.5	V
V_O	Output voltage V_{L2}, SEG_0–SEG_{17}		–0.3 to V_{L3}	V
V_O	Output voltage X_{OUT}		–0.3 to V_{CC} +0.3	V
Pd	Power dissipation	Ta = 25°C	300	mW
Topr	Operating temperature		–20 to 85	°C
Tstg	Storage temperature		–40 to 125	°C

RECOMMENDED OPERATING CONDITIONS

Table 13 Recommended operating conditions (1) (V_{CC} = 2.2 to 5.5 V, Ta = –20 to 85°C, unless otherwise noted)

Symbol	Parameter		Limits Min.	Typ.	Max.	Unit
V_{CC}	Power source voltage	High-speed mode f(X_{IN}) = 8 MHz	4.0	5.0	5.5	V
		Middle-speed mode f(X_{IN}) = 8 MHz	2.2	5.0	5.5	
		Low-speed mode	2.2	5.0	5.5	
V_{SS}	Power source voltage			0		V
V_{REF}	A-D, D-A conversion reference voltage		2.0		V_{CC}	V
AV_{SS}	Analog power source voltage			0		V
V_{IA}	Analog input voltage AN_0–AN_7		AV_{SS}		V_{CC}	V

Table 14 Recommended operating conditions (2) (V_{CC} = 2.5 to 5.5 V, Ta = –20 to 85°C, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min.	Typ.	Max.	
V_{IH}	"H" input voltage	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P4_0$, $P4_3$, $P4_5$, $P4_7$, $P5_0$–$P5_3$, $P5_6$, $P6_1$, $P6_4$–$P6_7$, $P7_1$–$P7_7$	0.7 V_{CC}		V_{CC}	V
V_{IH}	"H" input voltage	$P2_0$–$P2_7$, $P4_1$, $P4_2$, $P4_4$, $P4_6$, $P5_4$, $P5_5$, $P5_7$, $P6_0$, $P6_2$, $P6_3$, $P7_0$	0.8 V_{CC}		V_{CC}	V
V_{IH}	"H" input voltage	$\overline{RESET}$	0.8 V_{CC}		V_{CC}	V
V_{IH}	"H" input voltage	X_{IN}	0.8 V_{CC}		V_{CC}	V
V_{IL}	"L" input voltage	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P4_0$, $P4_3$, $P4_5$, $P4_7$, $P5_0$–$P5_3$, $P5_6$, $P6_1$, $P6_4$–$P6_7$, $P7_1$–$P7_7$	0		0.3 V_{CC}	V
V_{IL}	"L" input voltage	$P2_0$–$P2_7$, $P4_1$, $P4_2$, $P4_4$, $P4_6$, $P5_4$, $P5_5$, $P5_7$, $P6_0$, $P6_2$, $P6_3$, $P7_0$	0		0.2 V_{CC}	V
V_{IL}	"L" input voltage	$\overline{RESET}$	0		0.2 V_{CC}	V
V_{IL}	"L" input voltage	X_{IN}	0		0.2 V_{CC}	V

Table 15 Recommended operating conditions (3) (V_{CC} = 2.2 to 2.5 V, Ta = –20 to 85°C, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min.	Typ.	Max.	
V_{IH}	"H" input voltage	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P4_0$, $P4_3$, $P4_5$, $P4_7$, $P5_0$–$P5_3$, $P5_6$, $P6_1$, $P6_4$–$P6_7$, $P7_1$–$P7_7$	0.8 V_{CC}		V_{CC}	V
V_{IH}	"H" input voltage	$P2_0$–$P2_7$, $P4_1$, $P4_2$, $P4_4$, $P4_6$, $P5_4$, $P5_5$, $P5_7$, $P6_0$, $P6_2$, $P6_3$, $P7_0$	0.95 V_{CC}		V_{CC}	V
V_{IH}	"H" input voltage	$\overline{RESET}$	0.95 V_{CC}		V_{CC}	V
V_{IH}	"H" input voltage	X_{IN}	0.95 V_{CC}		V_{CC}	V
V_{IL}	"L" input voltage	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P4_0$, $P4_3$, $P4_5$, $P4_7$, $P5_0$–$P5_3$, $P5_6$, $P6_1$, $P6_4$–$P6_7$, $P7_1$–$P7_7$	0		0.2 V_{CC}	V
V_{IL}	"L" input voltage	$P2_0$–$P2_7$, $P4_1$, $P4_2$, $P4_4$, $P4_6$, $P5_4$, $P5_5$, $P5_7$, $P6_0$, $P6_2$, $P6_3$, $P7_0$	0		0.05 V_{CC}	V
V_{IL}	"L" input voltage	$\overline{RESET}$	0		0.05 V_{CC}	V
V_{IL}	"L" input voltage	X_{IN}	0		0.05 V_{CC}	V

Table 16 Recommended operating conditions (4) (V_{CC} = 2.2 to 5.5 V, Ta = –20 to 85°C, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min.	Typ.	Max.	
$\Sigma I_{OH(peak)}$	"H" total peak output current	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_7$ **(Note 1)**			–20	mA
$\Sigma I_{OH(peak)}$	"H" total peak output current	$P4_1$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$ **(Note 1)**			–20	mA
$\Sigma I_{OL(peak)}$	"L" total peak output current	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_7$ **(Note 1)**			20	mA
$\Sigma I_{OL(peak)}$	"L" total peak output current	$P4_1$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$ **(Note 1)**			20	mA
$\Sigma I_{OL(peak)}$	"L" total peak output current	$P4_0$, $P7_1$–$P7_7$ **(Note 1)**			80	mA
$\Sigma I_{OH(avg)}$	"H" total average output current	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_7$ **(Note 1)**			–10	mA
$\Sigma I_{OH(avg)}$	"H" total average output current	$P4_1$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$ **(Note 1)**			–10	mA
$\Sigma I_{OL(avg)}$	"L" total average output current	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_7$ **(Note 1)**			10	mA
$\Sigma I_{OL(avg)}$	"L" total average output current	$P4_1$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$ **(Note 1)**			10	mA
$\Sigma I_{OL(avg)}$	"L" total average output current	$P4_0$, $P7_1$–$P7_7$ **(Note 1)**			40	mA
$I_{OH(peak)}$	"H" peak output current	$P0_0$–$P0_7$, $P1_0$–$P1_5$, $P3_0$–$P3_7$ **(Note 2)**			–1.0	mA
$I_{OH(peak)}$	"H" peak output current	$P1_6$, $P1_7$, $P2_0$–$P2_7$, $P4_1$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$ **(Note 2)**			–5.0	mA
$I_{OL(peak)}$	"L" peak output current	$P0_0$–$P0_7$, $P1_0$–$P1_5$, $P3_0$–$P3_7$ **(Note 2)**			5.0	mA
$I_{OL(peak)}$	"L" peak output current	$P1_6$, $P1_7$, $P2_0$–$P2_7$, $P4_1$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$ **(Note 2)**			10	mA
$I_{OL(peak)}$	"L" peak output current	$P4_0$, $P7_1$–$P7_7$ **(Note 2)**			20	mA
$I_{OH(avg)}$	"H" average output current	$P0_0$–$P0_7$, $P1_0$–$P1_5$, $P3_0$–$P3_7$ **(Note 3)**			–0.5	mA
$I_{OH(avg)}$	"H" average output current	$P1_6$, $P1_7$, $P2_0$–$P2_7$, $P4_1$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$			–2.5	mA
$I_{OL(avg)}$	"L" average output current	$P0_0$–$P0_7$, $P1_0$–$P1_5$, $P3_0$–$P3_7$ **(Note 3)**			2.5	mA
$I_{OL(avg)}$	"L" average output current	$P1_6$, $P1_7$, $P2_0$–$P2_7$, $P4_1$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$ **(Note 3)**			5.0	mA
$I_{OL(avg)}$	"L" average output current	$P4_0$, $P7_1$–$P7_7$ **(Note 3)**			10	mA

Notes1: The total output current is the sum of all the currents flowing through all the applicable ports. The total average current is an average value measured over 100 ms. The total peak current is the peak value of all the currents.
2: The peak output current is the peak current flowing in each port.
3: The average output current is an average value measured over 100 ms.

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Table 17 Recommended operating conditions (5) (V_{CC} = 2.2 to 5.5 V, Ta = –20 to 85°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
$f(CNTR_0)$ $f(CNTR_1)$	Input frequency for timers X and Y (duty cycle 50%)	(4.0 V ≤ V_{CC} ≤ 5.5 V)			4.0	MHz
		(V_{CC} ≤ 4.0 V)			$(10 \times V_{CC} - 4)/9$	MHz
$f(X_{IN})$	Main clock input oscillation frequency **(Note 1)**	High-speed mode (4.0 V ≤ V_{CC} ≤ 5.5 V)			8.0	MHz
		High-speed mode (2.2 V ≤ V_{CC} ≤ 4.0 V)			$(20 \times V_{CC} - 8)/9$	MHz
		Middle-speed mode			8.0	MHz
$f(X_{CIN})$	Sub-clock input oscillation frequency **(Notes 1, 2)**			32.768	50	kHz

Notes1: When the oscillation frequency has a duty cycle of 50%.

2: When using the microcomputer in low-speed mode, make sure that the sub-clock input oscillation frequency on condition that $f(X_{CIN}) < f(X_{IN})/3$.

Table 18 Electrical characteristics (1) (V_{CC} =4.0 to 5.5 V, Ta = –20 to 85°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
V_{OH}	"H" output voltage $P0_0$–$P0_7$, $P1_0$–$P1_5$, $P3_0$–$P3_7$	I_{OH} = –1 mA	V_{CC}–2.0			V
		I_{OH} = –0.25 mA V_{CC} = 2.2 V	V_{CC}–0.8			V
V_{OH}	"H" output voltage $P1_6$, $P1_7$, $P2_0$–$P2_7$, $P4_1$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$ **(Note 1)**	I_{OH} = –5 mA	V_{CC}–2.0			V
		I_{OH} = –1.5 mA	V_{CC}–0.5			V
		I_{OH} = –1.25 mA V_{CC} = 2.2 V	V_{CC}–0.8			V
V_{OL}	"L" output voltage $P0_0$–$P0_7$, $P1_0$–$P1_5$, $P3_0$–$P3_7$	I_{OL} = 5 mA			2.0	V
		I_{OL} = 1.5 mA			0.5	V
		I_{OL} = 1.25 mA V_{CC} = 2.2 V			0.8	V
V_{OL}	"L" output voltage $P1_6$, $P1_7$, $P2_0$–$P2_7$, $P4_1$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$	I_{OL} = 10 mA			2.0	V
		I_{OL} = 3.0 mA			0.5	V
		I_{OL} = 2.5 mA V_{CC} = 2.2 V			0.8	V
V_{OL}	"L" output voltage $P4_0$, $P7_1$–$P7_7$	I_{OL} = 10 mA			0.5	V
		I_{OL} = 5 mA V_{CC} = 2.2 V			0.3	V
V_{T+} – V_{T-}	Hysteresis INT_0–INT_2, ADT, $CNTR_0$, $CNTR_1$, $P2_0$–$P2_7$			0.5		V
V_{T+} – V_{T-}	Hysteresis S_{CLK}, R_XD, S_{IN2}			0.5		V
V_{T+} – V_{T-}	Hysteresis $\overline{RESET}$			0.5		V
I_{IH}	"H" input current $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P4_0$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$, $P7_0$–$P7_7$	V_I = V_{CC}			5.0	µA
I_{IH}	"H" input current $\overline{RESET}$	V_I = V_{CC}			5.0	µA
I_{IH}	"H" input current X_{IN}	V_I = V_{CC}		4.0		µA
I_{IL}	"L" input current $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P4_1$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$	V_I = V_{SS} Pull-ups "off"			–5.0	µA
		V_{CC} = 5 V, V_I = V_{SS} Pull-ups "on"	–60.0	–120.0	–240.0	µA
		V_{CC} = 2.2 V, V_I = V_{SS} Pull-ups "on"	–5.0	–20.0	–40.0	µA
I_{IL}	"L" input current $P4_0$, $P7_0$–$P7_7$				–5.0	µA
I_{IL}	"L" input current $\overline{RESET}$	V_I = V_{SS}			–5.0	µA
I_{IL}	"L" input current X_{IN}	V_I = V_{SS}		–4.0		µA
I_{LOAD}	Output load current $P3_0$–$P3_7$	V_{CC} = 5.0 V, V_O = V_{CC}, Pullup ON Output transistors "off"	–60.0	–120.0	–240.0	µA
		V_{CC} = 2.2 V, V_O = V_{CC}, Pullup ON Output transistors "off"	–5.0	–20.0	–40.0	µA
I_{LEAK}	Output leak current $P3_0$–$P3_7$	V_O = V_{CC}, Pullup OFF Output transistors "off"			5.0	µA
		V_O = V_{SS}, Pullup OFF Output transistors "off"			–5.0	µA

Table 19 Electrical characteristics (2) (V_{CC} =2.2 to 5.5 V, Ta = –20 to 85°C, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			Unit
				Min.	Typ.	Max.	
V_{RAM}	RAM retention voltage	At clock stop mode		2.0		5.5	V
I_{CC}	Power source current	• High-speed mode, V_{CC} = 5 V $f(X_{IN})$ = 8 MHz $f(X_{CIN})$ = 32.768 kHz Output transistors “off” A-D converter in operating			8.0	15	mA
		• High-speed mode, V_{CC} = 5 V $f(X_{IN})$ = 8 MHz (in WIT state) $f(X_{CIN})$ = 32.768 kHz Output transistors “off” A-D converter stop			2.5	4.0	mA
		• Low-speed mode, V_{CC} = 5 V, Ta ≤ 55°C $f(X_{IN})$ = stopped $f(X_{CIN})$ = 32.768 kHz Output transistors “off”			45	67	µA
		• Low-speed mode, V_{CC} = 5 V, Ta = 25°C $f(X_{IN})$ = stopped $f(X_{CIN})$ = 32.768 kHz (in WIT state) Output transistors “off”			23	46	µA
		• Low-speed mode, V_{CC} = 3 V, Ta ≤ 55°C $f(X_{IN})$ = stopped $f(X_{CIN})$ = 32.768 kHz Output transistors “off”			18	36	µA
		• Low-speed mode, V_{CC} = 3 V, Ta = 25°C $f(X_{IN})$ = stopped $f(X_{CIN})$ = 32.768 kHz (in WIT state) Output transistors “off”			8	16	µA
		All oscillation stopped (in STP state) Output transistors “off”	Ta = 25 °C		0.1	1.0	µA
			Ta = 85 °C			10	
V_{L1}	Power source voltage	When using voltage multiplier		1.3	1.8	2.1	V
I_{L1}	Power source current (V_{L1}) **(Note)**	V_{L1} = 1.8 V			4.0		µA

Note: When the voltage multiplier control bit of the LCD mode register (bit 4 at address 0039_{16}) is “1”.

Table 20 A-D converter characteristics
(V_{CC} = 2.7 to 5.5 V, V_{SS} = AV_{SS} = 0 V, Ta = –20 to 85°C, f(X_{IN}) = 500 kHz to 8 MHz, in middle/high-speed mode unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
–	Resolution				8	Bits
–	Absolute accuracy (excluding quantization error)	V_{CC} = V_{REF} = 5 V			±2	LSB
t_{CONV}	Conversion time	f(X_{IN}) = 8 MHz			12.5 **(Note)**	µs
R_{LADDER}	Ladder resistor		12	35	100	kΩ
I_{VREF}	Reference power source input current	V_{REF} = 5 V	50	150	200	µA
I_{IA}	Analog port input current				5.0	µA

Note: When an internal trigger is used in middle-speed mode, it is 14 µs.

Table 21 D-A converter characteristics
(V_{CC} = 2.7 to 5.5 V, V_{CC} = V_{REF}, V_{SS} = AV_{SS} = 0 V, Ta = –20 to 85°C, in middle/high-speed mode unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
–	Resolution				8	Bits
–	Absolute accuracy	V_{CC} = V_{REF} = 5 V			1.0	%
		V_{CC} = V_{REF} = 2.7 V			2.0	%
t_{su}	Setting time			3		µs
R_O	Output resistor		1	2.5	4	kΩ
I_{VREF}	Reference power source input current	**(Note)**			3.2	mA

Note: Using one D-A converter, with the value in the D-A conversion register of the other D-A converter being "00_{16}", and excluding currents flowing through the A-D resistance ladder.

Table 22 Timing requirements 1 (V_{CC} = 4.0 to 5.5 V, V_{SS} = 0 V, Ta = –20 to 85°C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$t_{w(\overline{RESET})}$	Reset input “L” pulse width	2			µs
$t_{c(X_{IN})}$	Main clock input cycle time (X_{IN} input)	125			ns
$t_{wH(X_{IN})}$	Main clock input “H” pulse width	45			ns
$t_{wL(X_{IN})}$	Main clock input “L” pulse width	40			ns
$t_{c(CNTR)}$	$CNTR_0$, $CNTR_1$ input cycle time	250			ns
$t_{wH(CNTR)}$	$CNTR_0$, $CNTR_1$ input “H” pulse width	105			ns
$t_{wL(CNTR)}$	$CNTR_0$, $CNTR_1$ input “L” pulse width	105			ns
$t_{wH(INT)}$	INT_0 to INT_2 input “H” pulse width	80			ns
$t_{wL(INT)}$	INT_0 to INT_2 input “L” pulse width	80			ns
$t_{c(S_{CLK1})}$	Serial I/O1 clock input cycle time **(Note)**	800			ns
$t_{wH(S_{CLK1})}$	Serial I/O1 clock input “H” pulse width **(Note)**	370			ns
$t_{wL(S_{CLK1})}$	Serial I/O1 clock input “L” pulse width **(Note)**	370			ns
$t_{su(R_XD-S_{CLK1})}$	Serial I/O1 input set up time	220			ns
$t_{h(S_{CLK1}-R_XD)}$	Serial I/O1 input hold time	100			ns
$t_{c(S_{CLK2})}$	Serial I/O2 clock input cycle time **(Note)**	1000			ns
$t_{wH(S_{CLK2})}$	Serial I/O2 clock input “H” pulse width **(Note)**	400			ns
$t_{wL(S_{CLK2})}$	Serial I/O2 clock input “L” pulse width **(Note)**	400			ns
$t_{su(S_{IN2}-S_{CLK2})}$	Serial I/O2 input set up time	200			ns
$t_{h(S_{CLK2}-S_{IN2})}$	Serial I/O2 input hold time	200			ns

Note: When bit 6 of address $001A_{16}$ is “1”.
Divide this value by four when bit 6 of address $001A_{16}$ is “0”.

Table 23 Timing requirements 2 (V_{CC} = 2.2 to 4.0 V, V_{SS} = 0 V, Ta = –20 to 85°C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$t_{w(\overline{RESET})}$	Reset input “L” pulse width	2			µs
$t_{c(X_{IN})}$	Main clock input cycle time (X_{IN} input)	125			ns
$t_{wH(X_{IN})}$	Main clock input “H” pulse width	45			ns
$t_{wL(X_{IN})}$	Main clock input “L” pulse width	40			ns
$t_{c(CNTR)}$	$CNTR_0$, $CNTR_1$ input cycle time	900/(V_{CC}+0.4)			ns
$t_{wH(CNTR)}$	$CNTR_0$, $CNTR_1$ input “H” pulse width	$t_{c(CNTR)}$/2–20			ns
$t_{wL(CNTR)}$	$CNTR_0$, $CNTR_1$ input “L” pulse width	$t_{c(CNTR)}$/2–20			ns
$t_{wH(INT)}$	INT_0 to INT_2 input “H” pulse width	230			ns
$t_{wL(INT)}$	INT_0 to INT_2 input “L” pulse width	230			ns
$t_{c(S_{CLK1})}$	Serial I/O1 clock input cycle time **(Note)**	2000			ns
$t_{wH(S_{CLK1})}$	Serial I/O1 clock input “H” pulse width **(Note)**	950			ns
$t_{wL(S_{CLK1})}$	Serial I/O1 clock input “L” pulse width **(Note)**	950			ns
$t_{su(R_XD-S_{CLK1})}$	Serial I/O1 input set up time	400			ns
$t_{h(S_{CLK1}-R_XD)}$	Serial I/O1 input hold time	200			ns
$t_{c(S_{CLK2})}$	Serial I/O2 clock input cycle time **(Note)**	2000			ns
$t_{wH(S_{CLK2})}$	Serial I/O2 clock input “H” pulse width **(Note)**	950			ns
$t_{wL(S_{CLK2})}$	Serial I/O2 clock input “L” pulse width **(Note)**	950			ns
$t_{su(S_{IN2}-S_{CLK2})}$	Serial I/O2 input set up time	400			ns
$t_{h(S_{CLK2}-S_{IN2})}$	Serial I/O2 input hold time	300			ns

Note: When bit 6 of address $001A_{16}$ is “1”.
Divide this value by four when bit 6 of address $001A_{16}$ is “0”.

Table 24 Switching characteristics 1 (VCC = 4.0 to 5.5 V, VSS = 0 V, Ta = –20 to 85°C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$t_{WH}(S_{CLK1})$	Serial I/O1 clock output "H" pulse width	$t_C(S_{CLK1})/2–30$			ns
$t_{WL}(S_{CLK1})$	Serial I/O1 clock output "L" pulse width	$t_C(S_{CLK1})/2–30$			ns
$t_d(S_{CLK1}–T_XD)$	Serial I/O1 output delay time **(Note 1)**			140	ns
$t_v(S_{CLK1}–T_XD)$	Serial I/O1 output valid time **(Note 1)**	–30			ns
$t_r(S_{CLK1})$	Serial I/O1 clock output rising time			30	ns
$t_f(S_{CLK1})$	Serial I/O1 clock output falling time			30	ns
$t_{WH}(S_{CLK2})$	Serial I/O2 clock output "H" pulse width	$t_C(S_{CLK2})/2–160$			ns
$t_{WL}(S_{CLK2})$	Serial I/O2 clock output "L" pulse width	$t_C(S_{CLK2})/2–160$			ns
$t_d(S_{CLK2}–S_{OUT2})$	Serial I/O2 output delay time			$0.2 \times t_C(S_{CLK2})$	ns
$t_v(S_{CLK2}–S_{OUT2})$	Serial I/O2 output valid time	0			ns
$t_f(S_{CLK2})$	Serial I/O2 clock output falling time			40	ns
$t_r(CMOS)$	CMOS output rising time **(Note 2)**		10	30	ns
$t_f(CMOS)$	CMOS output falling time **(Note 2)**		10	30	ns

Notes1: When the P4₅/TxD P-channel output disable bit of the UART control register (bit 4 of address $001B_{16}$) is "0".
2: XOUT and XCOUT pins are excluded.

Table 25 Switching characteristics 2 (VCC = 2.2 to 4.0 V, VSS = 0 V, Ta = –20 to 85°C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$t_{WH}(S_{CLK1})$	Serial I/O1 clock output "H" pulse width	$t_C(S_{CLK1})/2–50$			ns
$t_{WL}(S_{CLK1})$	Serial I/O1 clock output "L" pulse width	$t_C(S_{CLK1})/2–50$			ns
$t_d(S_{CLK1}–T_XD)$	Serial I/O1 output delay time **(Note 1)**			350	ns
$t_v(S_{CLK1}–T_XD)$	Serial I/O1 output valid time **(Note 1)**	–30			ns
$t_r(S_{CLK1})$	Serial I/O1 clock output rising time			50	ns
$t_f(S_{CLK1})$	Serial I/O1 clock output falling time			50	ns
$t_{WH}(S_{CLK2})$	Serial I/O2 clock output "H" pulse width	$t_C(S_{CLK2})/2–240$			ns
$t_{WL}(S_{CLK2})$	Serial I/O2 clock output "L" pulse width	$t_C(S_{CLK2})/2–240$			ns
$t_d(S_{CLK2}–S_{OUT2})$	Serial I/O2 output delay time			$0.2 \times t_C(S_{CLK2})$	ns
$t_v(S_{CLK2}–S_{OUT2})$	Serial I/O2 output valid time	0			ns
$t_f(S_{CLK2})$	Serial I/O2 clock output falling time			50	ns
$t_r(CMOS)$	CMOS output rising time **(Note 2)**		20	50	ns
$t_f(CMOS)$	CMOS output falling time **(Note 2)**		20	50	ns

Notes1: When the $P4_5/T_XD$ P-channel output disable bit of the UART control register (bit 4 of address $001B_{16}$) is "0".
2: XOUT and XCOUT pins are excluded.

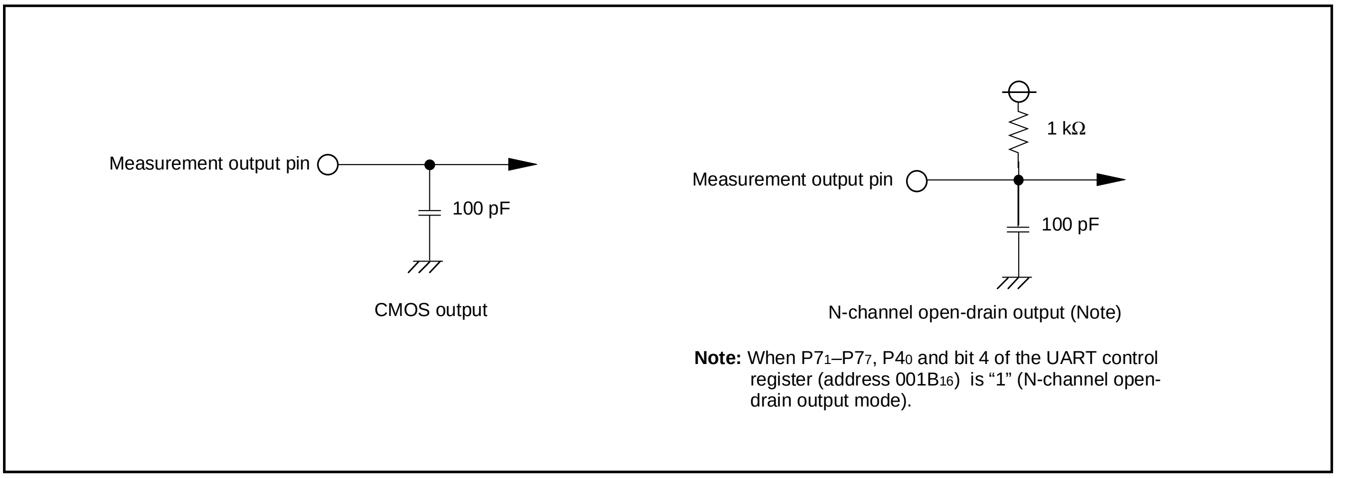


Fig. 56 Circuit for measuring output switching characteristics

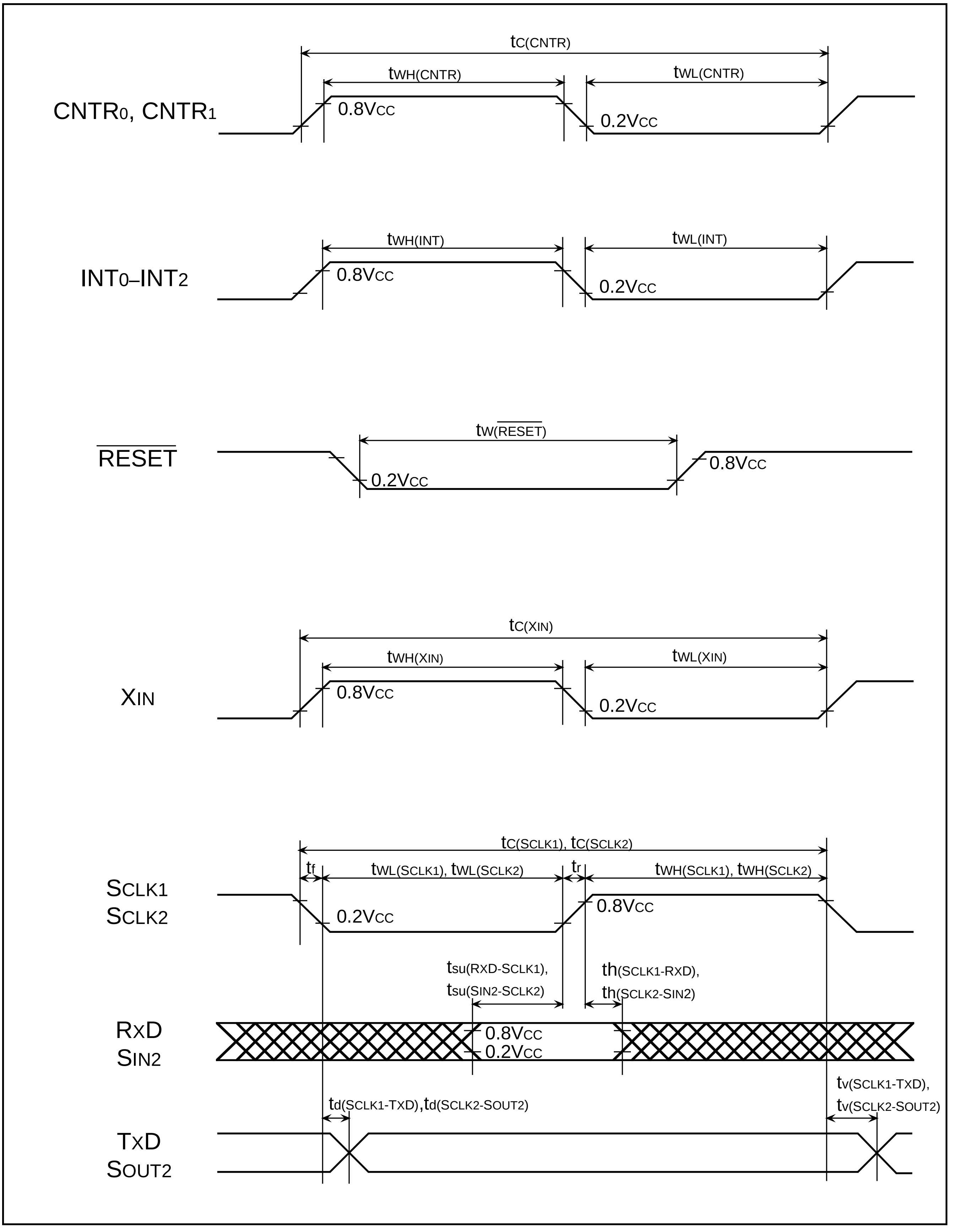


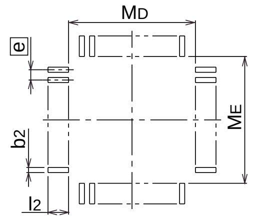
Fig. 57 Timing diagram

PACKAGE OUTLINE

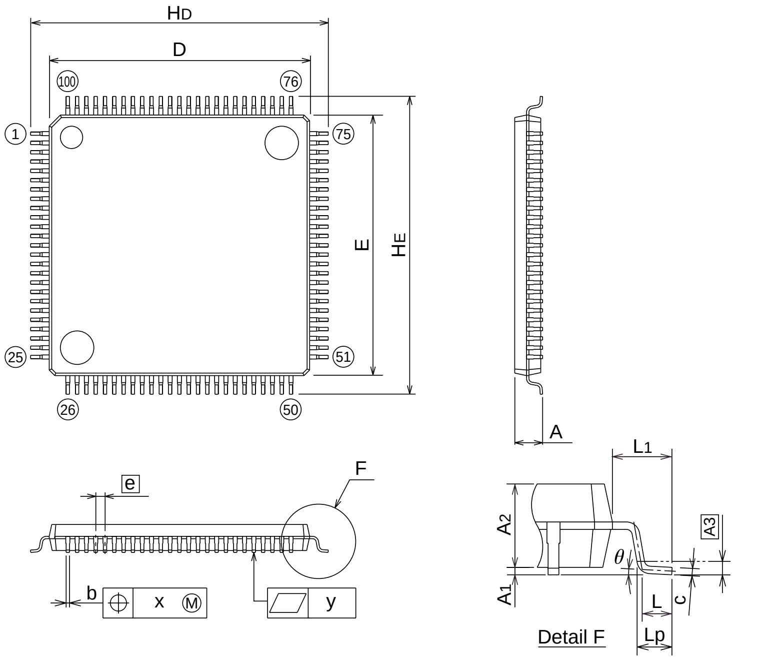
100P6Q-A (MMP)

Plastic 100pin 14X14mm body LQFP

EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
LQFP100-P-1414-0.50	–	0.63	Cu Alloy



Recommended Mount Pad

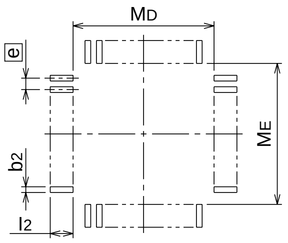


Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	–	–	1.7
A_1	0	0.1	0.2
A_2	–	1.4	–
b	0.13	0.18	0.28
c	0.105	0.125	0.175
D	13.9	14.0	14.1
E	13.9	14.0	14.1
e	–	0.5	–
H_D	15.8	16.0	16.2
H_E	15.8	16.0	16.2
L	0.3	0.5	0.7
L_1	–	1.0	–
Lp	0.45	0.6	0.75
A_3	–	0.25	–
x	–	–	0.08
y	–	–	0.1
θ	0°	–	10°
b_2	–	0.225	–
I_2	0.9	–	–
M_D	–	14.4	–
M_E	–	14.4	–

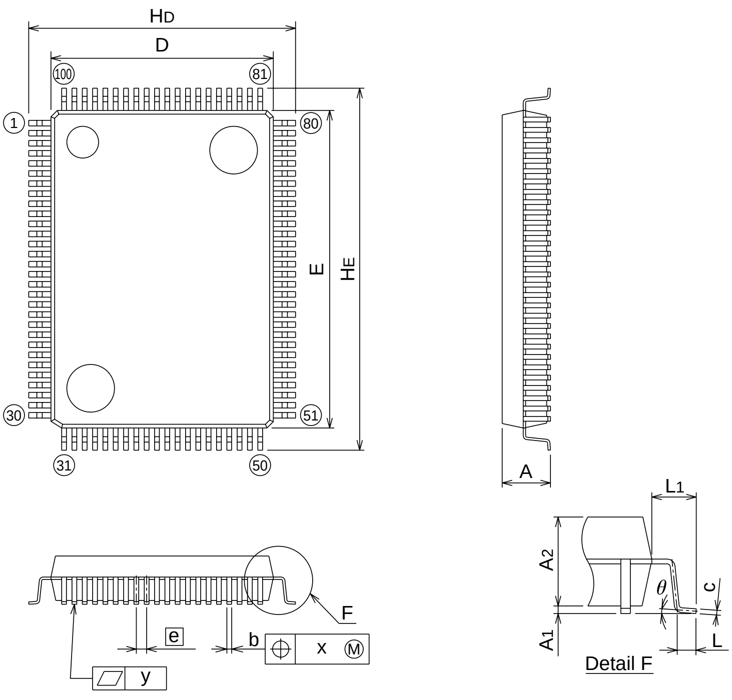
100P6S-A (MMP)

Plastic 100pin 14X20mm body QFP

EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
QFP100-P-1420-0.65	–	1.58	Alloy 42



Recommended Mount Pad



Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	–	–	3.05
A_1	0	0.1	0.2
A_2	–	2.8	–
b	0.25	0.3	0.4
c	0.13	0.15	0.2
D	13.8	14.0	14.2
E	19.8	20.0	20.2
e	–	0.65	–
H_D	16.5	16.8	17.1
H_E	22.5	22.8	23.1
L	0.4	0.6	0.8
L_1	–	1.4	–
x	–	–	0.13
y	–	–	0.1
θ	0°	–	10°
b_2	–	0.35	–
I_2	1.3	–	–
M_D	–	14.6	–
M_E	–	20.6	–

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REVISION HISTORY	7560 GROUP DATA SHEET

Rev.	Date	Description	
		Page	Summary
1.0	03/28/01		First Edition
1.1	06/08/01	52	Table 13 V_{REF} Min. V_{CC}+0.3 → V_{CC}