

# SONY® CXK581000P/M -10L/12L/15L -10LL/12LL/15LL

131072-word × 8-bit High Speed CMOS Static RAM

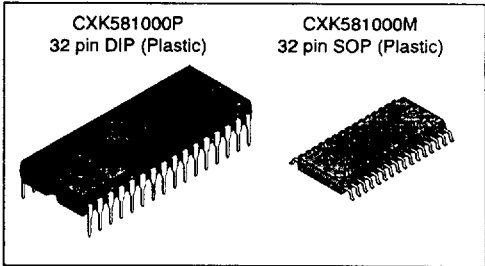
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### Description

CXK581000P/M is a general purpose high speed CMOS static RAM organized as 131, 072 words by 8 bits. Operating on a single 5V supply, this asynchronous IC is suitable for high speed and low power consumption applications where battery back up for nonvolatility is required.

### Features

- Fast access time : (Access time)  
 CXK581000P/M-10L/10LL 100ns (Max.)  
 CXK581000P/M-12L/12LL 120ns (Max.)  
 CXK581000P/M-15L/15LL 150ns (Max.)
- Low power consumption operation :  
 Standby /DC operation  
 CXK581000P/M-10L, 12L, 15L ; 10 μW (Typ.) /35mW (Typ.)  
 10LL, 12LL, 15LL ; 3.5 μW (Typ.) /35mW (Typ.)
- Single +5V supply : +5V ± 10%
- Fully static memory ... No clock or timing strobe required.
- Equal access and cycle time.
- Common data input and output:three state output.
- Directly TTL compatible : All inputs and outputs.
- Low voltage data retention : 2.0V (Min.)
- CXK581000P 600mil 32 pin DIP package  
 CXK581000M 525mil 32 pin SOP package



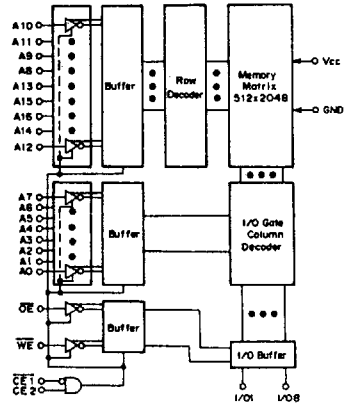
### Functions

131,072 word × 8 bit static RAM

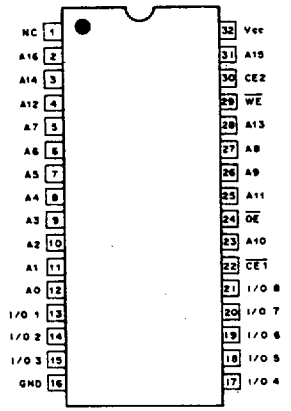
### Structure

Silicon gate CMOS IC

### Block Diagram



### Pin Configuration (Top View)



### Pin Description

Symbol	Description
A0 to A16	Address input
I/O 1 to I/O 8	Data input output
CE1, CE2	Chip enable 1, 2 input
WE	Write enable input
OE	Output enable input
Vcc	Power supply
GND	Ground
NC	No connection

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## Absolute Maximum Ratings

(Ta=25°C, GND=0V)

Item	Symbol	Rating	Unit
Supply voltage	V <sub>CC</sub>	- 0.5 to +7.0	V
Input voltage	V <sub>IN</sub>	- 0.5 * to V <sub>CC</sub> +0.5	V
Input and output voltage	V <sub>IO</sub>	- 0.5 * to V <sub>CC</sub> +0.5	V
Allowable power dissipation	P <sub>D</sub>	CXK581000P	1.0
		CXK581000M	0.7
Operating temperature	T <sub>opr</sub>	0 to +70	°C
Storage temperature	T <sub>stg</sub>	- 55 to +150	°C
Soldering temperature	T <sub>solder</sub>	260*10	°C * sec

\* V<sub>IN</sub>, V<sub>IO</sub> = - 3.0V Min. for pulse width less than 50ns.

## Truth Table

CE1	CE2	OE	WE	Mode	I/O pin	V <sub>CC</sub> current
H	X	X	X	Not selected	High Z	I <sub>SB1</sub> , I <sub>SB2</sub>
X	L	X	X	Not selected	High Z	I <sub>SB1</sub> , I <sub>SB2</sub>
L	H	H	H	Output disable	High Z	I <sub>CC1</sub> , I <sub>CC2</sub> , I <sub>CC3</sub>
L	H	L	H	Read	Data out	I <sub>CC1</sub> , I <sub>CC2</sub> , I <sub>CC3</sub>
L	H	X	L	Write	Data in	I <sub>CC1</sub> , I <sub>CC2</sub> , I <sub>CC3</sub>

X : "H" or "L"

## DC Recommended Operating Conditions (Ta=0 to +70°C, GND=0V)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	V <sub>CC</sub>	4.5	5.0	5.5	V
Input high voltage	V <sub>IH</sub>	2.2	—	V <sub>CC</sub> +0.3	V
Input low voltage	V <sub>IL</sub>	- 0.3 *	—	0.8	V

\* V<sub>IL</sub> = - 3.0V Min. for pulse width less than 50ns.

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## Electrical Characteristics

## • DC characteristics

(V<sub>CC</sub>=5V ± 10%, GND=0V, T<sub>a</sub>=0 to +70 °C)

Item	Symbol	Test conditions	- 10L/12L/15L			- 10LL/12LL/15LL			Unit	
			Min.	Typ. *	Max.	Min.	Typ. *	Max.		
Input leakage current	I <sub>LI</sub>	V <sub>IN</sub> =GND to V <sub>CC</sub>	-1	—	1	-1	—	1	μA	
Output leakage current	I <sub>LO</sub>	CE1=V <sub>IH</sub> or CE2=V <sub>IL</sub> or OE=V <sub>IH</sub> or WE=V <sub>IL</sub> V <sub>I/O</sub> =GND to V <sub>CC</sub>	-1	—	1	-1	—	1	μA	
Operating power supply current	I <sub>CC1</sub>	CE1=V <sub>IL</sub> , CE2=V <sub>IH</sub> V <sub>IN</sub> =V <sub>IH</sub> or V <sub>IL</sub> I <sub>OUT</sub> =0mA	—	7	15	—	7	15	mA	
Average operating current	I <sub>CC2</sub>	Min. cycle Duty=100% I <sub>OUT</sub> =0mA	Write cycle	—	35	60	—	35	60	mA
			Read cycle	—	25	40	—	25	40	
	I <sub>CC3</sub>	Cycle time 1 μs Duty=100% I <sub>OUT</sub> =0mA CE1 ≤ 0.2V, CE2 ≥ V <sub>CC</sub> - 0.2V V <sub>IL</sub> ≤ 0.2V, V <sub>IH</sub> ≥ V <sub>CC</sub> - 0.2V	Write cycle	—	10	20	—	10	20	mA
			Read cycle	—	5	10	—	5	10	
Standby current	I <sub>SB1</sub>	CE2 ≤ 0.2V or CE1 ≥ V <sub>CC</sub> - 0.2V or CE2 ≥ V <sub>CC</sub> - 0.2V	0 to 70 °C	—	—	100	—	—	20	μA
			0 to 40 °C	—	—	20	—	—	4	
			+25 °C	—	2	8	—	0.7	2	
	I <sub>SB2</sub>	CE1=V <sub>IH</sub> or CE2=V <sub>IL</sub>	—	0.6	3	—	0.6	3	mA	
Output high voltage	V <sub>OH</sub>	I <sub>OH</sub> = -1.0mA	2.4	—	—	2.4	—	—	V	
Output low voltage	V <sub>OL</sub>	I <sub>OL</sub> =2.1mA	—	—	0.4	—	—	0.4	V	

\* V<sub>CC</sub>=5V, T<sub>a</sub>=25 °C

## I/O capacitance

(T<sub>a</sub>=25 °C, f=1MHz)

Item	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Input capacitance	C <sub>IN</sub>	V <sub>IN</sub> =0V	—	—	6	pF
I/O capacitance	C <sub>I/O</sub>	V <sub>I/O</sub> =0V	—	—	8	pF

**Note)** This parameter is sampled and is not 100% tested.

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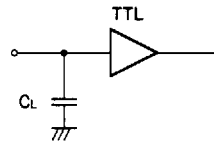
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**AC characteristics****• AC test conditions** ( $V_{CC}=5V \pm 10\%$ ,  $T_a=0$  to  $+70^\circ\text{C}$ )

Item	Conditions
Input pulse high level	$V_{IH}=2.2V$
Input pulse low level	$V_{IL}=0.8V$
Input rise time	$t_r=5ns$
Input fall time	$t_f=5ns$
Input and output reference level	1.5V
Output load conditions	$C_L^*=100pF$ , 1TTL

\*  $C_L$  includes scope and jig capacitances.**• Test circuit**

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• Read cycle ( $\overline{WE}="H"$ )

Item	Symbol	- 10L/10LL		- 12L/12LL		- 15L/15LL		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read cycle time	t <sub>RC</sub>	100	—	120	—	150	—	ns
Address access time	t <sub>AA</sub>	—	100	—	120	—	150	ns
Chip enable access time ( $\overline{CE1}$ )	t <sub>CO1</sub>	—	100	—	120	—	150	ns
Chip enable access time ( $\overline{CE2}$ )	t <sub>CO2</sub>	—	100	—	120	—	150	ns
Output enable to output valid	t <sub>OE</sub>	—	50	—	60	—	70	ns
Output hold from address change	t <sub>OH</sub>	15	—	15	—	15	—	ns
Chip enable to output in low Z ( $\overline{CE1}$ , $\overline{CE2}$ )	t <sub>LZ1</sub> , t <sub>LZ2</sub>	10	—	10	—	10	—	ns
Output enable to output in low Z ( $\overline{OE}$ )	t <sub>OLZ</sub>	5	—	5	—	5	—	ns
Chip disable to output in high Z ( $\overline{CE1}$ , $\overline{CE2}$ )	t <sub>HZ1</sub> *, t <sub>HZ2</sub> *	—	35	—	40	—	50	ns
Output disable to output in high Z ( $\overline{OE}$ )	t <sub>OHZ</sub> *	—	35	—	40	—	50	ns

\* t<sub>HZ1</sub>, t<sub>HZ2</sub> and t<sub>OHZ</sub> are defined as the time required for outputs to turn to high impedance state and are not referred to as output voltage levels.

## • Write cycle

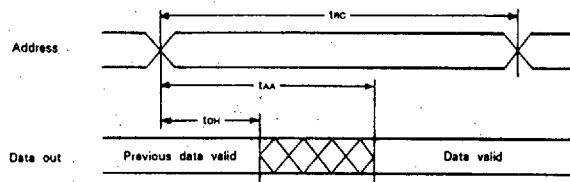
Item	Symbol	- 10L/10LL		- 12L/12LL		- 15L/15LL		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Write cycle time	t <sub>WC</sub>	100	—	120	—	150	—	ns
Address valid to end of write	t <sub>AW</sub>	70	—	85	—	100	—	ns
Chip enable to end of write	t <sub>CW</sub>	70	—	85	—	100	—	ns
Data to write time overlap	t <sub>DW</sub>	40	—	50	—	60	—	ns
Data hold from write time	t <sub>DH</sub>	0	—	0	—	0	—	ns
Write pulse width	t <sub>WP</sub>	70	—	80	—	90	—	ns
Address setup time	t <sub>AS</sub>	0	—	0	—	0	—	ns
Write recovery time ( $\overline{WE}$ )	t <sub>WR</sub>	0	—	0	—	0	—	ns
Write recovery time ( $\overline{CE1}$ , $\overline{CE2}$ )	t <sub>WR1</sub>	0	—	0	—	0	—	ns
Output active from end of write	t <sub>OW</sub>	10	—	10	—	10	—	ns
Write to output in high Z	t <sub>WHZ</sub> *	—	30	—	30	—	30	ns

\* t<sub>WHZ</sub> is defined as the time required for outputs to turn to high impedance state and is not referred to as output voltage level.

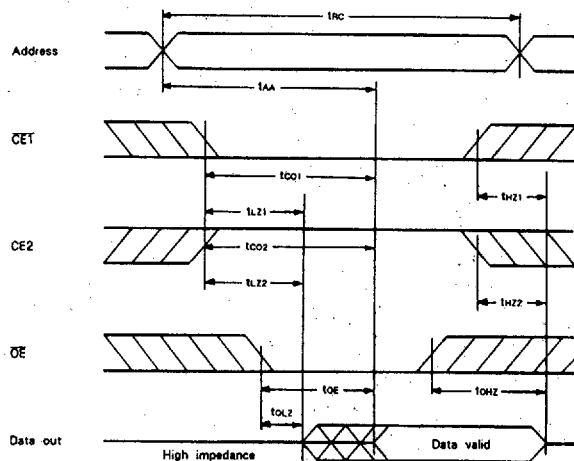
Timing Waveform

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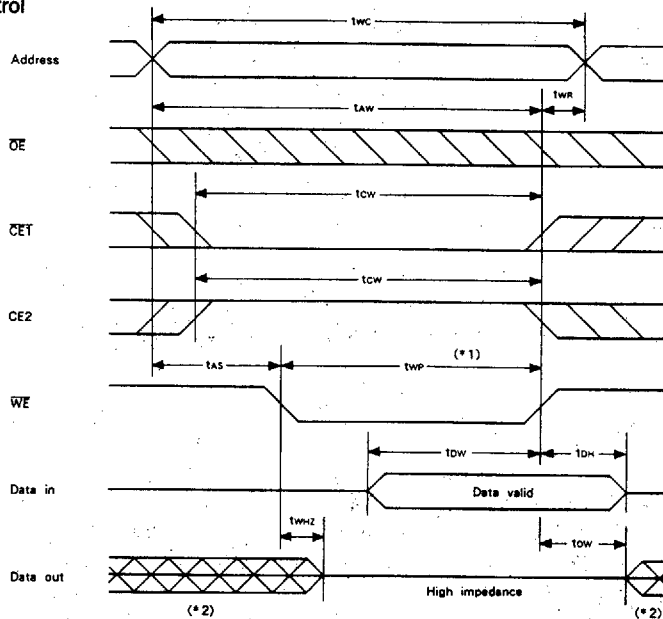
• Read cycle (1) :  $\overline{CE1}=\overline{OE}=V_{IL}$ ,  $CE2=V_{IH}$ ,  $\overline{WE}=V_{IH}$



• Read cycle (2) :  $\overline{WE}=V_{IH}$



• Write cycle (1) :  $\overline{WE}$  control



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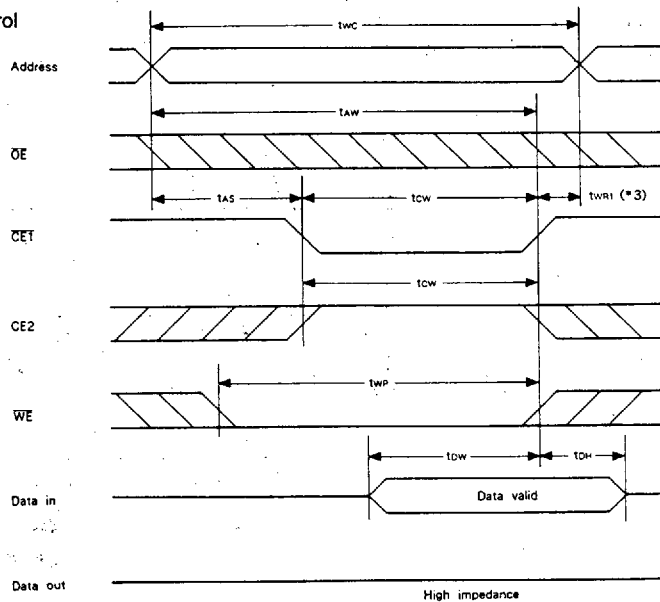
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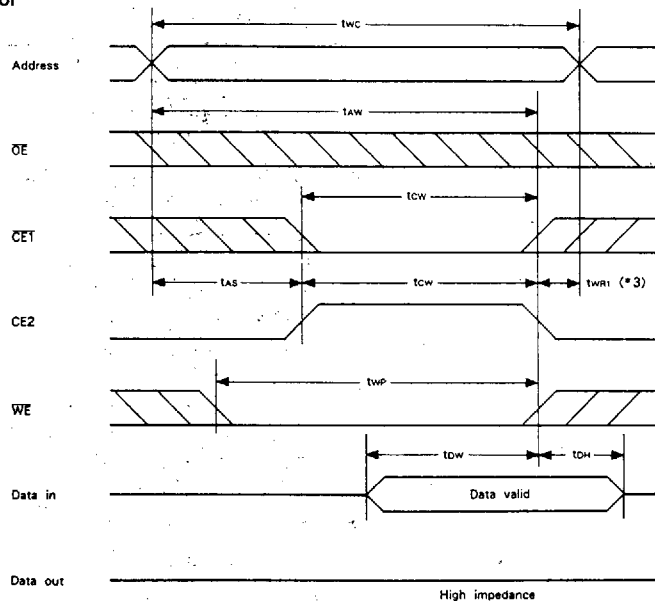
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• Write cycle (2) :  $\overline{CE1}$  control



• Write cycle (3) :  $\overline{CE2}$  control



**Note)**

- \*1. Write is executed when both  $\overline{CE1}$  and  $\overline{WE}$  are at low and  $\overline{CE2}$  is at high simultaneously.
- \*2. Do not apply the data input voltage of the opposite phase to the output while I/O pin is in output condition.
- \*3.  $t_{WR1}$  is tested from either the rising edge of  $\overline{CE1}$  or the falling edge of  $\overline{CE2}$ , whichever comes earlier, until the end of the write cycle.

Data Retention Characteristics

(Ta=0 to 70 °C)

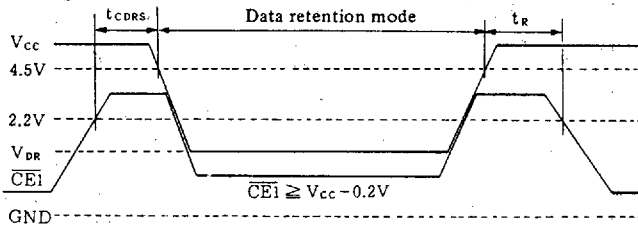
Item	Symbol	Test conditions	- 10L/12L/15L			- 10LL/12LL/15LL			Unit	
			Min.	Typ.	Max.	Min.	Typ.	Max.		
Data retention voltage	V <sub>DR</sub>	*1	2.0	—	5.5	2.0	—	5.5	V	
Data retention current	I <sub>CCDR1</sub>	V <sub>CC</sub> =3.0V *1	0 to 70 °C	—	—	50	—	—	12	μA
			0 to 40 °C	—	—	10	—	—	2.4	
			+25 °C	—	1	4	—	0.4	1.2	
	I <sub>CCDR2</sub>	V <sub>CC</sub> =2.0 to 5.5V *1	—	2	100	—	0.7	20	mA	
Data retention setup time	t <sub>CDRS</sub>	Chip disable to data retention mode	0	—	—	0	—	—	ns	
Recovery time	t <sub>R</sub>		t <sub>RC</sub> *2	—	—	t <sub>RC</sub> *2	—	—	ns	

Note)

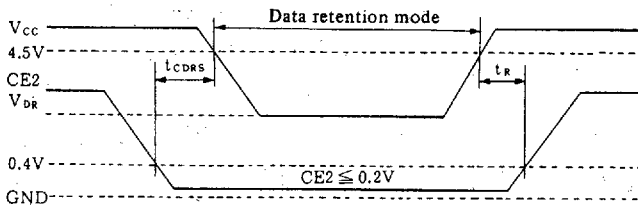
- \*1.  $\overline{CE1} \geq V_{CC} - 0.2V$ ,  $CE2 \geq V_{CC} - 0.2V$  ( $\overline{CE1}$  control) or  $CE2 \leq 0.2V$  ( $CE2$  control)
- \*2. t<sub>RC</sub> : Read cycle time

Data retention waveform

- Low supply voltage data retention waveform (1) ( $\overline{CE1}$  control)



- Low supply voltage data retention waveform (2) ( $CE2$  control)



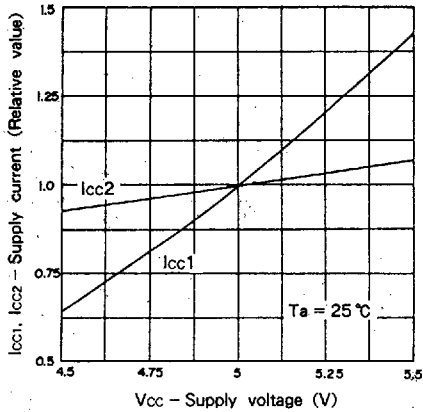
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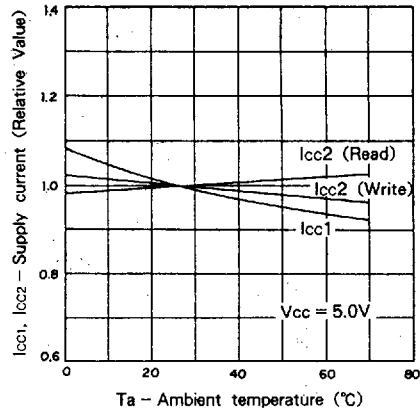
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Example of Representative Characteristics

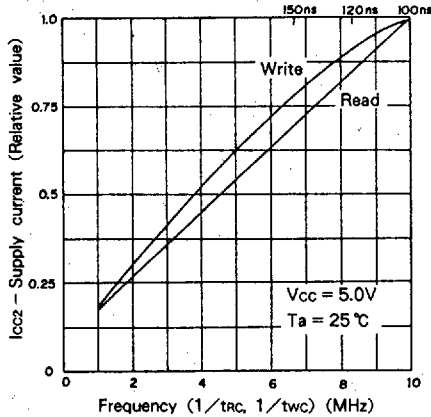
Supply current vs. Supply voltage



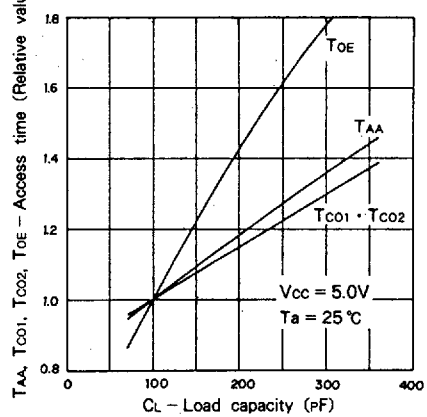
Supply current vs. Ambient temperature



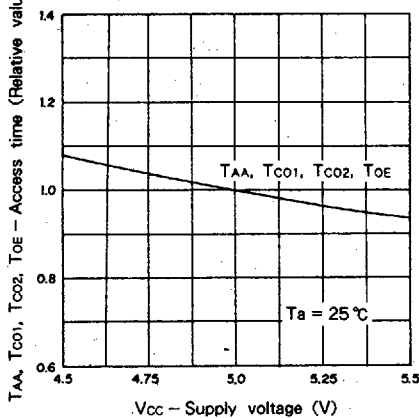
Supply current vs. Frequency



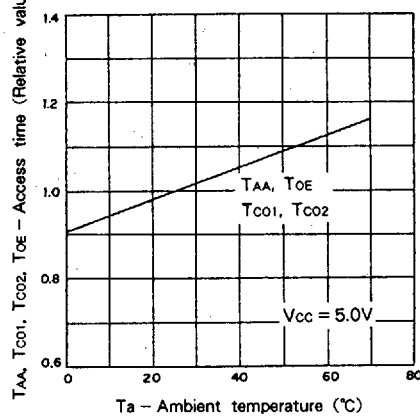
Access time vs. Load capacity



Access time vs. Supply voltage

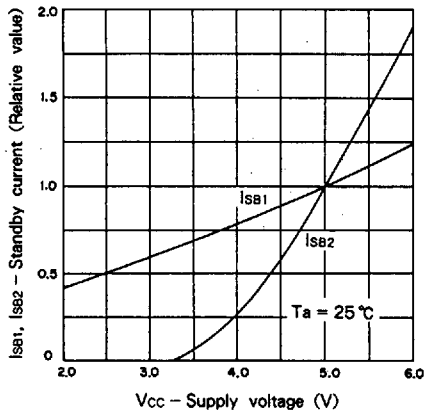


Access time vs. Ambient temperature

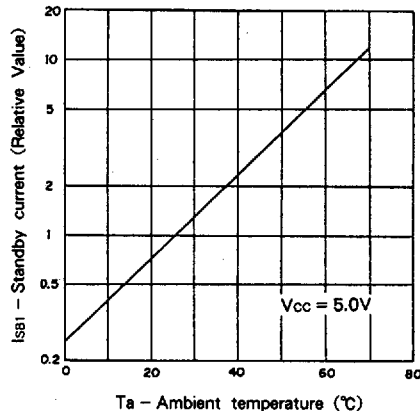


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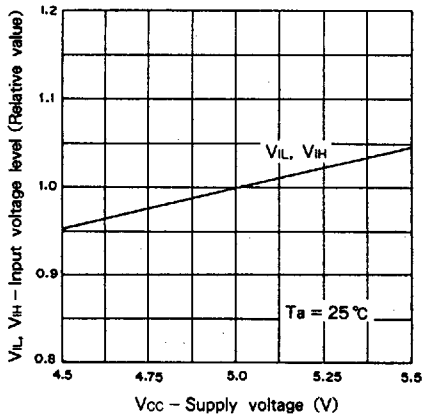
Standby current vs. Supply voltage



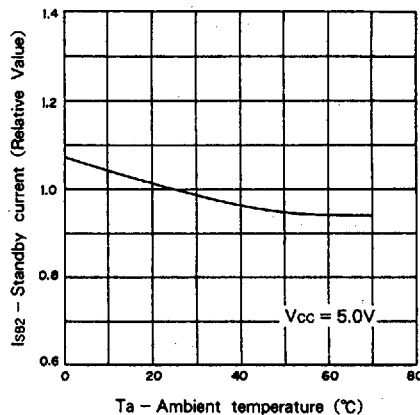
Standby current vs. Ambient temperature



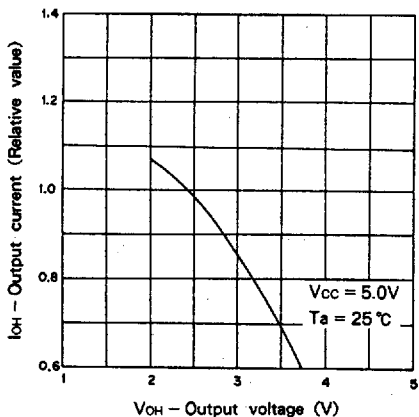
Input voltage level vs. Supply voltage



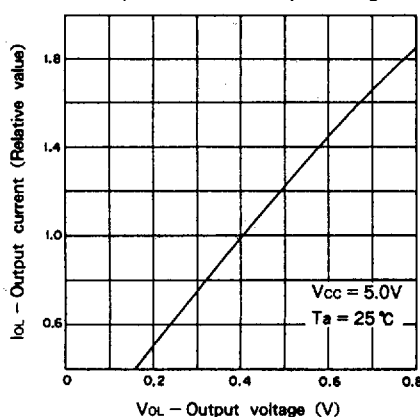
Standby current vs. Ambient temperature



Output current vs. Output voltage



Output current vs. Output voltage

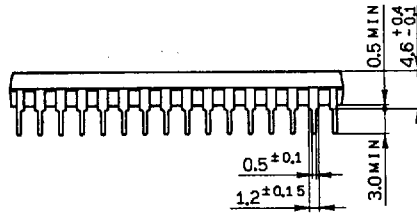
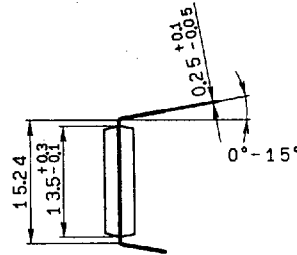
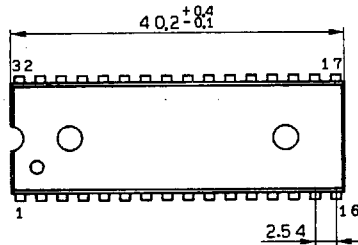


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Package Outline Unit : mm

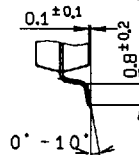
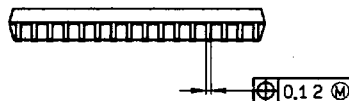
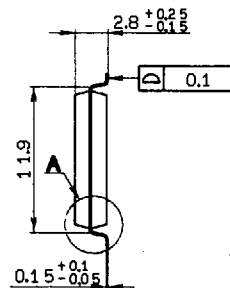
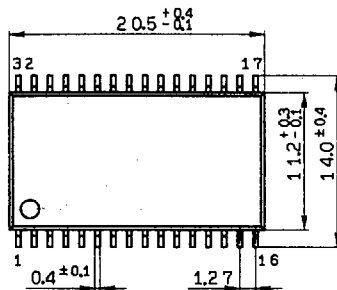
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CXK581000P 32Pin DIP (Plastic) 600mil 4.5g



SONY NAME	DIP-32P-01
EIAJ NAME	#DIP032-P-0600-A
JEDEC CODE	

CXK581000M 32Pin SOP (Plastic) 525mil 1.2g



Detailed diagram of A

SONY NAME	SOP-32P-L02
EIAJ NAME	#SOP032-P-0525-A
JEDEC CODE	