DATA SHEET

OQ2538HP; OQ2538U
SDH/SONET STM16/OC48 main amplifiers

Product specification
Supersedes data of 1998 Oct 14
File under Integrated Circuits, IC19

2000 Sep 29

Philips
Semiconductors

PHILIPS

SDH/SONET STM16/OC48 main amplifiers OQ2538HP; OQ2538U

FEATURES

- Differential 100 Ω outputs for direct connection to Current-Mode Logic (CML) inputs
- Wide bandwidth (3 GHz)
- 48.5 dB limiting gain
- Noise figure typically 11 dB
- Automatic offset compensation
- Input level-detection circuits for Automatic Gain Control (AGC) and Loss Of Signal (LOS) detection
- Low power dissipation (typically 270 mW)
- Single –4.5 V supply voltage
- Low cost LQFP48 plastic package.

APPLICATIONS

- Main amplifier in Synchronous Digital Hierarchy (SDH) and Synchronous Optical Network (SONET) systems for short, medium and long haul optical transmission
- Level detector for laser diode control loops
- Wideband RF gain block with internal level detectors.

GENERAL DESCRIPTION

The OQ2538HP is a limiting amplifier IC intended for use as the main amplifier in 2.5 Gbits/s Non-Return to Zero (NRZ) transmission systems (SDH/SONET).

Comprised of four amplifier stages with a total gain of 48.5 dB, it provides for a wide input signal dynamic range at a constant CML-compatible output level.

Two level-detection circuits are provided for monitoring AGC and LOS input signal levels. An internal automatic offset compensation circuit eliminates offset in the amplifier chain.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
OQ2538HP	LQFP48	plastic low profile quad flat package; 48 leads; body $7 \times 7 \times 1.4$ mm	SOT313-2
OQ2538U	–	bare die; dimensions $2070 \times 2070 \times 380$ μm	–

BLOCK DIAGRAM

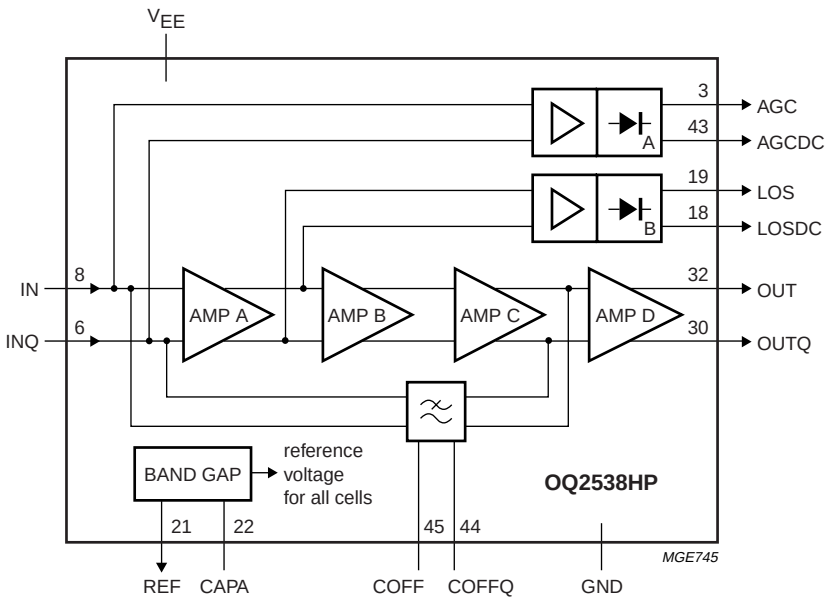


Fig.1 Block diagram.

PINNING

SYMBOL	PIN (OQ2538HP)	PAD (OQ2538U)	TYPE[1]	DESCRIPTION
V_{EE}	1, 12, 13, 24, 25, 36, 37, 48	2, 3, 11, 12, 28, 29[2]	S	negative power supply
n.c.	2, 11, 14, 15, 23, 26, 27, 35, 38, 40, 46, 47	20, 22[3]	–	not connected
AGC	3	30	O	rectifier A output
GND	4, 5, 7, 9, 10, 16, 17, 20, 28, 29, 31, 33, 34, 39, 41, 42	1, 4, 5, 8, 13, 14, 16, 18, 19, 21, 23, 24, 31, 32, 34, 36[2]	S	ground
INQ	6	33	I	main amplifier inverting input
IN	8	35	I	main amplifier input
LOSDC	18	6	O	rectifier B reference output
LOS	19	7	O	rectifier B output
REF	21	9	O	band gap reference
CAPA	22	10	A	pin for connecting band gap reference decoupling capacitor
OUTQ	30	15	O	main amplifier inverted output
OUT	32	17	O	main amplifier output
AGCDC	43	25	O	rectifier A reference output
COFFQ	44	26	A	pin for connecting automatic offset control capacitor (return)
COFF	45	27	A	pin for connecting automatic offset control capacitor

Notes

1. Pin type abbreviations: O = Output, I = Input, S = power Supply and A = Analog function.
2. **All** GND and V_{EE} pads must be bonded; **do not leave one single GND or V_{EE} pad unconnected!**
3. Pads denoted ‘n.c.’ should not be connected. Connections to these pads degrade device performance.

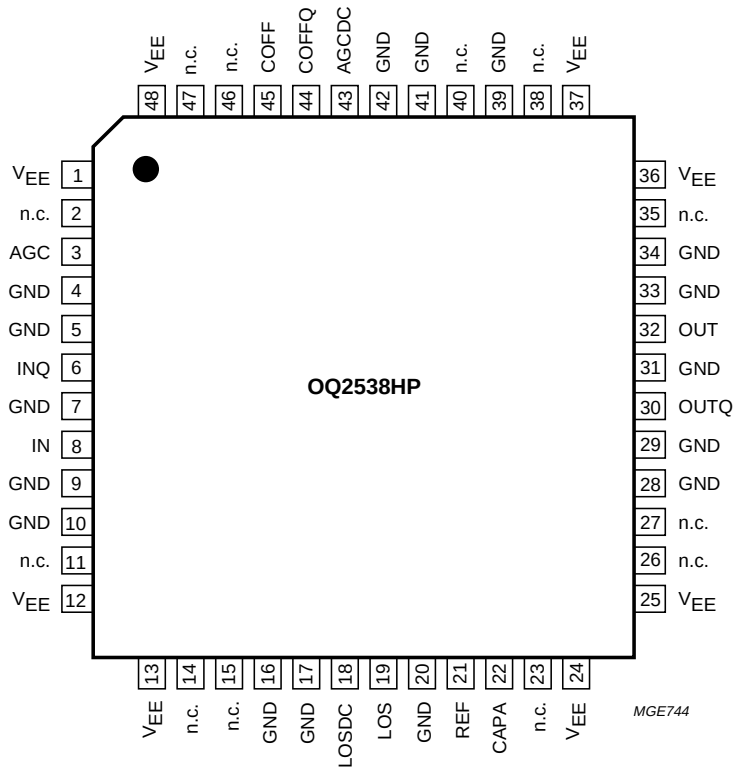


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The OQ2538HP is comprised of four DC-coupled amplifier stages along with additional circuitry for offset compensation and level detection.

The first amplifier stage contains a modified Cherry/Hooper amplifying cell with high gain (approximately 20 dB) and a wide bandwidth. Special attention is paid to minimizing the equivalent input noise at this stage, thus reducing the overall noise level. Additional feedback is applied at the second and third stages, improving isolation and reducing the gain to 14 dB per stage. The last stage is an output buffer, a unity gain amplifier, with an output impedance of 100 Ω.

The total gain of the OQ2538HP amounts to 48.5 dB, thus providing a constant CML-compatible output signal over a wide input signal range.

Two rectifier circuits are used to measure the input signal level. Two separate RF preamplifiers are used to generate the voltage gain needed to obtain a suitable rectifier output voltage. For rectifier A the gain is approximately 18 dB, for rectifier B it is about 14 dB. The output of rectifier A can be used for AGC at the preamplifier stage in front of the OQ2538HP. The output of rectifier B can be used for LOS detection. There is a linear relationship between the rectifier output voltage and the input signal level provided the amplifiers are not saturated.

Because the four gain stages are DC-coupled and provide a high overall gain, the effect of the input offset can be considerable. The OQ2538HP features an internal offset compensation circuit for eliminating the input offset. The bandwidth of the offset control loop is determined by an external capacitor.

COFF and COFFQ offset compensation

Automatic offset compensation eliminates the input offset of the OQ2538HP. This offset cancellation influences the low frequency gain of the amplifier stages. With a capacitance of 100 nF between COFF and COFFQ the loop bandwidth will be less than 1.5 kHz, small enough to have no influence on amplifier gain over the frequencies of interest. If the capacitor was omitted, the loop bandwidth would be greater than 30 MHz, which would influence the input signal gain. The loop bandwidth can be calculated from the following formula:

$$f_{loop} = \frac{1}{2\pi \times 1250\,\Omega \times C_{ext}} \quad (1)$$

where C_{ext} is the capacitance connected between COFF and COFFQ.

REF and CAPA band gap output and decoupling capacitance

To reduce band gap noise levels, a 1 nF decoupling capacitor on CAPA is recommended. Since the band gap is referenced to the negative power supply, the decoupling capacitor should be connected between CAPA and V_{EE}.

The band gap voltage is present on pin REF for test purposes only. It is not intended to serve as an external reference.

RF input and output connections

Striplines, or microstrips, with an odd mode characteristic impedance of $Z_{o(odd)}$ = 50 Ω must be used for the differential RF connections on the PCB. This applies to both the input signal pair IN and INQ and to the output signal pair OUT and OUTQ. The two lines in each pair should have the same length.

RF input matching circuit

The input circuit for pins IN and INQ contains internal 100 Ω resistors decoupled to ground via an internal common mode 6 pF capacitor. The topology is depicted in Fig.3.

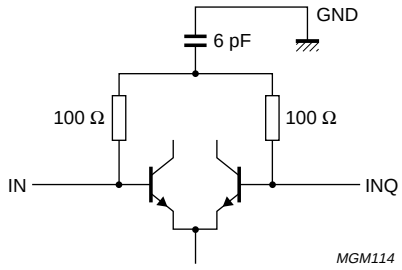


Fig.3 RF input topology.

An external 200 Ω resistor between IN and INQ is recommended in order to match the inputs to a differential transmission line, coupled microstrip or stripline with an odd mode impedance $Z_{o(odd)}$ = 50 Ω, as shown in Fig.4.

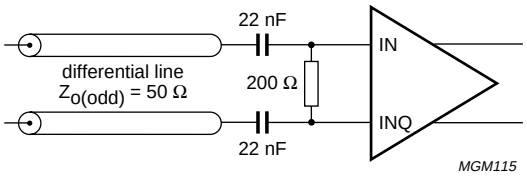


Fig.4 Differential input matching.

For single-ended excitation, separate matching networks on IN and INQ, as depicted in Fig.5, achieve optimum matching. Care should be taken to avoid DC loading, since the OQ2538HP controls its own DC input voltage.
The resistors on the unused input INQ may be combined for convenience.

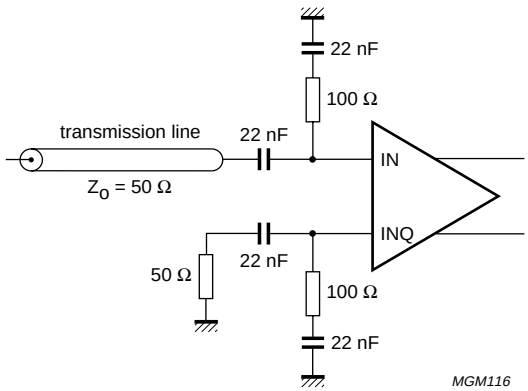


Fig.5 Single-ended input matching.

In both cases, the essence of good matching is the equity of the circuitry on both input pins. The impedance seen on pins IN and INQ should be as equal as possible. For more information see *"Application Note AN96051*" describing the OM5801 STM16 demo board.

RF output matching circuit

Matching of the main amplifier outputs, OUT and OUTQ, is not mandatory. In most applications, the receiving end of the transmission line will be properly matched, so very little reflection will occur. Matching the transmitting end to absorb these reflections is only recommended for very sensitive applications. In such cases, 100 Ω pull-up resistors should be connected from OUT and OUTQ to ground, as close as possible to the IC pins. These matching resistors will not be needed in most applications, however. The output circuit of the OQ2538HP is depicted in Fig.6. For more information see *"Application Note AN96051"* describing the OM5801 STM16 demo board.

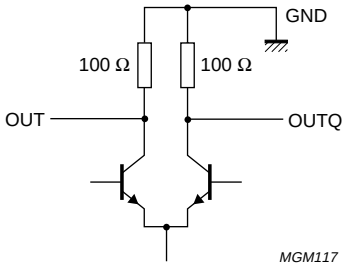


Fig.6 RF output topology.

RF gain and group delay measurements

The measurement set-up shown in Fig.7 was used to measure the single-ended small signal gain as specified in Chapter “Characteristics”. Since the network analyzer can only perform single-ended measurements, the single-ended matching scheme described above is used to match the inputs of the OQ2538HP to 50 Ω. For greater accuracy, the outputs are also matched. The gain measured with this set-up is denoted by S_{21}. Graphs of typical S_{21} and group delay characteristics are shown in Figs 8 and 9. The OQ2538HP test PCB used for these measurements can be supplied on request.

Although the differential voltage gain of the OQ2538HP cannot be measured directly, it can be calculated from S_{21}. The differential voltage gain is 6 dB greater than the measured S_{21} value, typically 46 dB (40 + 6 dB). If the 100 Ω matching resistors on the output are omitted, the differential voltage gain is increased by a further 2.4 dB, typically to 48.4 dB. This is due to the fact that the output load is increased from 25 to 33 Ω, so the output voltage is increased by a factor of 1.32 (2.4 dB).

When performing S_{21} measurements make sure the input power level is around −50 dBm, as indicated in Fig.7 (port 1 of the network analyzer). For correct measurement results the OQ2538 should not be limiting the input signal, but operate in its linear region. This can be achieved by using a very small input signal level of −50 dBm.

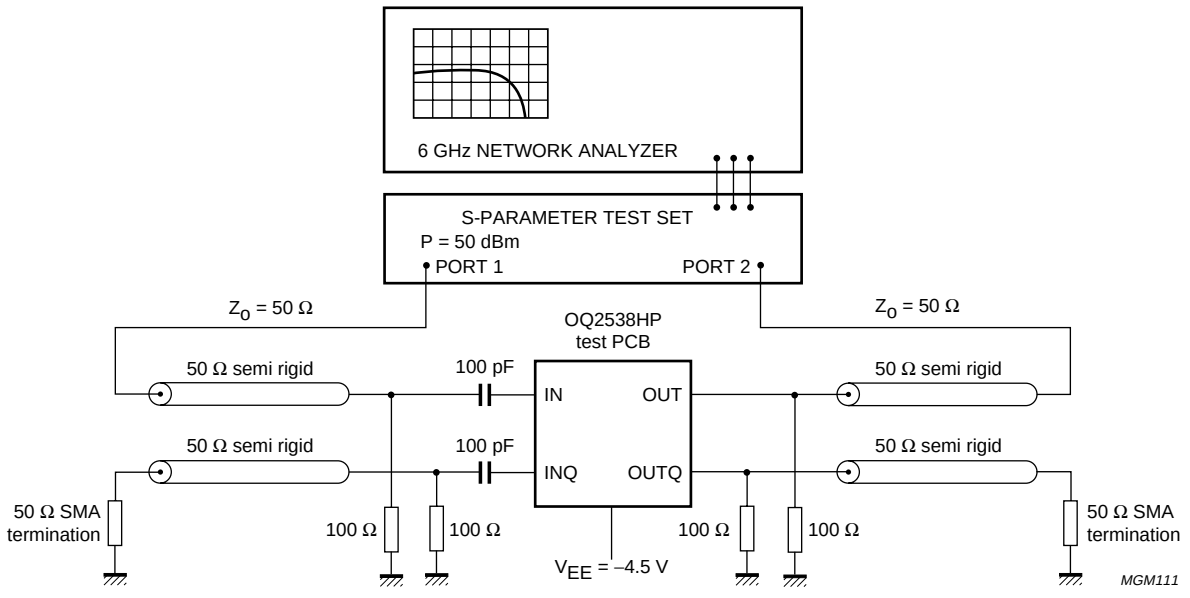
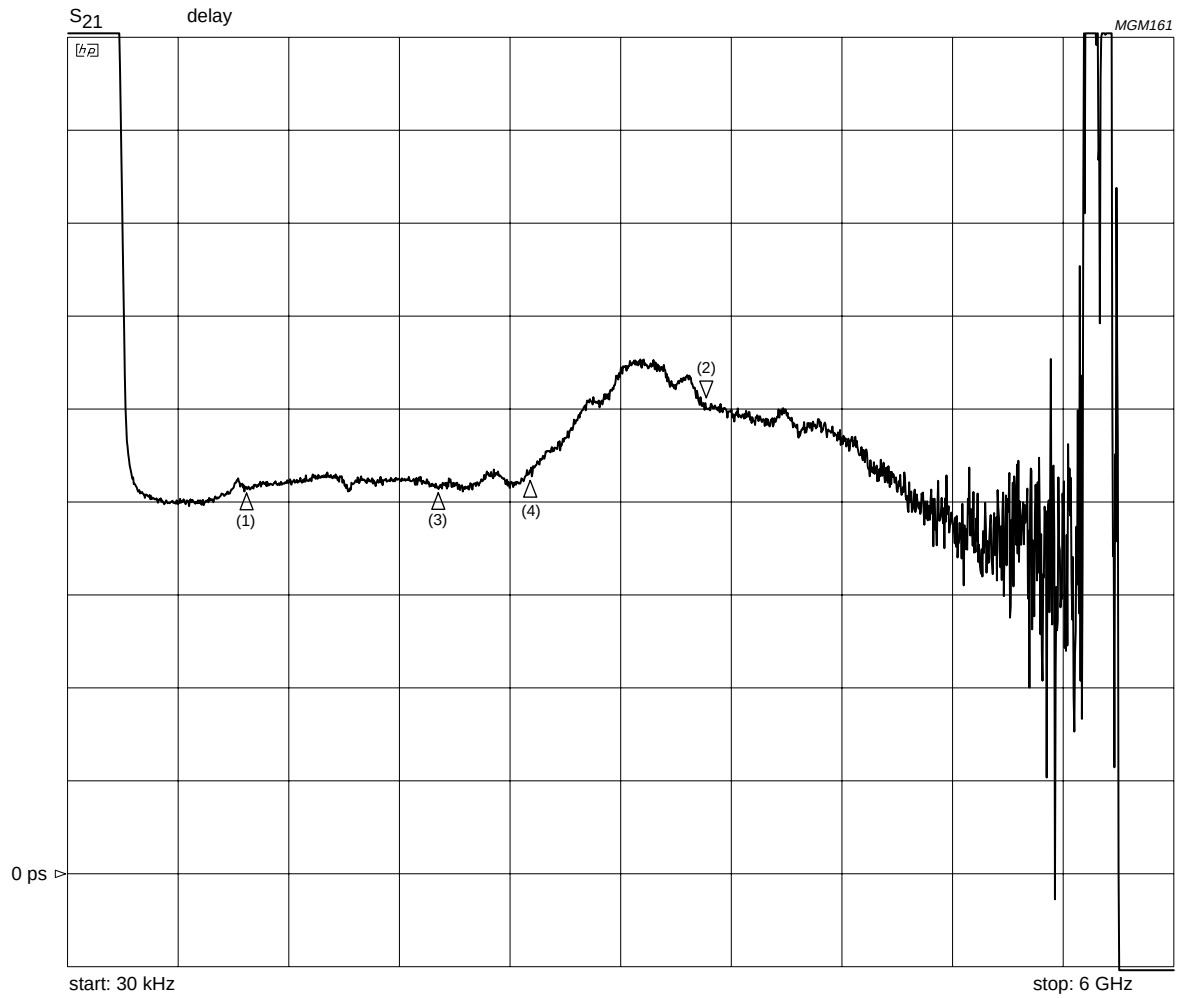


Fig.7 S_{21} and group delay measurement set-up.

Vertical scale 6 dB/division.
Linear frequency sweep; start: 30 kHz; stop: 6 GHz.
(1) 41.603 dB; 1 GHz.
(2) 38.633 dB; 3.45 GHz.
(3) 41.291 dB; 2 GHz.
(4) 41.386 dB; 2.5 GHz.

Fig.8 S_{21} characteristic, measured on the OQ2538HP test PCB.



Vertical scale 200 ps/division.
Linear frequency sweep; start: 30 kHz; stop: 6 GHz.
(1) 832.91 ps; 1 GHz.
(2) 1007.4 ps; 3.45 GHz.
(3) 834 ps; 2 GHz.
(4) 860.93 ps; 2.5 GHz.

Fig.9 Group delay characteristic, measured on the OQ2538HP test PCB.

Noise figure measurements

The noise figure is the ratio of signal-to-noise ratio at the input (S_i/N_i) to signal-to-noise ratio at the output (S_o/N_o) of the amplifier. This definition is true for both single-ended and differential amplifiers, provided the correct values for S_i/N_i and S_o/N_o are substituted in the formula. The noise figure is measured using the differential set-up shown in Fig.10. The total noise on the output (N_o in dBm) is measured using the spectrum analyzer at the frequency of interest. From this value, the actual (differential) noise figure for that frequency (spot noise figure) can be calculated using the following formula:

$$F = \frac{S_i/N_i}{S_o/N_o} = \frac{N_o}{2 \cdot S_{21} \cdot N_i} = \frac{N_o}{2 \cdot S_{21} \cdot kT}$$

The factor 2 in the denominator is present to compensate for the fact that S_{21} is the single-ended power gain, whereas the differential power gain is applicable in this situation. N_i can be replaced with the available noise power at the input, which is kT under matched conditions (k is Boltzmann's constant). The formula expressed in dBm makes calculation easier:

$$F = N_o - (S_{21} + 3) + 173.8 \quad [dB],$$

assuming log(kT) is –173.8 dBm (T = 298 K) and N_o measured in 1 Hz bandwidth and expressed in dBm. For the OQ2538HP, in the differential configuration (including the 100 Ω matching resistors), this yields a typical noise figure of 11 dB.

While the performance of this measurement set-up cannot match that of a dedicated noise analysis system, the results are comparable for an amplifier with a noise figure of 11 dB.

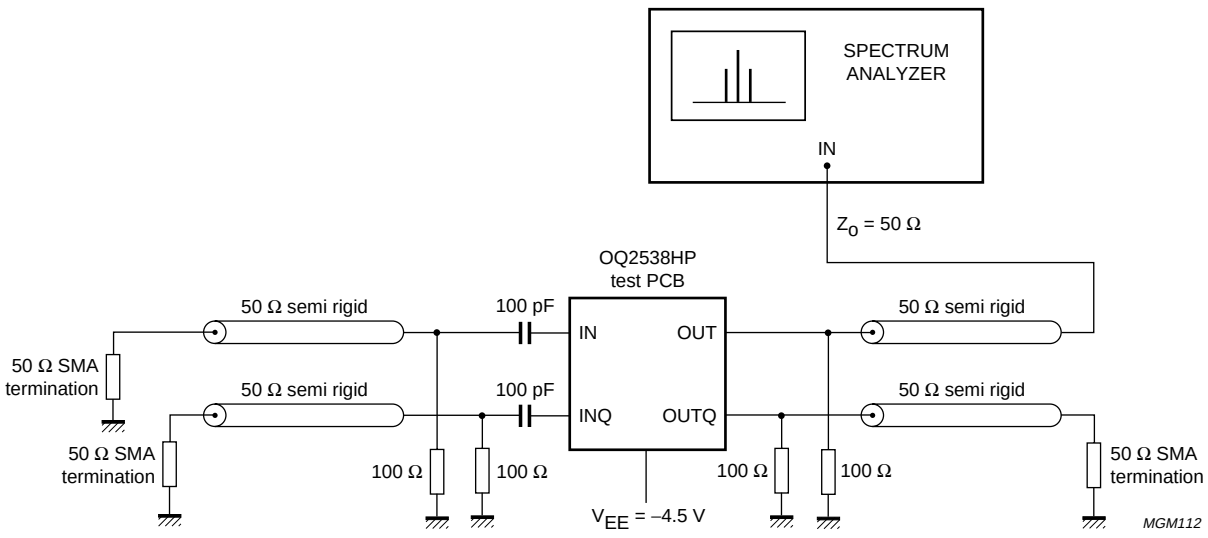
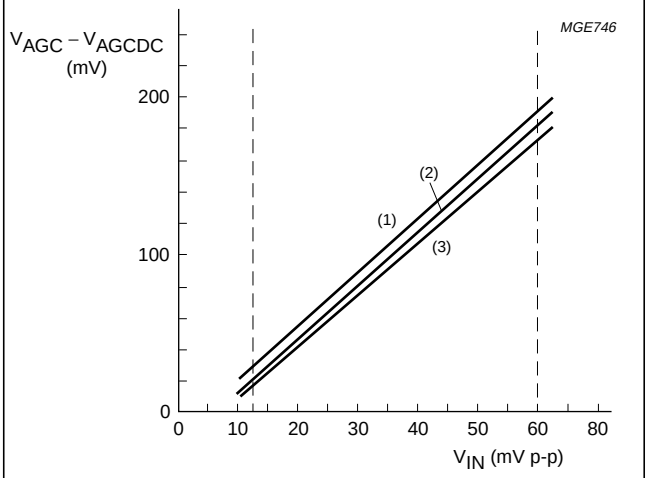
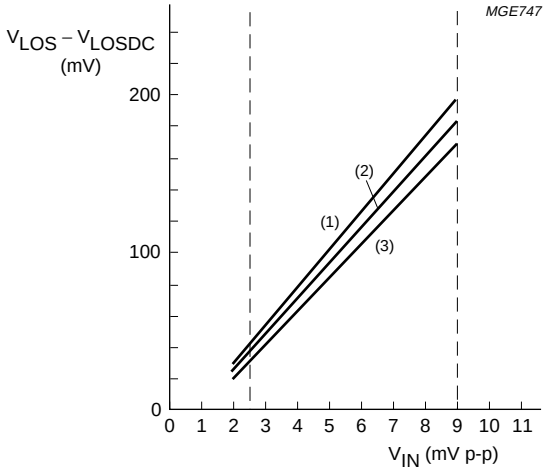


Fig.10 Noise figure measurement set-up.



(1) T_{amb} = –20 °C.
(2) T_{amb} = +25 °C.
(3) T_{amb} = +85 °C.

Fig.11 AGC transfer characteristics.



(1) T_{amb} = –20 °C.
(2) T_{amb} = +25 °C.
(3) T_{amb} = +85 °C.

Fig.12 LOS detection characteristics.

AGC and AGCDC level detection

When using rectifier A as an input signal level detector, the AGC and AGCDC pins must be decoupled to ground with 100 nF capacitors. The AGCDC output is intended as a reference voltage against which the actual AGC output voltage can be compared. This voltage difference, $V_{AGC} - V_{AGCDC}$, can be used as a control input in an AGC loop. A graph depicting output voltage difference as a function of the input signal level (typical) is shown in Fig.11. Note that an input signal with the specified peak-to-peak value is applied to both IN and INQ inputs, but with complementary phase.

LOS and LOSDC level detection

The output of rectifier B can be used for LOS detection. The LOSDC output provides a reference voltage against which the voltage at the LOS output can be compared. The voltage difference $V_{LOS} - V_{LOSDC}$ can be used as input to a LOS detection circuit. Both outputs need to be decoupled using 100 nF capacitors. A graph depicting $V_{LOS} - V_{LOSDC}$ as a function of the input signal level (typical) is shown in Fig.12. Note that an input signal with the specified peak-to-peak value is applied to both IN and INQ inputs, but with complementary phase.

Grounding and power supply decoupling

The ground connection on the PCB needs to be a large copper area fill connected to a common ground plane with as low inductance as possible, preferably positioned directly underneath the LQFP48 package. The large area fill will improve heat transfer to the PCB and thus aid IC cooling.

All V_{EE} pins (two at each corner) need to be connected to a common supply plane with as low inductance as possible. This plane should be decoupled to ground. To avoid high frequency resonance, multiple bypass capacitors should not be mounted at the same location. To minimize low frequency switching noise in the vicinity of the OQ2538HP, the power supply line should be filtered once using an LC-circuit with a low cut-off frequency (see Fig.14).

Using alternative supply voltages

Although the OQ2538HP is intended to be used with a single −4.5 V supply voltage, a slightly modified −5 V supply can also be used. By connecting a Schottky diode between the V_{EE} power supply line and the IC, an additional 0.5 V voltage drop is obtained, bringing the supply voltage on the pins of the OQ2538HP within the specified range. A BAS85 Schottky diode is recommended. A −5 V application schematic is shown in Fig.15.

Extrapolating from this case, a +5 V application is also possible. However, care should be taken with the RF transmission lines. The on-chip signals refer to the GND pins, which become the positive supply pins in a +5 V application. The external transmission lines will most likely be referenced to system ground (V_{EE} pins). The RF signals will change from one reference plane to another at the interface to the RF input and output pins. The positive supply application is very vulnerable to interference at this point. For a successful +5 V application, special care should be taken when designing board layout to reduce the influence of interference and keep the positive supply as clean as possible.

ESD protection

Exceptions have been made to the standard ESD protection scheme in order to achieve high frequency performance. The inputs IN and INQ and the outputs OUT and OUTQ have **no protection** against ESD. All other pins have a standard ESD protection structure, capable of withstanding 2 kV Human Body Model (HBM) zappings.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{EE}	negative supply voltage		–6.0	+0.5	V
ΔV_I	input voltage difference	note 1	–600	+600	mV
I_{IN}, I_{INQ}	input current		–2.0	+2.0	mA
I_n	DC current				
	pins 30 and 32		–6	+10	mA
	pins 3, 18, 19 and 43		–3	+3	mA
	pin 21		–2	+2	mA
	pins 44 and 45		–1	+1	mA
	pin 22		–0.1	+0.1	mA
P_{tot}	total power dissipation		–	380	mW
T_j	junction temperature		–	150	°C
T_{stg}	storage temperature		–65	+150	°C

Note

1. $\Delta V_I = V_{IN} - V_{INQ}$ (AC only). The DC level is internally controlled.

HANDLING

Precautions should be taken to avoid damage through electrostatic discharge. This is particularly important during assembly and handling of the bare die. Additional safety can be obtained by bonding the V_{EE} and GND pads first, the remaining pads may then be bonded to their external connections in any order (see also Section “ESD protection”).

THERMAL CHARACTERISTICS

SYMBOL	DESCRIPTION	CONDITIONS	VALUE	UNIT
$R_{th(j-s)}$	thermal resistance from junction to solder point		15	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	note 1	65	K/W

Note

1. $R_{th(j-a)}$ will be in the application from 15 to 65 K/W, dependent on the PCB layout.

CHARACTERISTICS

At nominal supply voltages; T_{amb} = –40 to +85 °C; 50 Ω measuring environment.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{EE}	negative supply voltage		–4.725	–4.5	–4.275	V
I_{EE}	negative supply current		–	60	80	mA
P_{tot}	total power dissipation	note 1	–	270	380	mW
T_{amb}	operating ambient temperature	note 2	–40	–	+85	°C
T_j	operating junction temperature		–40	–	+120	°C
Main amplifier inputs: IN and INQ; note 3						
$V_{i(sens)}$	input sensitivity	note 4	–	0.5	2.5	mV
$V_{i(p-p)}$	signal voltage swing (peak-to-peak value)	note 4	2.5	–	600	mV
V_I	DC input voltage	note 5	–2.4	–2.1	–1.7	V
V_{IO}	input offset voltage	note 6	–	0.2	–	mV
Z_i	single-ended input impedance	note 7	–	100	–	Ω
S_{21}	single-ended small signal gain	note 8	34	40	–	dB
$G_{v(dif)}$	differential voltage gain	note 9	–	48.5	–	dB
N_o	output noise power	note 10	–	–120	–	dBm
F	noise figure	note 10	–	11	–	dB
B_{-3dB}	3 dB bandwidth		2.4	3.0	–	GHz
Rectifier outputs: AGC and AGCDC; note 11						
$V_{O(ref)}$	DC reference voltage	open output	–3.3	–3.0	–2.5	V
$V_{i(p-p)}$	input voltages on pins IN and INQ for linear rectifier output (peak-to-peak value)		12.5	–	60	mV
ΔV	maximum input signal level related voltage difference	note 12	–	400	–	mV
V_{OO}	output offset voltage	note 13	–5	–	+5	mV
Rectifier outputs: LOS and LOSDC; note 11						
$V_{O(ref)}$	DC reference voltage	open output	–3.4	–3.1	–2.6	V
$V_{i(p-p)}$	input voltages on pins IN and INQ for linear recitifier output (peak-to-peak value)		2.5	–	9	mV
ΔV	maximum input signal level related voltage difference	note 12	–	450	–	mV
V_{OO}	output offset voltage	note 13	–15	–	+15	mV
Automatic offset compensation lowpass filter: COFF and COFFQ						
V_O	DC output voltage	open output	–2.4	–2.1	–1.7	V
R	offset compensation filter resistance		–	1250	–	Ω
Band gap reference: REF						
V_O	band gap voltage	referenced to V_{EE}; open output; note 14	1.1	1.3	1.5	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Band gap reference decoupling: CAPA						
V_O	decoupling voltage	referenced to V_{EE}; open output	–	2.9	–	V
Main amplifier outputs: OUT and OUTQ; note 15						
V_{OH}	HIGH-level output voltage		–20	–5	0	mV
V_{OL}	LOW-level output voltage	note 16	–280	–200	–140	mV
t_r	differential output rise time	input signal >2.5 mV (p-p)	–	100	150	ps
t_f	differential output fall time	input signal >2.5 mV (p-p)	–	100	150	ps
Z_o	single-ended output impedance	see Fig.6	83	100	117	Ω

Notes

1. No special cooling is required in the application if the total thermal resistance $R_{th(j-a)}$ is less than 90 K/W.
2. The temperature of the PCB in the vicinity of the IC is taken to be the ambient temperature.
3. The input signal must be AC-coupled to the inputs through a coupling capacitance >22 nF.
4. $V_{i(p-p)}$ is the input signal on IN and INQ for full output clipping. It is assumed that both inputs carry a complementary signal of the specified peak-to-peak value. The lower specified limit is usually called the input sensitivity. This value is defined as a 20% increase in rise and fall times when compared to rise and fall times with a complementary input signal of 10 mV (p-p) applied to IN and INQ.
5. The DC voltage is fixed internally; only AC-coupling of the input signal is allowed.
6. $V_{IO} = |V_{IN} - V_{INQ}|$
7. See Section “RF input matching circuit” for detailed information.
8. All signal ports are AC-matched to 50 Ω and are measured at 1 GHz (see Fig.7). Flatness deviations are within ±3 dB over the entire bandwidth.
9. See Section “RF gain and group delay measurements”.
10. F is the noise figure for a differential application and is measured at 1 GHz. See Section “Noise figure measurements”.
11. An external 100 nF capacitor is connected at each output to remove any spurious high frequency signals. Any circuitry driven from these pins must have an input impedance >50 kΩ.
12. Voltage difference between AGC (LOS) and AGCDC (LOSDC), measured with a differential square wave input signal of 600 mV (p-p) on IN and INQ.
13. The offset is measured with inputs IN and INQ shorted together.
14. The band gap voltage may not be used as an external reference.
15. Both outputs are connected to ground through a 50 Ω load resistance and carry complementary signals.
16. The output levels are dependent on load impedance. The specified values assume an external load impedance of 50 Ω. If the external 100 Ω matching resistors are connected at pins OUT and OUTQ, the output levels will fall to 75% of the specified values (see also Section “RF gain and group delay measurements”).

APPLICATION INFORMATION

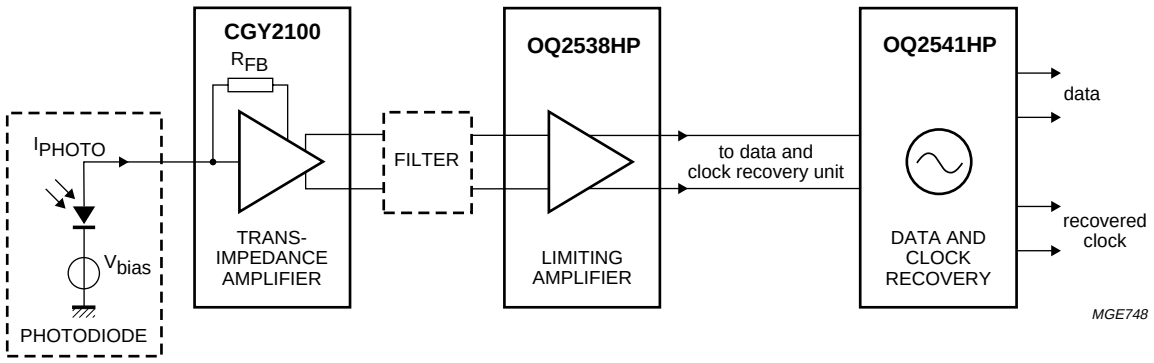


Fig.13 System application diagram.

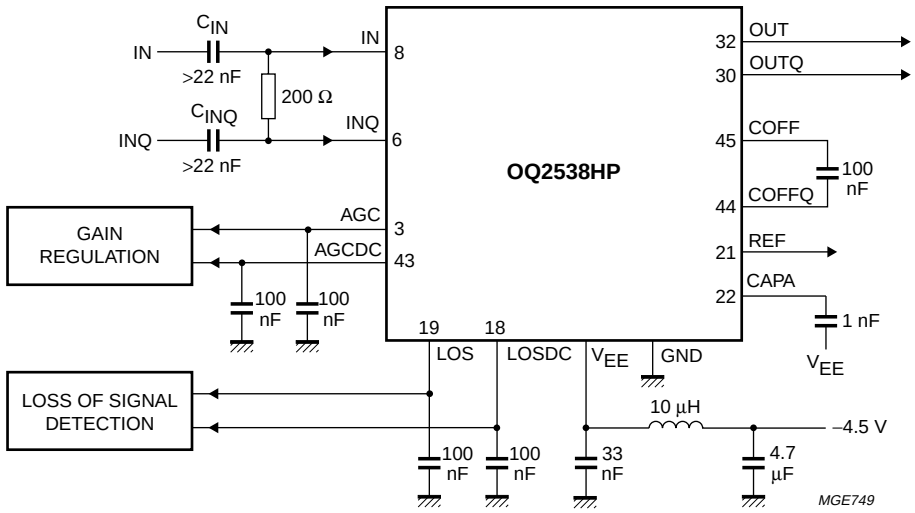


Fig.14 Typical application schematic.

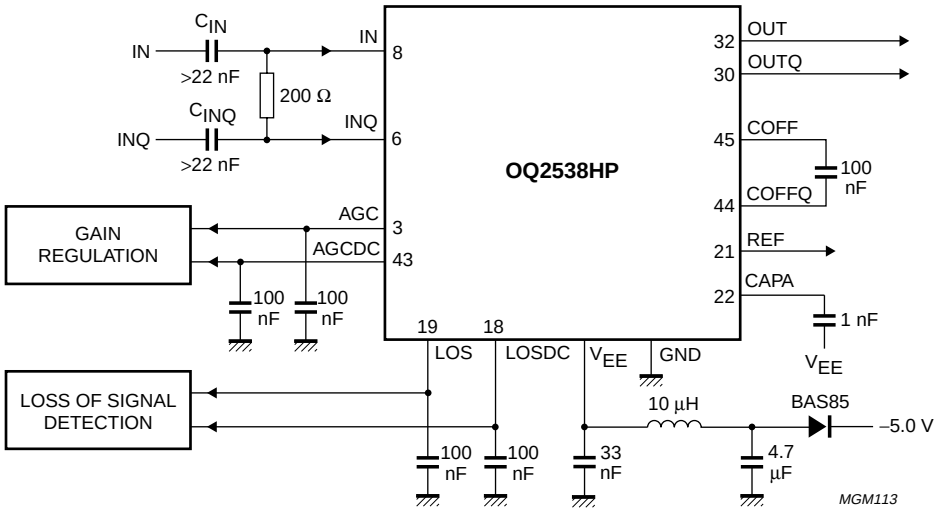
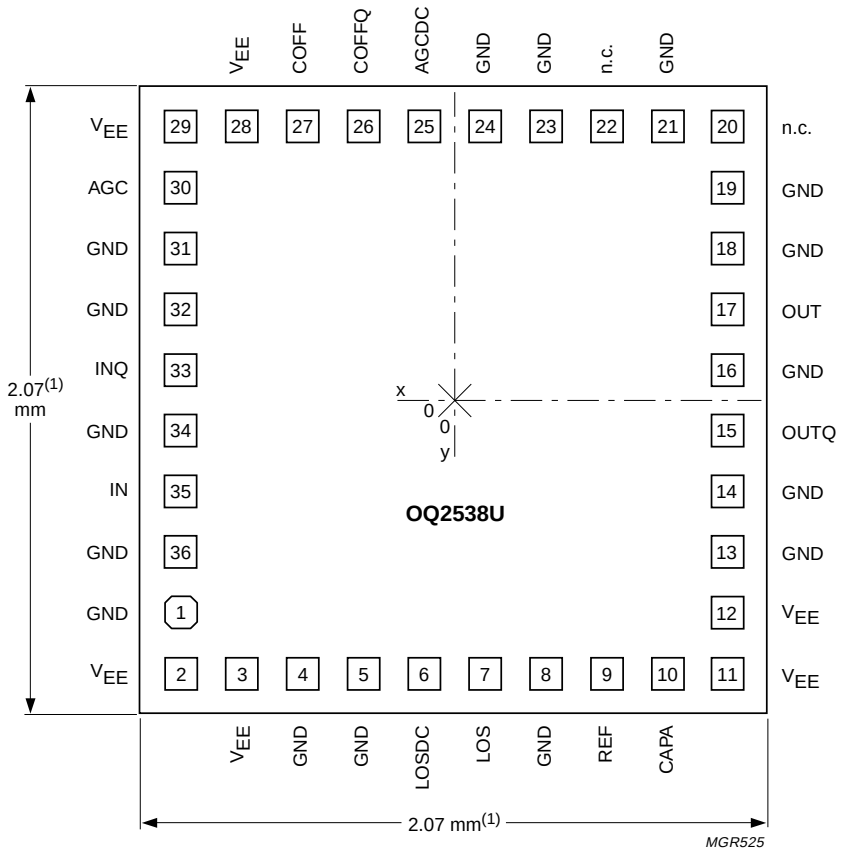


Fig.15 –5 V application schematic.

BONDING PAD LOCATIONS



(1) Typical value.

Fig.16 Bonding pad locations of OQ2538U.

Table 1 Bonding pad locations. All x/y coordinates represent the position of the centre of the pad with respect to the centre of the die (see Fig.16).

SYMBOL	PAD	COORDINATES	
		x	y
GND	1	–900	–700
V_{EE}	2	–900	–900
V_{EE}	3	–700	–900
GND	4	–500	–900
GND	5	–300	–900
LOSDC	6	–100	–900
LOS	7	+100	–900
GND	8	+300	–900
REF	9	+500	–900
CAPA	10	+700	–900
V_{EE}	11	+900	–900
V_{EE}	12	+900	–700
GND	13	+900	–500
GND	14	+900	–300
OUTQ	15	+900	–100
GND	16	+900	+100
OUT	17	+900	+300
GND	18	+900	+500

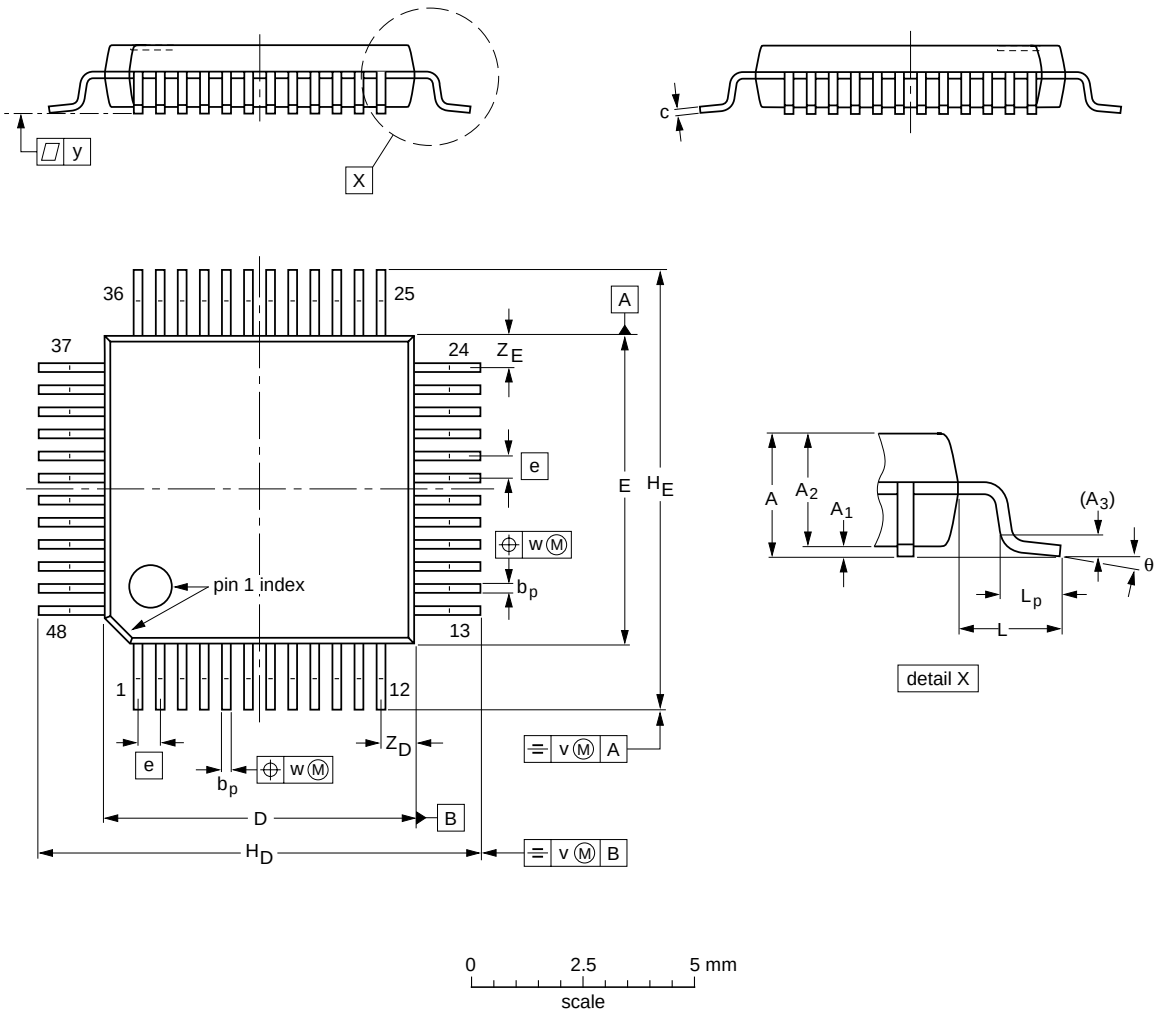
SYMBOL	PAD	COORDINATES	
		x	y
GND	19	+900	+700
n.c.	20	+900	+900
GND	21	+700	+900
n.c.	22	+500	+900
GND	23	+300	+900
GND	24	+100	+900
AGCDC	25	–100	+900
COFFQ	26	–300	+900
COFF	27	–500	+900
V_{EE}	28	–700	+900
V_{EE}	29	–900	+900
AGC	30	–900	+700
GND	31	–900	+500
GND	32	–900	+300
INQ	33	–900	+100
GND	34	–900	–100
IN	35	–900	–300
GND	36	–900	–500

Table 2 Physical characteristics of bare die

PARAMETER	VALUE
Glass passivation	0.8 μm silicon nitride on top of 0.9 μm PSG (PhosphoSilicate Glass)
Bonding pad dimension	minimum dimension of exposed metallization is 90 × 90 μm (pad size = 100 × 100 μm)
Metallization	1.8 μm AlCu (1% Cu)
Thickness	380 μm nominal
Size	2.070 × 2.070 mm (4.285 mm^2)
Backing	silicon; electrically connected to V_{EE} potential through substrate contacts
Attache temperature	<440 °C; recommended die attache is glue
Attache time	<15 s

PACKAGE OUTLINE

LQFP48: plastic low profile quad flat package; 48 leads; body 7 x 7 x 1.4 mm **SOT313-2**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.60	0.20 0.05	1.45 1.35	0.25	0.27 0.17	0.18 0.12	7.1 6.9	7.1 6.9	0.5	9.15 8.85	9.15 8.85	1.0	0.75 0.45	0.2	0.12	0.1	0.95 0.55	0.95 0.55	7^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT313-2	136E05	MS-026				~~99-12-27~~ 00-01-19

SOLDERING

Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferable be kept below 220 °C for thick/large packages, and below 235 °C for small/thin packages.

Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.
A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

Suitability of surface mount IC packages for wave and reflow soldering methods

PACKAGE	SOLDERING METHOD	
	WAVE	REFLOW[1]
BGA, LFBGA, SQFP, TFBGA	not suitable	suitable
HBCC, HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, SMS	not suitable[2]	suitable
PLCC[3], SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended[3][4]	suitable
SSOP, TSSOP, VSO	not recommended[5]	suitable

Notes

1. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *"Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods"*.
2. These packages are not suitable for wave soldering as a solder joint between the printed-circuit board and heatsink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).
3. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
4. Wave soldering is only suitable for LQFP, TQFP and QFP packages with a pitch (e) equal to or larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
5. Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

DATA SHEET STATUS

DATA SHEET STATUS	PRODUCT STATUS	DEFINITIONS (1)
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product specification	Production	This data sheet contains final specifications. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

Note

1. Please consult the most recently issued data sheet before initiating or completing a design.

DEFINITIONS

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

Application information — Applications that are described herein for any of these products are for illustrative purposes only. Philips Semiconductors make no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

DISCLAIMERS

Life support applications — These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips Semiconductors customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips Semiconductors for any damages resulting from such application.

Right to make changes — Philips Semiconductors reserves the right to make changes, without notice, in the products, including circuits, standard cells, and/or software, described or contained herein in order to improve design and/or performance. Philips Semiconductors assumes no responsibility or liability for the use of any of these products, conveys no licence or title under any patent, copyright, or mask work right to these products, and makes no representations or warranties that these products are free from patent, copyright, or mask work right infringement, unless otherwise specified.

NOTES

NOTES

NOTES

Philips Semiconductors – a worldwide company

Argentina: see South America

Australia: 3 Figtree Drive, HOMEBUSH, NSW 2140,
Tel. +61 2 9704 8141, Fax. +61 2 9704 8139

Austria: Computerstr. 6, A-1101 WIEN, P.O. Box 213,
Tel. +43 1 60 101 1248, Fax. +43 1 60 101 1210

Belarus: Hotel Minsk Business Center, Bld. 3, r. 1211, Volodarski Str. 6,
220050 MINSK, Tel. +375 172 20 0733, Fax. +375 172 20 0773

Belgium: see The Netherlands

Brazil: see South America

Bulgaria: Philips Bulgaria Ltd., Energoproject, 15th floor,
51 James Bourchier Blvd., 1407 SOFIA,
Tel. +359 2 68 9211, Fax. +359 2 68 9102

Canada: PHILIPS SEMICONDUCTORS/COMPONENTS,
Tel. +1 800 234 7381, Fax. +1 800 943 0087

China/Hong Kong: 501 Hong Kong Industrial Technology Centre,
72 Tat Chee Avenue, Kowloon Tong, HONG KONG,
Tel. +852 2319 7888, Fax. +852 2319 7700

Colombia: see South America

Czech Republic: see Austria

Denmark: Sydhavnsgade 23, 1780 COPENHAGEN V,
Tel. +45 33 29 3333, Fax. +45 33 29 3905

Finland: Sinikalliontie 3, FIN-02630 ESPOO,
Tel. +358 9 615 800, Fax. +358 9 6158 0920

France: 51 Rue Carnot, BP317, 92156 SURESNES Cedex,
Tel. +33 1 4099 6161, Fax. +33 1 4099 6427

Germany: Hammerbrookstraße 69, D-20097 HAMBURG,
Tel. +49 40 2353 60, Fax. +49 40 2353 6300

Hungary: see Austria

India: Philips INDIA Ltd, Band Box Building, 2nd floor,
254-D, Dr. Annie Besant Road, Worli, MUMBAI 400 025,
Tel. +91 22 493 8541, Fax. +91 22 493 0966

Indonesia: PT Philips Development Corporation, Semiconductors Division,
Gedung Philips, Jl. Buncit Raya Kav.99-100, JAKARTA 12510,
Tel. +62 21 794 0040 ext. 2501, Fax. +62 21 794 0080

Ireland: Newstead, Clonskeagh, DUBLIN 14,
Tel. +353 1 7640 000, Fax. +353 1 7640 200

Israel: RAPAC Electronics, 7 Kehilat Saloniki St, PO Box 18053,
TEL AVIV 61180, Tel. +972 3 645 0444, Fax. +972 3 649 1007

Italy: PHILIPS SEMICONDUCTORS, Via Casati, 23 - 20052 MONZA (MI),
Tel. +39 039 203 6838, Fax +39 039 203 6800

Japan: Philips Bldg 13-37, Kohnan 2-chome, Minato-ku,
TOKYO 108-8507, Tel. +81 3 3740 5130, Fax. +81 3 3740 5057

Korea: Philips House, 260-199 Itaewon-dong, Yongsan-ku, SEOUL,
Tel. +82 2 709 1412, Fax. +82 2 709 1415

Malaysia: No. 76 Jalan Universiti, 46200 PETALING JAYA, SELANGOR,
Tel. +60 3 750 5214, Fax. +60 3 757 4880

Mexico: 5900 Gateway East, Suite 200, EL PASO, TEXAS 79905,
Tel. +9-5 800 234 7381, Fax +9-5 800 943 0087

Middle East: see Italy

Netherlands: Postbus 90050, 5600 PB EINDHOVEN, Bldg. VB,
Tel. +31 40 27 82785, Fax. +31 40 27 88399

New Zealand: 2 Wagener Place, C.P.O. Box 1041, AUCKLAND,
Tel. +64 9 849 4160, Fax. +64 9 849 7811

Norway: Box 1, Manglerud 0612, OSLO,
Tel. +47 22 74 8000, Fax. +47 22 74 8341

Pakistan: see Singapore

Philippines: Philips Semiconductors Philippines Inc.,
106 Valero St. Salcedo Village, P.O. Box 2108 MCC, MAKATI,
Metro MANILA, Tel. +63 2 816 6380, Fax. +63 2 817 3474

Poland: Al.Jerozolimskie 195 B, 02-222 WARSAW,
Tel. +48 22 5710 000, Fax. +48 22 5710 001

Portugal: see Spain

Romania: see Italy

Russia: Philips Russia, Ul. Usatcheva 35A, 119048 MOSCOW,
Tel. +7 095 755 6918, Fax. +7 095 755 6919

Singapore: Lorong 1, Toa Payoh, SINGAPORE 319762,
Tel. +65 350 2538, Fax. +65 251 6500

Slovakia: see Austria

Slovenia: see Italy

South Africa: S.A. PHILIPS Pty Ltd., 195-215 Main Road Martindale,
2092 JOHANNESBURG, P.O. Box 58088 Newville 2114,
Tel. +27 11 471 5401, Fax. +27 11 471 5398

South America: Al. Vicente Pinzon, 173, 6th floor,
04547-130 SÃO PAULO, SP, Brazil,
Tel. +55 11 821 2333, Fax. +55 11 821 2382

Spain: Balmes 22, 08007 BARCELONA,
Tel. +34 93 301 6312, Fax. +34 93 301 4107

Sweden: Kottbygatan 7, Akalla, S-16485 STOCKHOLM,
Tel. +46 8 5985 2000, Fax. +46 8 5985 2745

Switzerland: Allmendstrasse 140, CH-8027 ZÜRICH,
Tel. +41 1 488 2741 Fax. +41 1 488 3263

Taiwan: Philips Semiconductors, 5F, No. 96, Chien Kuo N. Rd., Sec. 1,
TAIPEI, Taiwan Tel. +886 2 2134 2451, Fax. +886 2 2134 2874

Thailand: PHILIPS ELECTRONICS (THAILAND) Ltd.,
60/14 MOO 11, Bangna Trad Road KM. 3, Bagna, BANGKOK 10260,
Tel. +66 2 361 7910, Fax. +66 2 398 3447

Turkey: Yukari Dudullu, Org. San. Blg., 2.Cad. Nr. 28 81260 Umraniye,
ISTANBUL, Tel. +90 216 522 1500, Fax. +90 216 522 1813

Ukraine: PHILIPS UKRAINE, 4 Patrice Lumumba str., Building B, Floor 7,
252042 KIEV, Tel. +380 44 264 2776, Fax. +380 44 268 0461

United Kingdom: Philips Semiconductors Ltd., 276 Bath Road, Hayes,
MIDDLESEX UB3 5BX, Tel. +44 208 730 5000, Fax. +44 208 754 8421

United States: 811 East Arques Avenue, SUNNYVALE, CA 94088-3409,
Tel. +1 800 234 7381, Fax. +1 800 943 0087

Uruguay: see South America

Vietnam: see Singapore

Yugoslavia: PHILIPS, Trg N. Pasica 5/v, 11000 BEOGRAD,
Tel. +381 11 3341 299, Fax.+381 11 3342 553

For all other countries apply to: Philips Semiconductors,
Marketing Communications, Building BE-p, P.O. Box 218, 5600 MD EINDHOVEN,
The Netherlands, Fax. +31 40 27 24825

Internet: http://www.semiconductors.philips.com

Printed in The Netherlands 403510/03/pp28 Date of release: 2000 Sep 29 Document order number: 9397 750 07553

Let's make things better.

Philips Semiconductors

PHILIPS