



## 5-A Controlled Slew Rate Load Switch with Level Shift

### FEATURES

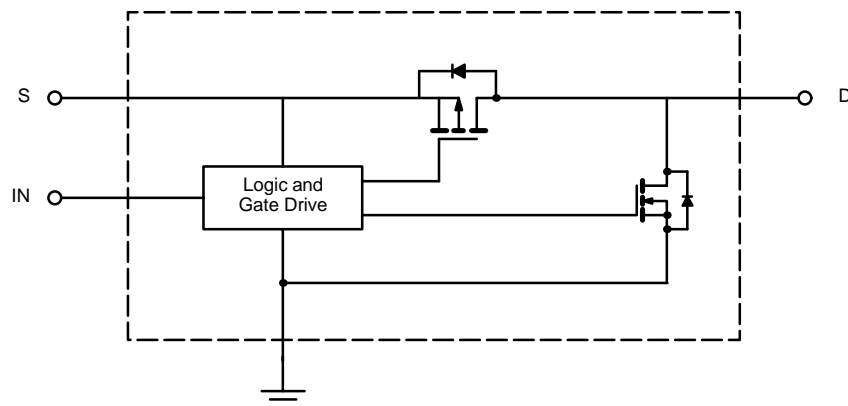
- 5-A Maximum Load
- Switches Voltages 1.8- to 5.5-V
- Ground Referenced Logic Inputs
- 1.8- to 5-V Logic Voltage Compatible
- 25-m $\Omega$  Maximum On-Resistance
- Level-Shifted Gate Drive Means The Control (Logic) Voltage Is Independent Of Power Voltage
- Slow Turn-On (Controlled Slew Rate) Eliminates High Inrush Currents
- Low Power Consumption In Off State
- Active Pull-Down On Output When In Off State

### DESCRIPTION

The Si4788CY is a p-channel MOSFET with a logic interface. The control input is compatible with all types of logic down to 1.8 V. The switch can be used to control voltages from 1.8 V to 5.5 V, and the logic input can be a lower voltage than the power. The switch also incorporates reduced switching speed

to reduce inrush when switching loads with a high value of capacitance. The Si4788CY is packaged in an 8-pin SOIC package and rated for the commercial temperature range of 0 to 85°C

### FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION



**ABSOLUTE MAXIMUM RATINGS**

Voltage Referenced to GND		Continuous P-Switch Current	5 A
$V_S, V_D^a$	-0.3 V to 7.0 V	Storage Temperature	-55 to 150°C
$V_{IN}$	-0.3 V to 7.0 V	Notes	
Power Dissipation (Continuous) <sup>a</sup>	1.5 W	a. Device mounted with all leads soldered to 1" x 1" FR4 with laminated copper PC board.	

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**RECOMMENDED OPERATING RANGE**

$V_S, V_D$	1.8 V to 5.5 V	Operating Temperature Range	-25 to 85°C
$V_{IN}$	0 V to 5.5 V	Junction Temperature	-25 to 150°C

This device has a maximum recommended operating junction temperature of 85°C. This temperature limit is used for electrical specifications such as logic transition voltages only and is not a reliability limit. The device can be used with junction temperatures up to 150°C if relaxed specifications can be tolerated, although limits for these specifications may not be given. Performance curves can be used to give an indication of specifications at higher temperatures, but are not guaranteed.

**THERMAL RESISTANCE RATINGS**

Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient <sup>NO TAG</sup>	Steady State	$R_{thJA}$	80	95	°C/W
Maximum Junction-to-Foot (Drain) <sup>NO TAG</sup>	Steady State	$R_{thJF}$	15	20	

## Notes

- Surface Mounted on 1" x 1" FR4 Board.
- Junction-to-foot thermal impedance represents the effective thermal impedance of all heat carrying leads in parallel and is intended for use in conjunction with the thermal impedance of the PC board pads to ambient ( $R_{thJA} = R_{thJF} + R_{thPCB-A}$ ). It can also be used to estimate chip temperature if power dissipation and the lead temperature of a heat carrying (drain) lead is known.

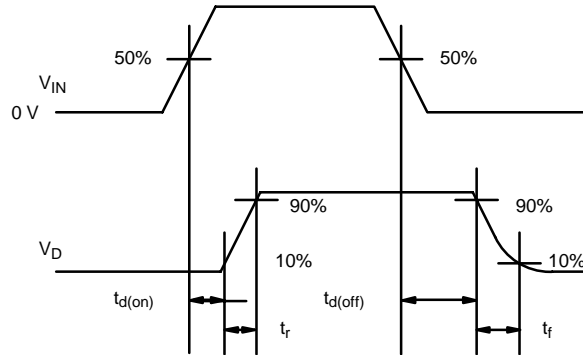
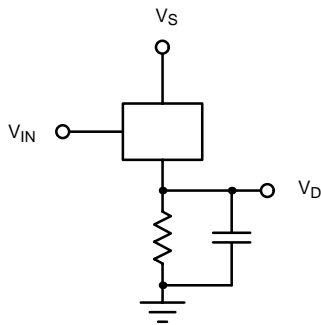
**SPECIFICATIONS**

Parameter	Symbol	Specific Test Conditions	Limits				Unit
			Temp <sup>a</sup>	Min <sup>b</sup>	Typ <sup>c</sup>	Max <sup>b</sup>	
On-Resistance	$r_{DS(on)}$	$V_S = 3.3\text{ V}, I_D = 1\text{ A}, V_{IN} = H$	Room		20	25	mΩ
		$V_S = 4.5\text{ V}, I_D = 1\text{ A}, V_{IN} = H$	Room		16	20	
Pull-Down Resistance	$r_{PULL-DOWN}$	$V_S = 3.3\text{ V to } 5\text{ V}, V_{IN} = L$	Room	8	12	20	Ω
Leakage Current	$I_{S(off)}$	$V_S = 1.8\text{ V to } 5\text{ V}, V_{IN} = L$	Room			1.2	μA
Logic Input Voltage Low	$V_{INL}$	$V_S = 3.3\text{ V to } 5\text{ V}$	Full			0.6	V
		$V_S = 1.8\text{ V to } 3.3\text{ V}$	Full			0.3	
Input Voltage High	$V_{INH}$	$V_S = 3.3\text{ V to } 5\text{ V}$	Full	2.2			V
		$V_S = 1.8\text{ V to } 3.3\text{ V}$	Full	1.5			
Turn-On Delay	$t_{d(on)}$	$V_{IN} = 5\text{ V}, I_{LOAD} = 1\text{ A}, C_{LOAD} = 100\text{ }\mu\text{F}$ Test Circuit 1	Room		16	35	μs
Turn-Off Delay	$t_{d(off)}$		Room		20	40	
Rise Time	$t_{RISE}$		Room		280	550	
Fall Time	$t_{FALL}$		Room		920	1800	
Maximum Turn-On Slew Rate	$dv/dt$		Room		20		

## Notes

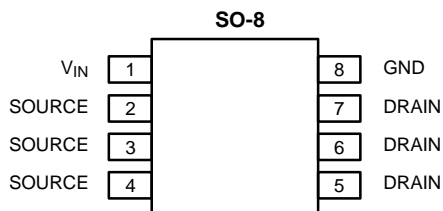
- Room = 25°C, Full = as determined by the operating temperature suffix.
- The algebraic convention whereby the most negative value is a minimum and the most positive a maximum.
- Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.

**TIMING DIAGRAMS**



TEST CIRCUIT 1

**PIN CONFIGURATION**



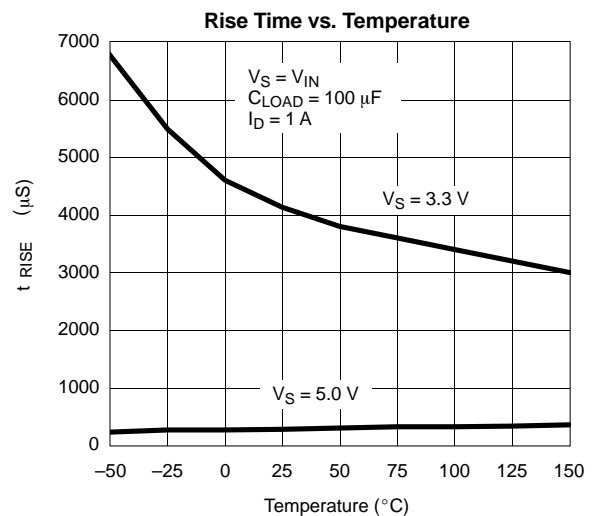
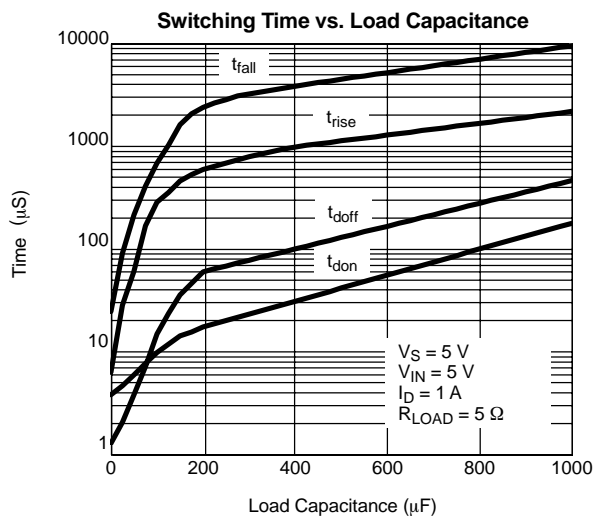
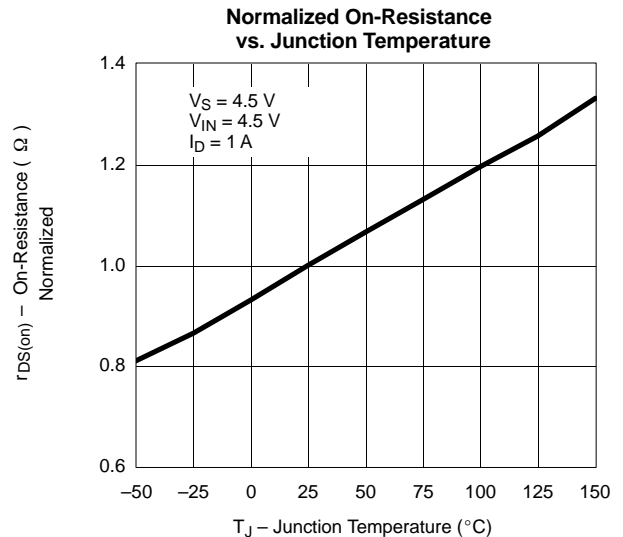
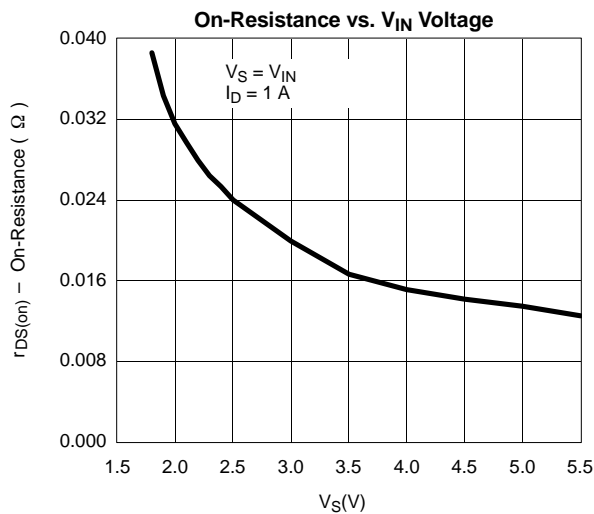
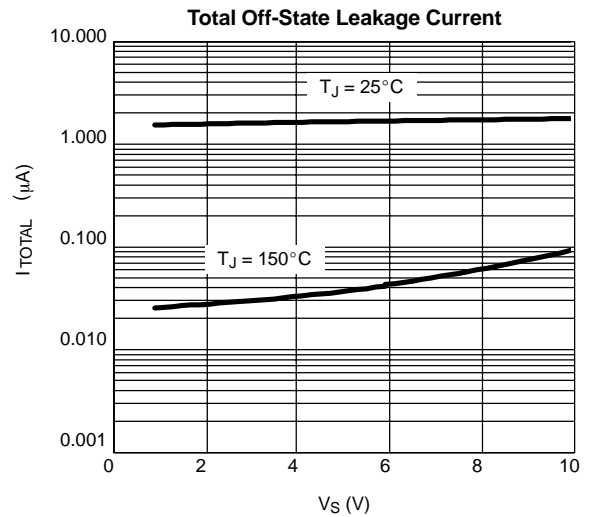
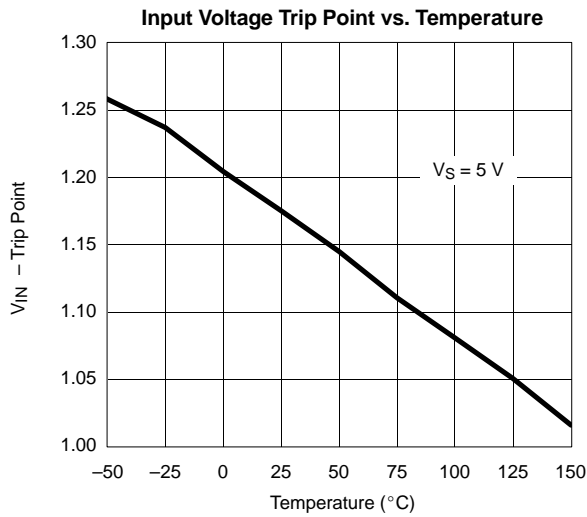
Top View

Order Number: **Si4788CY**

TRUTH TABLE	
$V_{IN}$	Switch
0	Off
1	On

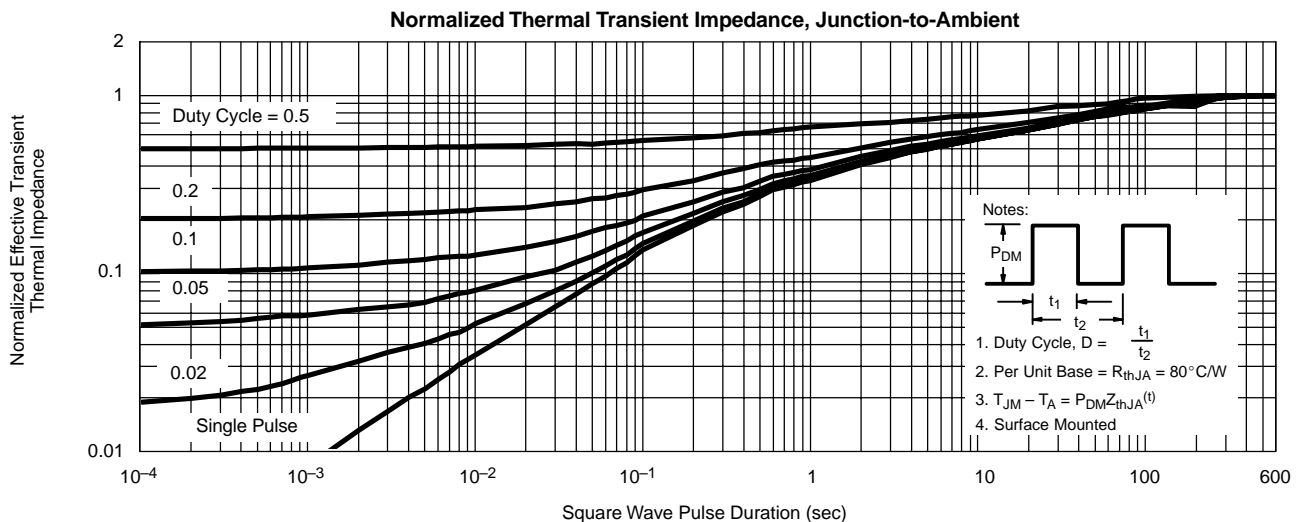
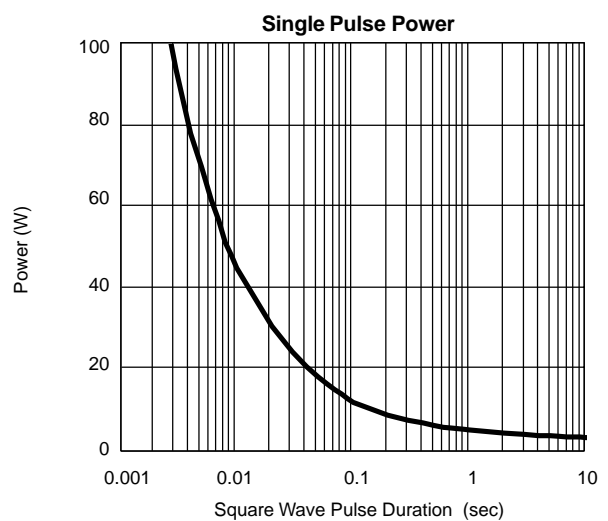
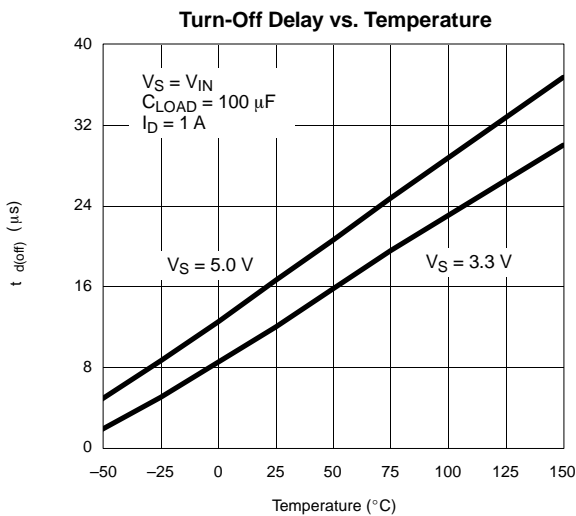
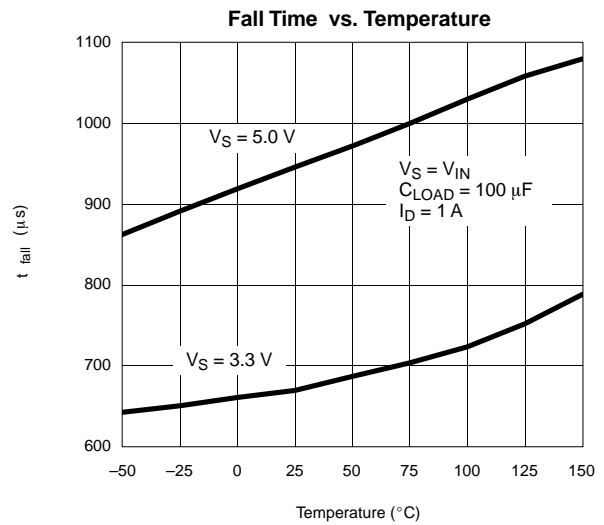
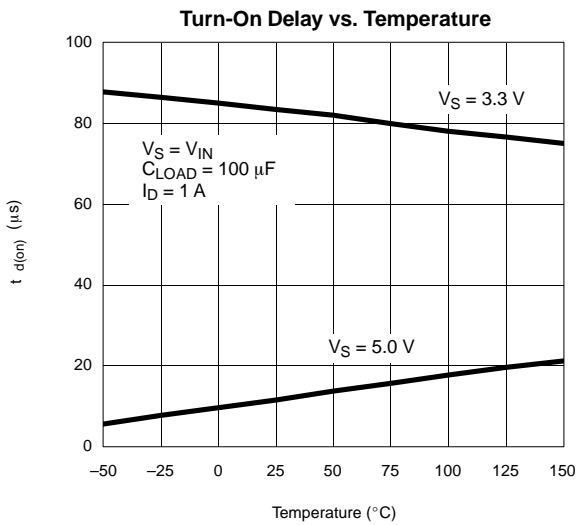
PIN DESCRIPTION		
Pin Number	Symbol	Description
1	$V_{IN}$	Input pin
2, 3, 4	SOURCE	
5, 6, 7	DRAIN	
8	GND	Ground

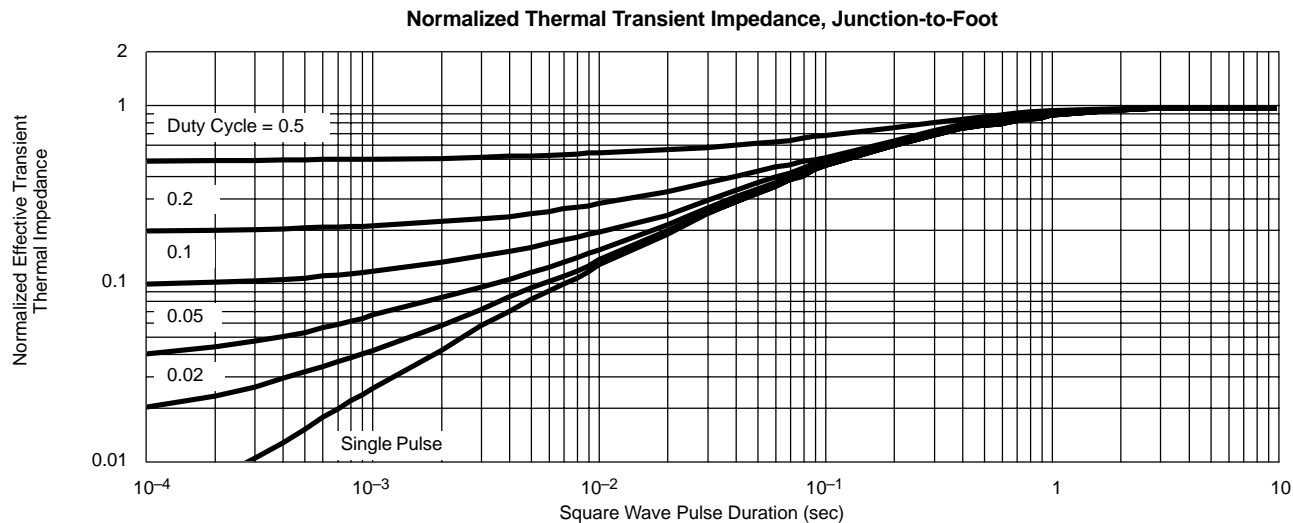
**TYPICAL CHARACTERISTICS (25 °C UNLESS NOTED)**





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**TYPICAL APPLICATIONS**

The Si4788CY can be used to control a load up to 5-Amp where the control logic voltage is different from the voltage of the load being controlled, and/or the load has a large capacitive component and inrush currents must be minimized during switching.

The low  $R_{DS(on)}$  of 20-m $\Omega$  typical makes the switch ideal for applications such as power bus switching in notebook computers and central office telecom equipment. For a load of 5 A, the voltage drop is only approximately 100 mV.

The control input is a CMOS compatible input with a minimum high input voltage of 2.2 V with a power rail voltage of 5 V. It is

therefore compatible with any CMOS logic voltage between 2.2 V and 5 V under these conditions with no extra configuration required. With a 3.3-V power rail voltage the minimum high input voltage is 1.5 V, making it compatible with 1.8-V logic.

The Si4788CY is designed to give a steady  $dv/dt$  on the output during turn-on even with capacitive loads. The output rise time is 280- $\mu$ s typical with a 100- $\mu$ F load, which corresponds to a  $dv/dt$  of about 20 V/ms, or a capacitive inrush current of around 2-A max with a 100- $\mu$ F load. Higher values of capacitance result in a slower switching speed, therefore even with very high values of capacitance, inrush should not be a problem.

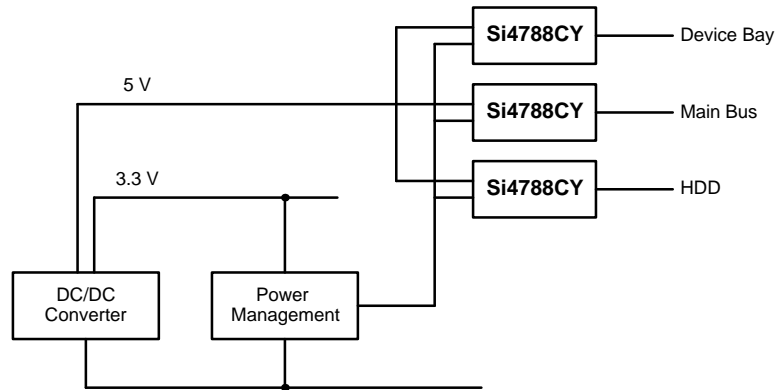


FIGURE 1. Si4788CY Used To Control 5-V Bus With 3.3-V Logic Control

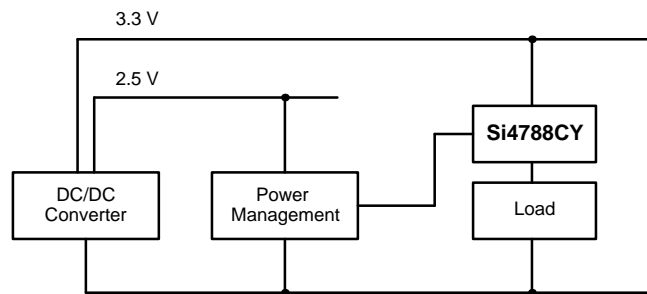


FIGURE 2. Si4788CY Used To Control 3.3-V Bus With 2.5-V Or 3.3-V Logic

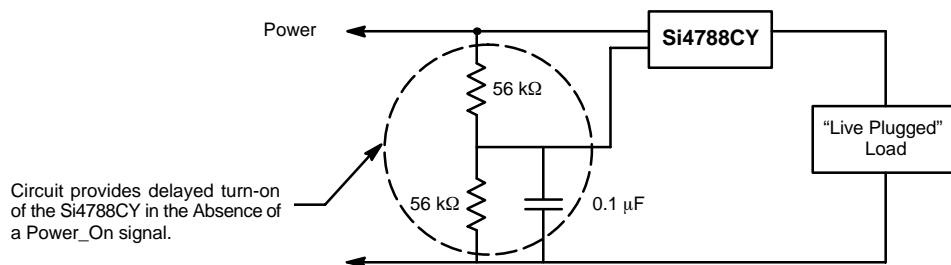


FIGURE 3. Si4788CY Used As Inrush Limiter On Removable Card