

# MC10EP446, MC100EP446

## 3.3V/5V 8-Bit CMOS/ECL/TTL Data Input Parallel/Serial Converter

The MC10/100EP446 is an integrated 8-bit parallel to serial data converter. The device is designed with unique circuit topology to operate for NRZ data rates up to 3.2 Gb/s. The conversion sequence from parallel data into a serial data stream is from bit D0 to D7. The parallel input pins D0–D7 are configurable to be threshold controlled by CMOS, ECL, or TTL level signals. The serial data rate output can be selected at internal clock data rate or twice the internal clock data rate using the CKSEL pin.

Control pins are provided to reset (SYNC) and disable internal clock circuitry (CKEN). In either CKSEL modes, the internal flip-flops are triggered on the rising edge for CLK and the multiplexers are switched on the falling edge of CLK, therefore, all associated specification limits are referenced to the negative edge of the clock input. Additionally, V<sub>BB</sub> pin is provided for single-ended input condition.

The 100 Series devices contain temperature compensation network.

- 3.2 Gb/s Typical Data Rate Capability
- Differential Clock and Serial Outputs
- V<sub>BB</sub> Output for Single-ended Input Applications
- Asynchronous Data Reset (SYNC)
- PECL Mode Operating Range:  
 $V_{CC} = 3.0\text{ V to }5.5\text{ V with }V_{EE} = 0\text{ V}$
- NECL Mode Operating Range:  
 $V_{CC} = 0\text{ V with }V_{EE} = -3.0\text{ V to }-5.5\text{ V}$
- Open Input Default State
- Safety Clamp on Inputs
- Parallel Interface Can Support PECL, TTL or CMOS



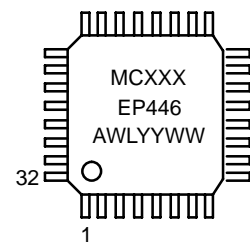
ON Semiconductor®

<http://onsemi.com>

### MARKING DIAGRAM\*



LQFP-32  
FA SUFFIX  
CASE 873A



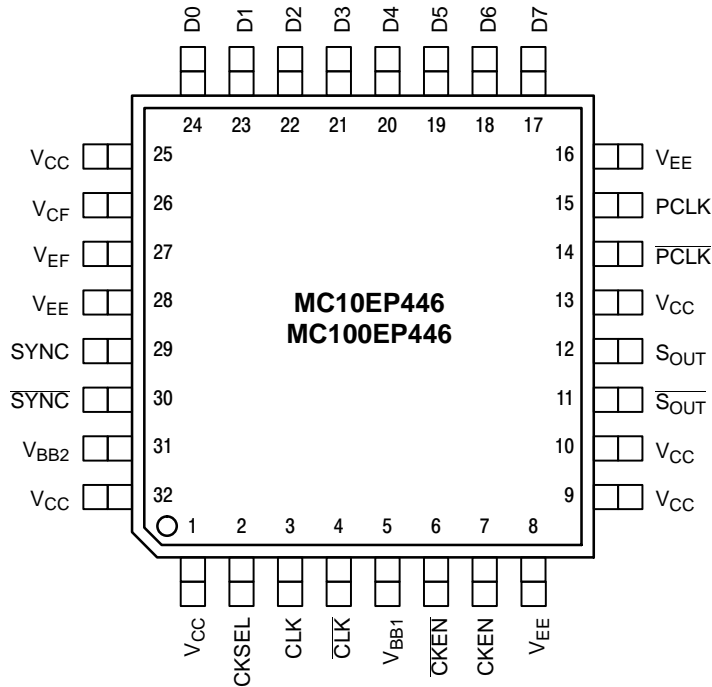
XXX = 10 or 100  
A = Assembly Location  
WL = Wafer Lot  
YY = Year  
WW = Work Week

\*For additional marking information, refer to Application Note AND8002/D.

### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 17 of this data sheet.

# MC10EP446, MC100EP446



Warning: All V<sub>CC</sub> and V<sub>EE</sub> pins must be externally connected to Power Supply to guarantee proper operation.

Figure 1. LQFP-32 Pinout (Top View)

Table 1. PIN DESCRIPTION

PIN	FUNCTION
D0*-D7*	ECL, CMOS, or TTL Parallel Data Input
S <sub>OUT</sub> , $\overline{S}_{OUT}$	ECL Differential Serial Data Output
CLK*, $\overline{CLK}$ *	ECL Differential Clock Input
PCLK, $\overline{PCLK}$	ECL Differential Parallel Clock Output
SYNC*, $\overline{SYNC}$ **	ECL Conversion Synchronizing Differential Input (Reset)***
CKSEL*	ECL Clock Input Selector
CKEN*, $\overline{CKEN}$ *	ECL Clock Enable Differential Input
V <sub>CF</sub>	ECL, CMOS, or TTL Input Selector
V <sub>EF</sub>	ECL Reference Mode Connection
V <sub>BB1</sub> , V <sub>BB2</sub>	Reference Voltage Output
V <sub>CC</sub>	Positive Supply
V <sub>EE</sub>	Negative Supply

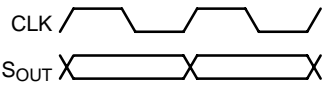
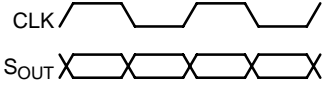
\* Pins will default LOW when left open.

\*\*Pins will default HIGH when left open.

\*\*\*The rising edge of SYNC will asynchronously reset the internal circuitry. The falling edge of the SYNC followed by the falling edge of CLK initiates the conversion process synchronously on the next rising edge of CLK.

# MC10EP446, MC100EP446

**Table 2. TRUTH TABLE**

Pin	Function	
	HIGH	LOW
CKSEL	S <sub>OUT</sub> : PCLK = 8:1 CLK: S <sub>OUT</sub> = 1:1 	S <sub>OUT</sub> : PCLK = 8:1 CLK: S <sub>OUT</sub> = 1:2 
CKEN	Synchronously Disables Normal Parallel to Serial Conversion	Synchronously Enables Normal Parallel to Serial Conversion
SYNC	Asynchronously Resets Internal Flip-Flops*	Synchronous Enable

\*The rising edge of SYNC will asynchronously reset the internal circuitry. The falling edge of the SYNC followed by the falling edge of CLK initiates the conversion process synchronously on the next rising edge of CLK.

**Table 3. INPUT VOLTAGE LEVEL SELECTION TABLE**

Input Function	Connect To V <sub>CF</sub> Pin
ECL Mode	V <sub>EF</sub> Pin
CMOS Mode	No Connect
TTL Mode*	1.5 V ± 100 mV

\*For TTL Mode, if no external voltage can be provided, the reference voltage can be provided by connecting the appropriate resistor between V<sub>CF</sub> and V<sub>EE</sub> pins.

**Table 4. DATA INPUT OPERATING VOLTAGE TABLE**

Power Supply (V <sub>CC</sub> , V <sub>EE</sub> )	Data Inputs (D [0:7])			
	CMOS	TTL	PECL	NECL
PECL	✓	✓	✓	N/A
NECL	N/A	N/A	N/A	✓

Power Supply	Resistor Value 10% (Tolerance)
3.3 V	1.5 kΩ
5.0 V	500 Ω

MC10EP446, MC100EP446

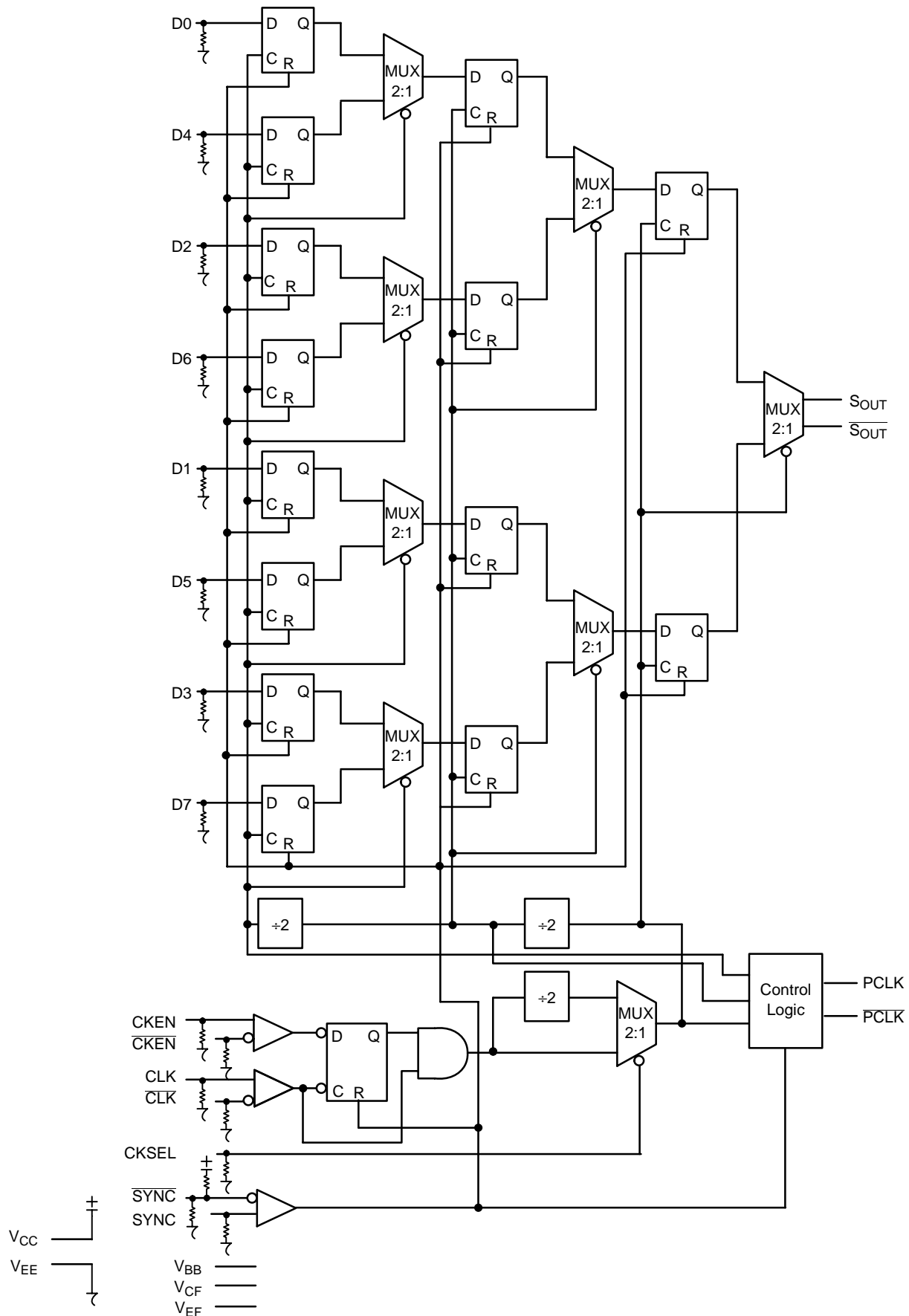


Figure 2. Logic Diagram

# MC10EP446, MC100EP446

**Table 5. ATTRIBUTES**

Characteristics	Value
Internal Input Pulldown Resistor	75 k $\Omega$
Internal Input Pullup Resistor	37.5 k $\Omega$
ESD Protection	Human Body Model Machine Model Charged Device Model
	> 2 kV > 100 V > 2 kV
Moisture Sensitivity (Note 1)	Level 2
Flammability Rating	Oxygen Index: 28 to 34
	UL 94 V-0 @ 0.125 in
Transistor Count	962 Devices
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test	

1. For additional information, see Application Note AND8003/D.

**Table 6. MAXIMUM RATINGS**

Symbol	Parameter	Condition 1	Condition 2	Rating	Unit
V <sub>CC</sub>	PECL Mode Power Supply	V <sub>EE</sub> = 0 V		6	V
V <sub>EE</sub>	NECL Mode Power Supply	V <sub>CC</sub> = 0 V		-6	V
V <sub>I</sub>	PECL Mode Input Voltage NECL Mode Input Voltage	V <sub>EE</sub> = 0 V V <sub>CC</sub> = 0 V	V <sub>I</sub> ≤ V <sub>CC</sub> V <sub>I</sub> ≥ V <sub>EE</sub>	6 -6	V V
I <sub>out</sub>	Output Current	Continuous Surge		50 100	mA mA
I <sub>BB</sub>	V <sub>BB</sub> Sink/Source			± 0.5	mA
T <sub>A</sub>	Operating Temperature Range			-40 to +85	°C
T <sub>stg</sub>	Storage Temperature Range			-65 to +150	°C
θ <sub>JA</sub>	Thermal Resistance (Junction-to-Ambient)	0 lfpm 500 lfpm	LQFP-32 LQFP-32	80 55	°C/W °C/W
θ <sub>JC</sub>	Thermal Resistance (Junction-to-Case)	Standard Board	LQFP-32	12 to 17	°C/W
T <sub>sol</sub>	Wave Solder	< 2 to 3 sec @ 248°C		265	°C

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

# MC10EP446, MC100EP446

**Table 7. 10EP DC CHARACTERISTICS, PECL**  $V_{CC} = 3.3\text{ V}$ ,  $V_{EE} = 0\text{ V}$  (Note 2)

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$I_{EE}$	Power Supply Current	90	110	130	90	110	130	95	115	135	mA
$V_{OH}$	Output HIGH Voltage (Note 3)	2165	2290	2415	2230	2355	2480	2290	2415	2540	mV
$V_{OL}$	Output LOW Voltage (Note 3)	1365	1490	1615	1430	1555	1680	1490	1615	1740	mV
$V_{IH}$	Input HIGH Voltage (Single-Ended)										
	CMOS	2000		3300	2000		3300	2000		3300	mV
	PECL	2090		3300	2155		3300	2215		3300	
TTL	2000		3300	2000		3300	2000		3300		
$V_{IL}$	Input LOW Voltage (Single-Ended)										
	CMOS	0		800	0		800	0		800	mV
	PECL	1365		1690	1460		1755	1490		1815	
TTL	0		800	0		800	0		800		
$V_{BB}$	Output Voltage Reference	1740	1840	1940	1805	1905	2005	1865	1965	2065	mV
$V_{IHCMR}$	Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 4)	2.0		3.3	2.0		3.3	2.0		3.3	V
$I_{IH}$	Input HIGH Current			150			150			150	$\mu\text{A}$
$I_{IL}$	Input LOW Current	0.5			0.5			0.5			$\mu\text{A}$

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

2. Input and output parameters vary 1:1 with  $V_{CC}$ .  $V_{EE}$  can vary +0.3 V to -2.2 V.

3. All loading with 50  $\Omega$  to  $V_{CC} - 2.0\text{ V}$ .

4.  $V_{IHCMR}$  min varies 1:1 with  $V_{EE}$ .  $V_{IHCMR}$  max varies 1:1 with  $V_{CC}$ . The  $V_{IHCMR}$  range is referenced to the most positive side of the differential input signal.

**Table 8. 10EP DC CHARACTERISTICS, PECL**  $V_{CC} = 5.0\text{ V}$ ,  $V_{EE} = 0\text{ V}$  (Note 5)

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$I_{EE}$	Power Supply Current	90	110	130	90	110	130	95	115	135	mA
$V_{OH}$	Output HIGH Voltage (Note 6)	3865	3950	4115	3930	4055	4180	3990	4115	4240	mV
$V_{OL}$	Output LOW Voltage (Note 6)	3065	3190	3315	3130	3255	3380	3190	3315	3440	mV
$V_{IH}$	Input HIGH Voltage (Single-Ended)										
	CMOS	3500		5000	3500		5000	3500		5000	mV
	PECL	3790		5000	3855		5000	3915		5000	
TTL	2000		5000	2000		5000	2000		5000		
$V_{IL}$	Input LOW Voltage (Single-Ended)										
	CMOS	0		1500	0		1500	0		1500	mV
	PECL	3065		3390	3130		3455	3190		3915	
TTL	0		800	0		800	0		800		
$V_{BB}$	Output Voltage Reference	3440	3540	3640	3505	3605	3705	3565	3665	3765	mV
$V_{IHCMR}$	Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 7)	2.0		5.0	2.0		5.0	2.0		5.0	V
$I_{IH}$	Input HIGH Current			150			150			150	$\mu\text{A}$
$I_{IL}$	Input LOW Current	0.5			0.5			0.5			$\mu\text{A}$

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

5. Input and output parameters vary 1:1 with  $V_{CC}$ .  $V_{EE}$  can vary +2.0 V to -0.5 V.

6. All loading with 50  $\Omega$  to  $V_{CC} - 2.0\text{ V}$ .

7.  $V_{IHCMR}$  min varies 1:1 with  $V_{EE}$ .  $V_{IHCMR}$  max varies 1:1 with  $V_{CC}$ . The  $V_{IHCMR}$  range is referenced to the most positive side of the differential input signal.

# MC10EP446, MC100EP446

**Table 9. 10EP DC CHARACTERISTICS, NECL**  $V_{CC} = 0\text{ V}$ ,  $V_{EE} = -5.5\text{ V}$  to  $-3.0\text{ V}$  (Note 8)

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$I_{EE}$	Power Supply Current	90	110	130	90	110	130	95	115	135	mA
$V_{OH}$	Output HIGH Voltage (Note 9)	-1135	-1010	-885	-1070	-945	-820	-1010	-885	-760	mV
$V_{OL}$	Output LOW Voltage (Note 9)	-1935	-1810	-1685	-1870	-1745	-1620	-1810	-1685	-1560	mV
$V_{IH}$	Input HIGH Voltage (Single-Ended)	-1210		-885	-1145		-820	-1085		-760	mV
$V_{IL}$	Input LOW Voltage (Single-Ended)	-1935		-1610	-1870		-1545	-1810		-1485	mV
$V_{BB}$	Output Voltage Reference	-1560	-1460	-1360	-1495	-1395	-1295	-1435	-1335	-1235	mV
$V_{IHCMR}$	Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 10)	$V_{EE}+2.0$		0.0	$V_{EE}+2.0$		0.0	$V_{EE}+2.0$		0.0	V
$I_{IH}$	Input HIGH Current			150			150			150	$\mu\text{A}$
$I_{IL}$	Input LOW Current	0.5			0.5			0.5			$\mu\text{A}$

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

8. Input and output parameters vary 1:1 with  $V_{CC}$ .

9. All loading with  $50\ \Omega$  to  $V_{CC} - 2.0\text{ V}$ .

10.  $V_{IHCMR}$  min varies 1:1 with  $V_{EE}$ ,  $V_{IHCMR}$  max varies 1:1 with  $V_{CC}$ . The  $V_{IHCMR}$  range is referenced to the most positive side of the differential input signal.

**Table 10. 100EP DC CHARACTERISTICS, PECL**  $V_{CC} = 3.3\text{ V}$ ,  $V_{EE} = 0\text{ V}$  (Note 11)

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$I_{EE}$	Power Supply Current	90	110	130	90	110	130	95	115	135	mA
$V_{OH}$	Output HIGH Voltage (Note 12)	2155	2280	2405	2155	2280	2405	2155	2280	2405	mV
$V_{OL}$	Output LOW Voltage (Note 12)	1355	1480	1605	1355	1480	1605	1355	1480	1605	mV
$V_{IH}$	Input HIGH Voltage (Single-Ended)										
	CMOS	2000		3300	2000		3300	2000		3300	mV
	PECL	2075		3300	2075		3300	2075		3300	
	TTL	2000		3300	2000		3300	2000		3300	
$V_{IL}$	Input LOW Voltage (Single-Ended)										
	CMOS	0		800	0		800	0		800	mV
	PECL	1355		1675	1355		1675	1355		1675	
	TTL	0		800	0		800	0		800	
$V_{BB}$	Output Voltage Reference	1775	1875	1975	1775	1875	1975	1775	1875	1975	mV
$V_{IHCMR}$	Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 13)	2.0		3.3	2.0		3.3	2.0		3.3	V
$I_{IH}$	Input HIGH Current			150			150			150	$\mu\text{A}$
$I_{IL}$	Input LOW Current	0.5			0.5			0.5			$\mu\text{A}$

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

11. Input and output parameters vary 1:1 with  $V_{CC}$ .  $V_{EE}$  can vary +0.3 V to -2.2 V.

12. All loading with  $50\ \Omega$  to  $V_{CC} - 2.0\text{ V}$ .

13.  $V_{IHCMR}$  min varies 1:1 with  $V_{EE}$ ,  $V_{IHCMR}$  max varies 1:1 with  $V_{CC}$ . The  $V_{IHCMR}$  range is referenced to the most positive side of the differential input signal.

# MC10EP446, MC100EP446

**Table 11. 100EP DC CHARACTERISTICS, PECL**  $V_{CC} = 5.0\text{ V}$ ,  $V_{EE} = 0\text{ V}$  (Note 14)

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$I_{EE}$	Power Supply Current	90	110	130	90	110	130	95	115	135	mA
$V_{OH}$	Output HIGH Voltage (Note 15)	3855	3980	4105	3855	3980	4105	3855	3980	4105	mV
$V_{OL}$	Output LOW Voltage (Note 15)	3055	3180	3305	3055	3180	3305	3055	3180	3305	mV
$V_{IH}$	Input HIGH Voltage (Single-Ended)										
	CMOS	3500		5000	3500		5000	3500		5000	mV
	PECL	3775		5000	3775		5000	3775		5000	
	TTL	2000		5000	2000		5000	2000		5000	
$V_{IL}$	Input LOW Voltage (Single-Ended)										
	CMOS	0		1500	0		1500	0		1500	mV
	PECL	3055		3375	3055		3375	3055		3375	
	TTL	0		800	0		800	0		800	
$V_{BB}$	Output Voltage Reference	3475	3575	3675	3475	3575	3675	3475	3575	3675	mV
$V_{IHCMR}$	Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 16)	2.0		5.0	2.0		5.0	2.0		5.0	V
$I_{IH}$	Input HIGH Current			150			150			150	$\mu\text{A}$
$I_{IL}$	Input LOW Current	0.5			0.5			0.5			$\mu\text{A}$

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

14. Input and output parameters vary 1:1 with  $V_{CC}$ .  $V_{EE}$  can vary +2.0 V to -0.5 V.

15. All loading with 50  $\Omega$  to  $V_{CC} - 2.0\text{ V}$ .

16.  $V_{IHCMR}$  min varies 1:1 with  $V_{EE}$ ,  $V_{IHCMR}$  max varies 1:1 with  $V_{CC}$ . The  $V_{IHCMR}$  range is referenced to the most positive side of the differential input signal.

**Table 12. 100EP DC CHARACTERISTICS, NECL**  $V_{CC} = 0\text{ V}$ ,  $V_{EE} = -5.5\text{ V}$  to  $-3.0\text{ V}$  (Note 17)

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$I_{EE}$	Power Supply Current	90	110	130	90	110	130	95	115	135	mA
$V_{OH}$	Output HIGH Voltage (Note 18)	-1145	-1020	-895	-1145	-1020	-895	-1145	-1020	-895	mV
$V_{OL}$	Output LOW Voltage (Note 18)	-1945	-1820	-1695	-1945	-1820	-1695	-1945	-1820	-1695	mV
$V_{IH}$	Input HIGH Voltage (Single-Ended)	-1225		-880	-1225		-880	-1225		-880	mV
$V_{IL}$	Input LOW Voltage (Single-Ended)	-1945		-1625	-1945		-1625	-1945		-1625	mV
$V_{BB}$	Output Voltage Reference	-1525	-1425	-1325	-1525	-1425	-1325	-1525	-1425	-1325	mV
$V_{IHCMR}$	Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 19)	$V_{EE}+2.0$		0.0	$V_{EE}+2.0$		0.0	$V_{EE}+2.0$		0.0	V
$I_{IH}$	Input HIGH Current			150			150			150	$\mu\text{A}$
$I_{IL}$	Input LOW Current	0.5			0.5			0.5			$\mu\text{A}$

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

17. Input and output parameters vary 1:1 with  $V_{CC}$ .

18. All loading with 50  $\Omega$  to  $V_{CC} - 2.0\text{ V}$ .

19.  $V_{IHCMR}$  min varies 1:1 with  $V_{EE}$ ,  $V_{IHCMR}$  max varies 1:1 with  $V_{CC}$ . The  $V_{IHCMR}$  range is referenced to the most positive side of the differential input signal.



# MC10EP446, MC100EP446

**Table 13. AC CHARACTERISTICS**  $V_{CC} = 0\text{ V}$ ;  $V_{EE} = -3.0\text{ V to }-5.5\text{ V}$  or  $V_{CC} = 3.0\text{ V to }5.5\text{ V}$ ;  $V_{EE} = 0\text{ V}$  (Note 20)

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$f_{max}$	Maximum Frequency (Figure 14)										GHz
	CKSEL High CKSEL Low	3.2 1.6	3.4 1.7		3.2 1.6	3.4 1.7		3.2 1.6	3.4 1.7		
$t_{PLH}$ , $t_{PHL}$	Propagation Delay to Output Differential CKSEL = 0										ps
	CLK TO $S_{OUT}$ , CLK TO PCLK	650 700	750 800	850 900	700 750	800 850	900 950	725 775	850 900	975 1025	
	CKSEL = 1										ps
	CLK TO $S_{OUT}$ , CLK TO PCLK	775 850	875 950	975 1050	825 900	925 1000	1025 1100	875 950	1000 1075	1125 1200	
$t_S$	Setup Time D to CLK+ (Figure 3)	-375	-425		-400	-450		-450	-500		ps
	SYNC- to CLK- (Figure 4)	200	140		200	140		200	140		
	CKEN+ to CLK- (Figure 5)	70	40		70	40		70	40		
$t_H$	Hold Time D to CLK+ (Figure 3)	-525	-575		-550	-600		-600	-650		ps
	SYNC- to CLK- (Figure 4)	0			0			0			
	CLK- to CKEN- (Figure 5)	75	45		75	45		75	45		
$t_{pw}$	Minimum Pulse Width (Note 22) Data (D0-D7)	150			150			150			ps
	SYNC	200			200			200			
	CKEN	145			145			145			
$t_{JITTER}$	Random Clock Jitter (RMS) $\leq f_{max}$ Typ		0.2	< 1		0.2	< 1		0.2	< 1	ps
$V_{PP}$	Input Differential Voltage Swing (Note 21)	150	800	1200	150	800	1200	150	800	1200	mV
$t_r$ $t_f$	Output Rise/Fall Times (20% – 80%) $S_{OUT}$	50	100	150	70	120	170	90	140	190	ps

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

20. Measured using a 750 mV source, 50% duty cycle clock source. All loading with 50  $\Omega$  to  $V_{CC} - 2.0\text{ V}$ .

21.  $V_{PP}(\text{min})$  is the minimum input swing for which AC parameters are guaranteed.

22. The minimum pulse width is valid only if the setup and hold times are respected.

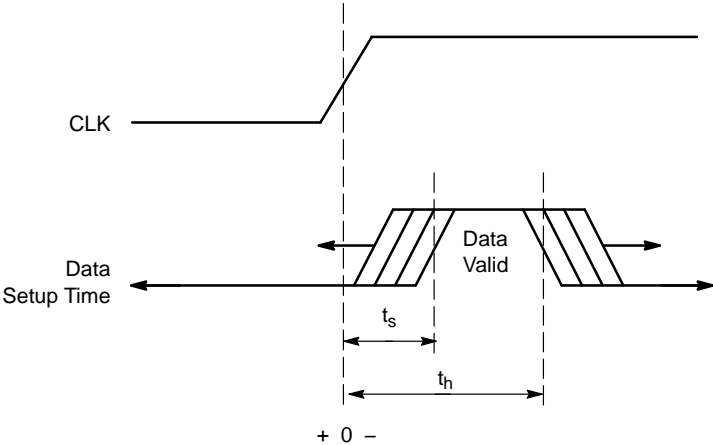


Figure 3. Setup and Hold Time for Data

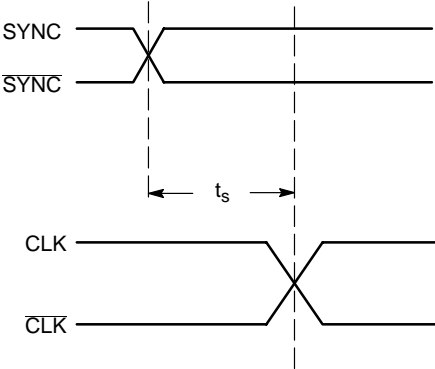


Figure 4. Setup Time for SYNC

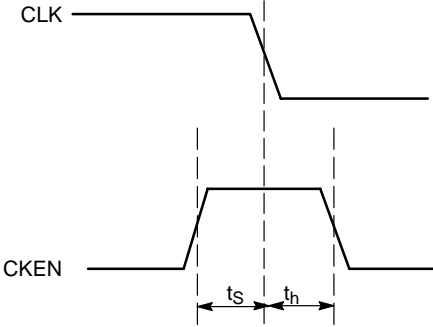


Figure 5. Setup and Hold Time for CKEN

# MC10EP446, MC100EP446

## APPLICATION INFORMATION

The MC10/100EP446 is an integrated 8:1 parallel to serial converter. An attribute for EP446 is that the parallel inputs D0–D7 (Pins 17 – 24) can be configured to accept either CMOS, ECL, or TTL level signals by a combination of interconnects between  $V_{EF}$  (Pin 27) and  $V_{CF}$  (Pin 26) pins. For CMOS input levels, leave  $V_{EF}$  and  $V_{CF}$  open. For ECL operation, short  $V_{CF}$  and  $V_{EF}$  (Pins 26 and 27). For TTL operation, connect a 1.5 V supply reference to  $V_{CF}$  and leave the  $V_{EF}$  pin open. The 1.5 V reference voltage to  $V_{CF}$  pin can be accomplished by placing a 1.5 k $\Omega$  or 500  $\Omega$  between  $V_{CF}$  and  $V_{EE}$  for 3.3 V or 5.0 V power supplies, respectively.

Note: all pins requiring ECL voltage inputs must have a 50  $\Omega$  terminating resistor to  $V_{TT}$  ( $V_{TT} = V_{CC} - 2.0$  V).

The CKSEL input (Pin 2) is provided to enable the user to select the serial data rate output between internal clock data rate or twice the internal clock data rate. For CKSEL LOW operation, the time from when the parallel data is latched ① to when the data is seen on the SOUT ② is on the falling edge of the 7<sup>th</sup> clock cycle plus internal propagation delay (Figure 6). Note the PCLK switches on the falling edge of CLK.

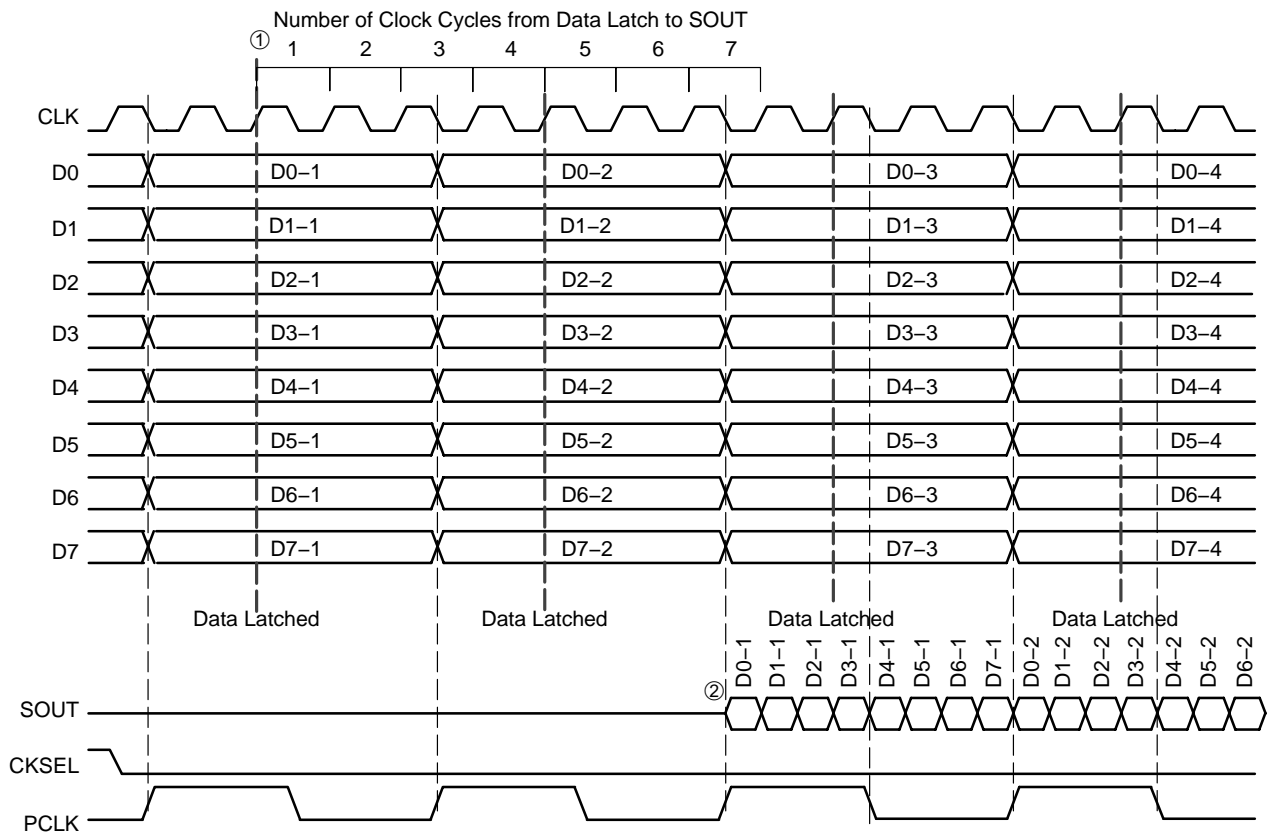


Figure 6. Timing Diagram 1:8 Parallel to Serial Conversion with CKSEL LOW

# MC10EP446, MC100EP446

Similarly, for CKSEL HIGH operation, the time from when the parallel data is latched ① to when the data is seen on the SOUT ② is on the rising edge of the 14<sup>th</sup> clock cycle plus internal propagation delay (Figure 7). Furthermore, the PCLK switches on the rising edge of CLK.

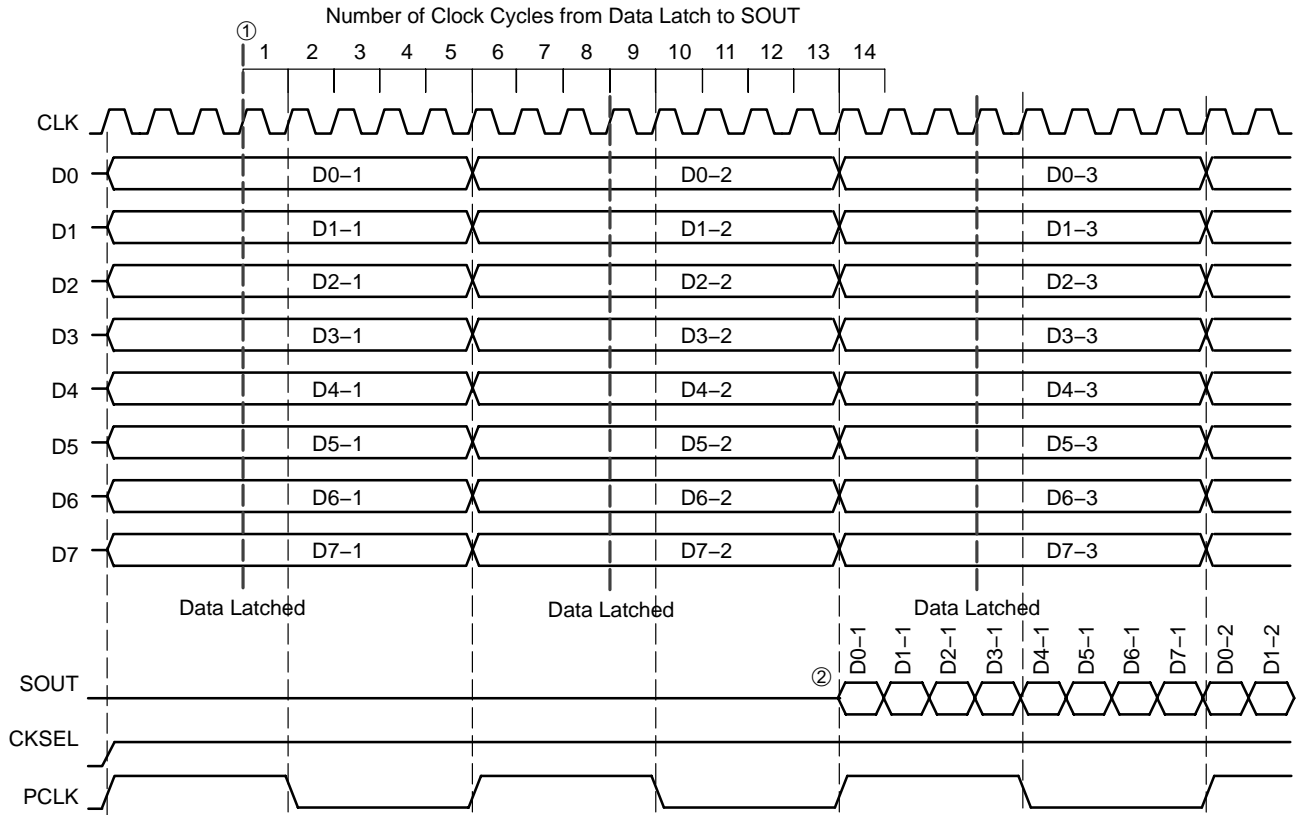


Figure 7. Timing Diagram 1:8 Parallel to Serial Conversion with CKSEL HIGH

# MC10EP446, MC100EP446

The device also features a differential SYNC input (Pins 29 and 30), which asynchronously reset all internal flip-flops and clock circuitry on the rising edge of SYNC. The release of SYNC is a synchronous process, which ensures that no runt serial data bits are generated. The falling edge of the SYNC followed by a falling edge of CLK initiates the start of the conversion process on the next rising edge of CLK (Figures 8 and 9). As shown in the figures below, the device will start to latch the parallel input data after the a falling edge of SYNC ①, followed by the falling edge CLK ②, on the next rising edge of edge of CLK ③ for CKSEL LOW

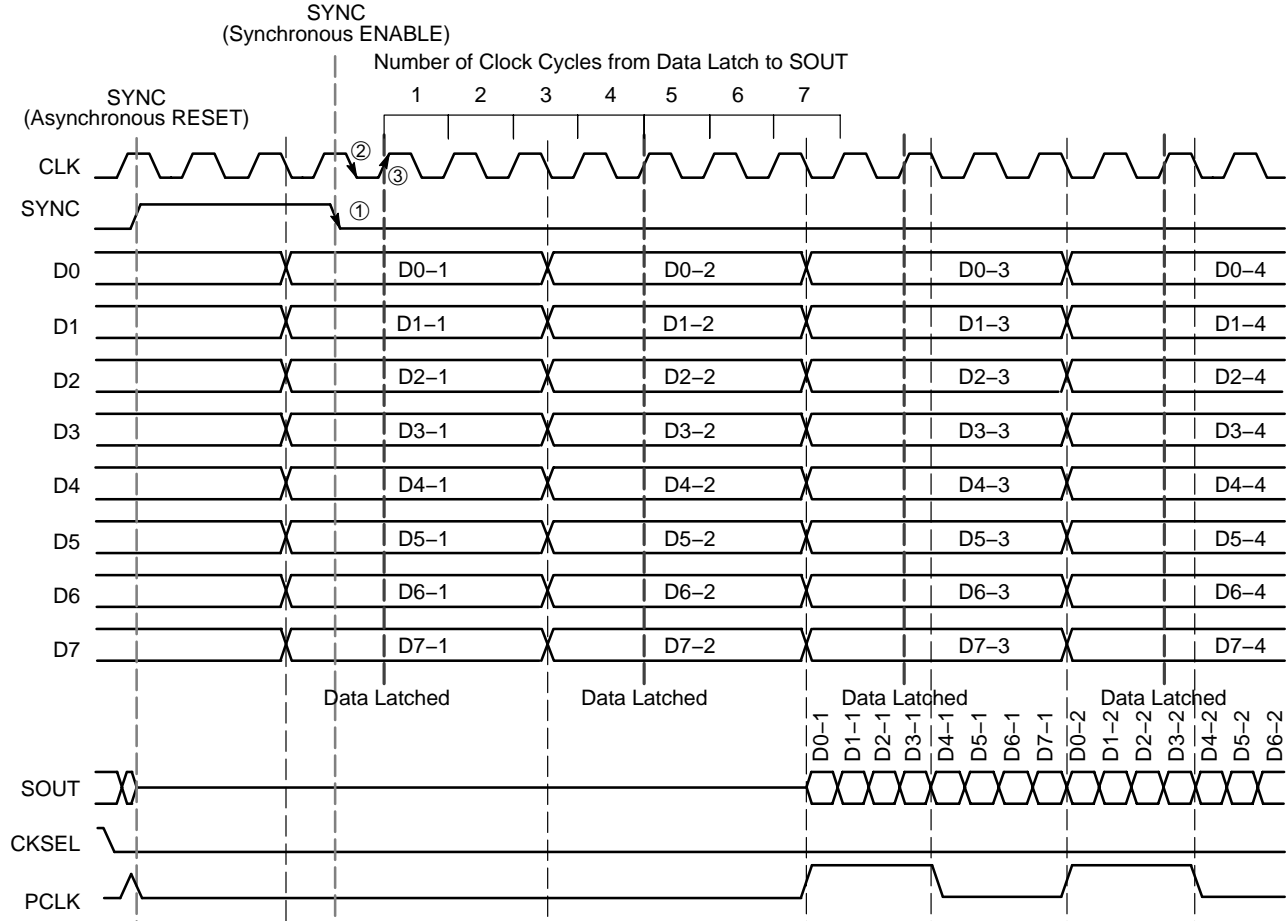


Figure 8. Timing Diagram 1:8 Parallel to Serial Conversion with CKSEL LOW and SYNC

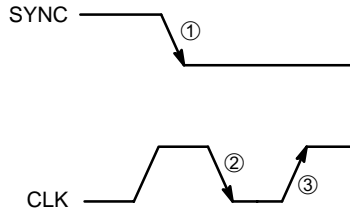


Figure 9. Synchronous Release of SYNC for CKSEL LOW

# MC10EP446, MC100EP446

For CKSEL HIGH, as shown in the timing diagrams below, the device will start to latch the parallel input data after the falling edge of SYNC ①, followed by the falling edge CLK ②, on the second rising edge of CLK ③ (Figures 10 and 11).

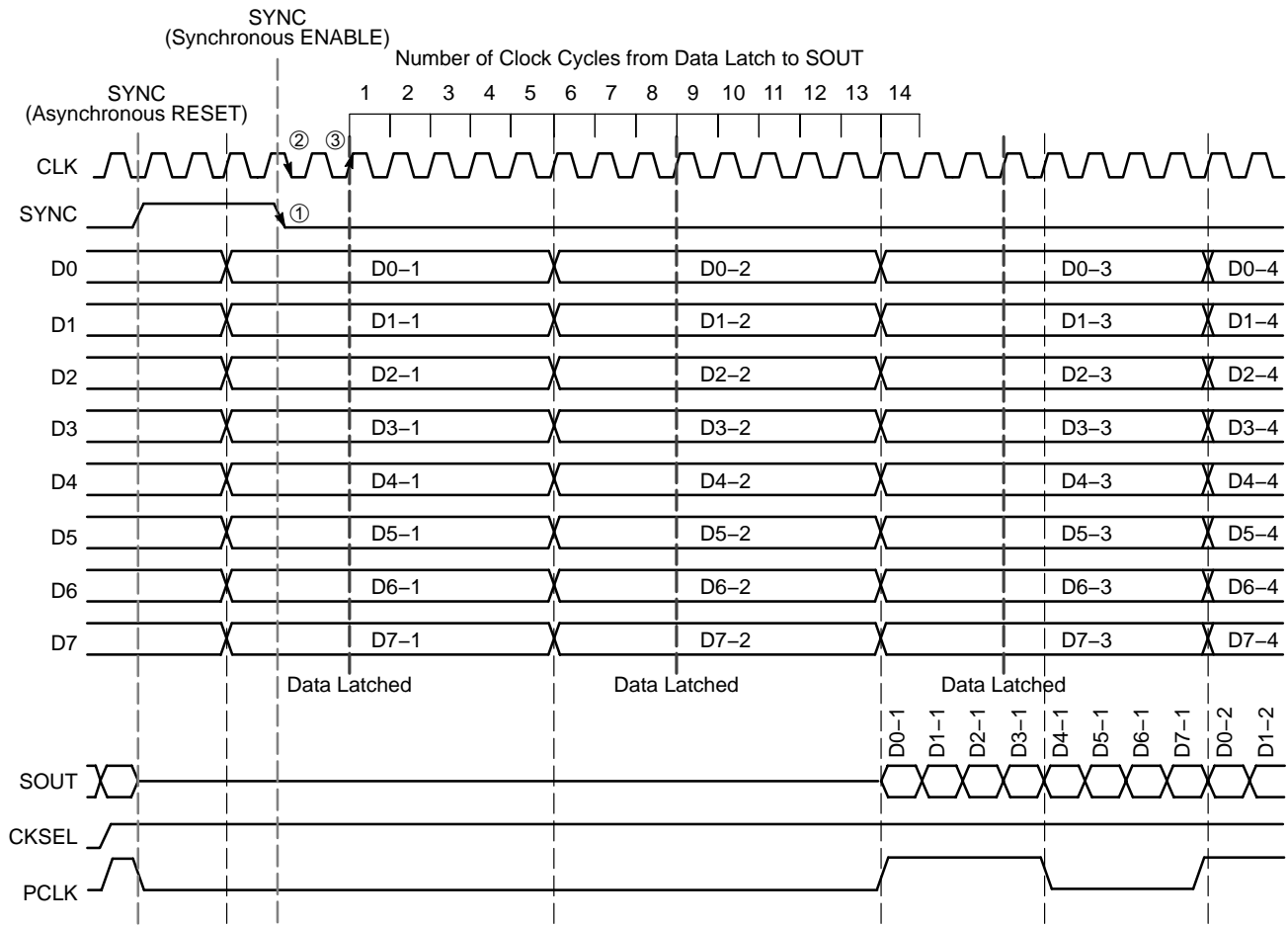


Figure 10. Timing Diagram 1:8 Parallel to Serial Conversion with CKSEL HIGH and SYNC

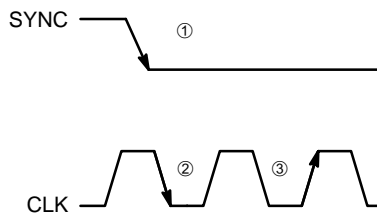


Figure 11. Synchronous Release of SYNC for CKSEL HIGH

## MC10EP446, MC100EP446

The differential synchronous CKEN inputs (Pins 6 and 7), disable the internal clock circuitry. The synchronous CKEN will suspend all of the device activities and prevent runt pulses from being generated. The rising edge of CKEN followed by the falling edge of CLK will suspend all activities. The falling edge of CKEN followed by the falling edge of CLK will resume all activities (Figure 12).

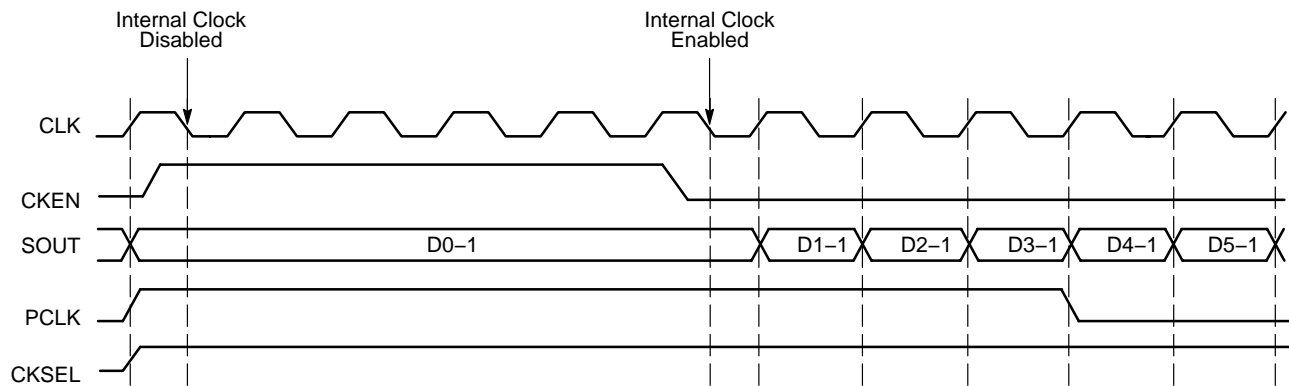


Figure 12. Timing Diagram with CKEN with CKSEL HIGH

The differential PCLK output (Pins 14 and 15) is a word framer and can help the user synchronize the serial data output,  $S_{OUT}$  (Pins 11 and 12), in their applications. Furthermore, PCLK can be used as a trigger for input parallel data (Figure 13).

An internally generated voltage supply, the  $V_{BB}$  pin, is available to this device only. For single-ended input

conditions, the unused differential input is connected to  $V_{BB}$  as a switching reference voltage.  $V_{BB}$  may also rebias AC coupled inputs. When used, decouple  $V_{BB}$  and  $V_{CC}$  via a  $0.01 \mu\text{F}$  capacitor and limit current sourcing or sinking to  $0.5 \text{ mA}$ . When not used,  $V_{BB}$  should be left open. Also, both outputs of the differential pair must be terminated ( $50 \Omega$  to  $V_{TT}$ ) even if only one output is used.

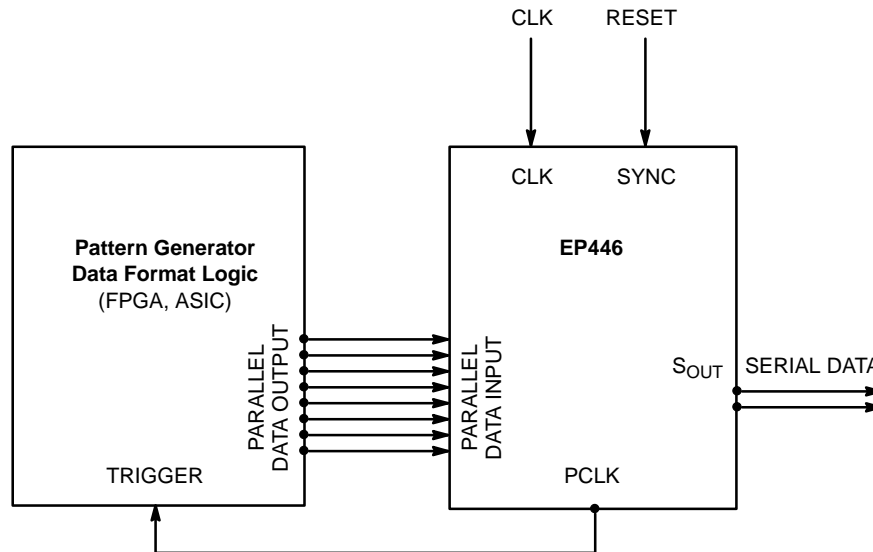
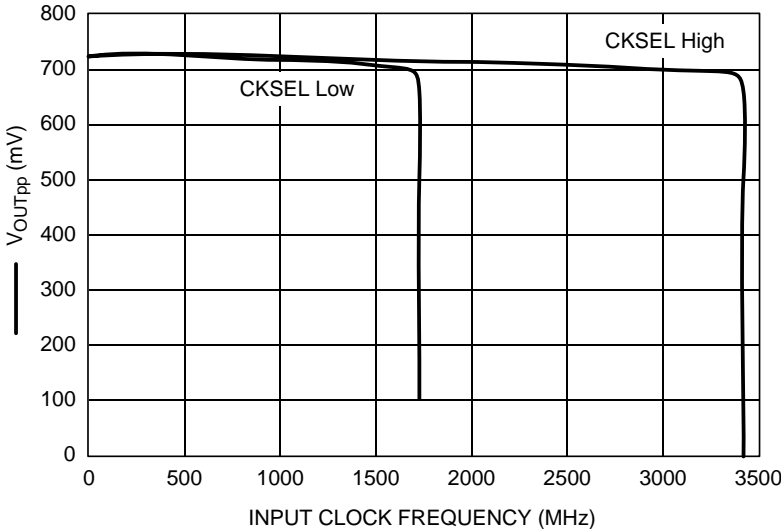
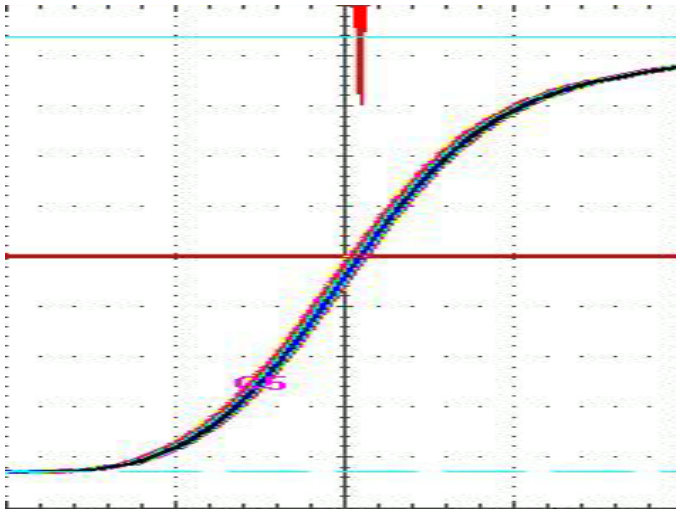


Figure 13. PCLK as Trigger Application

**MC10EP446, MC100EP446**



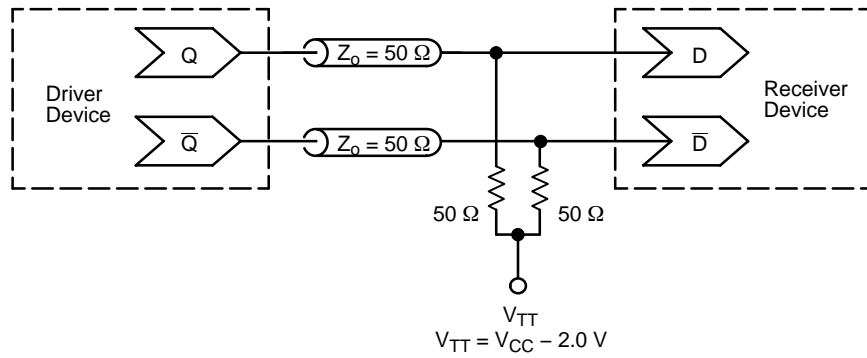
**Figure 14. Typical V<sub>OUTPP</sub> versus Input Clock Frequency, 25°C**



**Figure 15. SOUT System Jitter Measurement**  
 (Condition: 3.4 GHz input frequency, CKSEL HIGH, BEOFE32 bit pattern on SOUT)



## MC10EP446, MC100EP446



**Figure 16. Typical Termination for Output Driver and Device Evaluation  
(See Application Note AND8020/D – Termination of ECL Logic Devices.)**

### ORDERING INFORMATION

Device	Package	Shipping <sup>†</sup>
MC10EP446FA	LQFP-32	250 Units / Tray
MC10EP446FAR2	LQFP-32	2000 / Tape & Reel
MC100EP446FA	LQFP-32	250 Units / Tray
MC100EP446FAR2	LQFP-32	2000 / Tape & Reel

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

## MC10EP446, MC100EP446

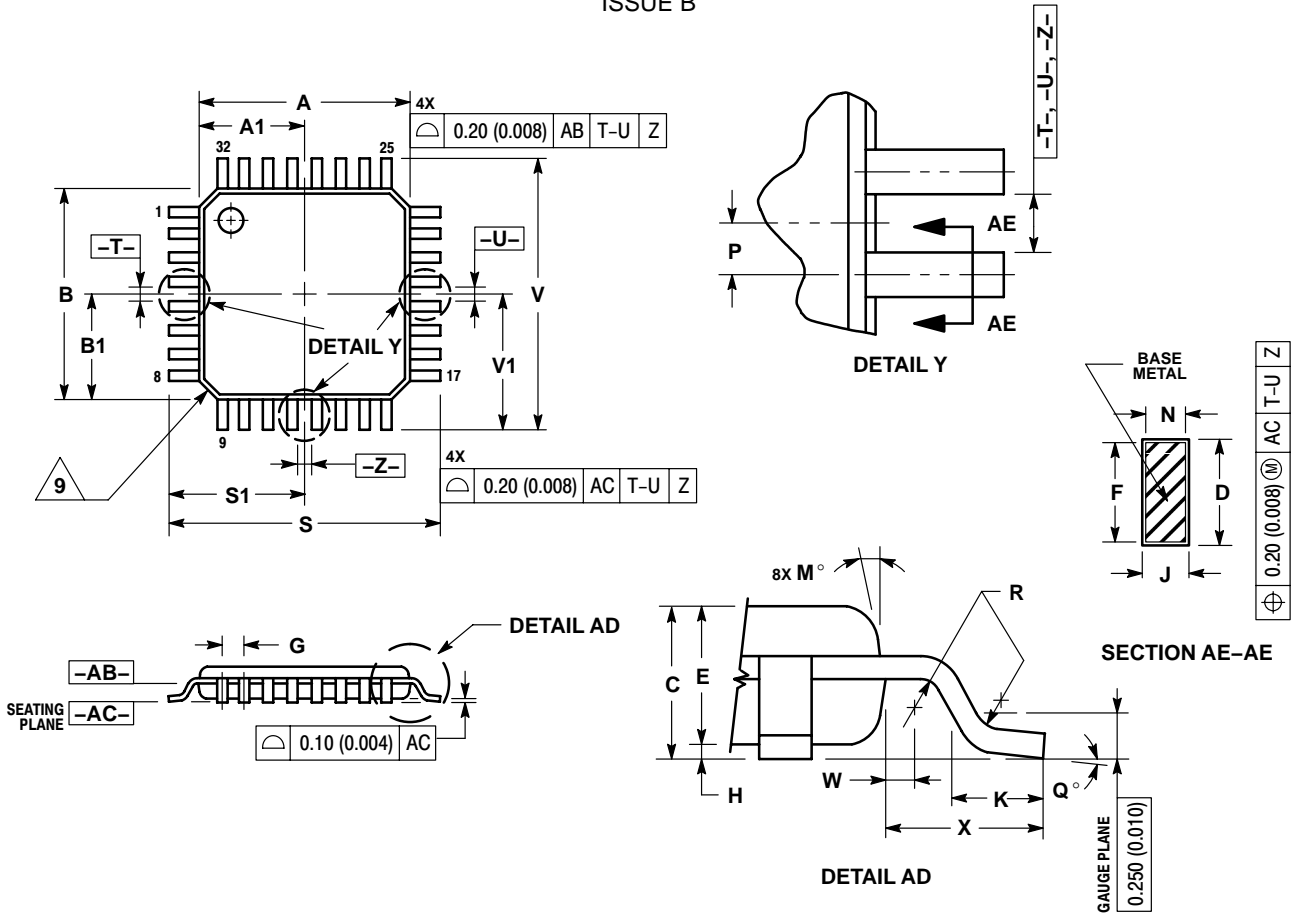
### Resource Reference of Application Notes

- AN1405/D** – ECL Clock Distribution Techniques
- AN1406/D** – Designing with PECL (ECL at +5.0 V)
- AN1503/D** – ECLinPS™ I/O SPICE Modeling Kit
- AN1504/D** – Metastability and the ECLinPS Family
- AN1568/D** – Interfacing Between LVDS and ECL
- AN1642/D** – The ECL Translator Guide
- AND8001/D** – Odd Number Counters Design
- AND8002/D** – Marking and Date Codes
- AND8020/D** – Termination of ECL Logic Devices
- AND8066/D** – Interfacing with ECLinPS
- AND8090/D** – AC Characteristics of ECL Devices

# MC10EP446, MC100EP446

## PACKAGE DIMENSIONS

LQFP  
FA SUFFIX  
32-LEAD PLASTIC PACKAGE  
CASE 873A-02  
ISSUE B




### NOTES:

- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
- CONTROLLING DIMENSION: MILLIMETER.
- DATUM PLANE -AB- IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
- DATUMS -T-, -U-, AND -Z- TO BE DETERMINED AT DATUM PLANE -AB-.
- DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE -AC-.
- DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.250 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -AB-.
- DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE D DIMENSION TO EXCEED 0.520 (0.020).
- MINIMUM SOLDER PLATE THICKNESS SHALL BE 0.0076 (0.0003).
- EXACT SHAPE OF EACH CORNER MAY VARY FROM DEPICTION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	7.000	BSC	0.276	BSC
A1	3.500	BSC	0.138	BSC
B	7.000	BSC	0.276	BSC
B1	3.500	BSC	0.138	BSC
C	1.400	1.600	0.055	0.063
D	0.300	0.450	0.012	0.018
E	1.350	1.450	0.053	0.057
F	0.300	0.400	0.012	0.016
G	0.800	BSC	0.031	BSC
H	0.050	0.150	0.002	0.006
J	0.090	0.200	0.004	0.008
K	0.500	0.700	0.020	0.028
M	12°	REF	12°	REF
N	0.090	0.160	0.004	0.006
P	0.400	BSC	0.016	BSC
Q	1°	5°	1°	5°
R	0.150	0.250	0.006	0.010
S	9.000	BSC	0.354	BSC
S1	4.500	BSC	0.177	BSC
V	9.000	BSC	0.354	BSC
V1	4.500	BSC	0.177	BSC
W	0.200	REF	0.008	REF
X	1.000	REF	0.039	REF

# MC10EP446, MC100EP446

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