OKI Semiconductor

This version: Jan. 1998
Previous version: Aug. 1996

MSM521004

262,144-Word × 4-Bit CMOS STATIC RAM

DESCRIPTION

The MSM521004 is a 262,144-word by 4-bit CMOS fast static RAM featuring a single 5 V power supply operation and direct TTL input/output compatibility. Since the circuitry is completely static, external clock and refreshing operations are unnecessary, making this device very easy to use. The MSM521004 uses NMOS cells and CMOS peripherals and provides high-speed operation at 17 ns access time. In addition, the MSM521004 is provided with a chip enable signal ($\overline{CE}$) suited to the power-down function, an output enable signal ($\overline{OE}$) suited to the I/O bus line control.

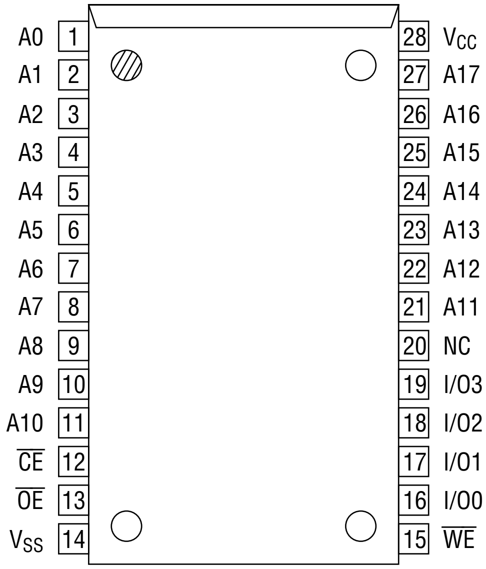
FEATURES

- 262,144-word × 4-bit configuration
- Single 5 V power supply
- Fully static operation
- Operating temperature range: Ta = 0°C to 70°C
- Power dissipation
  Standby: 1 mA (Max.)
  Operation:
  - 17 140 mA (Max.)
  - 20 130 mA (Max.)
  - 25 120 mA (Max.)
- Access time:
  - 17 17 ns (Max.)
  - 20 20 ns (Max.)
  - 25 25 ns (Max.)
- (Input/Output) TTL compatible
- Power-down function by chip enable signal
- 3-state output
- Package:
  28-pin 400 mil plastic SOJ (SOJ28-P-400-1.27) (Product : MSM521004-xxJS)
  xx indicates speed rank.

PRODUCT FAMILY

Family	Access Time (Max.)	Package
MSM521004-17	17 ns	400 mil 28-pin SOJ
MSM521004-20	20 ns	
MSM521004-25	25 ns	

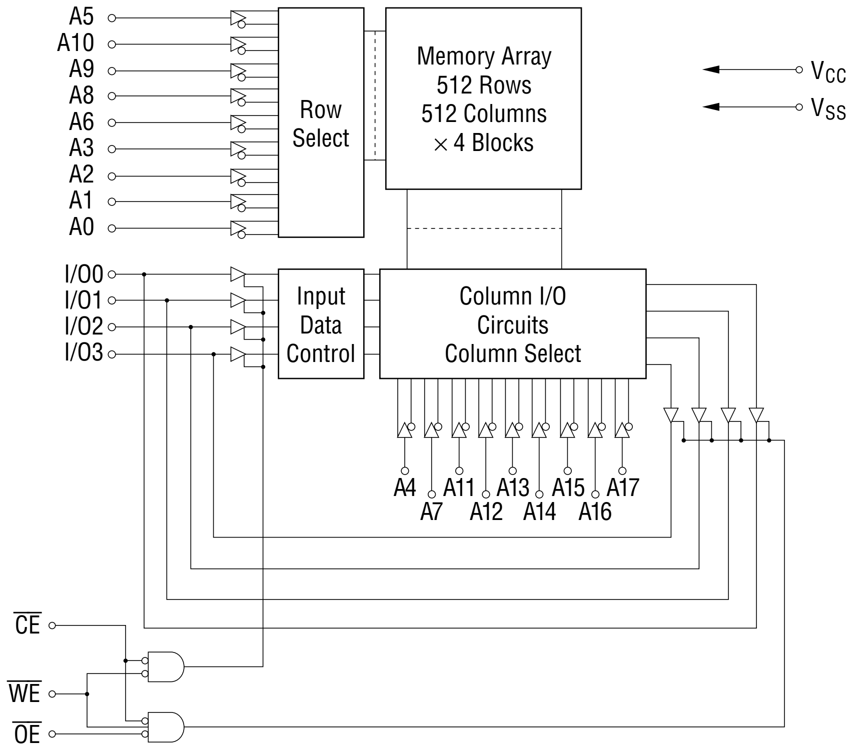
PIN CONFIGURATION (TOP VIEW)



28-Pin Plastic SOJ

Pin Name	Function
A0 - A17	Address Input
I/O0 - I/O3	Data Input/Output
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
V_{CC}, V_{SS}	Power Supply
NC	No Connection

BLOCK DIAGRAM



FUNCTION TABLE

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	Operating Mode	I/O Operation	Power Mode
H	*	*	Non Selectable	High-Z	Standby
L	L	H	Read Mode	D_{OUT}	Active
L	H	H	Read Mode	High-Z	Active
L	*	L	Write Mode	D_{IN}	Active

*Don't Care ("H" or "L")

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Power Supply Voltage	V_{CC}	Ta = 25°C, for V_{SS}	–0.3 to 7.0	V
Pin Voltage	V_T		–0.3* to V_{CC} + 0.3	V
Power Dissipation	P_D	Ta = 25°C	1.0	W
Operating Temperature	T_{opr}	—	0 to 70	°C
Storage Temperature	T_{stg}	—	–55 to 125	°C

* –3.0 V Min. for pulse width less than 10 ns.

Recommended Operating Conditions

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Power Supply Voltage	V_{CC}	—	4.5	5	5.5	V
	V_{SS}		0	0	0	V
Input High Voltage	V_{IH}	V_{CC} = 5 V ±10%	2.2	—	V_{CC} + 0.3	V
Input Low Voltage	V_{IL}		–0.3*	—	0.8	V
Load Capacitance	C_L	—	—	—	30	pF

* –3.0 V Min. for pulse width less than 10 ns.

Capacitance

(Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Condition	Min.	Max.	Unit
Input Capacitance	C_I	V_{IN} = 0 V	—	6	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$ = 0 V	—	8	pF

Note: This parameter is periodically sampled and not 100% tested.

DC Characteristics

(V_{CC} = 5 V ±10%, Ta = 0°C to 70°C)

Parameter	Symbol	Condition	MSM521004			Unit
			Min.	Typ.	Max.	
Input Leakage Current	I_{LI}	V_{IN} = 0 to V_{CC}	–10	—	10	µA
Output Leakage Current	I_{LO}	$\overline{CE} = V_{IH}$ or $\overline{OE} = V_{IH}$ or $\overline{WE} = V_{IL}$, V_{OUT} = 0 to V_{CC}	–10	—	10	µA
Output High Voltage	V_{OH}	I_{OH} = –4.0 mA	2.4	—	—	V
Output Low Voltage	V_{OL}	I_{OL} = 8.0 mA	—	—	0.4	V
Standby Power Supply Current	I_{CCS}	$\overline{CE} \geq V_{CC} - 0.2$ V, $V_{IN} \leq 0.2$ V or $V_{IN} \geq V_{CC} - 0.2$ V	—	—	1	mA
	I_{CCS1}	$\overline{CE} = V_{IH}$, T_{CYC} = Min. cycle	—	—	20	mA
Operating Power Supply Current	I_{CCA}	$\overline{CE} = V_{IL}$, T_{CYC} = Min. cycle, I_{OUT} = 0 mA	—	—	①	mA

① 521004-17 140 mA
521004-20 130 mA
521004-25 120 mA

AC Characteristics

Test Conditions

Parameter	Condition
Input Pulse Level	V_{IH} = 3 V, V_{IL} = 0 V
Input Rise and Fall Times	3 ns
Input/Output Timing Level	1.5 V
Output Load	See Figures

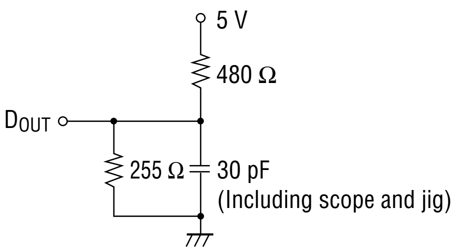


Figure 1 Output Load

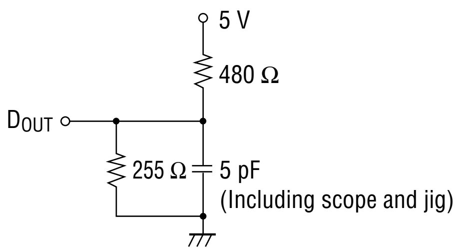


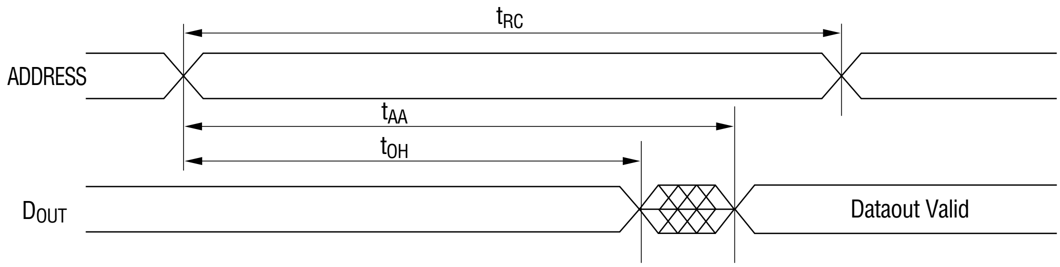
Figure 2 Output Load
(t_{OLZ}, t_{OHZ}, t_{CLZ}, t_{CHZ}, t_{WLZ}, t_{WHZ})

Read Cycle

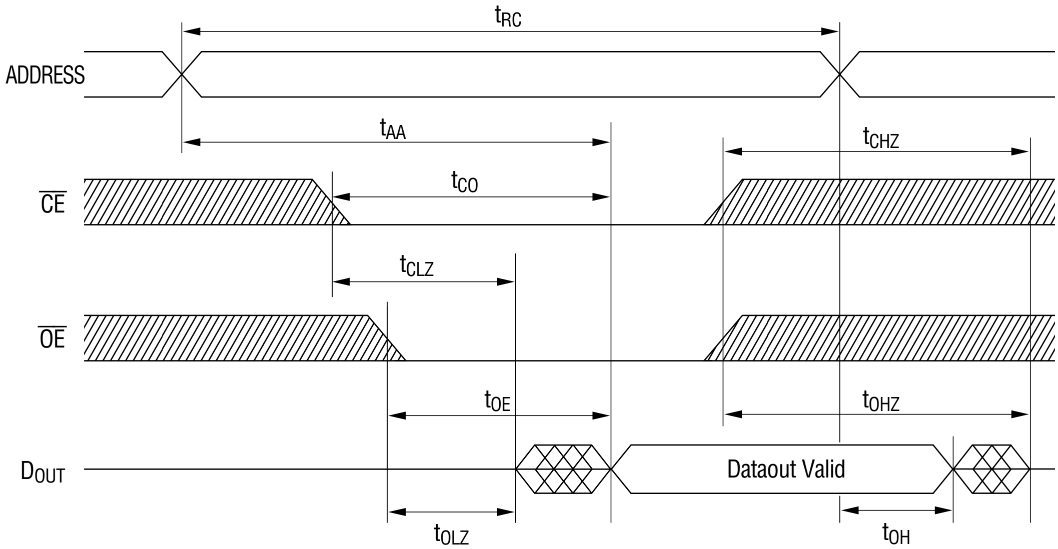
(V_{CC} = 5 V ±10%, Ta = 0°C to 70°C)

Parameter	Symbol	MSM521004-17		MSM521004-20		MSM521004-25		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle Time	t_{RC}	17	—	20	—	25	—	ns
Address Access Time	t_{AA}	—	17	—	20	—	25	ns
$\overline{CE}$ Access Time	t_{CO}	—	17	—	20	—	25	ns
$\overline{OE}$ Access Time	t_{OE}	—	9	—	10	—	12	ns
$\overline{CE}$ to Output in Low-Z	t_{CLZ}	3	—	3	—	3	—	ns
$\overline{OE}$ to Output in Low-Z	t_{OLZ}	0	—	0	—	0	—	ns
Output Hold Time from Address Change	t_{OH}	3	—	3	—	3	—	ns
$\overline{CE}$ to Output in High-Z	t_{CHZ}	—	7	—	8	—	10	ns
$\overline{OE}$ to Output in High-Z	t_{OHZ}	—	7	—	8	—	10	ns

Address Controlled Read ($\overline{WE}$ = H, $\overline{CE}$ = L, $\overline{OE}$ = L)



$\overline{CE}$, $\overline{OE}$ Controlled Read ($\overline{WE}$ = H)



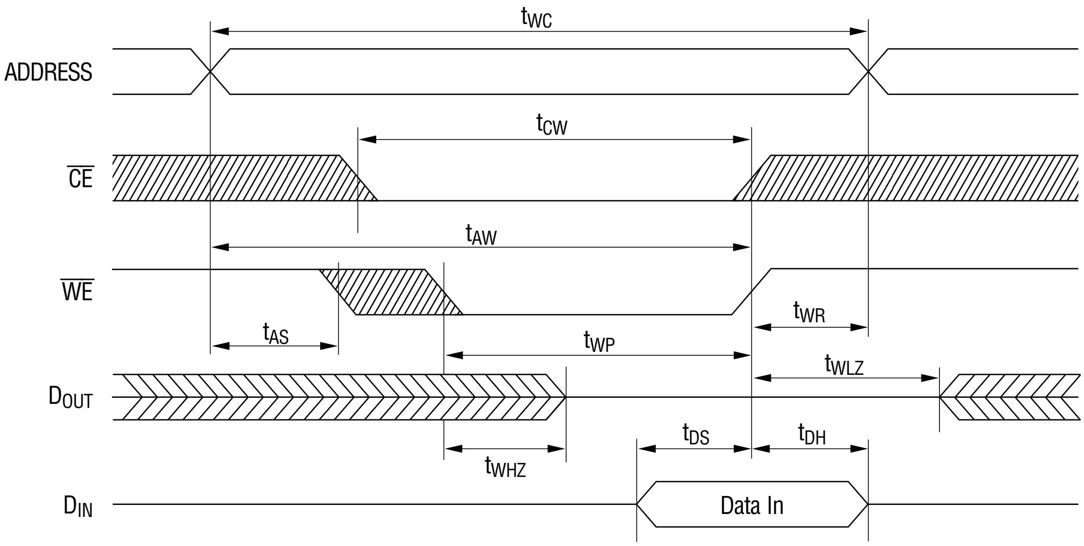
Notes :
1. A read cycle occurs during the overlap of $\overline{CE}$ = "L", $\overline{OE}$ = "L" and $\overline{WE}$ = "H".
2. t_{CHZ} and t_{OHZ} are specified by the time when DATA is floating, not defined by the output level.

Write Cycle

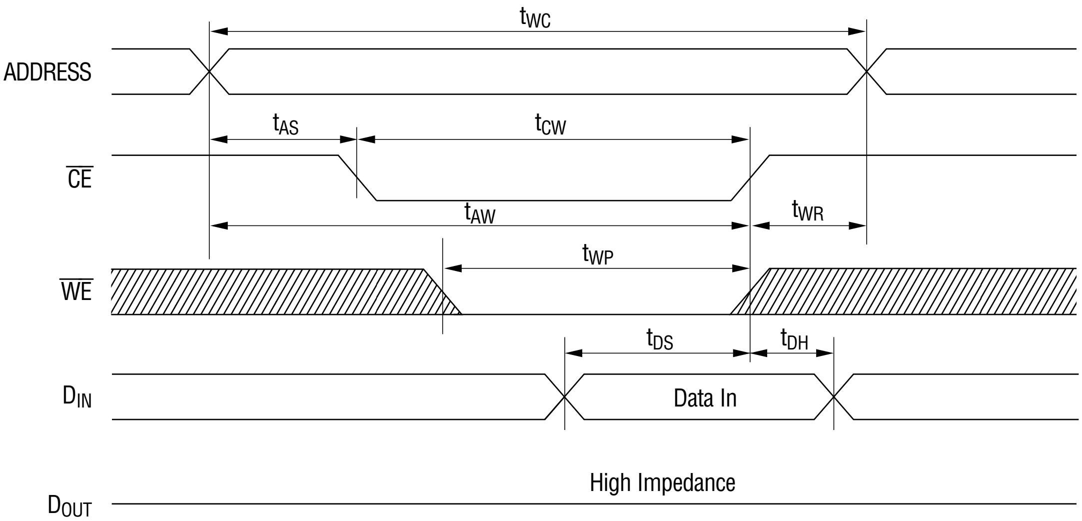
(V_{CC} = 5 V ±10%, Ta = 0°C to 70°C)

Parameter		Symbol	MSM521004-17		MSM521004-20		MSM521004-25		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
Write Cycle Time		t_{WC}	17	—	20	—	25	—	ns
Address Setup Time		t_{AS}	0	—	0	—	0	—	ns
Write Pulse Width		t_{WP}	13	—	15	—	20	—	ns
Write Recovery Time	$\overline{WE}$	t_{WR}	0	—	0	—	0	—	ns
	$\overline{CE}$		0	—	0	—	0	—	
Data Setup Time		t_{DS}	9	—	10	—	12	—	ns
Data Hold Time		t_{DH}	0	—	0	—	0	—	ns
$\overline{WE}$ to Output in High-Z		t_{WHZ}	—	7	—	8	—	10	ns
$\overline{CE}$ to End of Write		t_{CW}	13	—	15	—	20	—	ns
Address Valid to End of Write		t_{AW}	13	—	15	—	20	—	ns
Output Active from End of Write		t_{WLZ}	0	—	0	—	0	—	ns

$\overline{WE}$ Controlled Write ($\overline{OE}$ = L)



$\overline{CE}$ Controlled Write ($\overline{OE}$ = H)



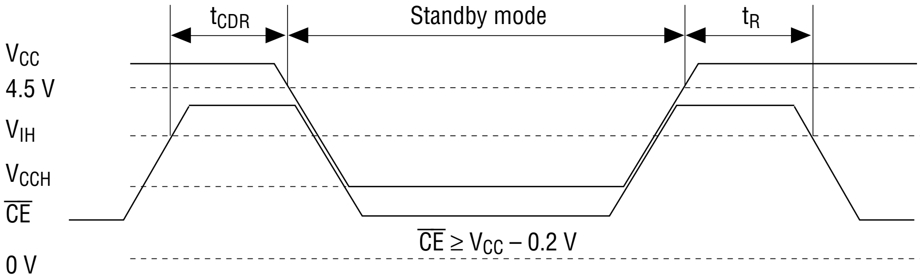
Notes:

1. A write cycle occurs during the overlap of $\overline{CE}$ = "L" and $\overline{WE}$ = "L".
2. $\overline{OE}$ may be either of "H" or "L" in the write cycle.
3. t_{AS} is specified from $\overline{CE}$ = "L" or $\overline{WE}$ = "L", whichever occurs last.
4. t_{WP} is an overlap time of $\overline{CE}$ = "L" and $\overline{WE}$ = "L".
5. t_{WR}, t_{DS} and t_{DH} are specified from $\overline{CE}$ = "H" or $\overline{WE}$ = "H", whichever occurs first.
6. t_{WHZ} is specified by the time when DATA output is floating, not defined by the output level.
7. When I/O pins are in the output mode, don't apply the inverted input signal to the output pins.

Data Retention Characteristics

(Ta = 0°C to 70°C)

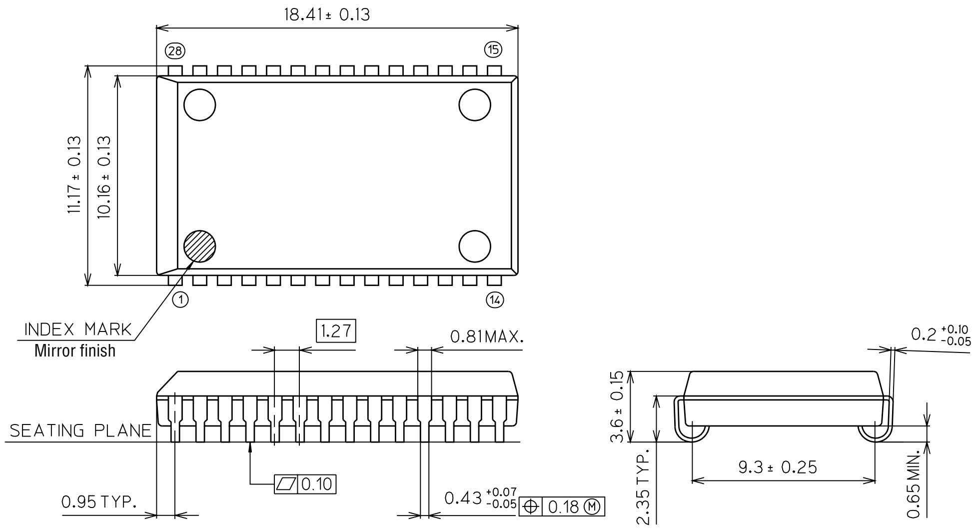
Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Data Retention Power Supply Voltage	V_{CCH}	$\overline{CE} \geq V_{CC} - 0.2$ V	2.0	—	—	V
Data Retention Power Supply Current	I_{CCH}	V_{CC} = 3 V, $\overline{CE} \geq V_{CC} - 0.2$ V	—	—	500	µA
Chip Deselect to Data Retention Time	t_{CDR}	—	0	—	—	ns
Operation Recovery Time	t_R	—	5	—	—	ms



PACKAGE DIMENSIONS

(Unit : mm)

SOJ28-P-400-1.27



Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating
Solder plate thickness	5 µm or more
Package weight (g)	1.30 TYP.

Notes for Mounting the Surface Mount Type Package

The SOP, QFP, TSOP, SOJ, QFJ (PLCC), SHP and BGA are surface mount type packages, which are very susceptible to heat in reflow mounting and humidity absorbed in storage.
Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).