PDSP16330/A/B

PYTHAGORAS PROCESSOR

(Supersedes version in December 1993 Digital Video & Digital Signal Processing IC Handbook, HB3923-1)

The PDSP16330 is a high speed digital CMOS IC that converts Cartesian data (Real and Imaginary) into Polar form (Magnitude and Phase), at rates up to 20MHz. Cartesian 16+16 bit 2's complement or Sign-Magnitude data is converted into 16 bit Phase format. The Magnitude output may be scaled in amplitude by powers of 2. The Phase output represents a full 2 x π field to eliminate phase ambiguities.

Polyimide is used as an inter-layer dielectric and as glassivation.

The PDSP16330 is offered in three speed grades: a basic 10MHz part (PDSP16330), a 20MHz version (PDSP16330A) and a 25MHz version (PDSP16330). A MIL-STD-883 version is also detailed in a separate datasheet.

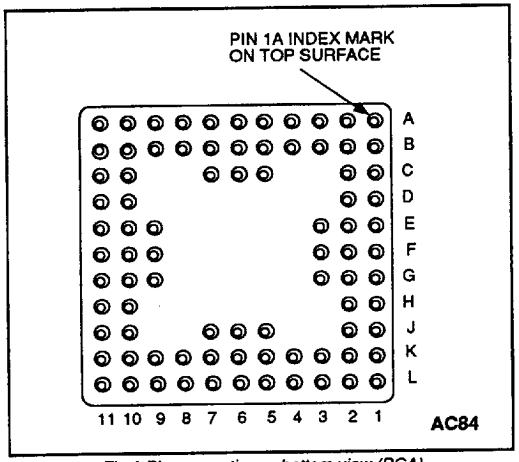

Fig.1 Pin connections - bottom view (PGA)

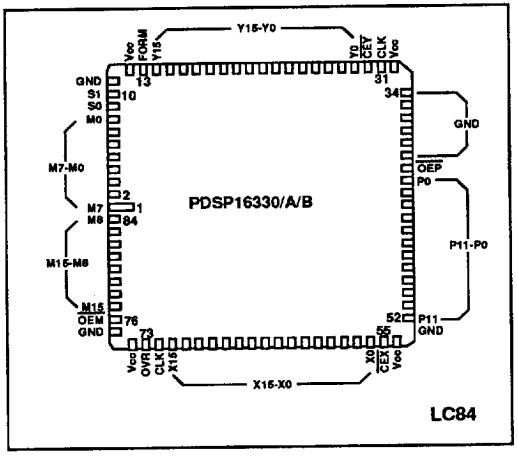

Fig.2 Pin connections - LCC Package

FEATURES

- 25MHz Cartesian to Polar Conversion
- 16-Bit Cartesian Inputs
- 16-Bit Magnitude Output
- 12-Bit Phase Output
- 2's Complement or Sign-Magnitude Input Formats
- Three-state Outputs and Independent Data Enables Simplify System Interfacing
- Magnitude Scaling Facility with Overflow Flag
- Less than 400 mW Power Dissipation at 10MHz
- 84-pin PGA or 100 pin QFP Package or 84 LCC

APPLICATIONS

- Digital Signal Processing
- Digital Radio
- Radar Processing
- Sonar Processing
- Robotics

ASSOCIATED PPODUCTS

PDSP16112	16 X 12 Complex Multiplier
PDSP16116	16 X 16 Complex Multiplier
PDSP16318	Complex Accumulator
PDSP16340	Polar to Cartesian Converter
PDSP16350	I/Q Splitter and NCO
PDSP16510A	Stand Alone FFT Processor

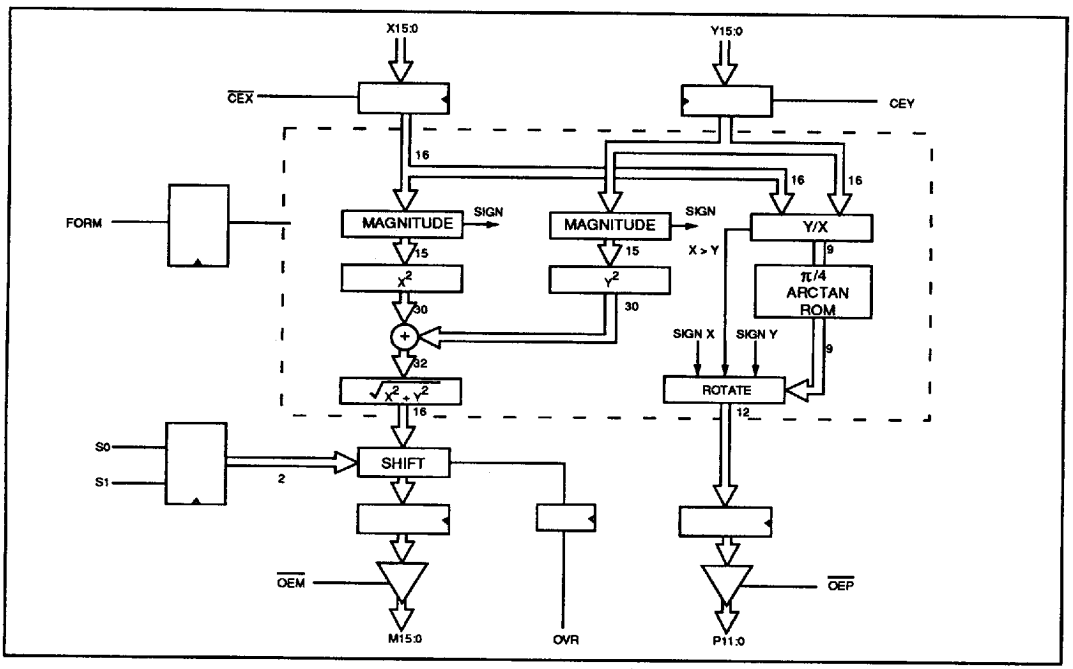

Fig.2 Block diagram

FUNCTIONAL DESCRIPTION

The PDSP16330 converts incoming Cartesian Data into the equivalent Polar Values. The device accepts new 16 + 16 bit complex data every cycle, and delivers a 16 bit + 12 bit Polar equivalent after 24 clock cycles. The input data can be in 2s' Complement or Sign Magnitude format selected via the FORM input. The output is in a magnitude format for both the Magnitude output and the Phase. Phase data is zero for data with a zero Y input and positive X, and is 400 hex for zero X data and positive Y, is 800 hex for zero Y data and negative X, and is C00 hex for zero X and negative Y. The LSB weighting (bit 0) is 2 x π/4096 radians. The 16 bit Magnitude result may be scaled by shifting one, two, or three places in the more significant direction, effectively multiplying the Magnitude result by 2,4 or 8 respectively. Any of these shifts can under certain conditions cause an invalid result to be output from the device. Under these circumstances the OVR output will become active. The PDSP16330 has independent clock enables and three state output controls for all ports.

FORM

This input selects the format of the X and Y input data. A low level on FORM indicates that the Input data is twos' complement format (Note: input data 8000 hex is not valid in 2s' complement mode). This input refers to the format of the current Input data and may be changed on a per cycle basis if desired. The level of FORM is latched at the same time as the data to which it refers.

S1-0

These inputs select the scaling factor to be applied to the Magnitude output. They are latched by the rising edge of CLK and determine the scaling of the output in the cycle after they are loaded into the device. The scale factor applied is determined by the table. Should the scaling factor applied cause an invalid Magnitude result to be output on the M Port, then the OVR Flag will become active for the period that the M Port output is invalid.

S1	S0	Scaling Factor
0	0	x1
0	1	x2
1	0	x4
1	1	x8

The output number range is from 0 to 2 when the scaling factor is set at x1.

PIN DESCRIPTIONS

Symbol	Pin Name and Description
CLK	**Clock:** Common Clock to device Registers. Register contents change on the rising edge of clock. Both pins must be connected.
$\overline{CEX}$	**Clock Enable:** Clock Enable for X Port. The clock to the X port is enabled by a low level.
$\overline{CEY}$	**Clock Enable:** Clock Enable for Y Port The clock to the Y port is enabled by a low level.
X15-X0	**X Data Input** Data presented to this input is loaded into the device by the rising edge of CLK. X15 is the MSB
Y15-Y0	**Y Data Input** Data presented to this input is loaded into the device by the rising edge of CLK. Y15 is the MSB
M15-M0	**M Data Output:** Magnitude data generated by the device is output on this port. Data changes on the rising edge of CLK, M15 is the MSB. The weighting of M15 is determined by the Scale factor selected .
P11-P0	**P Data Output:** Phase data generated by the device is output on this port. Data changes on the rising edge of CLK, P11 is the MSB. The weighting of P11 is π radians.
$\overline{OEM}$	**Output Enable:** Output Enable for M Port. The M Port is in a high impedance state when this input is high.
$\overline{OEP}$	**Output Enable:** Output Enable for P Port. The P Port is in a high impedance state when this input is high.
FORM	**Format Select** This input selects the format of the Cartesian Data input on the X and Y ports. This input is latched by the rising edge of CLK, and is applied at the same time as the data to which it refers. A low level indicates that two's complement data is applied, a high indicates Sign-Magnitude
S1-S0	**Scaling Control:** Control input for scaling of Magnitude Data. This input is latched by the rising edge of CLK, and determines the scaling to be applied to the Magnitude result. The Scaling is applied to the output data in the cycle following the cycle in which the control was latched.
OVR	**Overflow:** Overflow flag. This signal becomes active if the scaling currently selected causes an invalid value to be presented to the Magnitude output.
Vcc	**+5V supply.** All Vcc pins must be connected.
GND	**0V supply.** All GND pins must be connected.

INPUT DATA RANGE

2's Complement	Sign Magnitude
7FFF	7FFF
.	.
.	.
.	.
0001	0001
0000	0000
FFFF	8000
.	.
.	.
.	.
8001	FFF

PIN FUNCTION

Pin No. AC	GG	LC	Function	Pin No. AC	GG	LC	Function	Pin No. AC	GG	LC	Function
F3	91	1	M7	L9	23	29	YO	A9	59	57	X1
G3	92	2	M6	L10	24	30	$\overline{CEY}$	B8	60	58	X2
G1	93	3	M5	K9	25	31	CLK	A8	61	59	X3
G2	94	4	M4	L11	26	32	Vcc	B6	62	60	X4
F1	95	5	M3	K10	31	33	GND	B7	63	61	X5
H1	96	6	M2	J10	32	34	GND	A7	64	62	X6
H2	97	7	M1	K11	33	35	GND	C7	65	63	X7
J1	98	8	M0	J11	34	36	GND	C6	66	64	X8
K1	99	9	S0	H10	35	37	GND	A6	67	65	X9
J2	100	10	S1	H11	36	38	GND	A5	68	66	X10
L1	1	11	GND	F10	37	39	GND	B5	69	67	X11
K2	6	12	Vcc	G10	38	40	$\overline{OEP}$	C5	70	68	X12
K3	7	13	FORM	G11	39	41	P0	A4	71	69	X13
L2	8	14	Y15	G9	40	42	P1	B4	72	70	X14
L3	9	15	Y14	F9	41	43	P2	A3	73	71	X15
K4	10	16	Y13	F11	42	44	P3	A2	74	72	CLK
L4	11	17	Y12	E11	43	45	P4	B3	75	73	OVR
J5	12	18	Y11	E10	44	46	P5	A1	76	74	Vcc
K5	13	19	Y10	E9	45	47	P6	B2	81	75	GND
L5	14	20	Y9	D11	46	48	P7	C2	82	76	$\overline{OEM}$
K6	15	21	Y8	D10	47	49	P8	B1	83	77	M15
J6	16	22	Y7	C11	48	50	P9	C1	84	78	M14
J7	17	23	Y6	B11	49	51	P10	D2	85	79	M13
L7	18	24	Y5	C10	50	52	P11	D1	86	80	M12
K7	19	25	Y4	A11	51	53	GND	E3	87	81	M11
L6	20	26	Y3	B10	52	54	Vcc	E2	88	82	M10
L8	21	27	Y2	B9	57	55	$\overline{CEX}$	E1	89	83	M9
K8	22	28	Y1	A10	58	56	X0	F2	90	84	M8

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated): T_{amb} (Commercial) = 0°C to + 70°C, T_{amb} (Industrial) = -40°C to + 85°C
V_{cc} (Commercial) = 5.0V ± 5%, V_{cc} (Industrial and Military) = 5.0V ± 1%, GND = 0V

STATIC CHARACTERISTICS

Characteristic	Symbol	Value			Units	Sub-group	Conditions
		Min.	Typ.	Max.			
* Output high voltage	V_{OH}	2.4			V	1,2,3	IOH = 3.2mA
* Output low voltage	V_{OL}			0.6	V	1,2,3	IOL=-3.2mA
* Input high voltage (CMOS)	V_{IH}	3.0			V	1,2,3	Inputs $\overline{CEX}$, $\overline{CEY}$ and CLK only
* Input low voltage (CMOS)	V_{IL}			1.0	V	1,2,3	Inputs $\overline{CEX}$, $\overline{CEY}$ and CLK only
* Input high voltage (TTL)	V_{IH}	2.2			V	1,2,3	All other inputs
* Input low voltage (TTL)	V_{IL}			0.8	V	1,2,3	All other inputs
* Input leakage current (Note 1)	I_{IL}	-10		+ 120	µA	1,2,3	GND ≤ V_{IN} ≤ V_{CC}
† Input capacitance	C_{IN}		10		pF		
* Output leakage current	I_{oz}	-50		+ 50	µA	1,2,3	GND ≤ V_{IN} ≤ V_{cc}
† Output SC current	I_{os}	-50		230	mA		V_{cc} = Max

NOTES
1. All inputs except clock inputs have high value pull-down resistors
2. All parameters marked * are tested during production. Parameters marked † are guaranteed by design and characterisation.

SWITCHING CHARACTERISTICS

	Characteristic	Value						Units	Conditions
		PDSP16330		PDSP16330A		PDSP16330B			
		Min.	Max.	Min.	Max.	Min.	Max.		
†	Input data setup to clock rising edge	15		12		12		ns	
†	Input data Hold after clock rising edge	2		2		2		ns	
†	$\overline{CEX}$, $\overline{CEY}$ Setup to clock rising edge	30		12		12		ns	
†	$\overline{CEX}$, $\overline{CEY}$ Hold aher clock rising edge	0		0		0		ns	
†	FORM, S1:0 Setup to clock rising edge	15		12		12		ns	
†	FORM, S1:0 Hold after clock rising edge	7		2		2		ns	
†	Clock rising edge to valid data	5	40	5	25	5	25	ns	2 x LSTTL + 20pF
*	Clock period	100		50		40		ns	
†	Clock high time	25		15		15		ns	
†	Clock low time	25		15		15		ns	
†	Latency	24	24	24	24	24	24	cycles	
†	$\overline{OEM}$, $\overline{OEP}$ low to data high data valid		30		25	25		ns	2 x LSTTL + 20pF
†	$\overline{OEM}$, $\overline{OEP}$ low to data low data valid		30		25	25		ns	2 x LSTTL + 20pF
†	$\overline{OEM}$, $\overline{OEP}$ high to data high impedance		30		25	25		ns	2 x LSTTL + 20pF
†	$\overline{OEM}$, $\overline{OEP}$ low to data high impedance		30		25	25		ns	2 x LSTTL + 20pF
†	Vcc current (TTL input levels)		110		180	225		mA	V_{CC} = Max Outputs unloaded Clock freq. = Max
†	Vcc current (CMOS input levels)		70		120	150		mA	V_{CC} = Max Outputs unloaded Clock freq. = Max

NOTES
1. LSTTL is equivalent to I_{OH} = 20µA, I_{OL} = -0.4mA
2. Current is defined as negative into the device
3. CMOS input levels are defined as: $V_{IH} = V_{DD}$ - 0.5V, V_{IL} = +0.5V
4. All parameters marked * are tested during production.
   Parameters marked † are guaranteed by design and characterisation.
5. All timings are dependent on silicon speed. This speed is tested by measuring clock period.
   This guarantees all other timings by characterisation and design.

ABSOLUTE MAXIMUM RATINGS

Supply voltage, V_{CC}	-0.5V to + 7.0V
Input voltage, V_{IN}	-0.5V to VCC + 0.5V
Output voltage, V_{OUT}	-0.5V to VCC + 0.5V
Clamp diode current per pin, I_K (see Note 2)	±18mA
Static discharge voltage (HMB), V_{STAT}	500V
Storage temperature. T_{stg}	-65°C to + 150°C
Ambient temperature with power applied T_{amb}:	
Commercial	0°C to + 70°C
Industrial	-40°C to + 85°C
Military	-55 °C to + 125°C
Package power dissipation P_{TOT}	1200mW
Junction temperature	150°C

THERMAL CHARACTERISTICS

Package Type	θ_{JC}°C/W	θ_{JA}°C/W
AC	12	36
LC	12	35

NOTES
1. Exceeding these ratings may cause permanent damage. Functional operation under these conditions is not implied.
2. Maximum dissipation or 1 second should not be exceeded; only one output to be tested at any one time.
3. Exposure to Absoulte Maximum Ratings for extended periods may affect device reliability.

ORDERING INFORMATION

Commercial (0°C to +70°C)

PDSP16330	CO LC	(10MHZ - LCC Package)
PDSP16330	CO AC	(10MHZ - PGA Package)
PDSP16330	CO GG	(10MHZ - GG Package)
PDSP16330A	CO LC	(20MHZ - LCC Package)
PDSP16330A	CO AC	(20MHZ - PGA Package)
PDSP16330A	CO GG	(20MHZ - GG Package)
PDSP16330B	CO AC	(25MHZ - PGA Package)

Industrial (-40°C to +85°C)

PDSP16330	BO LC	10MHZ - LCC Package
PDSP16330	BO AC	10MHZ - PGA Package
PDSP16330	BO GG	10MHZ - GG Package
PDSP16330A	BO LC	20MHZ - LCC Package
PDSP16330A	BO AC	20MHZ - PGA Package
PDSP16330A	BO GG	20MHZ - GG Package
PDSP16330B	BO AC	25MHZ - PGA Package

Military (-55°C to +125°C)

PDSP16330	AO LC	10MHZ - LCC Package
PDSP16330	AO AC	10MHZ - PGA Package
PDSP16330	AO GG	10MHZ - GG Package
PDSP16330A	AO LC	20MHZ - LCC Package
PDSP16330A	AO AC	20MHZ - PGA Package
PDSP16330A	AO GG	20MHZ - GG Package

Test	Waveform - measurement level
Delay from ouput high to output high impedance	V_H 0.5V
Delay from ouput low to output high impedance	V_L 0.5V
Delay from ouput high impedance to Output low	1.5V 0.5V
Delay from ouput high impedance to Output high	1.5V 0.5V

NOTES
1. V_H - Voltage reached when output driven high
2. V_L - Voltage reached when output driven low

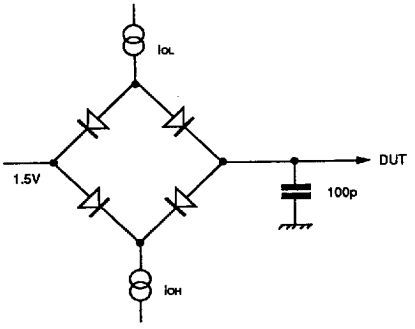

Fig.3 Three state delay measurement load