FEATURES

- Low Resistance Pass Transistor: 0.25Ω
- Dropout Voltage: 0.75V at 3A
- ±1% Reference Voltage
- **Accurate** Programmable Current Limit
- Shutdown Capability
- Internal Reference Available
- Standard 5-Lead Packages
- Full Remote Sense
- Low Quiescent Current: ≈2.5mA
- Good High Frequency Ripple Rejection

DESCRIPTION

The LT1185 is a 3A low dropout regulator with adjustable current limit and remote sense capability. It can be used as a positive output regulator with floating input or as a standard negative regulator with grounded input. The output voltage range is 2.5V to 25V, with ±1% accuracy on the internal reference voltage.

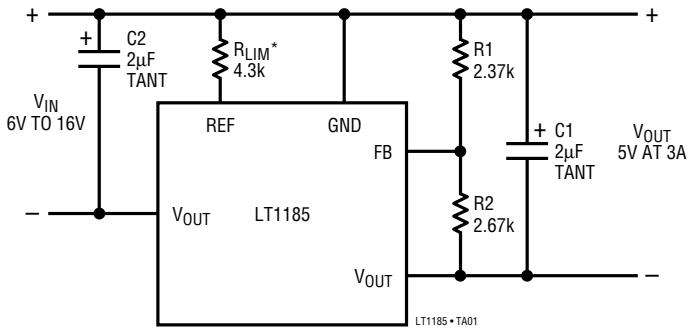
The LT1185 uses a saturation-limited NPN transistor as the pass element. This device gives the linear dropout characteristics of an FET pass element with significantly less die area. High efficiency is maintained by using special anti-saturation circuitry that adjusts base drive to track load current. The "on resistance" is typically 0.25Ω.

Accurate current limit is programmed with a single 1/8W external resistor, with a range of zero to three amperes. A second, fixed internal limit circuit prevents destructive currents if the programming current is accidentally over-ranged. Shutdown of the regulator output is guaranteed when the program current is less than 1μA, allowing external logic control of output voltage.

The LT1185 has all the protection features of previous LTC regulators, including power limiting and thermal shutdown. The 4-lead TO-3 package is specified for –55°C to 150°C operation and the 5-lead TO-220 is specified over 0°C to 125°C.

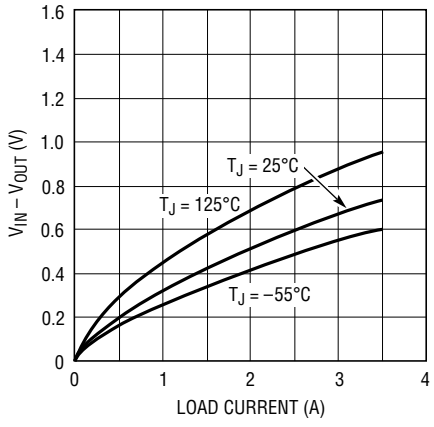
TYPICAL APPLICATION

5V, 3A Regulator with 3.5A Current Limit



*CURRENT LIMIT = 15k/R_{LIM} = 3.5A

Dropout Voltage

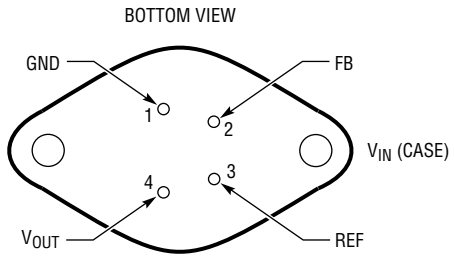


ABSOLUTE MAXIMUM RATINGS

Input Voltage 35V
Input-Output Differential 30V
FB Voltage 7V
REF Voltage 7V
Output Voltage 30V
Output Reverse Voltage 2V
Operating Ambient Temperature Range
  LT1185C ..... 0°C to 70°C
  LT1185M ..... –55°C to 125°C
Operating Junction Temperature Range*
Control Section
  LT1185C ..... 0°C to 125°C
  LT1185I ..... –40°C to 125°C
  LT1185M ..... –55°C to 150°C
Power Transistor Section
  LT1185C ..... 0°C to 150°C
  LT1185I ..... –40°C to 150°C
  LT1185M ..... –55°C to 175°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec)..... 300°C

*See Application Section for details on calculating Operation Junction Temperature

PACKAGE/ORDER INFORMATION

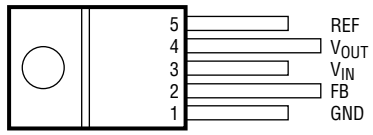


K PACKAGE
4-LEAD TO-3 METAL CAN

$\theta_{JC\ MAX}$ = 2.5°C/W, θ_{JA} = 35°C/W

ORDER PART NUMBER

LT1185MK



T PACKAGE
5-LEAD TO-220

$\theta_{JC\ MAX}$ = 2.5°C/W, θ_{JA} = 50°C/W

ORDER PART NUMBER

LT1185CT
LT1185IT

ELECTRICAL CHARACTERISTICS

Adjustable Version, V_{IN} = 7.4V, V_{OUT} = V_{REF}, I_{OUT} = 1mA, R_{LIM} = 4.02k, unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Reference Voltage (At FB Pin)				2.37		V
Reference Voltage Tolerance (At FB Pin) (Note 1)	$V_{IN} – V_{OUT}$ = 5V			0.3	±1	%
	1mA ≤ I_{OUT} ≤ 3A $V_{IN} – V_{OUT}$ = 1.2V to V_{IN} = 30V P ≤ 25W (Note 5), V_{OUT} = 5V $T_{MIN} ≤ T_J ≤ T_{MAX}$ (Note 8)	●		1	±2.5	%
Feedback Pin Bias Current		●		0.7	2	µA
Droput Voltage (Note 2)	I_{OUT} = 0.5A, V_{OUT} = 5V I_{OUT} = 3A, V_{OUT} = 5V			0.20 0.67	0.37 1.00	V V
Load Regulation (Note 6)	I_{OUT} = 5mA to 3A $V_{IN} – V_{OUT}$ = 1.5V to 10V, V_{OUT} = 5V			0.05	0.3	%
Line Regulation (Note 6)	$V_{IN} – V_{OUT}$ = 1V to 20V, V_{OUT} = 5V			0.002	0.01	%/V
Minimum Input Voltage	I_{OUT} = 1A (Note 3) I_{OUT} = 3A			4.0 4.3		V V
Internal Current Limit (See Graph for Guaranteed Curve) (Note 11)	1.5V ≤ $V_{IN} – V_{OUT}$ ≤ 10V		3.3	3.6	4.0	A
		●	3.1		4.2	A
	$V_{IN} – V_{OUT}$ = 15V	●	2.0	3.0	4.0	A
	$V_{IN} – V_{OUT}$ = 20V	●	1.0	1.7	2.6	A
	$V_{IN} – V_{OUT}$ = 30V	●	0.2	0.4	1.0	A

ELECTRICAL CHARACTERISTICS

Adjustable Version, V_{IN} = 7.4V, V_{OUT} = V_{REF}, I_{OUT} = 1mA, R_{LIM} = 4.02k, unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
External Current Limit Programming Constant	$5k \le R_{LIM} \le 15k$, V_{OUT} = 1V (Note 10)	●		15k		A•Ω
External Current Limit Error	$1A \le I_{LIM} \le 3A$			0.02 I_{LIM}	0.06 I_{LIM} + 0.03	A
	$R_{LIM} = 15k \times A/I_{LIM}$	●		0.04 I_{LIM}	0.09 I_{LIM} + 0.05	A
Quiescent Supply Current	I_{OUT} = 5mV $4V \le V_{IN} \le 25V$ (Note 4)	●		2.5	3.5	mA
Supply Current Change with Load	$V_{IN} - V_{OUT} = V_{SAT}$ (Note 9)	●		25	40	mA/A
	$V_{IN} - V_{OUT} \ge 2V$	●		10	25	mA/A
REF Pin Shutoff Current		●	0.4	2	7	µA
Thermal Regulation (See Applications Information)	$V_{IN} - V_{OUT}$ = 10V I_{OUT} = 5mA to 2A			0.005	0.014	%/W
Reference Voltage Temperature Coefficient	(Note 7)			0.003	0.01	%/°C
Thermal Resistance Junction to Case	TO-3 Control Area				1	°C/W
	Power Transistor				3	°C/W
	TO-220 Control Area				1	°C/W
	Power Transistor				3	°C/W

The ● denotes specifications which apply over the full operating temperature range.

Note 1: Reference voltage is guaranteed both at nominal conditions (no load, 25°C) and at worst case conditions of load, line, power and temperature. An intermediate value can be calculated by adding the effects of these variables in the actual application. See the Applications Information section of this data sheet.

Note 2: Dropout voltage is tested by reducing input voltage until the output drops 1% below its nominal value. Tests are done at 0.5A and 3A. The power transistor looks basically like a pure resistance in this range so that minimum differential at any intermediate current can be calculated by interpolation; $V_{DROPOUT} = 0.25V + 0.25\Omega \times I_{OUT}$. For load current less than 0.5A, see graph.

Note 3: "Minimum input voltage" is limited by base emitter voltage drive of the power transistor section, not saturation as measured in Note 2. For output voltages below 4V, "minimum input voltage" specification may limit dropout voltage before transistor saturation limitation.

Note 4: Supply current is measured on the ground pin, and does not include load current, R_{LIM}, or output divider current.

Note 5: The 25W power level is guaranteed for an input-output voltage of 8.3V to 17V. At lower voltages the 3A limit applies, and at higher voltages the internal power limiting may restrict regulator power below 25W. See graphs.

Note 6: Line and load regulation are measured on a pulse basis with a pulse width of ≈2ms, to minimize heating. DC regulation will be affected by thermal regulation and temperature coefficient of the reference. See Application Section for details.

Note 7: Guaranteed by design and correlation to other tests, but not tested.

Note 8: T_{JMIN} = 0°C for the LT1185C, –40°C for LT1185I, and –55°C for the LT1185M. Power transistor area and control circuit area have different maximum junction temperatures. Control area limits are T_{JMAX} = 125°C for the LT1185C and LT1185I and 150°C for the LT1185M. Power area limits are 150°C for LT1185C and LT1185I and 175°C for LT1185M.

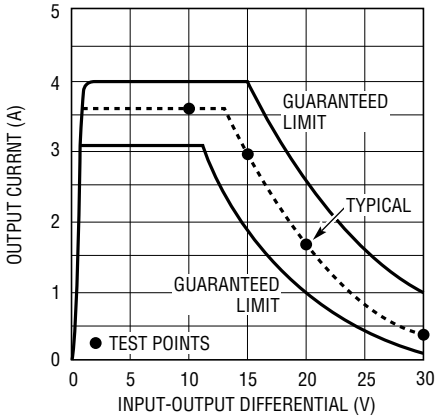
Note 9: V_{SAT} is the maximum specified dropout voltage; $0.25V + 0.25 \times I_{OUT}$.

Note 10: Current limit is programmed with a resistor from REF pin to GND pin. The value is $15k/I_{LIM}$.

Note 11: For $V_{IN} - V_{OUT}$ = 1.5V; V_{IN} = 5V, V_{OUT} = 3.5V. V_{OUT} = 1V for all other current limit tests.

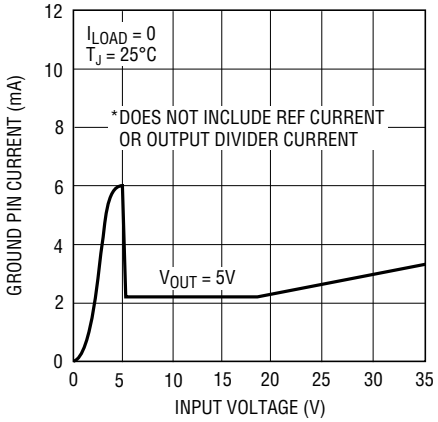
TYPICAL PERFORMANCE CHARACTERISTICS

Internal Current Limit



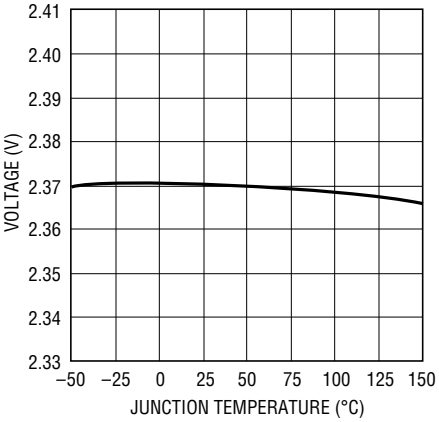
LT1185 • TPC01

Quiescent Ground Pin Current*



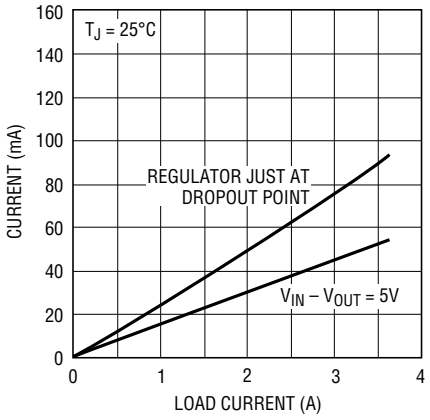
LT1185 • TPC02

Feedback Pin Voltage Temperature Drift



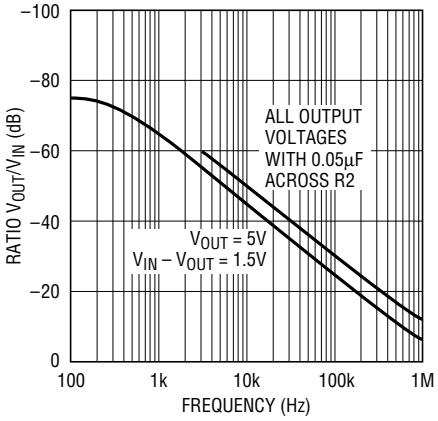
LT1185 • TPC03

Ground Pin Current



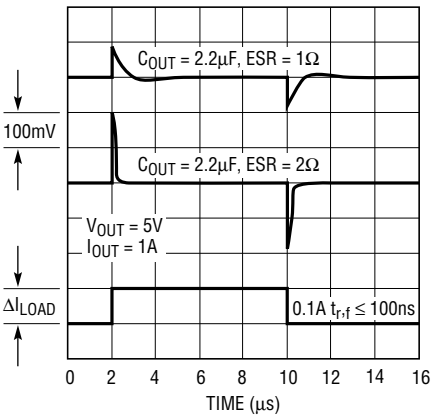
LT1185 • TPC04

Ripple Rejection vs Frequency



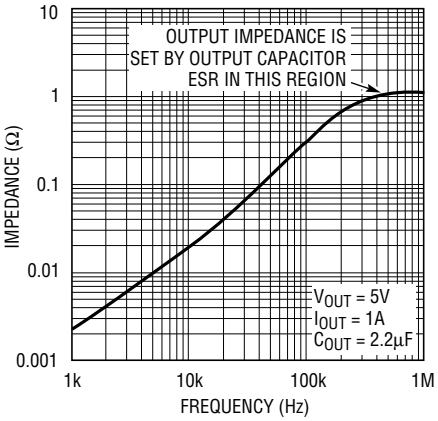
LT1185 • TPC05

Load Transient Response



LT1185 • TPC06

Output Impedance



LT1183 • TPC07

APPLICATIONS INFORMATION

Block Diagram

A simplified block diagram of the LT1185 is shown in Figure 1. A 2.37V bandgap reference is used to bias the input of the error amplifier A1, and the reference amplifier A2. A1 feeds a triple NPN pass transistor stage which has the two driver collectors tied to ground so that the main pass transistor can completely saturate. This topology normally has a problem with unlimited current in Q1 and Q2 when the input voltage is less than the minimum required to create a regulated output. The standard "fix" for this problem is to insert a resistor in series with Q1 and Q2 collectors, but this resistor must be low enough in value to supply full base current for Q3 under worst case conditions, resulting in very high supply current when the input voltage is low. To avoid this situation, the LT1185 uses an auxiliary emitter on Q3 to create a drive limiting feedback loop which automatically adjusts the drive to Q1 so that the base drive to Q3 is just enough to saturate Q3, but no more. Under saturation conditions, the auxiliary emitter is acting like a collector to shunt away the output current of A1. When the input voltage is high enough to keep Q3 out of saturation, the auxiliary emitter current drops to zero even when Q3 is conducting full load current.

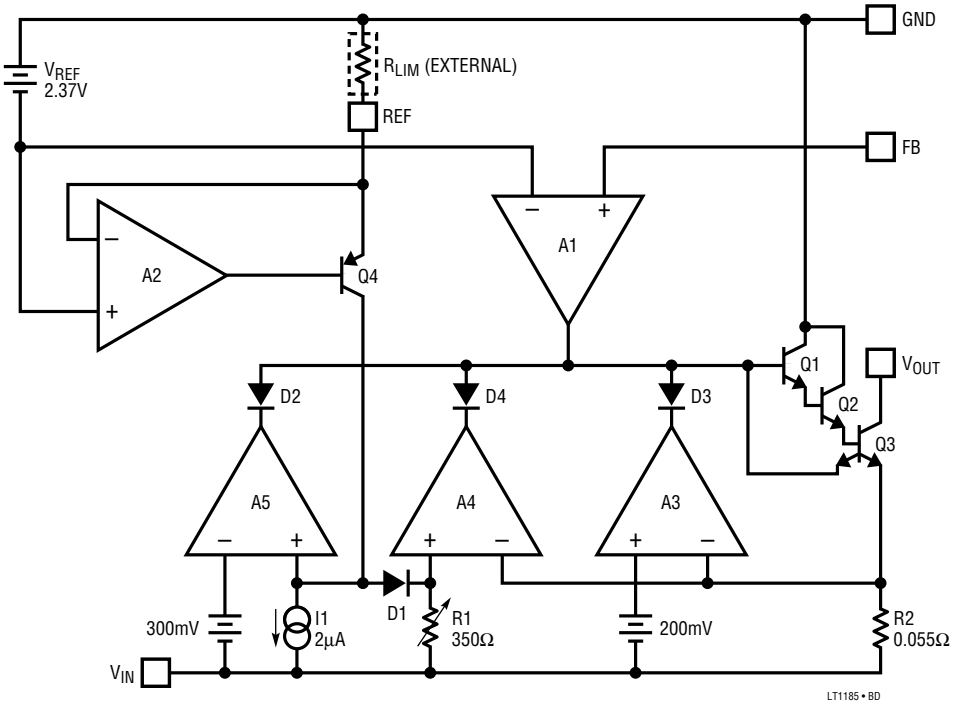


Figure 1. Block Diagram

APPLICATIONS INFORMATION

Amplifier A2 is used to generate an internal current through Q4 when an external resistor is connected from the REF pin to ground. This current is equal to 2.37V divided by R_{LIM}. It generates a current limit sense voltage across R1. The regulator will current limit via A4 when the voltage across R2 is equal to the voltage across R1. These two resistors essentially form a current "amplifier" with a gain of 350/0.055 = 6,360. Good temperature drift is inherent because R1 and R2 are made from the same diffusions. Their ratio, not absolute value, determines current limit. Initial accuracy is enhanced by trimming R1 slightly at wafer level. Current limit is equal to $15k\Omega/R_{LIM}$.

D1 and I1 are used to guarantee regulator shutdown when REF pin current drops below 2μA. A current less than 2μA through Q4 causes the + input of A5 to go low and shut down the regulator via D2.

A3 is an internal current limit amplifier which can override the external current limit. It provides "goof proof" protection for the pass transistor. Although not shown, A3 has a nonlinear foldback characteristic at input-output voltages above 12V to guarantee safe area protection for Q3. See the graph, Internal Current Limit in the Typical Performance Characteristics of this data sheet.

Setting Output Voltage

The LT1185 output voltage is set by two external resistors (see Figure 2). Internal reference voltage is trimmed to 2.37V so that a standard 1% 2.37k resistor (R1) can be used to set divider current at 1mA. R2 is then selected from:

$$R2 = \frac{(V_{OUT} - 2.37)\ R1}{V_{REF}}$$

for R1 = 2.37k and V_{REF} = 2.37V, this reduces to:

$$R2 = V_{OUT} - 2.37k$$

suggested values of 1% resistors are shown.

V_{OUT}	R2 WHEN R1 = 2.37k
5V	2.67k
5.2V	2.87k
6V	3.65k
12V	9.76k
15V	12.7k

Output Capacitor

The LT1185 has a collector output NPN pass transistor, which makes the open-loop output impedance much higher than an emitter follower. Open-loop gain is a direct function of load impedance, and causes a main-loop "pole" to be created by the output capacitor, in addition to an internal pole in the error amplifier. To ensure loop stability, the output capacitor must have an ESR (effective series resistance) which has an upper limit of 2Ω, and a lower limit of 0.2 divided by the capacitance in μF. A 2μF output capacitor, for instance, should have a maximum ESR of 2Ω, and a minimum of 0.2/2 = 0.1Ω. These values are easily encompassed by standard solid tantalum capacitors, but occasionally a solid tantalum unit will have abnormally high ESR, especially at very low temperatures. The suggested 2μF value shown in the circuit applications should be increased to 4.7μF for –40°C and –55°C designs if the 2μF units cannot be guaranteed to stay below 2Ω at these temperatures.

Although solid tantalum capacitors are suggested, other types can be used if they meet the ESR requirements. Standard aluminum electrolytic capacitors need to be upward of 25μF in general to hold 2Ω maximum ESR, especially at low temperatures. Ceramic, plastic film, and monolithic capacitors have a problem with ESR being too *low*. These types should have a 1Ω carbon resistor in series to guarantee loop stability.

The output capacitor should be located close to the regulator (≤3") to avoid excessive impedance due to lead inductance. A six inch lead length (2 × 3") will generate an extra 0.8Ω inductive reactance at 1MHz, and unity-gain frequency can be up to that value.

For remote sense applications, the capacitor should still be located close to the regulator. Additional capacitance can be added at the remote sense point, but the remote capacitor must be at least 2μF solid tantalum. It cannot be a low ESR type like ceramic or mylar unless a 0.5Ω to 1Ω carbon resistor is added in series with the capacitor. Logic boards with multiple low ESR bypass capacitors should have a solid tantalum unit added in parallel whose value is approximately five times the combined value of low ESR capacitors.

APPLICATIONS INFORMATION

Large output capacitors (electrolytic or solid tantalum) will not cause the LT1185 to oscillate, but they will cause a damped "ringing" at light load currents where the ESR of the capacitor is several orders of magnitude lower than the load resistance. This ringing only occurs as a result of transient load or line conditions and normally causes no problems because of its low amplitude (≤25mV).

Heat Sinking

The LT1185 will normally be used with a heat sink. The size of the heat sink is determined by load current, input and output voltage, ambient temperature, and the thermal resistance of the regulator, junction-to-case (θ_{JC}). The LT1185 has two separate values for θ_{JC}: one for the power transistor section, and a second, lower value for the control section. The reason for two values is that the power transistor is capable of operating at higher continuous temperature than the control circuitry. At low power levels, the two areas are at nearly the same temperature, and maximum temperature is limited by the control area. At high power levels, the power transistor will be at a significantly higher temperature than the control area and its maximum operating temperature will be the limiting factor.

To calculate heat sink requirements, you must solve a thermal resistance formula twice, one for the power transistor and one for the control area. The *lowest* value obtained for heat sink thermal resistance must be used. In these equations, two values for maximum junction temperature and junction-to-case thermal resistance are used, as given in Electrical Specifications.

$$\theta_{HS} = \frac{(T_{JMAX} - T_{AMAX})}{P} - \theta_{JC} - \theta_{CHS}.$$

θ_{HS} = Maximum heat sink thermal resistance.

θ_{JC} = LT1185 junction-to-case thermal resistance.

θ_{CHS} = Case-to-heat sink (interface) thermal resistance, including any insulating washers.

T_{JMAX} = LT1185 maximum operating junction temperature.

T_{AMAX} = Maximum ambient temperature in customers application.

$$P = \text{Device dissipaton} = (V_{IN} - V_{OUT})(I_{OUT}) + \frac{I_{OUT}}{40}(V_{IN}).$$

Example: A commercial version of the LT1185 in the TO-220 package is to be used with a maximum ambient temperature of 60°C. Output voltage is 5V at 2A. Input voltage can vary from 6V to 10V. Assume an interface resistance of 1°C/W.

First solve for control area, where the maximum junction temperature is 125°C for the TO-220 package, and θ_{JC} = 1°C/W:

$$P = (10V - 5V)(2A) + \frac{2A}{40}(10V) = 10.5W$$

$$\theta_{HS} = \frac{125°C - 60°C}{10.5W} - 1°C/W - 1°C/W = 4.2°C/W$$

Next, solve for power transistor limitation, with T_{JMAX} = 150°C, θ_{JC} = 3°C/W:

$$\theta_{HS} = \frac{150 - 60}{10.5} - 3 - 1 = 4.6°C/W$$

The lowest number must be used, so heat sink resistance must be less than 4.2°C/W.

Some heat sink data sheets show graphs of heat sink temperature rise vs power dissipation instead of listing a value for thermal resistance. The formula for θ_{HS} can be rearranged to solve for maximum heat sink temperature rise:

$$\Delta T_{HS} = T_{JMAX} - T_{AMAX} - P(\theta_{JC} + \theta_{CHS})$$

Using numbers from the previous example:

ΔT_{HS} = 125°C – 60 – 10.5(1 + 1) = 44°C control section

ΔT_{HS} = 150°C – 60 – 10.5(3 + 1) = 48°C power transistor

The smallest rise must be used, so heat sink temperature rise must be less than 44°C at a power level of 10.5W.

For board level applications, where heat sink size may be critical, one is often tempted to use a heat sink which barely meets the requirements. This is permissible *if* correct assumptions were made concerning maximum ambient temperature and power levels. One complicating

APPLICATIONS INFORMATION

factor is that local ambient temperature may be somewhat higher because of the point source of heat. The consequences of excess junction temperature include poor reliability, especially for plastic packages, and the possibility of thermal shutdown or degraded electrical characteristics. The final design should be checked *in situ* with a thermocouple attached to the regulator case under worst case conditions of high ambient, high input voltage, and full load.

What About Overloads?

IC regulators with thermal shutdown, like the LT1185, allow heat sink designs which concentrate on worst case "normal" conditions and ignore "fault" conditions. An output overload or short may force the regulator to exceed its maximum junction temperature rating, but thermal shutdown is designed to prevent regulator failure under these conditions. A word of caution however; thermal shutdown temperatures are typically 175°C in the control portion of the die and 180°C to 225°C in the power transistor section. Extended operation at these temperatures can cause permanent degradation of plastic encapsulation. Designs which may be subjected to extended periods of overload should either use the hermetic TO-3 package or increase heat sink size. Foldback current limiting can be implemented to minimize power levels under fault conditions.

External Current Limit

The LT1185 requires a resistor to set current limit. The value of this resistor is 15k divided by the desired current limit (in amps). The resistor for 2A current limit would be 15k/2A = 7.5k. Tolerance over temperature is ±10%, so current limit is normally set 15% above maximum load current. Foldback limiting can be employed if short-circuit current must be lower than full load current (see Typical Applications).

The LT1185 has internal current limiting which will override external current limit if power in the pass transistor is excessive. The internal limit is ≈3.6A with a foldback characteristic which is dependent on input-output voltage, not output voltage *per se* (see Typical Performace Characteristics).

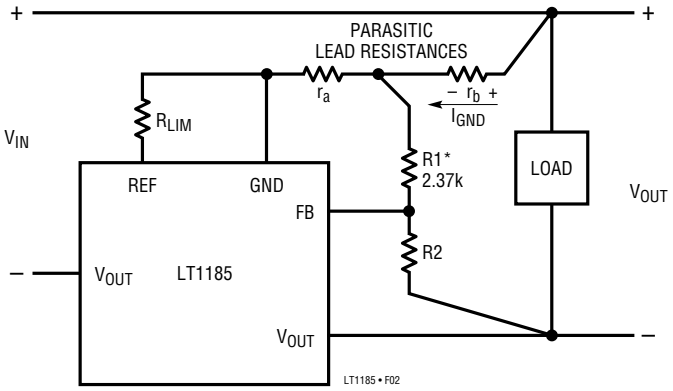
Ground Pin Current

Ground pin current for the LT1185 is approximately 2mA plus $I_{OUT}/40$. At I_{OUT} = 3A, ground pin current is typically 2mA + 3/40 = 77mA. Worst case guarantees on the ratio of I_{OUT} to ground pin current are contained in the Electrical Specifications.

Ground pin current can be important for two reasons. It adds to power dissipation in the regulator and it can affect load/line regulation if a long line is run from the ground pin to load ground. The additional power dissipation is found by multiplying ground pin current by input voltage. In a typical example, with V_{IN} = 8V, V_{OUT} = 5V and I_{OUT} = 2A, the LT1185 will dissipate (8V – 5V)(2A) = 6W in the pass transistor and (2A/40)(8V) = 0.4W in the internal drive circuitry. This is only a 1.5% efficiency loss, and a 6.7% increase in regulator power dissipation, but these values will increase at higher output voltages.

Ground pin current can affect regulation as shown in Figure 2. Parasitic resistance in the ground pin lead will create a voltage drop which *increases* output voltage as load current is increased. Similarly, output voltage can *decrease* as input voltage increases because the "$I_{OUT}/40$" component of ground pin current drops significantly at higher input-output differentials. These effects are small enough to be ignored for local regulation applications, but for remote sense applications, they may need to be considered. Ground lead resistance of 0.4Ω would cause an output voltage error of up to (3A/40)(0.4Ω) = 30mV, or 0.6% at V_{OUT} = 5V. Note that if the sense leads are connected as shown in Figure 2, with $r_a \approx 0\Omega$, this error is a fixed number of millivolts, and does not increase as a function of DC output voltage.

APPLICATIO NS I NFOR MATIO N



*R1 SHOULD BE CONNECTED DIRECTLY TO GROUND LEAD, NOT TO THE LOAD, SO THAT $r_a \approx 0\Omega$. THIS LIMITS THE OUTPUT VOLTAGE ERROR TO $(I_{GND})(r_b)$. ERRORS CREATED BY r_a ARE MULTIPLIED BY (1 + R2/R1). NOTE THAT V_{OUT} *INCREASES* WITH INCREASING GROUND PIN CURRENT. R2 SHOULD BE CONNECTED DIRECTLY TO LOAD FOR REMOTE SENSING.

Figure 2. Proper Connection of Positive Sense Lead

Shutdown Techniques

The LT1185 can be shut down by open-circuiting the REF pin. The current flowing into this pin must be less than 0.4µA to guarantee shutdown. Figure 3 details several ways to create the "open" condition, with various logic levels. For variations on these schemes, simply remember that the voltage on the REF pin is 2.4V negative with respect to the ground pin.

Output Overshoot

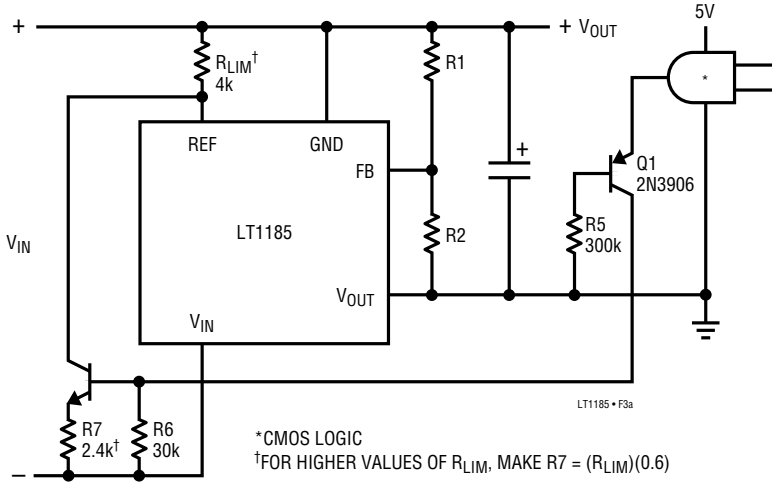
Very high input voltage slew rate during start-up may cause the LT1185 output to overshoot. Up to 20% overshoot could occur with input voltage ramp-up rate exceeding 1V/µs. This condition cannot occur with normal 50Hz to 400Hz rectified AC inputs because parasitic resistance and inductance will limit rate of rise even if the power switch is closed at the peak of the AC line voltage. This assumes that the switch is in the AC portion of the circuit.

If instead, a switch is placed directly in the regulator input so that a large filter capacitor is precharged, fast input slew rates will occur on switch closure. The output of the regulator will slew at a rate set by current limit and output capacitor size; $dVdt = I_{LIM}/C_{OUT}$. With $I_{LIM} = 3.6A$ and $C_{OUT} = 2.2\mu F$, the output will slew at 1.6V/µs and overshoot can occur. This overshoot can be reduced to a few hundred millivolts or less by increasing the output capacitor to 10µF and/or reducing current limit so that output slew rate is held below 0.5V/µs.

A second possibility for creating output overshoot is recovery from an output short. Again, the output slews at a rate set by current limit and output capacitance. To avoid overshoot, the ratio I_{LIM}/C_{OUT} should be less than 0.5×10^6. Remember that load capacitance can be added to C_{OUT} for this calculation. Many loads will have multiple supply bypass capacitors that total more than C_{OUT}.

APPLICATIO NS I NFOR MATIO N

5V Logic, Positive Regulated Output



5V Logic, Negative Regulated Output

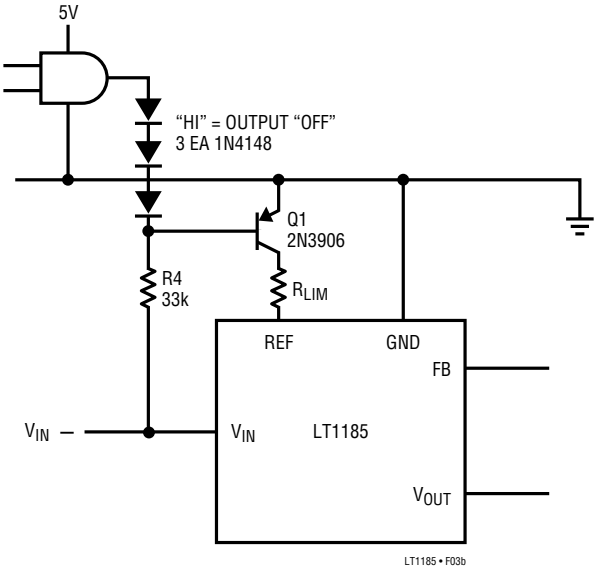


Figure 3. Shutdown Techniques

APPLICATIONS INFORMATION

Thermal Regulation

IC regulators have a regulation term not found in discrete designs because the power transistor is thermally coupled to the reference. This creates a shift in the output voltage which is proportional to power dissipation in the regulator.

$$\Delta V_{OUT} = P(K1 + K2\ \theta_{JA})$$
$$= (I_{OUT})(V_{IN} - V_{OUT})(K1 + K2\ \theta_{JA})$$

K1 and K2 are constants. K1 is a fast time constant effect caused by die temperature *gradients* which are established within 50ms of a power change. K1 is specified on the data sheet as thermal regulation, in percent per watt.

K2 is a long time constant term caused by the temperature drift of the regulator reference voltage. It is also specified, but in percent per degree centigrade. It must be multiplied by overall thermal resistance, junction-to-ambient, θ_{JA}.

As an example, assume a 5V regulator with an input voltage of 8V, load current of 2A, and a total thermal resistance of 4°C/W, including junction-to-case, (use control area specification), interface, and heat sink resistance. K1 and K2, respectively, from the data sheet are 0.014%/W and 0.01%/°C.

$$\Delta V_{OUT} = (2A)(8V - 5V)(0.014 + 0.01 \times 4)$$
$$= 0.32\%$$

This shift in output voltage could be in either direction because K1 and K2 can be either positive or negative.

Thermal regulation is already included in the worst case reference specification.

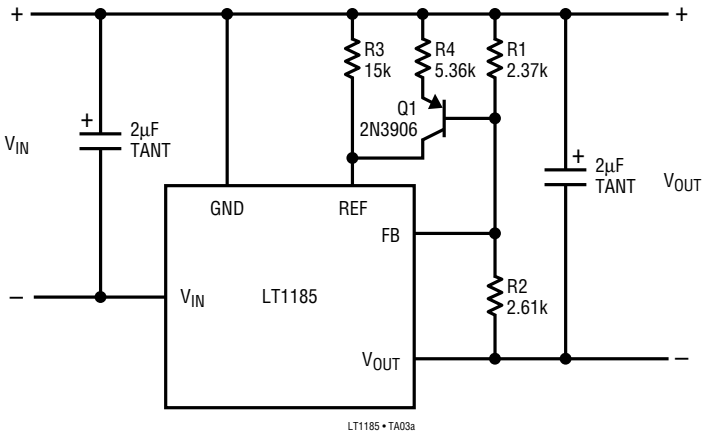
Output Voltage Reversal

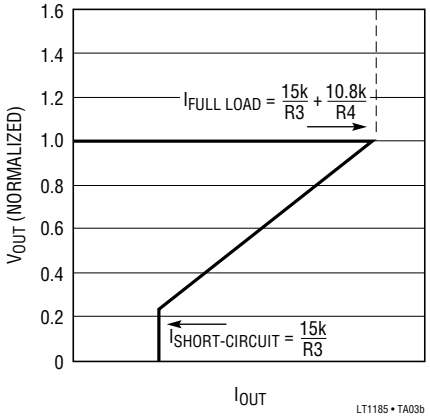
Some IC regulators suffer from a latch-up state when their output is forced to a reverse voltage of as little as one diode drop. The latch-up state can be triggered without a fault condition when the load is connected to an opposite polarity supply instead of to ground. If the second supply is turned on first, it will pull the output of the first supply to a reverse voltage through the load. The first supply may then latch off when turned on. This problem is particularly annoying because the diode clamps which should always be used to protect against polarity reversal do not usually stop the latch-up problem.

The LT1185 is designed to allow output reverse polarity of several volts without damage or latch-up, so that a simple diode clamp can be used.

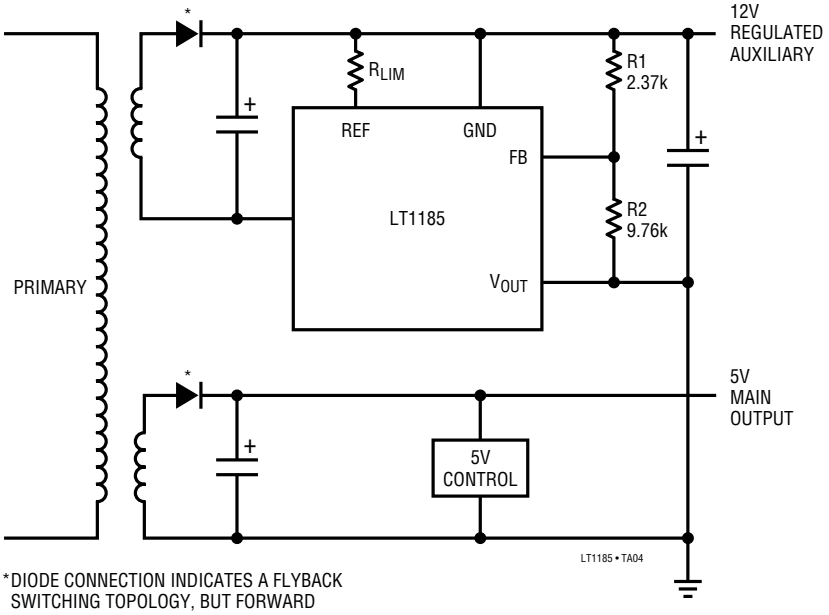
TYPICAL APPLICATIONS

Foldback Current Limiting





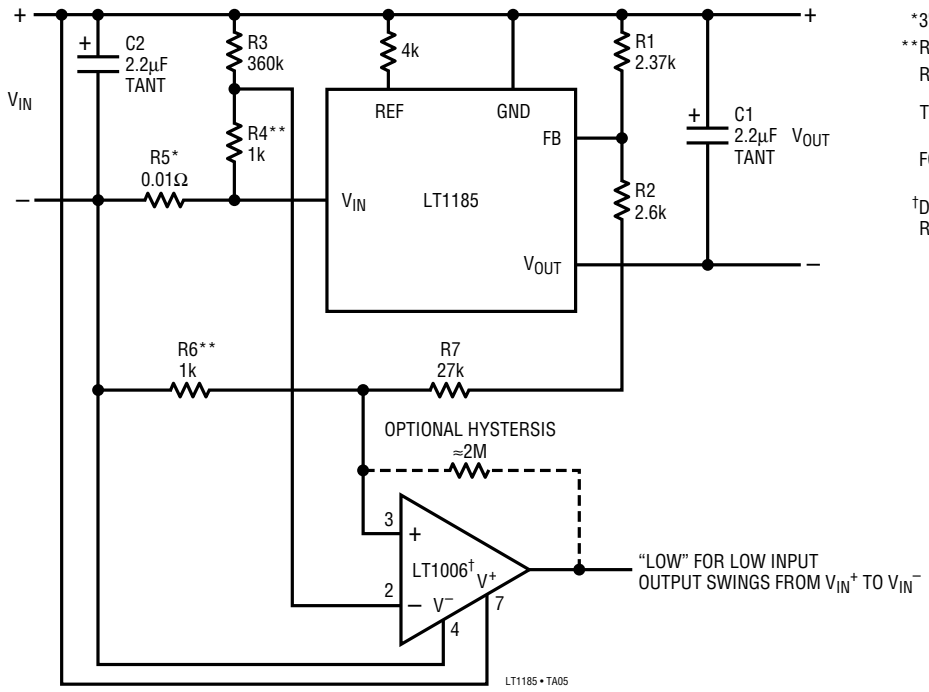
Auxiliary + 12V Low Dropout Regulator for Switching Supply



*DIODE CONNECTION INDICATES A FLYBACK SWITCHING TOPOLOGY, BUT FORWARD CONVERTERS MAY ALSO BE USED.

TYPICAL APPLICATIONS

Low Input Voltage Monitor Tracks Dropout Characteristics



*3" #26 WIRE

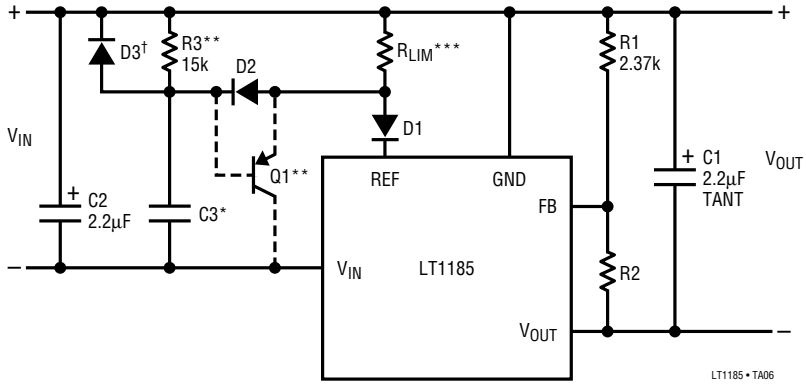
**R4 DETERMINES TRIP POINT AT I_{OUT} = 0.
R6 DETERMINES INCREASE OF TRIP POINT AS I_{OUT} INCREASES.

TRIP POINT FOR $V_{IN} = V_{OUT}\left(1 + \frac{R4 \times R7}{R3 \times R6}\right) + I_{OUT}\frac{R5 \times R7}{R6}$

FOR VALUES SHOWN, TRIP POINT FOR V_{IN} IS:
V_{OUT} + 0.37V AT I_{OUT} = 0 AND V_{OUT} = 1.18V AT I_{OUT} = 3A

†DO NOT SUBSTITUTE. OP AMP MUST HAVE COMMON-MODE RANGE EQUAL TO NEGATIVE SUPPLY.

Time Delayed Start-Up



ALL DIODES 1N4148

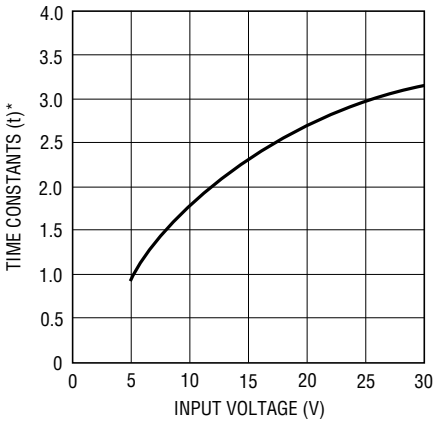
*SEE CHART FOR DELAY TIME VERSUS (C3)(R3//R_{LIM}) PRODUCT.

**FOR LONG DELAY TIMES, REPLACE D2 WITH 2N3906 TRANSISTOR AND USE R3 ONLY FOR CALCULATING DELAY TIME. R3 CAN INCREASE TO 100k.

***I_{LIM} IS ≈11k/R_{LIM}, INSTEAD OF 15k, BECAUSE OF VOLTAGE DROP IN D1. TEMPERATURE COEFFICIENT OF I_{LIM} WILL BE ≈0.11%/°C, SO ADEQUATE MARGIN MUST BE ALLOWED FOR COLD OPERATION.

†D3 PROVIDES FAST RESET OF TIMING. INPUT MUST DROP TO A LOW VALUE TO RESET TIMING.

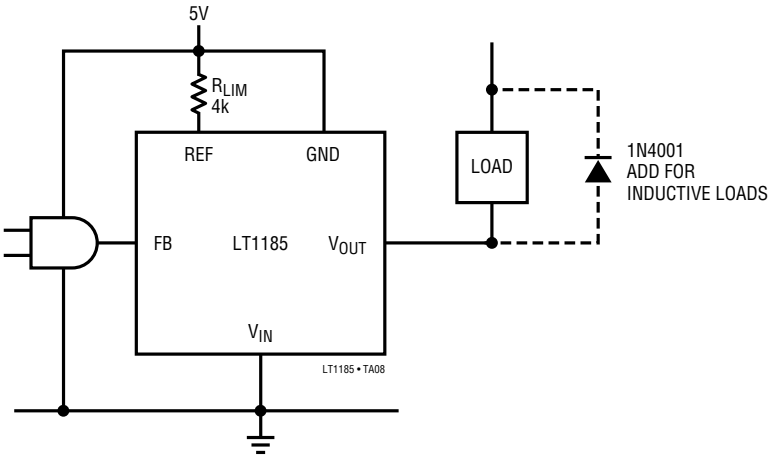
Delay Time



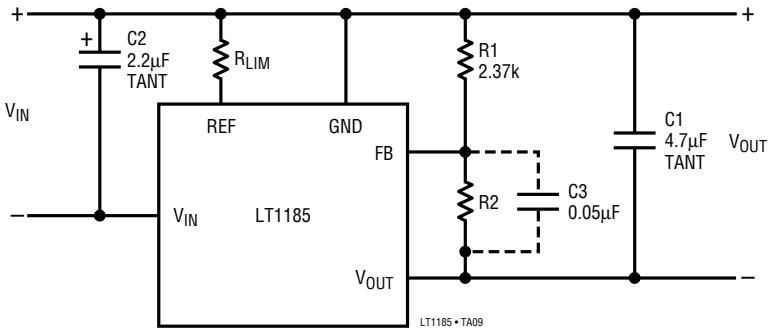
*$t = (R3//R_{LIM})(C3) = \left(\frac{R3 \times R_{LIM}}{R3 + R_{LIM}}\right)(C3)$

TYPICAL APPLICATIO NS

Logic Controlled 3A Low-Side Switch with Fault Protection

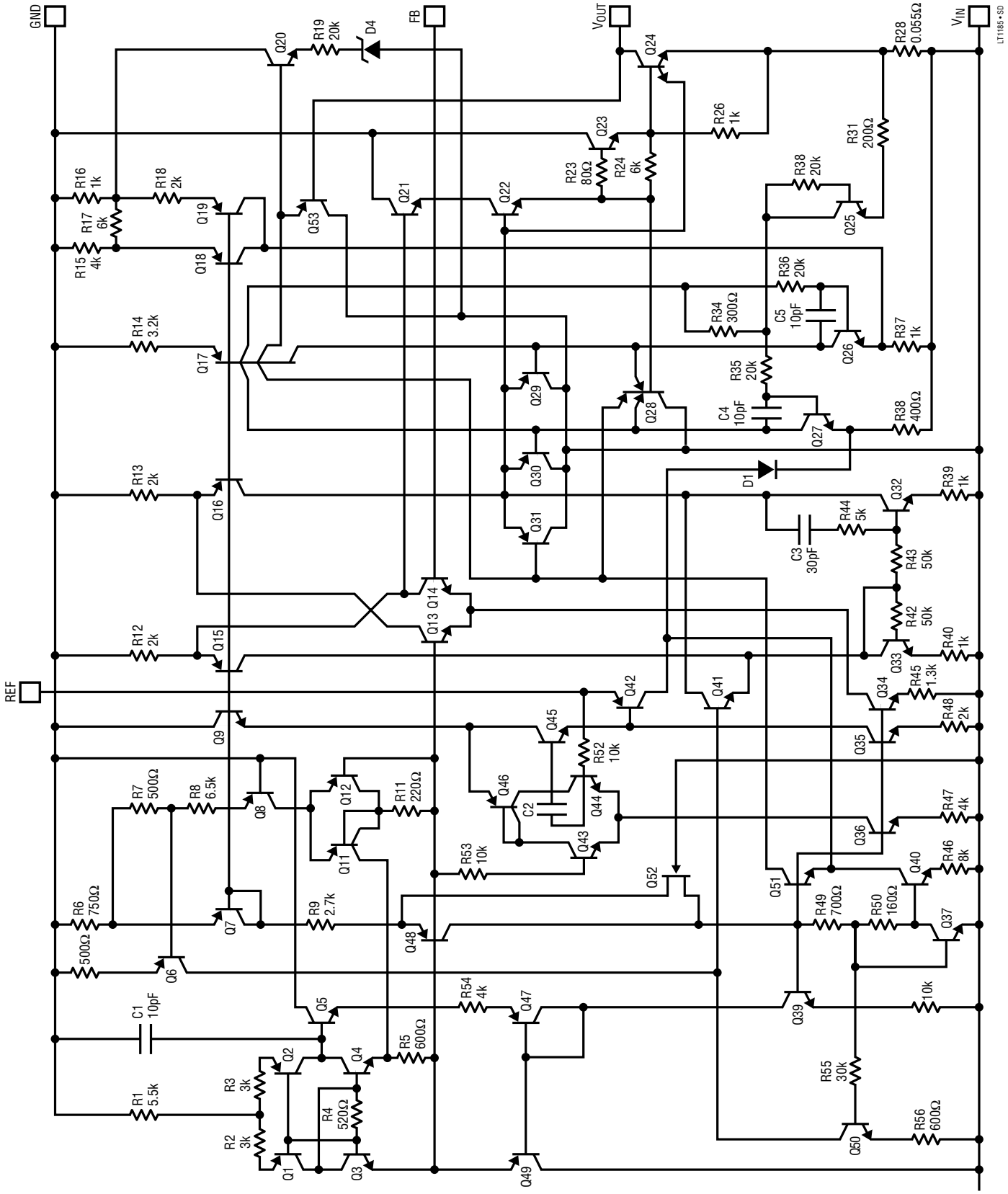


Improved High Frequency Ripple Rejection



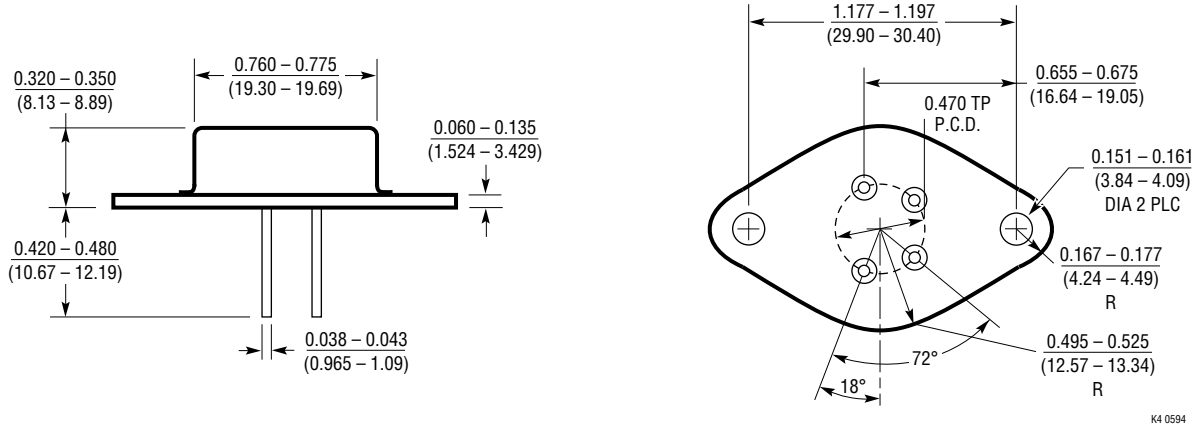
NOTE: C3 IMPOVES HIGH FREQUENCY RIPPLE REJECTION BY 6dB AT V_{OUT} = 5V, AND BY 14dB AT V_{OUT} = 12V. C1 IS INCREASED TO 4.7µF TO ENSURE GOOD STABILTITY WHEN C3 IS USED.

SCHEMATIC DIAGRAM

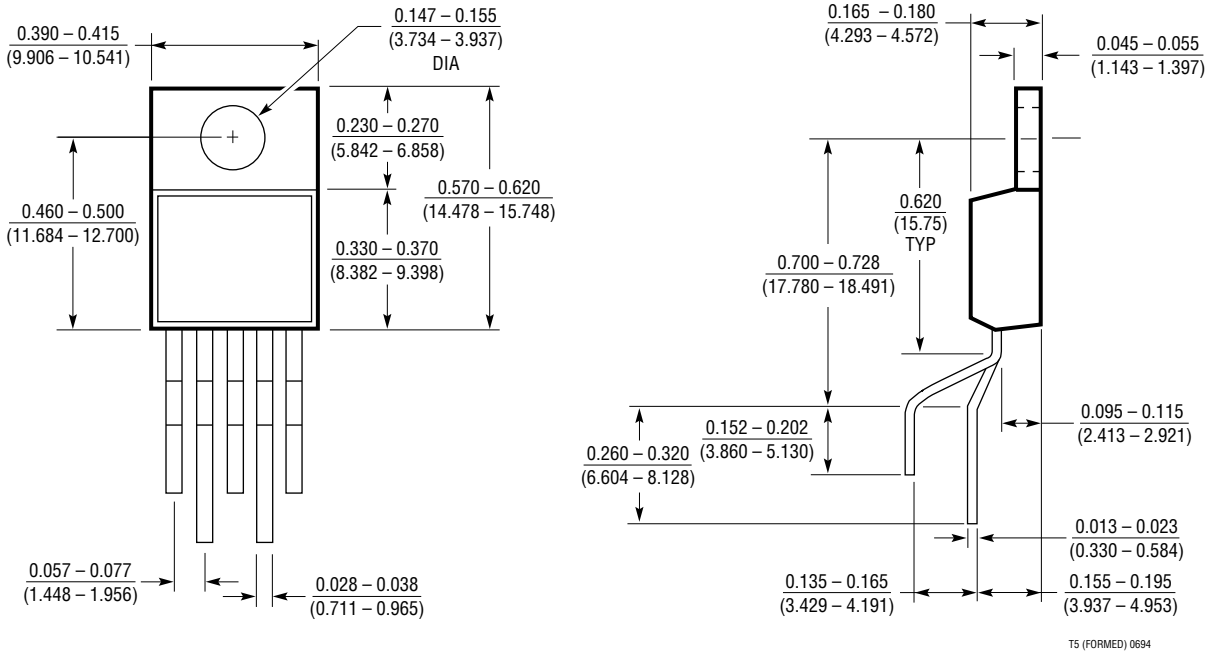


PACKAGE DESCRIPTION Dimensions in inches (millimeters) unless otherwise noted.

K Package
4-Lead TO-3 Metal Can



T Package
5-Lead TO-220 (Formed)



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