NCV7702B

1 A Dual H-Bridge Driver

This dual full−bridge driver IC is intended for 14 V automotive stepper and DC motor applications. Its four half−bridge outputs are configured as two channels and are programmed by six TTL compatible inputs, allowing flexible control of bridge operation. The device operates in standby mode, run mode, or brake mode and typically consumes less than 1 μA while in standby. In run mode, each half−bridge output can deliver load current in either direction. Brake mode activates the low side transistors or high side transistors at the selected outputs. On−chip recirculation diodes are provided, and the IC has multiple fault protection modes. Overcurrent detection protects against shorted loads between outputs and shorts to supply or ground at each output. An overcurrent fault condition activates an internal timer, which modulates faulted outputs at low duty cycle. An overcurrent condition in one channel does not affect operation in the other. Overvoltage and overtemperature detection are also provided, and turn off all bridge outputs during these fault conditions. Recovery from all fault conditions is automatic; the IC will resume normal operation in its previously selected mode upon fault resolution. Diagnostic ability is provided by two open−collector STATUS outputs which report the fault status of each channel independently during overcurrent faults, and together during overvoltage or overtemperature faults.

Features

- Single 7 V−16 V Supply
- Low Standby Current:
  - < 1.0 μA Typically
- 3.3 V / 5 V Compatible Inputs
- Independent Channel Enable
- Channels Configurable as:
  - Full−Bridge Drive
  - Half−Bridge, High Side or Low Side Drive
- On−Chip Recirculation Diodes
- Fault Protection with Automatic Recovery for:
  - Overcurrent
  - Overvoltage
  - Overtemperature
- Fault Diagnostic STATUS Outputs
- Internally Fused Leads in SO–24L Package
- These are Pb−Free Devices

Applications

- Automotive and Industrial Driver for:
  - DC or Stepper Motors
  - Relays or Solenoids
  - Unipolar or Bipolar Loads

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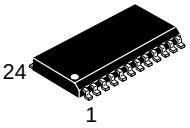
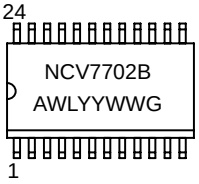


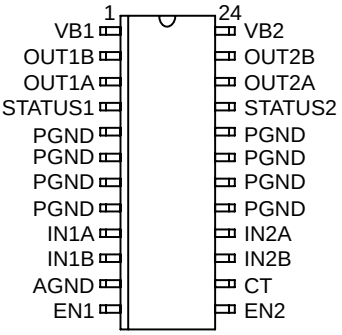
SO−24L
DW SUFFIX
CASE 751E

MARKING DIAGRAM



A	= Assembly Location
WL	= Wafer Lot
YY	= Year
WW	= Work Week
G	= Pb−Free Device

PIN CONNECTIONS



ORDERING INFORMATION

Device	Package	Shipping†
NCV7702BDWG	SO−24L (Pb−Free)	31 Units/Rail
NCV7702BDWR2G	SO−24L (Pb−Free)	1000 Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

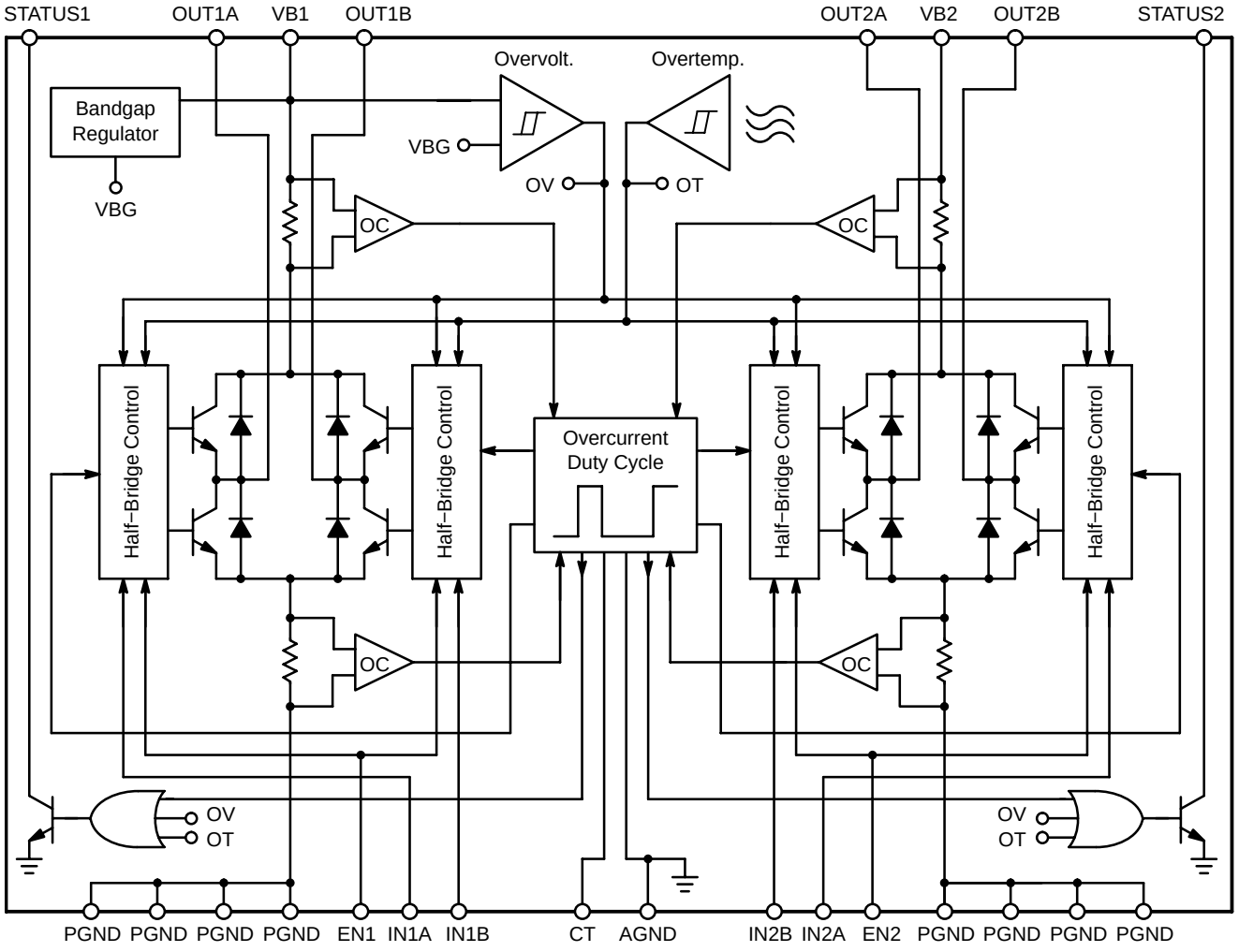


Figure 1. Block Diagram

MAXIMUM RATINGS

Rating		Value	Unit
Power Supply Voltage, VB		−0.5 to 30	V
Peak Transient Voltage (46 V Load Dump @ VB = 14 V)		60	V
Logic Inputs & Status Outputs		−0.3 to 7.0	V
Junction Temperature, T_J		150	°C
Storage Temperature Range		−65 to 150	°C
Package Thermal Resistance: Junction−to−Case, $R_{\theta JC}$ Junction−to−Ambient, $R_{\theta JA}$		 9 55	 °C/W °C/W
ESD Capability	Human Body Model Machine Model	2.0 200	kV V
Peak Reflow Soldering Temperature (60 to 150 seconds at 217°C) (Note 1)		260 peak	°C
Moisture Sensitivity Level (MSL)		3	−

Maximum Ratings are those values beyond which damage (latent or otherwise) to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute maximum−rated conditions is not implied. Voltages are with respect to device substrate.

1. For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

ELECTRICAL CHARACTERISTICS (7.0 V ≤ VB ≤ 16 V, −40°C ≤ T_J ≤ 125°C; unless otherwise specified.) Notes 2 and 3.

Characteristic	Test Conditions	Min	Typ	Max	Unit
General Characteristics					
Quiescent Current	Standby Mode, VB ≤ 12.8 V Run Mode, I_{OUT} = 750 mA, Both Channels	− −	1.0 −	10 40	μA mA
Logic Inputs					
High Level Input Voltage, V_{IH}	−	2.0	−	−	V
Low Level Input Voltage, V_{IL}	−	−	−	0.8	V
IN_X Input Current	V_{IN} = 5.0 V V_{IN} = 0 V	− −5.0	0 0	5.0 −	μA μA
EN_X Input Current	V_{IN} = 5.0 V V_{IN} = 0 V	− −5.0	130 0	200 5.0	μA μA
EN_X Delay, t_{PE}	50% of EN_X to 50% of OUT_X; Note 4 Turn ON Turn Off	− −	− −	25 60	μs
Status Outputs					
Saturation Voltage, V_{SL}	I_{STATUS} = 4.0 mA	−	−	0.4	V
Leakage Current	V_{STATUS} = 5.0 V	−	−	10	μA
Half−Bridge Driver Outputs					
Total Output Saturation Voltage	I_{OUT} = 750 mA, Each Channel	−	2.5	3.0	V
Output Saturation Voltage High	I_{OUT} = 750 mA, VB − V_{OUT}, Each Driver	−	1.25	1.6	V
Output Saturation Voltage Low	I_{OUT} = 750 mA, V_{OUT} − V_{PGND}, Each Driver	−	1.25	1.6	V
Output Leakage	V_{OUT} = VB V_{OUT} = V_{PGND}	− −5.0	0 0	5.0 −	μA μA
Overcurrent Threshold, I_{OC}	Low Side, Each Channel High Side, Each Channel	0.9 0.775	1.25 0.900	1.6 1.10	A
Overcurrent Duty Cycle	470 pF ≤ C_T ≤ 1500 pF; Note 5	3.0	4.0	6.0	%
Switching Delay, t_{PI} Sink to Source Source to Sink	 50% of IN_X to 60% of OUT_X; Note 6 50% of IN_X to 40% of OUT_X; Note 6	 0.20 0.20	 − −	 14 10	μs
Dead Band Time, t_{DB}	Note 6	0.10	−	10	μs
Recirculation Diode Forward Voltage	I_{DIODE} = 750 mA	−	−	2.5	V
Delay Timer					
Charge Current, I_{CHG}	−	−85	−65	−45	μA
Discharge Current, I_{DCH}	−	1.25	2.0	3.25	μA
Input Threshold High, V_{CH}	−	1.85	2.0	2.15	V
Input Threshold Low, V_{DC}	−	200	300	400	mV
Global Fault Protection					
Overtemperature Detection Threshold	Note 7	150	−	210	°C
Overtemperature Hysteresis	Note 7	−	15	−	°C
Overvoltage Detection Threshold	Note 8	26	28	30	V
Overvoltage Hysteresis	−	500	850	1200	mV

2. Designed to meet these characteristics over the stated voltage and temperature recommended operating ranges, though may not be 100% parametrically tested in production.
3. Operation is guaranteed down to VB = 6.0 V. Electrical characteristics may be outside the limits at that voltage.
4. See Figures 2 and 3; VB = 14 V, R = 100 Ω.
5. C_T must remain in this range to guarantee proper operation, and to ensure part integrity, during hard short conditions.
6. See Figures 2 and 4; VB = 14 V, R = 100 Ω.
7. Guaranteed by design.
8. Consult factory for no overvoltage detection or lower overvoltage detection threshold options.

PACKAGE PIN DESCRIPTION

PACKAGE PIN #	PIN SYMBOL	FUNCTION
1	VB1	Power supply input voltage; overvoltage detection occurs at this pin.
2	OUT1B	Half−bridge output controlled by IN1B.
3	OUT1A	Half−bridge output controlled by IN1A.
4	STATUS1	Diagnostic output; reports channel #1 fault condition.
5	PGND	Power supply return.
6	PGND	Power supply return.
7	PGND	Power supply return.
8	PGND	Power supply return.
9	IN1A	Logic level input.
10	IN1B	Logic level input.
11	AGND	Analog supply return; reference for external C_T capacitor, device substrate.
12	EN1	Enable for OUT1A and OUT1B.
13	EN2	Enable for OUT2A and OUT2B.
14	CT	External capacitor; sets overcurrent delay time and duty cycle.
15	IN2B	Logic level input.
16	IN2A	Logic level input.
17	PGND	Power supply return.
18	PGND	Power supply return.
19	PGND	Power supply return.
20	PGND	Power supply return.
21	STATUS2	Diagnostic output; reports channel #2 fault condition.
22	OUT2A	Half−bridge output controlled by IN2A.
23	OUT2B	Half−bridge output controlled by IN2B.
24	VB2	Power supply input voltage.

INPUT LOGIC TABLE

EN1 = EN2 = 0 = Standby Mode											
Channel #1						Channel #2					
EN1	IN1A	IN1B	OUT1A	OUT1B	Mode	EN2	IN2A	IN2B	OUT2A	OUT2B	Mode
1	0	0	Low	Low	Brake Low	1	0	0	Low	Low	Brake Low
1	0	1	Low	High	Run	1	0	1	Low	High	Run
1	1	0	High	Low	Run	1	1	0	High	Low	Run
1	1	1	High	High	Brake High	1	1	1	High	High	Brake High
0	X	X	|Z|	|Z|	Off	0	X	X	|Z|	|Z|	Off

NOTE: X = Don't Care; |Z| = Output Off.

STATUS OUTPUT TABLE

STATUS1	STATUS2	Fault Diagnostic
1	1	No Fault.
0	1	Channel 1 Overcurrent; Note 9
1	0	Channel 2 Overcurrent; Note 9
0	0	Overvoltage, Overtemperature or Overcurrent in Both Channels; Notes 9 and 10

9. During overcurrent, the STATUS outputs will be modulated at the overcurrent duty cycle rate. See Figure 5.
10. During overtemperature, the STATUS outputs will be modulated by the thermal time constants.

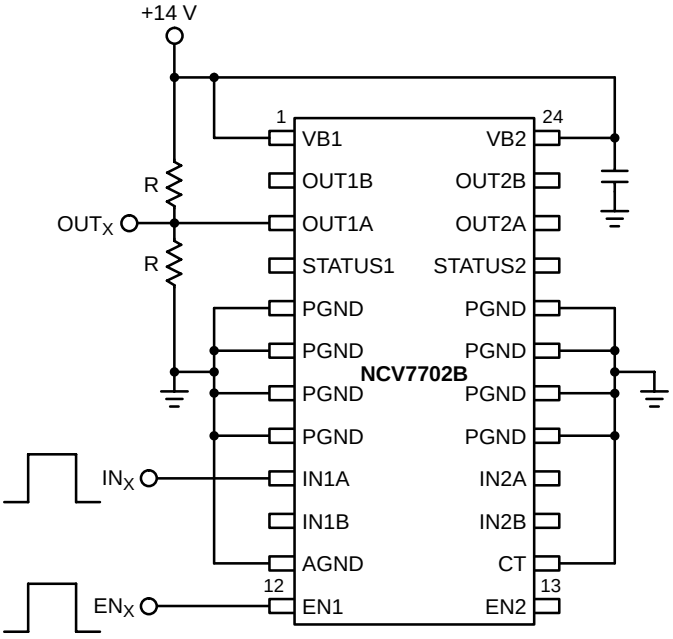


Figure 2. Propagation Delay and Dead Band Timing Test Circuit

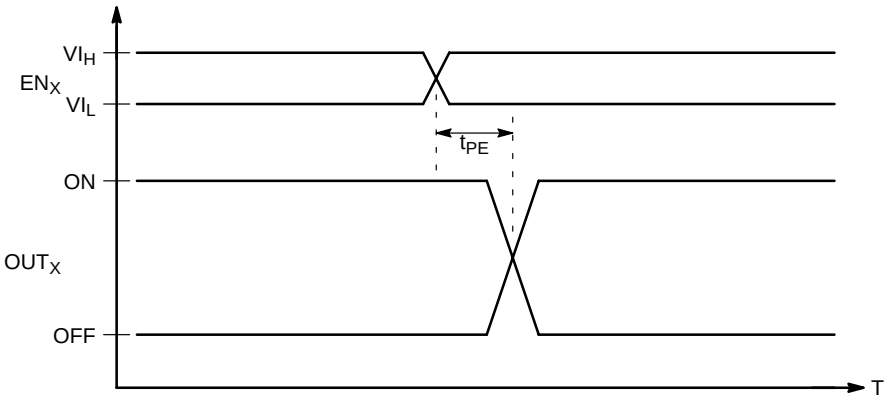


Figure 3. EN_X Propagation Delay

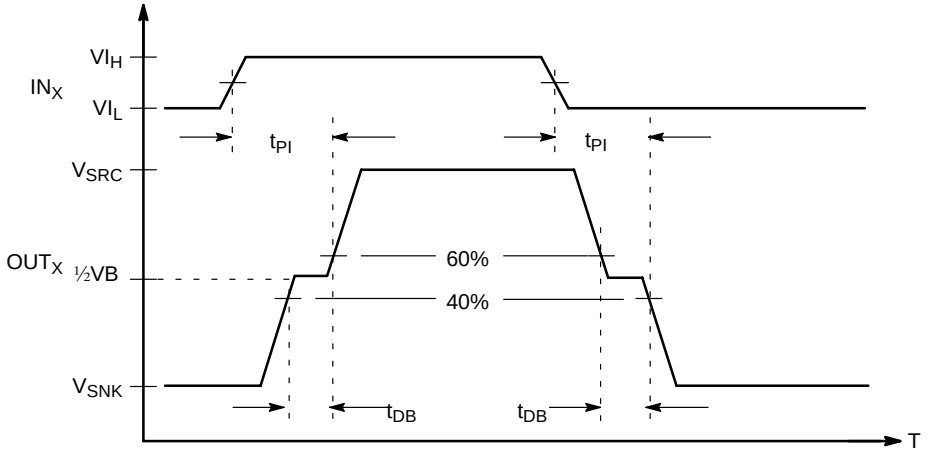


Figure 4. OUT_X Propagation Delay and Dead Band Timing

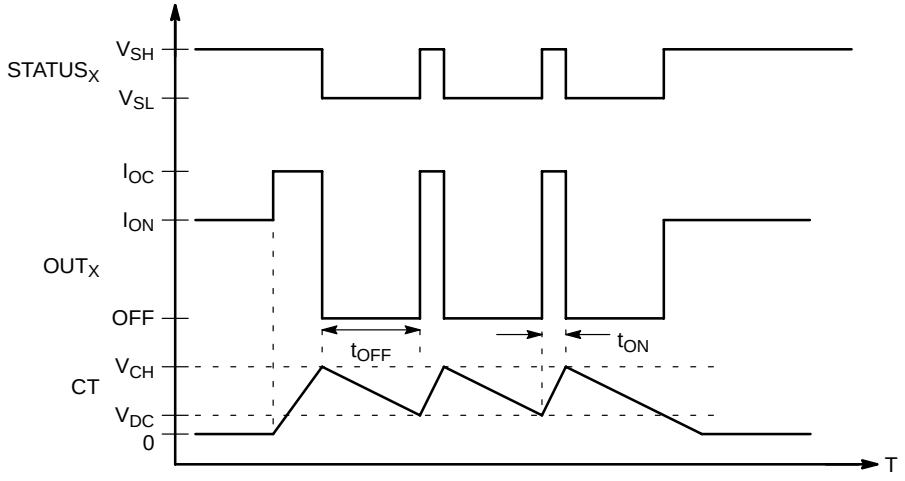


Figure 5. Overcurrent, Status and Duty Cycle Timing

Functional Description

The NCV7702B is arranged as four half−bridge drivers in two independent channels. Each channel can be operated as a full−bridge or half−bridge to drive multiple load configurations. Separate ENable inputs are used to control which channel is active. Each ENable input has a nominal 50 kΩ internal pull−down resistor to ensure that the outputs remain off during power−up. The four IN_X control inputs address each half−bridge output, and each output follows the state of its input. When IN_X is at logic one, OUT_X is sourcing current from the VB supply; when IN_X is at logic zero, OUT_X is sinking current to the PGND return.

Half−Bridge Drivers

The half−bridge drivers of each OUT_X are comprised of an NPN Darlington driver on the low−side and a compound PNP−NPN driver on the high−side. Each half−bridge driver is capable of 1 A (min) peak current and is overcurrent protected against load and system faults. Cross conduction currents within each half−bridge are suppressed by the use of a dead−band timer. Each IN_X input contains an independent dead−band timer that is activated on either edge of the input transition.

Overcurrent detection circuitry is provided in both the low−side and high−side drivers of each half−bridge output. When activated, the overcurrent detectors trigger an internal timer which causes both half−bridge drivers in the same channel to be modulated at 4% (Typ.) duty cycle. The timer also activates the channel's STATUS output, causing it to be similarly modulated (see Figure 5.) Upon removal of the fault condition, the channel automatically resumes operation in its previously programmed mode and its STATUS output returns to a no−fault state.

Recirculation diodes at each OUT_X clamp load transients to either VB or PGND and help contain switching currents within each load loop.

Overcurrent Duty Cycle Timer

A single timer for overcurrent duty cycle is common to both channels. The timer is triggered when a half−bridge in either channel has detected an overcurrent fault. An external capacitor connected to the NCV7702B's C_T pin is used to program the period of the timer, and the ratio of two internally fixed currents programs the timer's duty cycle. The capacitor voltage is normally kept at zero by discharge current I_{DCH}. Upon detection of overcurrent, charging current I_{CHG} is switched on and the C_T capacitor begins charging from zero towards the timer's upper threshold ($V_{DH.}$) When the capacitor voltage crosses V_{DH} the faulted channel's outputs are switched off and the channel's STATUS output is switched from V_{SH} to V_{SL} (see Figure 5.) The charging current is switched off, and the capacitor voltage decreases toward the timer's lower (V_{DL}) threshold. Upon crossing the lower threshold, the channel's outputs are switched on and the channel's STATUS output returns to its V_{SH} voltage. This behavior continues until the fault condition is resolved. If the fault condition is resolved before V_{DH} is reached, the timer is reset and no modulation of the previously faulted channel's half−bridge or STATUS outputs occurs.

After the timer's initial charge cycle, the output off time is: $t_{OFF} = C_T (V_{CH} - V_{Dc})/ I_{DCH}$.

The output on time is: $t_{ON} = C_T (V_{CH} - V_{Dc})/ I_{CHG}$.

The timer period is: $T = t_{OFF} + t_{ON}$.

The value of the C_T capacitor is required to be in the range of 470 to 1500 pF. Values below 470 pF may cause timer mis−operation due to internal delays, while values above 1500 pF may cause excessive power dissipation. Connecting the C_T pin to ground will prevent operation of the current limit function.

Overvoltage and Overtemperature Protection

Overvoltage detection circuitry is intended to allow limited operation of the NCV7702B during double−battery conditions. Detection is via the VB1 pin and causes both channels of the IC to be switched off when the detection threshold is exceeded. Hysteresis is provided to improve noise immunity of the overvoltage function.

Overtemperature detection circuitry monitors the junction temperature internal to the IC and is intended to ensure reliability by preventing excessive power dissipation. The detection circuitry is centrally located on the IC and causes both channels of the IC to be switched off when the detection threshold is exceeded. Hysteresis is provided to improve noise immunity of the overtemperature function.

Both STATUS outputs are switched to the V_{SL} state during either overvoltage or overtemperature faults. Normal operation of the IC is resumed automatically upon resolution the fault, and the STATUS outputs return to the V_{SH} State.

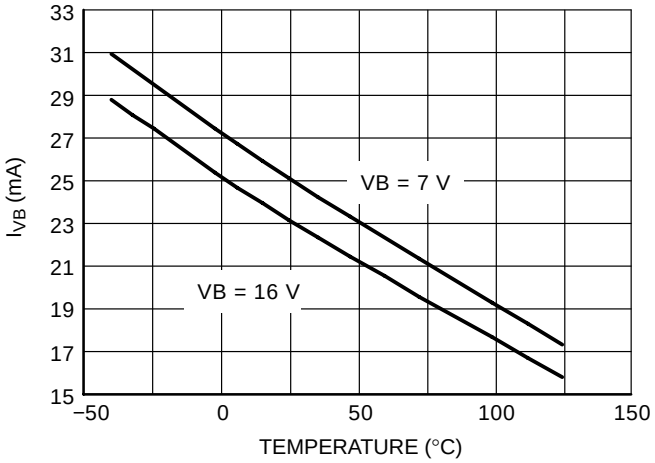


Figure 6. Run Mode Bias Current vs. Temperature

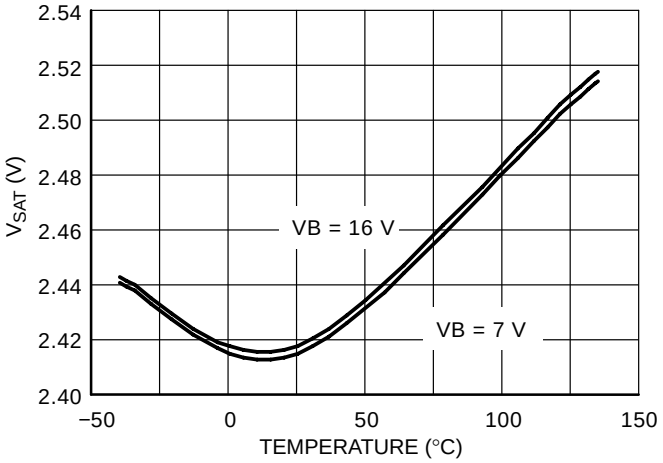


Figure 7. Total V_{SAT} vs. Temperature

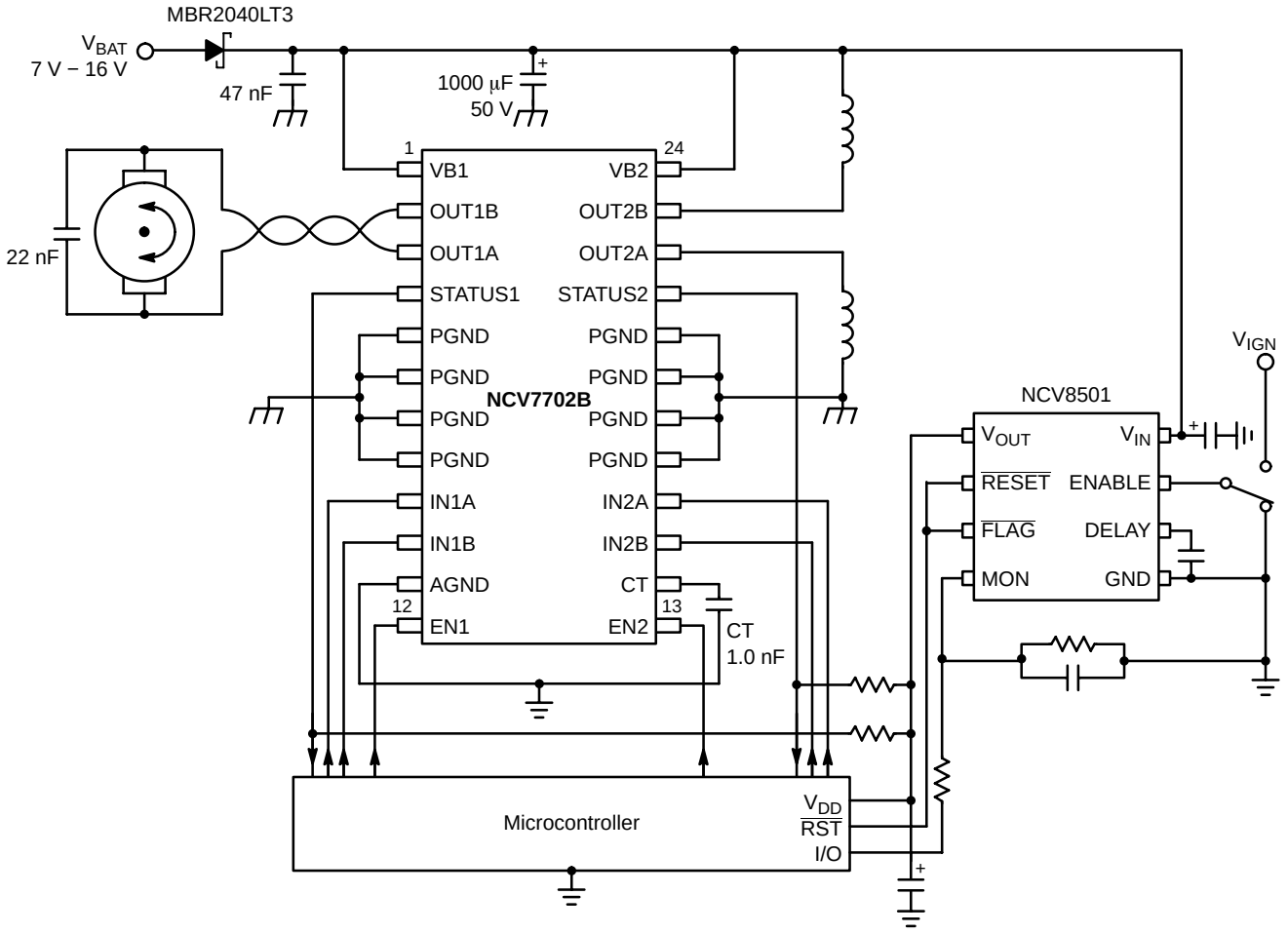
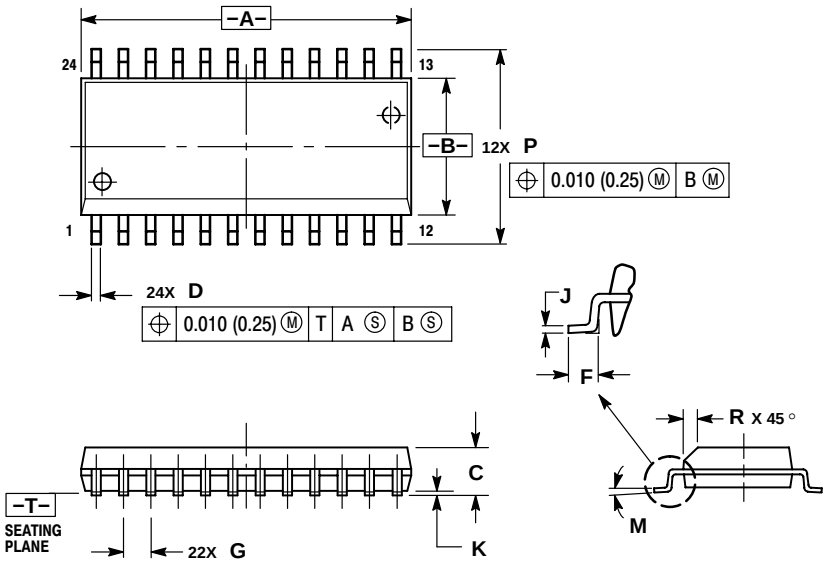


Figure 8. Application Diagram

NOTE: Both V_B inputs must be connected to the power supply. All PGND pins must be connected to the power supply return (GND). For best thermal performance, the PGND pins should be connected to a thermal plane (heat sink) on the PC board.

PACKAGE DIMENSIONS

SO−24L
DW SUFFIX
CASE 751E−04
ISSUE E



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	15.25	15.54	0.601	0.612
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.41	0.90	0.016	0.035
G	1.27 BSC		0.050 BSC	
J	0.23	0.32	0.009	0.013
K	0.13	0.29	0.005	0.011
M	0°	8°	0°	8°
P	10.05	10.55	0.395	0.415
R	0.25	0.75	0.010	0.029

PUBLICATION ORDERING INFORMATION

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NCV7702B/D