87C196KT/87C196KS 20 MHz ADVANCED 16-BIT CHMOS MICROCONTROLLER

Automotive

(−40°C to +125°C Ambient)

- **High Performance CHMOS 16-Bit CPU**
- **Up to 32 Kbytes of On-Chip EPROM**
- **Up to 1 Kbyte of On-Chip Register RAM**
- **Up to 512 Bytes of Additional RAM (Code RAM)**
- **Register-Register Architecture**
- **8 Channel/10-Bit A/D with Sample/Hold**
- **37 Prioritized Interrupt Sources**
- **Up to Seven 8-Bit (56) I/O Ports**
- **Full Duplex Serial I/O Port**
- **Dedicated Baud Rate Generator**
- **Interprocessor Communication Slave Port**
- **Selectable Bus Timing Modes for Flexible Interfacing**
- **Oscillator Fail Detection Circuitry**
- **High Speed Peripheral Transaction Server (PTS)**
- **Two Dedicated 16-Bit High-Speed Compare Registers**
- **10 High Speed Capture/Compare (EPA)**
- **Full Duplex Synchronous Serial I/O Port (SSIO)**
- **Two Flexible 16-Bit Timer/Counters**
- **Quadrature Counting Inputs**
- **Flexible 8-/16-Bit External Bus (Programmable)**
- **Programmable Bus (HLD/HLDA)**
- **1.4 μs 16 x 16 Multiply**
- **2.4 μs 32/16 Divide**
- **68-Pin PLCC Package**
- **20 MHz Operation**

The 87C196Kx devices represents the 4th generation of MCS® 96 microcontroller products implemented on Intel's advanced 1 micron process technology. These products are based on the 80C196KB device with enhancements ideal for automotive applications. The instruction set is a true super set of the 80C196KB with a few new instructions.

The MCS 96 microcontroller family members are all high performance microcontrollers with a 16-bit CPU. The 87C196KT is composed of the high speed (20 MHz) KX macrocore as well as the following peripherals: Up to 32 Kbytes of Program EPROM, up to 1 Kbytes of Register RAM (00-3FFH including SFRs), up to 512 bytes of code RAM (16-bit addressing modes) with the ability to execute from this RAM space, an eight channel-10 Bit ±3LSB analog to digital converter with programmable S/H times with conversion times <20 μs at 16 MHz, an asynchronous/synchronous serial I/O port (8096 compatable) with a dedicated 16-bit baud rate generator, an additional synchronous serial I/O port with full duplex master/slave transceivers, a flexible timer/counter structure with prescaler, cascading, and quadrature capabilities, 10 modularized multiplexed high speed I/O for capture and compare (called Event Processor Array) with 200 ns resolution and double buffered inputs, and a sophisticated prioritized interrupt structure with programmable Peripheral Transaction Server (PTS). The PTS has several channel modes, including single/burst block transfers from any memory location to any memory location, a PWM and PWM toggle mode to be used in conjunction with the EPA, and an A/D scan mode.

Additional SFR space is allocated for the EPA and can be ''windowed'' into the lower Register RAM area.

NOTICE: This is a production data sheet. The specifications are subject to change without notice.

November 1995 **Order Number: 272513-003**

Device	Pins/Package	EPROM	Reg RAM	Code RAM	I/O	EPA	SIO	SSIO	A/D
87C196KT	68-Pin PLCC	32K	1K	512b	56	10	Y	Y	8
87C196KS	68-Pin PLCC	24K	1K	256b	56	10	Y	Y	8

NOTE:
This is a PRODUCT PREVIEW DATA SHEET. The AC and DC parameters contained within this data sheet may change after full automotive temperature characterization of the device has been performed. Contact your local sales office before finalizing the Timing and D.C. characteristics of a design to verify you have the latest information.

ARCHITECTURE

The KT/KS are new members of the MCS-96 family having the same architecture and use the same instruction set as the 80C196KB. Many new features have been added including:

CPU FEATURES

- **Powerdown and Idle Modes**
- **20 MHz Operating Frequency**
- **A High Performance Peripheral Transaction Server (PTS)**
- **37 Interrupt Vectors**
- **Up to 512 Bytes of Additional Code RAM**
- **Up to 1 Kbyte of Additional Register RAM**
- **"Windowing" Allows 8-Bit Addressing to some 16-Bit Addresses**
- **1.4 μs 16 x 16 Multiply**
- **2.4 μs 32/16 Divide**
- **Oscillator Fail Detect Circuitry**

PERIPHERAL FEATURES

— Programmable A/D Conversion and S/H Times

— 10 Capture/Compare I/O with 2 Flexible Timers (200 ns Resolution and Double Buffered Inputs)

— Synchronous Serial I/O Port for Full Duplex Serial I/O

— Synchronous/Asynchronous Serial I/O Port (with Dedicated 16-Bit Baud Rate Generator)

— Total Utilization of ALL Available Pins (I/O Mux'd with Control)

— (2) 16-Bit Timers with Prescale, Cascading, and Quadrature Counting Capabilities

— Up to 12 Externally Triggered Interrupts

NEW INSTRUCTIONS

XCH/XCHB Exchange the contents of two locations, either Word or Byte is supported.

BMOVI Interruptable Block Move Instruction, allows the user to be interrupted during long executing Block Moves.

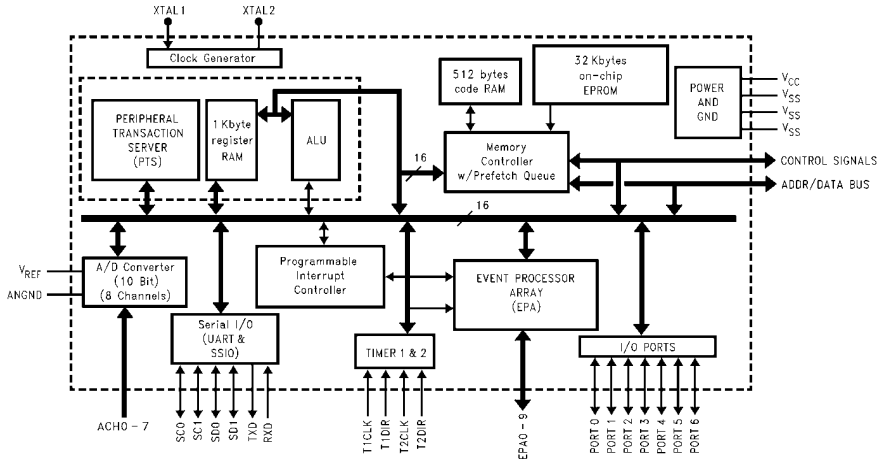
TIJMP Table Indirect JUMP. This instruction incorportes a way to do complex CASE level branches through one instruction. An example of such code savings: several interrupt sources and only one interrupt vector. The TIJMP instruction will sort through the sources and branch to the appropriate subcode level in one instruction. This instruction was added especially for the EPA structure, but has other code saving advantages.

EPTS/DPTS Enable and Disable Interrupts (Works like EI and DI).

SFR OPERATION

A total of 1 Kbyte of Register RAM is implemented on the 87C196KT/KS devices. These locations support the on-chip peripherals that the 87C196KT/KS has (SFR's), as well as offering a data storage area. These locations are all 8-bit directly addressable by use of the windowing technique. Any 32-, 64- or 128-byte section can be relocated into the upper 32-, 64- or 128-byte area of the Register RAM area 080H–0FFH.

87C196KT Block Diagram



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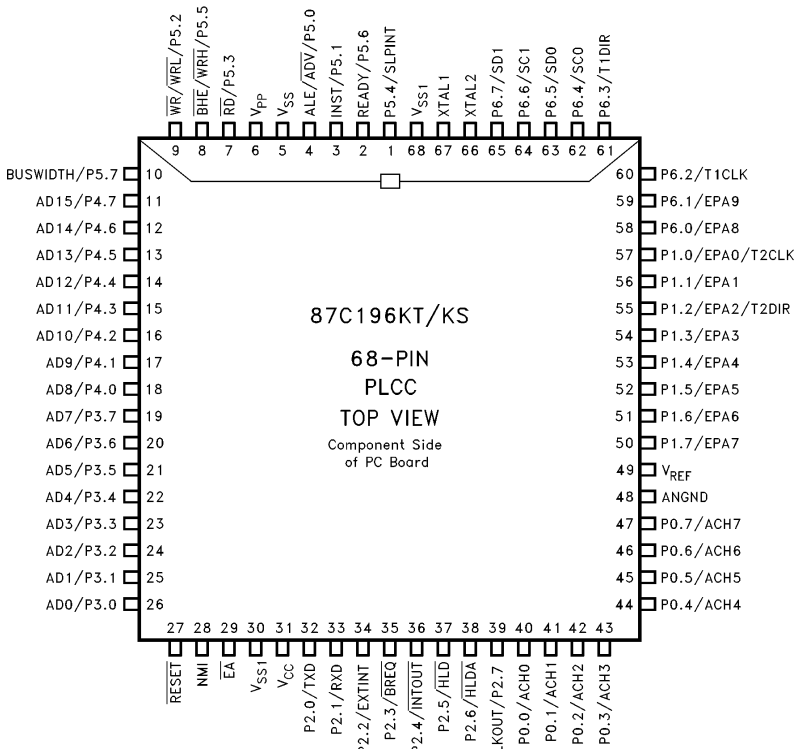

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PIN DESCRIPTIONS

Symbol	Name and Function
V_{CC}	Main supply voltage (+5V).
V_{SS}, V_{SSI}, V_{SSI}	Digital circuit ground (0V). There are three V_{SS} pins, all of which MUST be connected.
V_{REF}	Reference for the A/D converter (+5V). V_{REF} is also the supply voltage to the analog portion of the A/D converter and the logic used to read Port 0. Must be connected for A/D and Port 0 to function.
V_{PP}	Programming voltage for the EPROM parts. It should be +12.5V for programming. It is also the timing pin for the return from powerdown circuit. Connect this pin with a 1 μF capacitor to V_{SS} and a 1 MΩ resistor to V_{CC}. If this function is not used, V_{PP} may be tied to V_{CC}.
ANGND	Reference ground for the A/D converter. Must be held at nominally the same potential as V_{SS}.
XTAL1	Input of the oscillator inverter and the internal clock generator.
XTAL2	Output of the oscillator inverter.
P2.7/CLKOUT	Output of the internal clock generator. The frequency is ½ the oscillator frequency. It has a 50% duty cycle. Also LSIO pin.
$\overline{\text{RESET}}$	Reset input to the chip. Input low for at least 16 state times will reset the chip. The subsequent low to high transition resynchronizes CLKOUT and commences a 10-state time sequence in which the PSW is cleared, bytes are read from 2018H and 201AH loading the CCBs, and a jump to location 2080H is executed. Input high for normal operation. $\overline{\text{RESET}}$ has an internal pullup.
P5.7/BUSWIDTH	Input for bus width selection. If CCR bit 1 is a one and CCR1 bit 2 is a one, this pin dyamically controls the Buswidth of the bus cycle in progress. If BUSWIDTH is low, an 8-bit cycle occurs, if BUSWIDTH is high, a 16-bit cycle occurs. If CCR bit 1 is ''0'' and CCR1 bit 2 is ''1'', all bus cycles are 8-bit, if CCR bit 1 is ''1'' and CCR1 bit 2 is ''0'', all bus cycles are 16-bit. CCR bit 1 = ''0'' and CCR1 bit 2 = ''0'' is illegal. Also an LSIO pin when not used as BUSWIDTH.
NMI	A positive transition causes a non maskable interrupt vector through memory location 203EH.
P5.1/INST	Output high during an external memory read indicates the read is an instruction fetch. INST is valid throughout the bus cycle. INST is active only during external memory fetches, during internal EPROM fetches INST is held low. Also LSIO when not INST.
$\overline{\text{EA}}$	Input for memory select (External Access). $\overline{\text{EA}}$ equal to a high causes memory accesses to locations 2000H through 9FFFH to be directed to on-chip EPROM/ROM. $\overline{\text{EA}}$ equal to a low causes accesses to these locations to be directed to off-chip memory. $\overline{\text{EA}}$ = +12.5V causes execution to begin in the Programming Mode. $\overline{\text{EA}}$ is latched at reset.
P5.0/ALE/$\overline{\text{ADV}}$	Address Latch Enable or Address Valid output, as selected by CCR. Both pin options provide a latch to demultiplex the address from the address/data bus. When the pin is $\overline{\text{ADV}}$, it goes inactive (high) at the end of the bus cycle. $\overline{\text{ADV}}$ can be used as a chip select for external memory. ALE/$\overline{\text{ADV}}$ is active only during external memory accesses. Also LSIO when not used as ALE.
P5.3/$\overline{\text{RD}}$	Read signal output to external memory. $\overline{\text{RD}}$ is active only during external memory reads or LSIO when not used as $\overline{\text{RD}}$.
P5.2/$\overline{\text{WR}}$/$\overline{\text{WRL}}$	Write and Write Low output to external memory, as selected by the CCR, $\overline{\text{WR}}$ will go low for every external write, while $\overline{\text{WRL}}$ will go low only for external writes where an even byte is being written. $\overline{\text{WR}}$/$\overline{\text{WRL}}$ is active during external memory writes. Also an LSIO pin when not used as $\overline{\text{WR}}$/$\overline{\text{WRL}}$.

PIN DESCRIPTIONS (Continued)

Symbol	Name and Function
P5.5/$\overline{BHE}$/$\overline{WRH}$	Byte High Enable or Write High output, as selected by the CCR. $\overline{BHE}$ = 0 selects the bank of memory that is connected to the high byte of the data bus. A0 = 0 selects that bank of memory that is connected to the low byte. Thus accesses to a 16-bit wide memory can be to the low byte only (A0 = 0, $\overline{BHE}$ = 1), to the high byte only (A0 = 1, $\overline{BHE}$ = 0) or both bytes (A0 = 0, $\overline{BHE}$ = 0). If the $\overline{WRH}$ function is selected, the pin will go low if the bus cycle is writing to an odd memory location. $\overline{BHE}$/$\overline{WRH}$ is only valid during 16-bit external memory write cycles. Also an LSIO pin when not BHE/$\overline{WRH}$.
P5.6/READY	Ready input to lengthen external memory cycles, for interfacing with slow or dynamic memory, or for bus sharing. If the pin is high, CPU operation continues in a normal manner. If the pin is low prior to the falling edge of CLKOUT, the memory controller goes into a wait state mode until the next positive transition in CLKOUT occurs with READY high. When external memory is not used, READY has no effect. The max number of wait states inserted into the bus cycle is controlled by the CCR/ CCR1. Also an LSIO pin when READY is not selected.
P5.4/SLPINT	Dual function I/O pin. As a bidirectional port pin or as a system function. The system function is a Slave Port Interrupt Output Pin.
P6.2/T1CLK	Dual function I/O pin. Primary function is that of a bidirectional I/O pin, however, it may also be used as a TIMER1 Clock input. The TIMER1 will increment or decrement on both positive and negative edges of this pin.
P6.3/T1DIR	Dual function I/O pin. Primary function is that of a bidirectional I/O pin, however, it may also be used as a TIMER1 Direction input. The TIMER1 will increment when this pin is high and decrements when this pin is low.
PORT1/EPA0–7 P6.0–6.1/EPA8–9	Dual function I/O port pins. Primary function is that of bidirectional I/O. System function is that of High Speed capture and compare. EPA0 and EPA2 have yet another function of T2CLK and T2DIR of the TIMER2 timer/counter.
PORT 0/ACH0–7	8-bit high impedance input-only port. These pins can be used as digital inputs and/or as analog inputs to the on-chip A/D converter. These pins are also used as inputs to EPROM parts to select the Programming Mode.
P6.3–6.7/SSIO	Dual function I/O ports that have a system function as Synchronous Serial I/O. Two pins are clocks and two pins are data, providing full duplex capability.
PORT 2	8-bit multi-functional port. All of its pins are shared with other functions.
PORT 3 and 4	8-bit bidirectional I/O ports with open drain outputs. These pins are shared with the multiplexed address/data bus which has strong internal pullups.

CCB (2018H : Byte)

0	PD	=	''1'' Enables Powerdown
1	BW0	=	See Table
2	WR	=	''1'' = $\overline{WR}$/BHE - ''0'' = $\overline{WRL}$/$\overline{WRH}$
3	ALE	=	''1'' = ALE - ''0'' = $\overline{ADV}$
4	IRC0	=	See Table
5	IRC1	=	
6	LOC0	=	See Table
7	LOC1	=	

CCB1 (201AH : Byte)

0	0	=	Reserved Must Be ''0''
1	IRC2	=	See Table
2	BW1	=	See Table
3	WDE	=	''0'' = Always Enabled
4	1	=	Reserved Must Be ''01''
5	0	=	
6	MSEL0	=	See Table
7	MSEL1	=	

LOC1	LOC0	Function
0	0	Read and Write Protected
0	1	Write Protected Only
1	0	Read Protected Only
1	1	No Protection

IRC2	IRC1	IRC0	Max Wait States
0	0	0	Zero Wait States
1	0	0	1 Wait State
1	0	1	2 Wait States
1	1	0	3 Wait States
1	1	1	INFINITE

MSEL1	MSEL0	Bus Timing Mode
0	0	Mode 0 (1-Wait KR)
0	1	Mode 1
1	0	Mode 2
1	1	Mode 3 (KR)

BW1	BW0	Bus Width
0	0	ILLEGAL
0	1	16-Bit Only
1	0	8-Bit Only
1	1	BW Pin Controlled

Mode 0 (1-Wait KR): Designed to be similar to the 87C196KR bus timing with 1 automatic wait state.

See AC Timings section for actual timings data.

Mode 1: $\overline{RD}$, $\overline{WR}$, advanced 1 T_{OSC}
ALE advanced 0.5 T_{OSC}
ALE pulse width remains 1 T_{OSC}

Mode 2: $\overline{RD}$, $\overline{WR}$, advanced 1 T_{OSC}
ALE advanced 0.5 T_{OSC}
ALE pulse width remains 1 T_{OSC}
Address advanced 0.5 T_{OSC}

Mode 3 (KR): Designed to be similar to the 87C196KR bus timing.

See AC Timings section for actual timings data.

ABSOLUTE MAXIMUM RATINGS*

Storage Temperature . . . . . −60°C to +150°C

Voltage from V_{PP} or $\overline{EA}$ to V_{SS} or ANGND . . . . . −0.5V to +13.0V

Voltage from Any Other Pin to V_{SS} or ANGND . . . . . −0.5 to +7.0V
This includes V_{PP} on ROM and CPU devices.

Power Dissipation 0.5W

NOTICE: This is a production data sheet. The specifications are subject to change without notice.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Units
T_A	Ambient Temperature Under Bias	−40	+125	°C
V_{CC}	Digital Supply Voltage	4.50	5.50	V
V_{REF}	Analog Supply Voltage	4.50	5.50	V
F_{OSC}	Oscillator Frequency	4	20	MHz (Note 4)

NOTE:
ANGND and V_{SS} should be nominally at the same potential.

DC CHARACTERISTICS (Under Listed Operating Conditions)

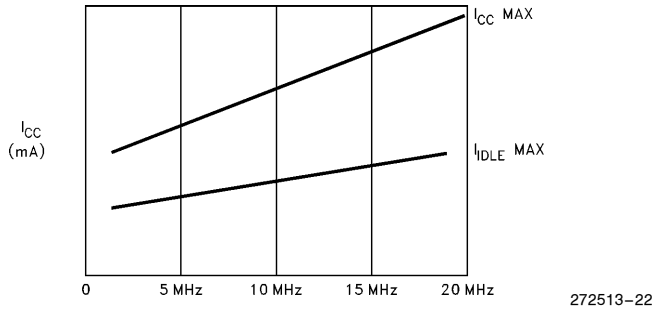
Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
I_{CC}	V_{CC} Supply Current (−40°C to +125°C Ambient)	XTAL1 = 20 MHz, $V_{CC} = V_{PP} = V_{REF} = 5.5V$ (While device in Reset)			95	mA
I_{REF}	A/D Reference Supply Current				5	mA
I_{IDLE}	Idle Mode Current	XTAL1 = 20 MHz, $V_{CC} = V_{PP} = V_{REF} = 5.5V$			45	mA
I_{PD}	Powerdown Mode Current	$V_{CC} = V_{PP} = V_{REF} = 5.5V$(6, 9)		50	TBD	µA
V_{IL}	Input Low Voltage (all pins)	For PORT0(8)	−0.5V		0.3 V_{CC}	V
V_{IH}	Input High Voltage	For PORT0(8)	0.7 V_{CC}		V_{CC} + 0.5	V
V_{IH1}	Input High Voltage XTAL1	XTAL1 Input Pin Only(1)	0.7 V_{CC}		V_{CC} + 0.5	V
V_{IH2}	Input High Voltage on RESET	RESET input pin only	0.7 V_{CC}		V_{CC} + 0.5	V
V_{OL}	Output Low Voltage (Outputs Configured as Complementary)	I_{OL} = 200 µA(3,5) I_{OL} = 3.2 mA I_{OL} = 7.0 mA			0.3 0.45 1.5	V V V
V_{OH}	Output High Voltage (Outputs Configured as Complementary)	I_{OH} = −200 µA(3,5) I_{OH} = −3.2 mA I_{OH} = −7.0 mA	V_{CC} − 0.3 V_{CC} − 0.7 V_{CC} − 1.5			V V V
I_{LI}	Input Leakage Current (Std. Inputs)	$V_{SS} < V_{IN} < V_{CC}$			±10	µA

DC CHARACTERISTICS (Under Listed Operating Conditions) (Continued)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
I_{LI1}	Input Leakage Current (Port 0)	$V_{SS} < V_{IN} < V_{REF}$			±1.5	μA
V_{OH1}	SLPINT (P5.4) and HLDA (P2.6) Output High Voltage in RESET	I_{OH} = 0.8 mA(7)	2.0			V
V_{OH2}	Output High Voltage in RESET	I_{OH} = −15 μA(1,8)	V_{CC} − 1V			V
I_{OH2}	Output High Current in RESET	$V_{OH2} = V_{CC} - 1.0V$ $V_{OH2} = V_{CC} - 2.5V$ $V_{OH2} = V_{CC} - 4.0V$	−30 −75 −90		−120 −240 −280	μA μA μA
C_S	Pin Capacitance (Any pin to V_{SS})	f_{test} = 1.0 MHz(6)			10	pF
V_{OL3}	Output Low Voltage in RESET (RESET Pin Only)	I_{OL3} = 4 mA(10) I_{OL3} = 6 mA I_{OL3} = 8 mA			0.3 0.5 0.8	V
R_{WPU}	Weak Pullup Resistance	(Note 6)		150K		Ω
R_{RST}	Reset Pullup Resistor		65K		180K	Ω

NOTES:
1. All BD (bidirectional) pins except INST and CLKOUT. INST and CLKOUT are excluded due to their not being weakly pulled high in reset. BD pins include Port1, Port2, Port3, Port4, Port5 and Port6 except SPLINT (P5.4) and HLDA (P2.6).
2. Standard input pins include XTAL1, $\overline{EA}$, RESET, and Port 1/2/5/6 when setup as inputs.
3. All bidirectional I/O pins when configured as Outputs (Push/Pull).
4. Device is static and should operate below 1 Hz, but only tested down to 4 MHz.
5. Maximum I_{OL}/I_{OH} currents per pin will be characterized and published at a later date.
6. Typicals are based on limited number of samples and are not guaranteed. The values listed are at room temperature and $V_{REF} = V_{CC} = 5.0V$.
7. Violating these specifications in reset may cause the device to enter test modes (P5.4 and P2.6).
8. When P0 is used as analog inputs, refer to A/D specifications for this characteristic.
9. For temperatures <100°C typical is 10 μA.
10. This specification is not tested in production and is based upon theoretical estimates and/or product characterization.

I_{CC} vs Frequency



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NOTES:
I_{CC}Max = 3.25 × Freq. + 30.
I_{IDLE}Max = 1.25 × Freq. + 20.

AC CHARACTERISTICS (Over Specified Operating Conditions)

Test Conditions: Capacitance Load on All Pins = 100 pF, Rise and Fall Times = 10 ns.

The 87C196KT will meet these specifications

Symbol	Parameter	Min	Max	Units
F_{XTAL}	Frequency on XTAL1	4.0	20	MHz(1)
T_{OSC}	XTAL1 Period ($1/F_{XTAL}$)	50.0	250	ns
T_{XHCH}	XTAL1 High to CLKOUT High or Low	+20	110	ns
T_{OFD}	Clock Failure to Reset Pulled Low(6)	4	40	μs
T_{CLCL}	CLKOUT Period	2 T_{OSC}		ns
T_{CHCL}	CLKOUT High Period	T_{OSC} − 10	T_{OSC} + 30	ns
T_{CLLH}	CLKOUT Low to ALE/$\overline{ADV}$ High	−10	+15	ns
T_{LLCH}	ALE/$\overline{ADV}$ Low to CLKOUT High	−25	+15	ns
T_{LHLH}	ALE/$\overline{ADV}$ Cycle Time	4 T_{OSC}		ns(5)
T_{LHLL}	ALE/$\overline{ADV}$ High Time	T_{OSC} − 10	T_{OSC} + 10	ns
T_{AVLL}	Address Valid to ALE Low	T_{OSC} − 15		ns
T_{LLAX}	Address Hold After ALE/$\overline{ADV}$ Low	T_{OSC} − 40		ns
T_{LLRL}	ALE/$\overline{ADV}$ Low to $\overline{RD}$ Low	T_{OSC} − 40		ns
T_{RLCL}	$\overline{RD}$ Low to CLKOUT Low	−5	+35	ns
T_{RLRH}	$\overline{RD}$ Low Period	T_{OSC} − 5		ns(5)
T_{RHLH}	$\overline{RD}$ High to ALE/$\overline{ADV}$ High	T_{OSC}	T_{OSC} + 25	ns(3)
T_{RLAZ}	$\overline{RD}$ Low to Address Float		+5	ns
T_{LLWL}	ALE/$\overline{ADV}$ Low to $\overline{WR}$ Low	T_{OSC} − 10		ns
T_{CLWL}	CLKOUT Low to $\overline{WR}$ Low	−10	+25	ns
T_{QVWH}	Data Valid before $\overline{WR}$ High	T_{OSC} − 23		ns
T_{CHWH}	CLKOUT High to $\overline{WR}$ High	−10	+15	ns
T_{WLWH}	$\overline{WR}$ Low Period	T_{OSC} − 30		ns(5)
T_{WHQX}	Data Hold after $\overline{WR}$ High	T_{OSC} − 30		ns
T_{WHLH}	$\overline{WR}$ High to ALE/$\overline{ADV}$ High	T_{OSC} − 10	T_{OSC} + 15	ns(3)
T_{WHBX}	$\overline{BHE}$, INST Hold after $\overline{WR}$ High	T_{OSC} − 10		ns
T_{WHAX}	AD8–15 Hold after $\overline{WR}$ High	T_{OSC} − 30		ns(4)
T_{RHBX}	$\overline{BHE}$, INST Hold after $\overline{RD}$ High	T_{OSC} − 10		ns
T_{RHAX}	AD8–15 Hold after $\overline{RD}$ High	T_{OSC} − 30		ns(4)

NOTES:

1. Testing performed at 4.0 MHz, however, the device is static by design and will typically operate below 1 Hz.
2. Typical specifications, not guaranteed.
3. Assuming back-to-back bus cycles.
4. 8-bit bus only.
5. If wait states are used, add 2 Tosc × n, where n = number of wait states. If mode 0 (1 automatic wait state added) operation is selected, add 2 T_{OSC} to specification.
6. T_{OFD} is the time for the oscillator fail detect circuit (OFD) to react to a clock failure. The OFD circuitry is enabled by programming the UPROM location 0778H with the value 0004H. KT/KS customer QROM codes need to equate location 2016H to the value 0CDEH if the oscillator fail detect (OFD) function is desired. Intel manufacturing uses location 2016H as a flag to determine whether or not to program the Clock Detect Enable (CDE) bit. Programming the CDE bit enables oscillator fail detection.

AC CHARACTERISTICS (Over Specified Operating Conditions)

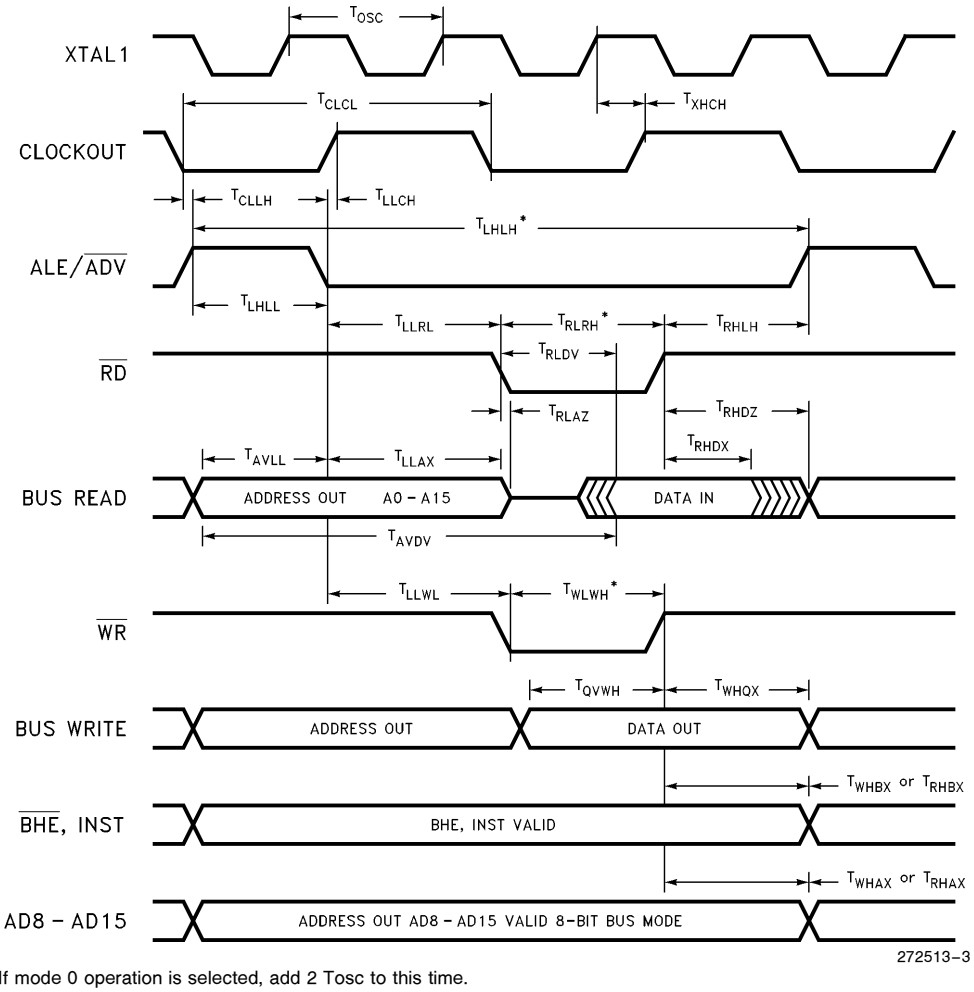
Test Conditions: Capacitance Load on All Pins = 100 pF, Rise anf Fall Times = 10 ns.

The system must meet these specifications to work with the 87C196KT.

Symbol	Parameter	Min	Max	Units
T_{AVYV}	Address Valid to Ready Setup		$2\,T_{OSC} - 75$	ns(3)
T_{LLYV}	ALE Low to READY Setup		$T_{OSC} - 70$	ns(3)
T_{YLYH}	Non READY Time	No Upper Limit		ns
T_{CLYX}	READY Hold after CLKOUT Low	0	$T_{OSC} - 30$	ns(1)
T_{AVGV}	Address Valid to BUSWIDTH Setup		$2\,T_{OSC} - 75$	ns(2, 3)
T_{LLGV}	ALE Low to BUSWIDTH Setup		$T_{OSC} - 60$	ns(2, 3)
T_{CLGX}	BUSWIDTH Hold after CLKOUT Low	0		ns
T_{AVDV}	Address Valid to Input Data Valid		$3\,T_{OSC} - 60$	ns(2)
T_{RLDV}	$\overline{RD}$ active to input Data Valid		$T_{OSC} - 30$	ns(2)
T_{CLDV}	CLKOUT Low to Input Data Valid		$T_{OSC} - 60$	ns
T_{RHDZ}	End of $\overline{RD}$ to Input Data Float		T_{OSC}	ns
T_{RHDX}	Data Hold after $\overline{RD}$ High	0		ns

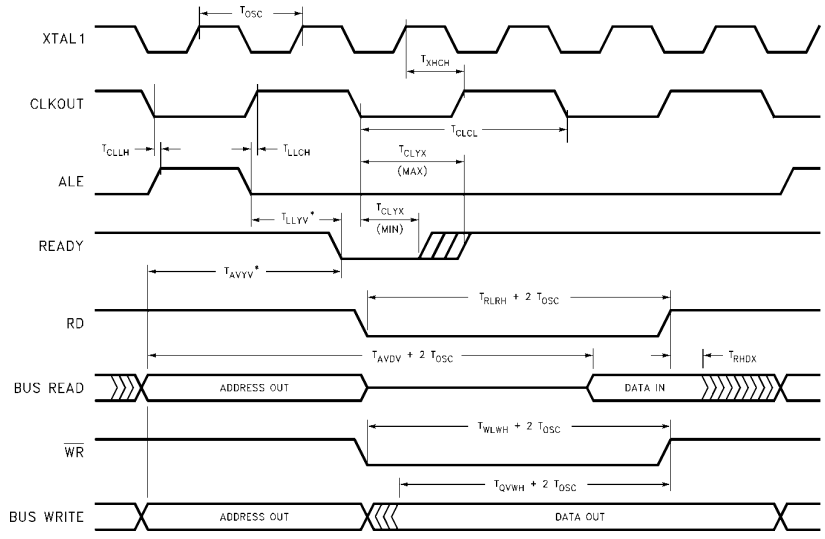
NOTES:
1. If Max is exceeded, additional wait states will occur.
2. If wait states are used, add 2 Tosc × n, where n = number of wait states.
3. If mode 0 is selected, one wait state minimum is always added. If additional wait states are required, add 2 Tosc to the specification.

87C196KT SYSTEM BUS TIMING



* If mode 0 operation is selected, add 2 Tosc to this time.

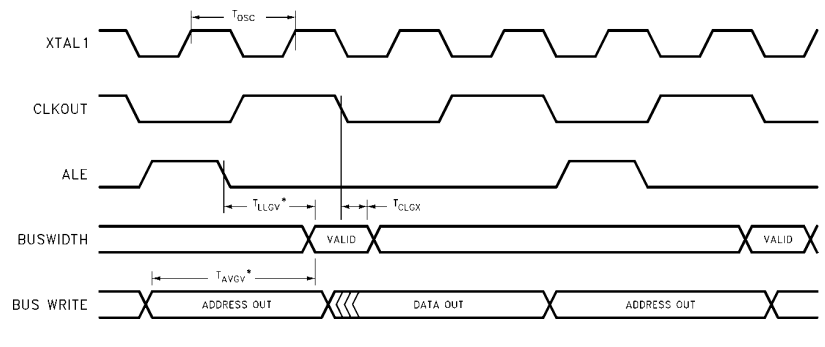
87C196KT READY TIMINGS (ONE WAIT STATE)



272513–4

*If mode 0 selected, one wait state is always added. If additional wait states are required, add 2 Tosc to these specifications.

87C196KT BUSWIDTH TIMINGS



272513–5

*If mode 0 selected, add 2 Tosc to these specifications.

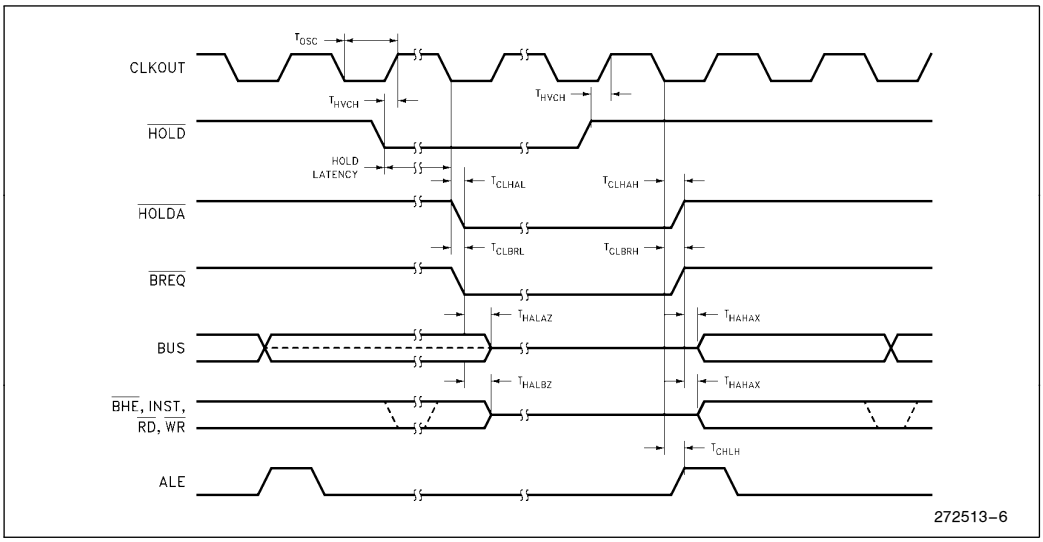
HOLD/HOLDA TIMINGS (Over Specified Operation Conditions)

Test Conditions: Capacitance Load on All Pins = 100 pF, Rise and Fall Times = 10 ns.

Symbol	Parameter	Min	Max	Units
T_{HVCH}	HOLD Setup Time	+65		ns(1)
T_{CLHAL}	CLKOUT Low to HLDA Low	−15	+15	ns
T_{CLBRL}	CLKOUT Low to BREQ Low	−15	+15	ns
T_{AZHAL}	HLDA Low to Address Float		+20	ns
T_{BZHAL}	HLDA Low to $\overline{BHE}$, INST, $\overline{RD}$, $\overline{WR}$ Weakly Driven		+25	ns
T_{CLHAH}	CLKOUT Low to HLDA High	−25	+15	ns
T_{CLBRH}	CLKOUT Low to BREQ High	−25	+25	ns
T_{HAHAX}	HLDA High to Address No Longer Float	−15		ns
T_{HAHBV}	HLDA High to $\overline{BHE}$, INST, $\overline{RD}$, $\overline{WR}$ Valid	−10	+15	ns

NOTE:
1. To guarantee recognition at next clock.

8XC196KT $\overline{HOLD}$/$\overline{HOLDA}$ TIMINGS



BUS MODE 1—AC CHARACTERISTICS (Over Specified Operating Conditions)

Test Conditions: Capacitance Load on All Pins = 100 pF, Rise and Fall Times = 10 ns.

The 87C196KT will meet these specifications

Symbol	Parameter	Min	Max	Units
F_{XTAL}	Frequency on XTAL1	8.0	20.0	MHz(1)
T_{OSC}	XTAL1 Period ($1/F_{XTAL}$)	50.0	125	ns
T_{XHCH}	XTAL1 High to CLKOUT High or Low	+20	110	ns
T_{CLCL}	CLKOUT Period	2 T_{OSC}		ns
T_{CHCL}	CLKOUT High Period	T_{OSC} − 10	T_{OSC} + 27	ns
T_{CHLH}	CLKOUT HIGH to ALE/$\overline{ADV}$ High	0.5 T_{OSC} − 15	0.5 T_{OSC} + 20	ns
T_{CLLL}	CLKOUT LOW to ALE/$\overline{ADV}$ Low	0.5 T_{OSC} − 25	0.5 T_{OSC} + 15	ns
T_{LHLH}	ALE/$\overline{ADV}$ Cycle Time	4 T_{OSC}		ns(5)
T_{LHLL}	ALE/$\overline{ADV}$ High Time	T_{OSC} − 10	T_{OSC} + 10	ns
T_{AVLL}	Address Valid to ALE Low	0.5 T_{OSC} − 15		ns
T_{LLAX}	Address Hold After ALE/$\overline{ADV}$ Low	0.5 T_{OSC} − 20		ns
T_{LLRL}	ALE/$\overline{ADV}$ Low to $\overline{RD}$ Low	0.5 T_{OSC} − 30		ns
T_{RLCL}	$\overline{RD}$ Low to CLKOUT Low	T_{OSC} − 10	T_{OSC} + 30	ns
T_{RLRH}	$\overline{RD}$ Low Period	2 T_{OSC} − 20		ns(5)
T_{RHLH}	$\overline{RD}$ High to ALE/$\overline{ADV}$ High	0.5 T_{OSC}	0.5 T_{OSC} + 25	ns(3)
T_{RLAZ}	$\overline{RD}$ Low to Address Float		+5	ns
T_{LLWL}	ALE/$\overline{ADV}$ Low to $\overline{WR}$ Low	0.5 T_{OSC} − 10		ns
T_{CLWL}	CLKOUT Low to $\overline{WR}$ Low	T_{OSC} − 15	T_{OSC} +25	ns
T_{QVWH}	Data Valid before $\overline{WR}$ High	2 T_{OSC} − 23		ns
T_{CHWH}	CLKOUT High to $\overline{WR}$ High	−10	+15	ns
T_{WLWH}	$\overline{WR}$ Low Period	2 T_{OSC} − 15		ns(5)
T_{WHQX}	Data Hold after $\overline{WR}$ High	0.5 T_{OSC} − 25		ns
T_{WHLH}	$\overline{WR}$ High to ALE/$\overline{ADV}$ High	0.5 T_{OSC} − 10	0.5 T_{OSC} + 15	ns(3)
T_{WHBX}	$\overline{BHE}$ Hold after $\overline{WR}$ High	T_{OSC} − 15		ns
T_{WHIX}	INST Hold after $\overline{WR}$ High	0.5 T_{OSC} − 15		
T_{WHAX}	AD8–15 Hold after $\overline{WR}$ High	0.5 T_{OSC} − 30		ns(4)
T_{RHBX}	$\overline{BHE}$ Hold after $\overline{RD}$ High	T_{OSC} − 32		ns
T_{RHAX}	AD8–15 Hold after $\overline{RD}$ High	0.5 T_{OSC} − 32		
T_{RHAX}	AD8–15 Hold after $\overline{RD}$ High	0.5 T_{OSC} − 30		ns(4)

NOTES:
1. Testing performed at 8.0 MHz, however, the device is static by design and will typically operate below 1 Hz.
2. Typical specifications, not guaranteed.
3. Assuming back-to-back bus cycles.
4. 8-bit bus only.
5. If wait states are used, add 2 T_{OSC} × n, where n = number of wait states.

BUS MODE 1—AC CHARACTERISTICS (Over Specified Operating Conditions) (Continued)

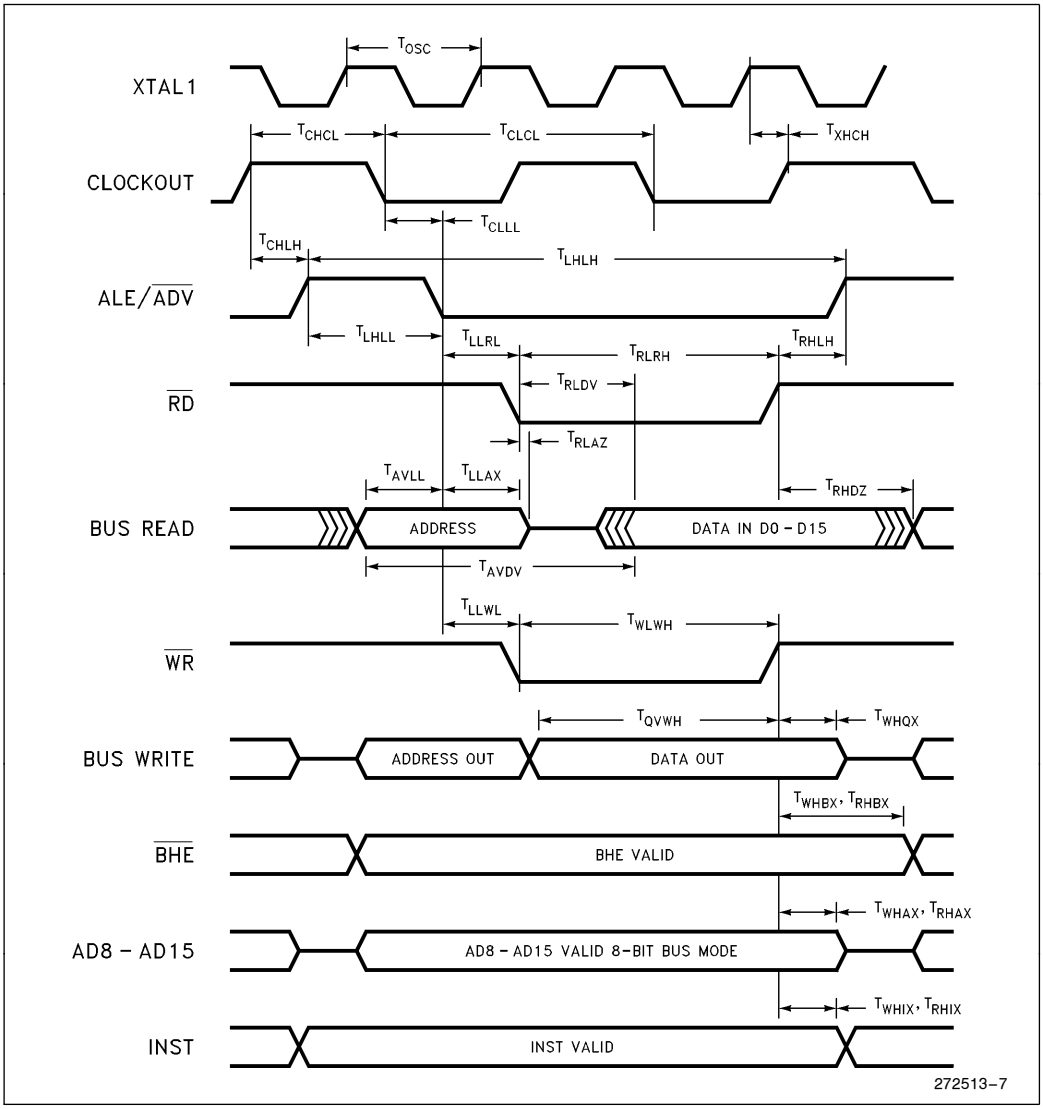
Test Conditions: Capacitance Load on All Pins = 100 pF, Rise and Fall Times = 10 ns.

The system must meet these specifications to work with the 87C196KT.

Symbol	Parameter	Min	Max	Units
T_{AVYV}	Address Valid to Ready Setup		2 T_{OSC} − 75	ns
T_{LLYV}	ALE Low to READY Setup		1.5 T_{OSC} − 70	ns
T_{YLYH}	Non READY Time	No Upper Limit		ns
T_{CLYX}	READY Hold after CLKOUT Low	0	T_{OSC} − 30	ns(1)
T_{AVGV}	Address Valid to BUSWIDTH Setup		2 T_{OSC} − 75	ns
T_{LLGV}	ALE Low to BUSWIDTH Setup		1.5 T_{OSC} − 60	ns
T_{CLGX}	BUSWIDTH Hold after CLKOUT Low	0		ns
T_{AVDV}	Address Valid to Input Data Valid		3 T_{OSC} − 65	ns(2)
T_{RLDV}	$\overline{RD}$ active to input Data Valid		2 T_{OSC} − 44	ns(2)
T_{CLDV}	CLKOUT Low to Input Data Valid		T_{OSC} − 60	ns
T_{RHDZ}	End of $\overline{RD}$ to Input Data Float		T_{OSC}	ns
T_{RHDX}	Data Hold after $\overline{RD}$ High	0		ns

NOTES:
1. If Max is exceeded, additional wait states will occur.
2. If wait states are used, add 2 T_{OSC} × n, where n = number of wait states. If mode 0 (1 automatic wait state added) operation is selected, add 2 T_{OSC} to specification.

MODE 1—87C196KT SYSTEM BUS TIMING



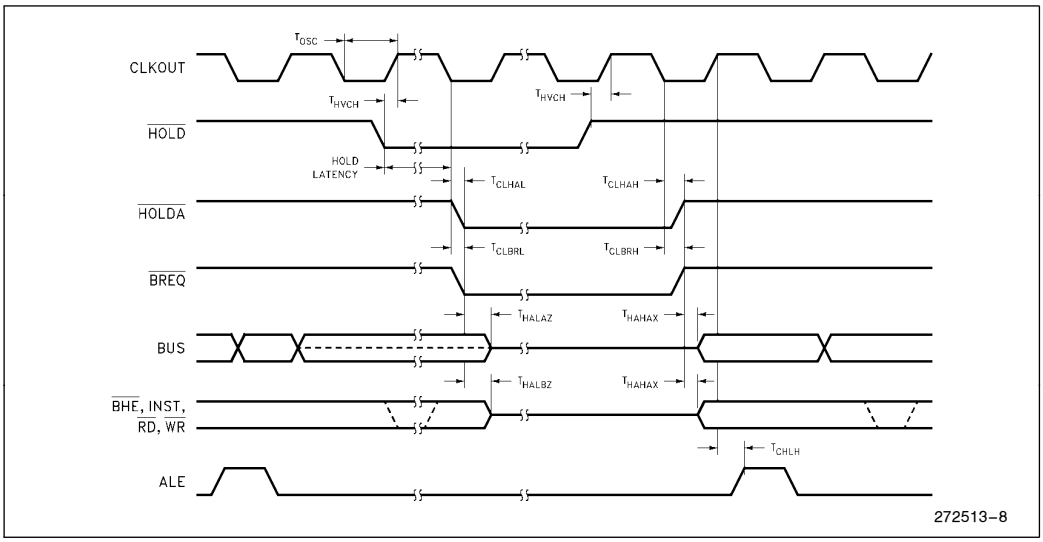
BUS MODE 1—HOLD/HOLDA TIMINGS (Over Specified Operation Conditions)

Test Conditions: Capacitance Load on All Pins = 100 pF, Rise and Fall Times = 10 ns.

Symbol	Parameter	Min	Max	Units
T_{HVCH}	HOLD Setup Time	+65		ns(1)
T_{CLHAL}	CLKOUT Low to HLDA Low	−15	+15	ns
T_{CLBRL}	CLKOUT Low to BREQ Low	−15	+15	ns
T_{AZHAL}	HLDA Low to Address Float		+25	ns
T_{BZHAL}	HLDA Low to $\overline{BHE}$, INST, $\overline{RD}$, $\overline{WR}$ Weakly Driven		+25	ns
T_{CLHAH}	CLKOUT Low to HLDA High	−25	+15	ns
T_{CLBRH}	CLKOUT Low to BREQ High	−25	+15	ns
T_{HAHAX}	HLDA High to Address No Longer Float	−15		ns
T_{HAHBV}	HLDA High to $\overline{BHE}$, INST, $\overline{RD}$, $\overline{WR}$ Valid	−10		ns

NOTE:
1. To guarantee recognition at next clock.

MODE 1—8XC196KT $\overline{HOLD}$/$\overline{HOLDA}$ TIMINGS



BUS MODE 2—AC CHARACTERISTICS (Over Specified Operating Conditions)

Test Conditions: Capacitance Load on All Pins = 100 pF, Rise and Fall Times = 10 ns.

The 87C196KT will meet these specifications

Symbol	Parameter	Min	Max	Units
F_{XTAL}	Frequency on XTAL1	8.0	20.0	MHz(1)
T_{OSC}	XTAL1 Period ($1/F_{XTAL}$)	50.0	125	ns
T_{XHCH}	XTAL1 High to CLKOUT High or Low	+20	+85	ns
T_{CLCL}	CLKOUT Period	2 T_{OSC}		ns
T_{CHCL}	CLKOUT High Period	T_{OSC} − 10	T_{OSC} + 27	ns
T_{CHLH}	CLKOUT HIGH to ALE/$\overline{ADV}$ High	0.5 T_{OSC} − 15	0.5 T_{OSC} + 20	ns
T_{CLLL}	CLKOUT LOW to ALE/$\overline{ADV}$ Low	0.5 T_{OSC} − 25	0.5 T_{OSC} + 15	ns
T_{LHLH}	ALE/$\overline{ADV}$ Cycle Time	4 T_{OSC}		ns(5)
T_{LHLL}	ALE/$\overline{ADV}$ High Time	T_{OSC} − 10	T_{OSC} + 10	ns
T_{AVLL}	Address Valid to ALE Low	T_{OSC} − 15		ns
T_{LLAX}	Address Hold After ALE/$\overline{ADV}$ Low	0.5 T_{OSC} − 20		ns
T_{LLRL}	ALE/$\overline{ADV}$ Low to $\overline{RD}$ Low	0.5 T_{OSC} − 30		ns
T_{RLCL}	$\overline{RD}$ Low to CLKOUT Low	T_{OSC} − 10	T_{OSC} + 30	ns
T_{RLRH}	$\overline{RD}$ Low Period	2 T_{OSC} − 20		ns(5)
T_{RHLH}	$\overline{RD}$ High to ALE/$\overline{ADV}$ High	0.5 T_{OSC} − 5	0.5 T_{OSC} + 25	ns(3)
T_{RLAZ}	$\overline{RD}$ Low to Address Float		+5	ns
T_{LLWL}	ALE/$\overline{ADV}$ Low to $\overline{WR}$ Low	0.5 T_{OSC} − 10		ns
T_{CLWL}	CLKOUT Low to $\overline{WR}$ Low	T_{OSC} − 22	T_{OSC} + 25	ns
T_{QVWH}	Data Valid before $\overline{WR}$ High	2 T_{OSC} − 25		ns
T_{CHWH}	CLKOUT High to $\overline{WR}$ High	−10	+15	ns
T_{WLWH}	$\overline{WR}$ Low Period	2 T_{OSC} − 20		ns(5)
T_{WHQX}	Data Hold after $\overline{WR}$ High	0.5 T_{OSC} − 25		ns
T_{WHLH}	WR High to ALE/$\overline{ADV}$ High	0.5 T_{OSC} − 10	0.5 T_{OSC} + 10	ns(3)
T_{WHBX}	$\overline{BHE}$ Hold after $\overline{WR}$ High	T_{OSC} − 15		ns
T_{WHIX}	INST Hold after $\overline{WR}$ High	0.5 T_{OSC} − 15		
T_{WHAX}	AD8–15 Hold after $\overline{WR}$ High	0.5 T_{OSC} − 30		ns(4)
T_{RHBX}	$\overline{BHE}$ Hold after $\overline{RD}$ High	T_{OSC} − 32		ns
T_{RHIX}	INST Hold after $\overline{RD}$ High	0.5 T_{OSC} − 32		
T_{RHAX}	AD8–15 Hold after $\overline{RD}$ High	0.5 T_{OSC} − 30		ns(4)

NOTES:
1. Testing performed at 8.0 MHz, however, the device is static by design and will typically operate below 1 Hz.
2. Typical specifications, not guaranteed.
3. Assuming back-to-back bus cycles.
4. 8-bit bus only.
5. If wait states are used, add 2 T_{OSC} × n, where n = number of wait states.

BUS MODE 2—AC CHARACTERISTICS (Over Specified Operating Conditions)

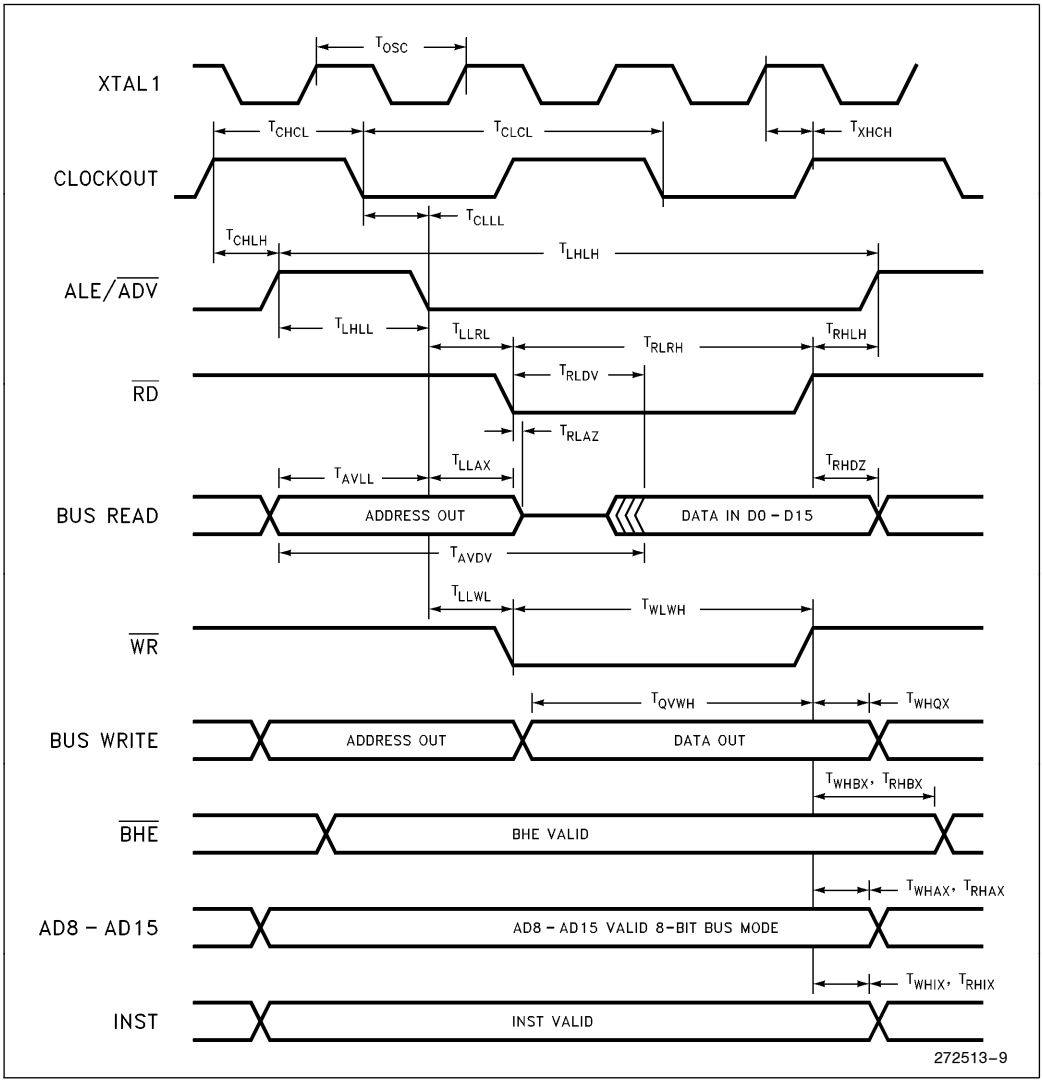
Test Conditions: Capacitance Load on All Pins = 100 pF, Rise and Fall Times = 10 ns.

The system must meet these specifications to work with the 87C196KT.

Symbol	Parameter	Min	Max	Units
T_{AVYV}	Address Valid to Ready Setup		2.5 T_{OSC} − 75	ns
T_{LLYV}	ALE Low to READY Setup		1.5 T_{OSC} − 70	ns
T_{YLYH}	Non READY Time	No Upper Limit		ns
T_{CLYX}	READY Hold after CLKOUT Low	0	T_{OSC} − 30	ns(1)
T_{AVGV}	Address Valid to BUSWIDTH Setup		2.5 T_{OSC} − 75	ns
T_{LLGV}	ALE Low to BUSWIDTH Setup		1.5 T_{OSC} − 60	ns
T_{CLGX}	BUSWIDTH Hold after CLKOUT Low	0		ns
T_{AVDV}	Address Valid to Input Data Valid		3.5 T_{OSC} − 60	ns(2)
T_{RLDV}	$\overline{RD}$ active to Input Data Valid		2 T_{OSC} − 44	ns(2)
T_{CLDV}	CLKOUT Low to Input Data Valid		T_{OSC} − 60	ns
T_{RHDZ}	End of $\overline{RD}$ to Input Data Float		0.5 T_{OSC}	ns
T_{RHDX}	Data Hold after $\overline{RD}$ High	0		ns

NOTES:
1. If Max is exceeded, additional wait states will occur.
2. If wait states are used, add 2 T_{OSC} × n, where n = number of wait states. If mode 0 (1 automatic wait state added) operation is selected, add 2 T_{OSC} to specification.

MODE 2—87C196KT SYSTEM BUS TIMING



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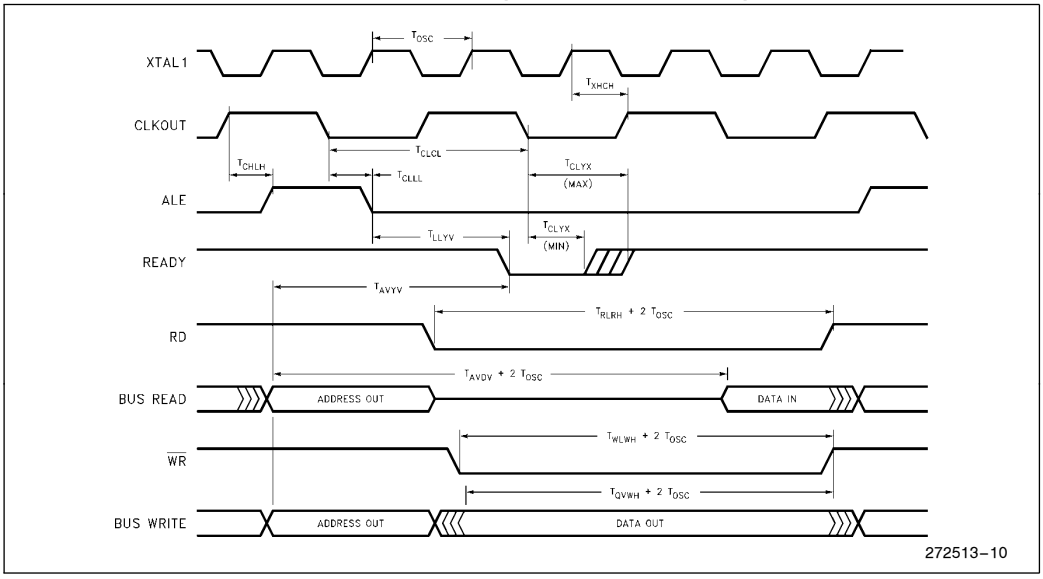
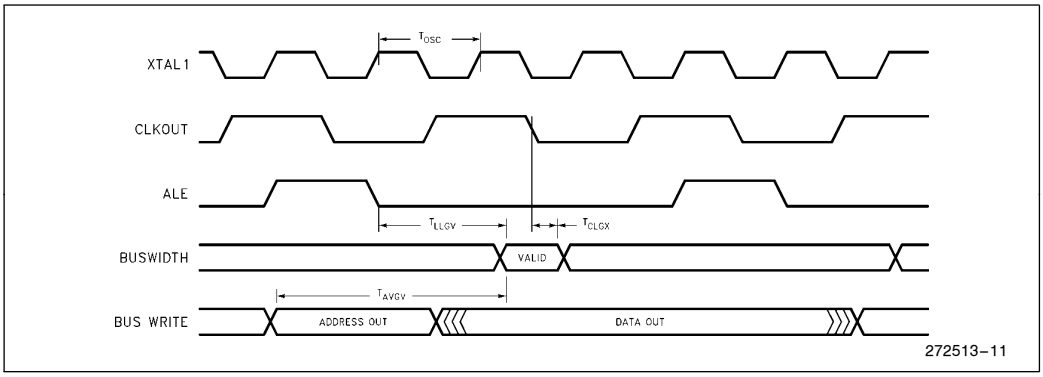
MODE 2—87C196KT READY TIMINGS (ONE WAIT STATE)



MODE 2—87C196KT BUSWIDTH TIMINGS



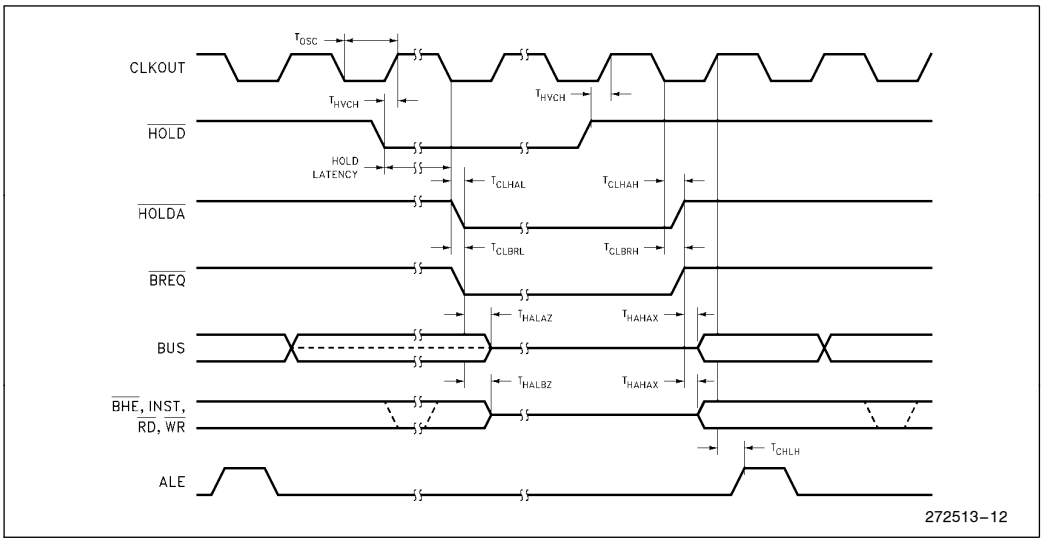
BUS MODE 2—HOLD/HOLDA TIMINGS (Over Specified Operation Conditions)

Test Conditions: Capacitance Load on All Pins = 100 pF, Rise and Fall Times = 10 ns.

Symbol	Parameter	Min	Max	Units
T_{HVCH}	HOLD Setup Time	+65		ns(1)
T_{CLHAL}	CLKOUT Low to HLDA Low	−15	+15	ns
T_{CLBRL}	CLKOUT Low to BREQ Low	−15	+15	ns
T_{AZHAL}	HLDA Low to Address Float		+25	ns
T_{BZHAL}	HLDA Low to $\overline{BHE}$, INST, $\overline{RD}$, $\overline{WR}$ Weakly Driven		+25	ns
T_{CLHAH}	CLKOUT Low to HLDA High	−25	+15	ns
T_{CLBRH}	CLKOUT Low to BREQ High	−25	+15	ns
T_{HAHAX}	HLDA High to Address No Longer Float	−15		ns
T_{HAHBV}	HLDA High to $\overline{BHE}$, INST, $\overline{RD}$, $\overline{WR}$ Valid	−10		ns

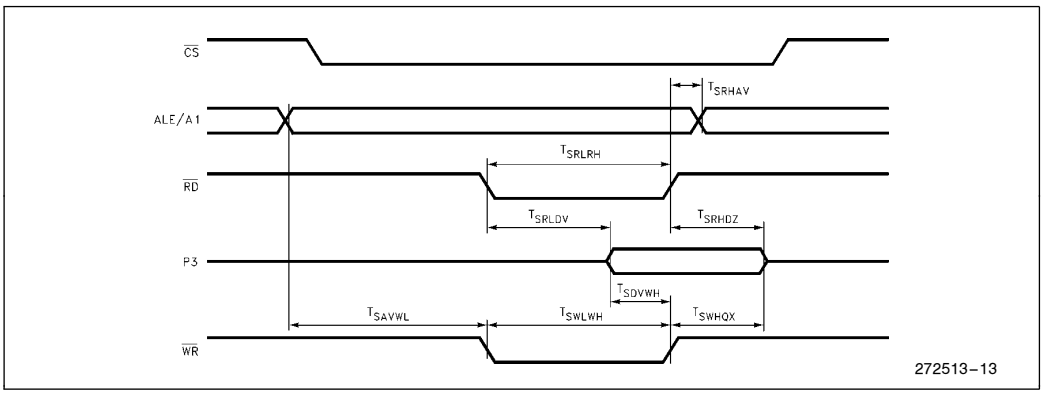
NOTE:
1. To guarantee recognition at next clock.

MODE 2—8XC196KT $\overline{HOLD}$/$\overline{HOLDA}$ TIMINGS



AC CHARACTERISTICS—SLAVE PORT

SLAVE PORT WAVEFORM—(SLPL = 0)



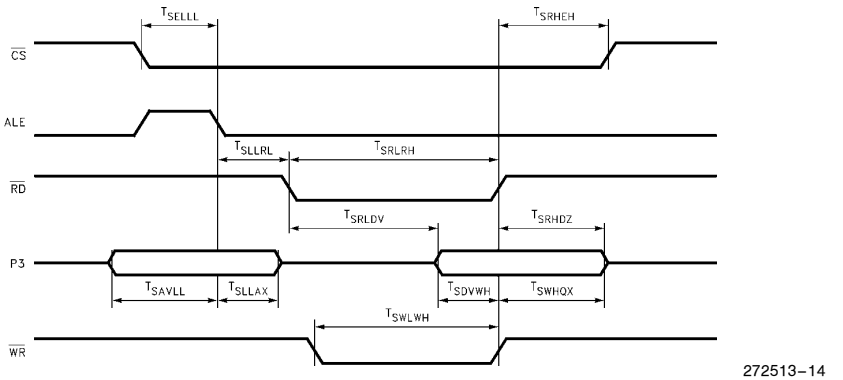
SLAVE PORT TIMING—(SLPL = 0, 1, 2, 3)

Symbol	Parameter	Min	Max	Units
T_{SAVWL}	Address Valid to $\overline{WR}$ Low	50		ns
T_{SRHAV}	$\overline{RD}$ High to Address Valid	60		ns
T_{SRLRH}	$\overline{RD}$ Low Period	T_{OSC}		ns
T_{SWLWH}	$\overline{WR}$ Low Period	T_{OSC}		ns
T_{SRLDV}	$\overline{RD}$ Low to Output Data Valid		60	ns
T_{SDVWH}	Input Data Setup to $\overline{WR}$ High	20		ns
T_{SWHQX}	$\overline{WR}$ High to Data Invalid	30		ns
T_{SRHDZ}	$\overline{RD}$ High to Data Float	15		ns

NOTES:
1. Test Conditions: F_{OSC} = 20 MHz, T_{OSC} = 60 ns. Rise/Fall Time = 10 ns. Capacitive Pin Load = 100 pF.
2. These values are not tested in production, and are based upon theoretical estimates and/or laboratory tests.
3. Specifications above are advanced information and are subject to change.

AC CHARACTERISTICS—SLAVE PORT (Continued)

SLAVE PORT WAVEFORM—(SLPL = 1)



SLAVE PORT TIMING—(SLPL = 1, 2, 3)

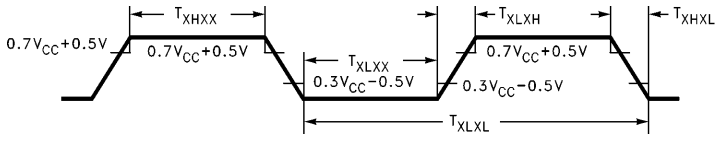
Symbol	Parameter	Min	Max	Units
T_{SELLL}	$\overline{CS}$ Low to ALE Low	20		ns
T_{SRHEH}	$\overline{RD}$ or $\overline{WR}$ High to $\overline{CS}$ High	60		ns
T_{SLLRL}	ALE Low to $\overline{RD}$ Low	T_{OSC}		ns
T_{SRLRH}	$\overline{RD}$ Low Period	T_{OSC}		ns
T_{SWLWH}	$\overline{WR}$ Low Period	T_{OSC}		ns
T_{SAVLL}	Address Valid to ALE Low	20		ns
T_{SLLAX}	ALE Low to Address Invalid	20		ns
T_{SRLDV}	$\overline{RD}$ Low to Output Data Valid		60	ns
T_{SDVWH}	Input Data Setup to $\overline{WR}$High	20		ns
T_{SWHQX}	$\overline{WR}$ High to Data Invalid	30		ns
T_{SRHDZ}	$\overline{RD}$ High to Data Float	15		ns

NOTES:
1. Test Conditions: F_{OSC} = 20 MHz, T_{OSC} = 60 ns. Rise/Fall Time = 10 ns. Capacitive Pin Load = 100 pF.
2. These values are not tested in production, and are based upon theoretical estimates and/or laboratory tests.
3. Specifications above are advanced information and are subject to change.

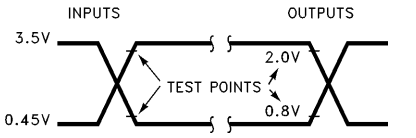
EXTERNAL CLOCK DRIVE

Symbol	Parameter	Min	Max	Units
$1/T_{XLXL}$	Oscillator Frequency	4	20	MHz
T_{XLXL}	Oscillator Period (T_{OSC})	50.0	250	ns
T_{XHXX}	High Time	0.35 × T_{OSC}	0.65 T_{OSC}	ns
T_{XLXX}	Low Time	0.35 × T_{OSC}	0.65 T_{OSC}	ns
T_{XLXH}	Rise Time		10	ns
T_{XHXL}	Fall Time		10	ns

EXTERNAL CLOCK DRIVE WAVEFORMS

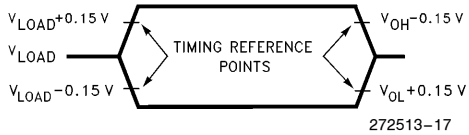


AC TESTING INPUT, OUTPUT WAVEFORMS



AC Testing inputs are driven at 3.5V for a logic "1" and 0.45V for a logic "0". Timing measurements are made at 2.0V for a logic "1" and 0.8V for logic "0".

FLOAT WAVEFORMS



For timing purposes a Port Pin is no longer floating when a 150 mV change from load voltage occurs and begins to float when a 150 mV change from the loading V_{OH}/V_{OL} level occurs $I_{OL}/I_{OH} \leq 15$ mA.

THERMAL CHARACTERISTICS

Device and Package	θ_{JA}	θ_{JC}
AN87C196KT/KS (68-Lead PLCC)	36.5°C/W	13°C/W

NOTES:
1. θ_{JA} = Thermal resistance between junction and the surrounding environmental (ambient). Measurements are taken 1 ft. away from case in air flow environment. θ_{JC} = Thermal resistance between junction and package surface (case).
2. All values of θ_{JA} and θ_{JC} may fluctuate depending on the environment (with or without airflow, and how much airflow) and device power dissipation at temperature of operation. Typical variations are ±2°C/W.
3. Values listed are at a maximum power dissipation of 0.50W.

EXPLANATION OF AC SYMBOLS

Each symbol is two pairs of letters prefixed by "T" for time. The characters in a pair indicate a signal and its condition, respectively. Symbols represent the time between the two signal/condition points.

Conditions:
H—High
L—Low
V—Valid
X—No Longer Valid
Z—Floating

Signals:
A—Address
B—$\overline{BHE}$
BR—$\overline{BREQ}$
C—CLKOUT
D—DATA
G—Buswidth
H—$\overline{HOLD}$
HA—$\overline{HLDA}$
L—ALE/$\overline{ADV}$
Q—Data Out
RD—$\overline{RD}$
W—$\overline{WR}$/$\overline{WRH}$/$\overline{WRI}$
X—XTAL1
Y—READY

EPROM SPECIFICATIONS

AC EPROM PROGRAMMING CHARACTERISTICS

Operating Conditions: Load Capacitance = 150 pF; T_C = 25°C ±5°C, V_{CC}, V_{REF} = 5.0V ±0.5V, V_{SS}, ANGND = 0V.
V_{PP} = 12.5V ±0.25V; $\overline{EA}$ = 12.5V ± 0.25V; Fosc = 5.0 MHz.

Symbol	Parameter	Min	Max	Units
T_{AVLL}	Address Setup Time	0		T_{OSC}
T_{LLAX}	Address Hold Time	100		T_{OSC}
T_{DVPL}	Data Setup Time	0		T_{OSC}
T_{PLDX}	Data Hold Time	400		T_{OSC}
T_{LLLH}	$\overline{PALE}$ Pulse Width	50		T_{OSC}
T_{PLPH}	$\overline{PROG}$ Pulse Width(2)	50		T_{OSC}
T_{LHPL}	$\overline{PALE}$ High to $\overline{PROG}$ Low	220		T_{OSC}
T_{PHLL}	$\overline{PROG}$ High to next $\overline{PALE}$ Low	220		T_{OSC}
T_{PHDX}	Word Dump Hold Time		50	T_{OSC}
T_{PHPL}	$\overline{PROG}$ High to next $\overline{PROG}$ Low	220		T_{OSC}
T_{LHPL}	$\overline{PALE}$ High to $\overline{PROG}$ Low	220		T_{OSC}
T_{PLDV}	$\overline{PROG}$ Low to Word Dump Valid		50	T_{OSC}
T_{SHLL}	$\overline{RESET}$ High to First $\overline{PALE}$ Low	1100		T_{OSC}
T_{PHIL}	$\overline{PROG}$ High to $\overline{AINC}$ Low	0		T_{OSC}
T_{ILIH}	$\overline{AINC}$ Pulse Width	240		T_{OSC}
T_{ILVH}	PVER Hold after $\overline{AINC}$ Low	50		T_{OSC}
T_{ILPL}	$\overline{AINC}$ Low to $\overline{PROG}$ Low	170		T_{OSC}
T_{PHVL}	$\overline{PROG}$ High to $\overline{PVER}$ Valid		220	T_{OSC}

NOTES:
1. Run-time programming is done with Fosc = 6.0 MHz to 10.0 MHz, V_{CC}, V_{PD}, V_{REF} = 5V ±0.5V, T_C = 25°C ±5°C and V_{PP} = 12.5V ±0.25V. For run-time programming over a full operating range, contact factory.
2. Programming specifications are not tested, but guaranteed by design.
3. This specification is for the word dump mode. For programming pulses use 300 Tosc + 100 μs.

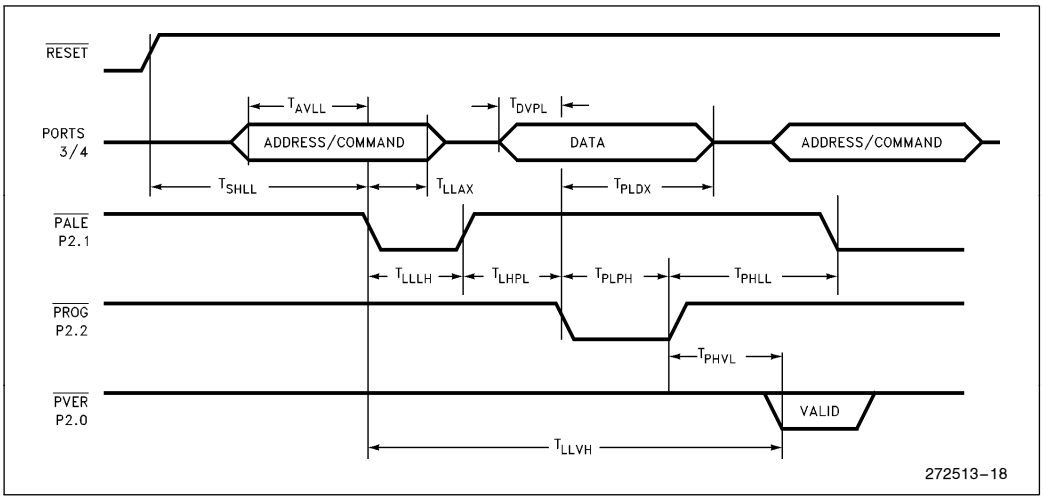
DC EPROM PROGRAMMING CHARACTERISTICS

Symbol	Parameter	Min	Max	Units
I_{PP}	V_{PP} Programming Supply Current		200	mA

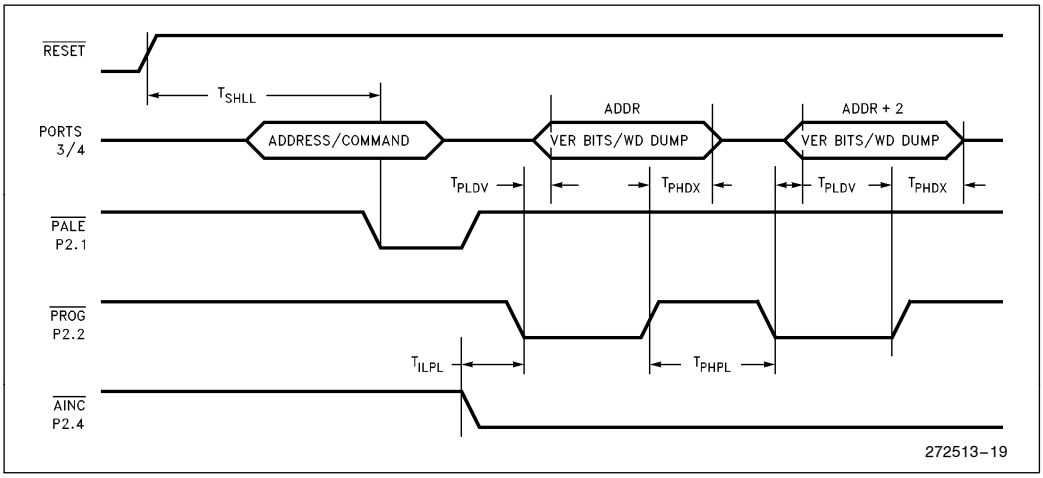
NOTE:
V_{PP} must be within 1V of V_{CC} while V_{CC} < 4.5V. V_{PP} must not have a low impedance path to ground or V_{SS} while V_{CC} > 4.5V.

EPROM PROGRAMMING WAVEFORMS

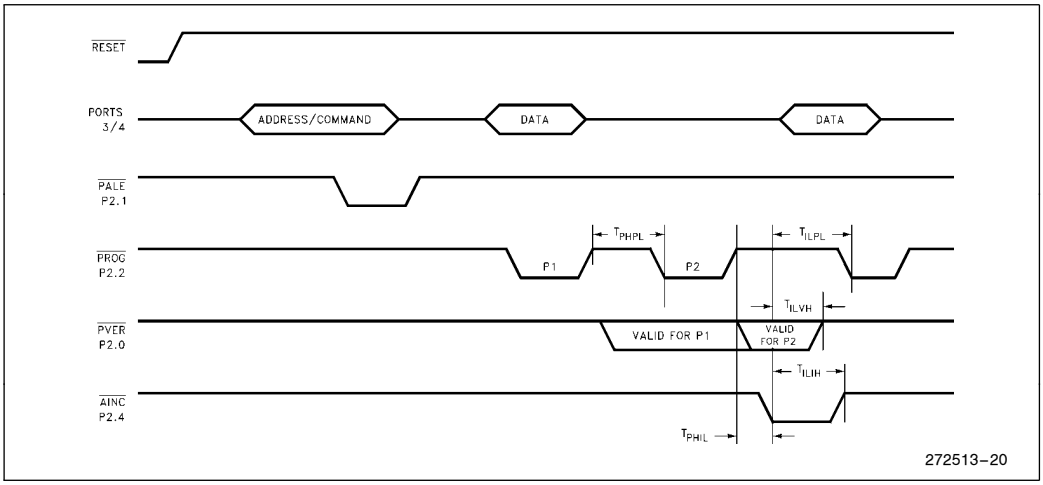
SLAVE PROGRAMMING MODE DATA PROGRAM MODE WITH SINGLE PROGRAM PULSE



SLAVE PROGRAMMING MODE IN WORD DUMP OR DATA VERIFY MODE WITH AUTO INCREMENT



SLAVE PROGRAMMING MODE TIMING IN DATA PROGRAM MODE WITH REPEATED PROG PULSE AND AUTO INCREMENT



AC CHARACTERISTICS—SERIAL PORT-SHIFT REGISTER MODE

SERIAL PORT TIMING—SHIFT REGISTER MODE 0

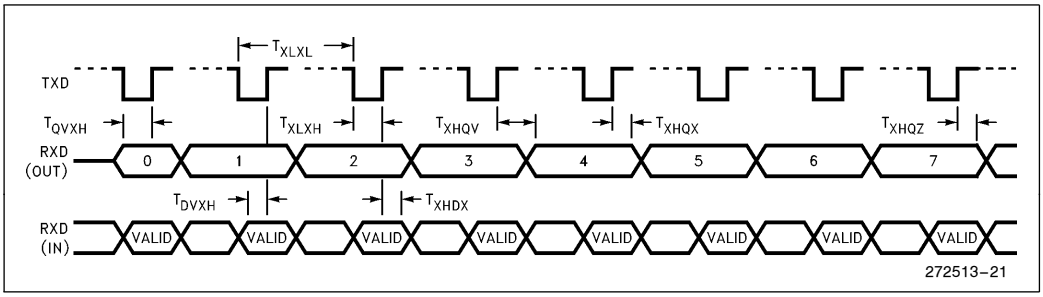
Test Conditions: $T_A = -40°C$ to $+125°C$; $V_{CC} = 5.0V \pm 10\%$; $V_{SS} = 0.0V$; Load Capacitance = pF

Symbol	Parameter	Min	Max	Units
T_{XLXL}	Serial Port Clock Period	$8\ T_{OSC}$		ns
T_{XLXH}	Serial Port Clock Falling Edge to Rising Edge	$4\ T_{OSC} - 50$	$4\ T_{OSC} + 50$	ns
T_{QVXH}	Output Data Setup to Clock Rising Edge	$3\ T_{OSC}$		ns
T_{XHQX}	Output Data Hold after Clock Rising Edge	$2\ T_{OSC} - 50$		ns
T_{XHQV}	Next Output Data Valid after Clock Rising Edge		$2\ T_{OSC} + 50$	ns
T_{DVXH}	Input Data Setup to Clock Rising Edge	$2\ T_{OSC} + 200$		ns
T_{XHDX}(8)	Input Data Hold after Clock Rising Edge	0		ns
T_{XHQZ}(8)	Last Clock Rising to Output Float		$5\ T_{OSC}$	ns

NOTE:
8. Parameters not tested.

WAVEFORM—SERIAL PORT—SHIFT REGISTER MODE

SERIAL PORT WAVEFORM—SHIFT REGISTER MODE



A TO D CHARACTERISTICS

The sample and conversion time of the A/D converter in the 8-bit or 10-bit modes is programmed by loading a byte into the AD__TIME Special Function Register. This allows optimizing the A/D operation for specific applications. The AD__TIME register is functional for all possible values, but the accuracy of the A/D converter is only guaranteed for the times specified in the operating conditions table.

The value loaded into AD__TIME bits 5, 6, 7 determines the sample time, SAMP. The value loaded into AD__TIME bits 0, 1, 2, 3 and 4 determines the bit conversion time, CONV. These bits, as well as the equation for calculating the total conversion time, T, are shown in the following table:

AD__TIME 1FAFH:Byte

7	6	5	4	3	2	1	0
Sample Time				Bit Conversion Time			

(SAMP)	(CONV)
4n + 1 state times	n + 1 state times
n = 1 to 7	n = 2 to 31

Equation: T = (SAMP) + Bx (CONV) + 2.5
T = total conversion time (states)
B = number of bits conversion (8 or 10)
n = programmed register value

The converter is ratiometric, so absolute accuracy is dependent on the accuracy and stability of V_{REF}. V_{REF} must be close to V_{CC} since it supplies both the resistor ladder and the analog portion of the converter and input port pins. There is also an AD__TEST SFR that allows for conversion on ANGND and V_{REF} as well as adjusting the zero offset. The absolute error listed is without doing any adjustments.

A/D CONVERTER SPECIFICATION

The specifications given assume adherence to the operating conditions section of this data sheet. Testing is performed with V_{REF} = 5.12V and 20 MHz operating frequency. After a conversion is started, the device is placed in IDLE mode until the conversion is complete.

10-BIT MODE A/D OPERATING CONDITIONS

Symbol	Description	Min	Max	Units
T_A	Ambient Temperature	−40	+125	°C
V_{CC}	Digital Supply Voltage	4.50	5.50	V
V_{REF}	Analog Supply Voltage	4.50	5.50	V(1)
T_{SAM}	Sample Time	2.0		μs(2)
T_{CONV}	Conversion Time	15	18	μs(2)
F_{OSC}	Oscillator Frequency	4.0	20.0	MHz

NOTES:
1. V_{REF} must be within 0.5V of V_{CC}.
2. The value of AD__TIME is selected to meet these specifications.

10-BIT MODE A/D CHARACTERISTICS (Using Above Operating Conditions)(6)

Parameter	Typ*(1)	Min	Max	Units*
Resolution		1024 10	1024 10	Level Bits
Absolute Error		0	±3.0	LSBs
Full Scale Error	0.25 ±0.5			LSBs
Zero Offset Error	0.25 ±0.5			LSBs
Non-Linearity	1.0 ±2.0		±3.0	LSBs
Differential Non-Linearity		−0.75	+0.75	LSBs
Channel-to-Channel Matching	±0.1	0	±1.0	LSBs
Repeatability	±0.25	0		LSBs(1)
Temperature Coefficients: Offset Full Scale Differential Non-Linearity	 0.009 0.009 0.009			 LSB/C(1) LSB/C(1) LSB/C(1)
Off Isolation		−60		dB(1,2,3)
Feedthrough	−60			dB(1,2)
V_{CC} Power Supply Rejection	−60			dB(1,2)
Input Resistance		750	1.2K	Ω(4)
DC Input Leakage	±1.0	0	±3.0	μA
Sampling Capacitor	3.0			pF

*An ''LSB'' as used here has a value of approximately 5 mV.

NOTES:
1. These values are expected for most parts at 25°C, but are not tested or guaranteed.
2. DC to 100 KHz.
3. Multiplexer break-before-make is guaranteed.
4. Resistance from device pin, through internal MUX, to sample capacitor.
5. All conversions performed with processor in IDLE mode.

8-BIT MODE A/D OPERATING CONDITIONS

Symbol	Description	Min	Max	Units
T_A	Ambient Temperature	−40	+125	°C
V_{CC}	Digital Supply Voltage	4.50	5.50	V
V_{REF}	Analog Supply Voltage	4.50	5.50	V(1)
T_{SAM}	Sample Time	2.0		μs(2)
T_{CONV}	Conversion Time	12	15	μs(2)
F_{OSC}	Oscillator Frequency	4.0	20.0	MHz

NOTES:
1. V_{REF} must be within 0.5V of V_{CC}.
2. The value of AD__TIME is selected to meet these specifications.

8-BIT MODE A/D CHARACTERISTICS (Using Above Operating Conditions)(6)

Parameter	Typ*(1)	Min	Max	Units*
Resolution		256 8	256 8	Level Bits
Absolute Error		0	±1.0	LSBs
Full Scale Error	±0.5			LSBs
Zero Offset Error	±0.5			LSBs
Non-Linearity		0	±1.0	LSBs
Differential Non-Linearity		−0.5	+0.5	LSBs
Channel-to-Channel Matching		0	±1.0	LSBs
Repeatability	±0.25	0		LSBs(1)
Temperature Coefficients: Offset Full Scale Differential Non-Linearity	 0.003 0.003 0.003			 LSB/C(1) LSB/C(1) LSB/C(1)
Off Isolation		−60		dB(1,2,3)
Feedthrough	−60			dB(1,2)
V_{CC} Power Supply Rejection	−60			dB(1,2)
Input Resistance		750	1.2K	Ω(4)
DC Input Leakage	±1.0	0	±1.5	μA
Sampling Capacitor	3.0			pF

*An ''LSB'' as used here has a value of approximately 20 mV.

NOTES:
1. These values are expected for most parts at 25°C, but are not tested or guaranteed.
2. DC to 100 KHz.
3. Multiplexer break-before-make is guaranteed.
4. Resistance from device pin, through internal MUX, to sample capacitor.
5. Applying voltage beyond these specifications will degrade the accuracy of other channels being converted.
6. All conversions performed with processor in IDLE mode.

87C196KT/KS ERRATA

The following is a list of all known functional deviations for 87C196KT/KS devices. B-step and later devices can be identified by a special mark following the eight digit FPO number on the top of the package. For C-step devices, this mark is a ''C''.

1. **HOLD OR READY DURING DIVIDE; (A-step):**

   There is a bug in the DIV and DIVB (signed divide) instructions such that if the following 2 conditions are met, there may be an error of 1 in the quotient:

   a) HOLD or READY is asserted during the first state of execution of the DIV and DIVB instruction.

   b) HOLD or READY duration is 16 state times for the DIVB or 24 state times for a DIV instruction.

2. **P2.7 (CLKOUT); (A-step):**

   Port 2.7 (CLKOUT) does not operate in open drain mode.

3. **P2__REG.7 AND P6__REG.4 THROUGH P6__ REG.7 CLEARED: (A-step):**

   P2__REG.7 is cleared when P2__SSEL.7 bit is changed from a 1 to a 0 (special function to LSIO). P6__Reg.4–.7 is cleared when the corresponding P6__SSEL.4–.7 is changed from a 1 to a 0.

4. **INDIRECT SHIFT INSTRUCTION; (A-step):**

   The upper three bits of the byte register holding the shift count are not masked completely. If the shift count register has the value 32 x n, where n = 1, 3, 5 or 7, the operand wil be shifted 32 times. The above condition results in NO shift taking place.

5. **INTERNAL RAM POWERDOWN LEAKAGE; (A-step):**

   If an invalid address is applied to the internal RAM during power-down, the address lines float. This can cause increased current consumption during power-down. To insure a valid address on the internal RAM, execute the idle/power-down instruction from internal RAM.

6. **INST PIN; (A-step):**

   On A-step devices, the INST pin is pulled medium low for approx. 200 ns after RESET and then pulled weakly *HIGH* until P5SSEL is written to. This is corrected on B-step devices where the INST pin is pulled medium low for approx. 200 ns after RESET and is then pulled weakly *LOW* until P5SSEL is written to.

7. **REGISTER RAM OVERWRITE; (A-step, B-step):**

   If a write is performed to a byte/word location within the SFR range of 1F60h to 1FFFh, the data to be written is also written to a corresponding location located within the REGISTER RAM space 360h to 3FFh. To determine the address of the REGISTER RAM location that is overwritten, an offset of 1C00h can be subtracted from the byte/word addressed in the SFR range.

8. **BUS TIMING MODES 1 AND 2 (A-step, B-step):**

   Bus timing modes 1 and 2 are not featured or specified on A-step and B-step parts. On C-step parts Mode 1 is selected by setting bits MSEL1 = 0 and MSEL0 = 1 in the CCB1 register. Mode 2 is similarly selected by setting MSEL1 = 1 and MSEL0 = 0. Timings are altered by Mode 1 and Mode 2 as follows (for actual values see the Bus Mode 1 and Bus Mode 2 AC Characteristics in this data sheet):

   Mode 1: $\overline{RD}$, $\overline{WR}$ advanced 1 T_{OSC}

   ALE advanced 0.5 T_{OSC}

   ALE pulse width remains 1 T_{OSC}

   Mode 2: $\overline{RD}$, $\overline{WR}$ advanced 1 T_{OSC}

   ALE advanced 0.5 T_{OSC}

   ALE pulse width remains 1 T_{OSC}

   Address advanced 0.5 T_{OSC}

9. **V_{OH2} (A-step, b-step):**

   A- and B-step parts are capable of $V_{OH2} = V_{CC} - 1V$ with $I_{OH} = -6\ \mu A$. C-step devices meet the target values of $V_{OH2} = V_{CC} - 1V$ with $I_{OH} = -15\ \mu A$.

10. **CLKOUT DURING RESET (A-step, B-step, C-step):**

    For all steppings of the 87C196KT, the CLKOUT function during RESET (P2.7) differs from the 87C196KR C-step. During RESET on the 87C196KT, CLKOUT does not toggle and remains in the high state. During RESET on the 87C196KR C-step CLKOUT countinues to toggle.

87C196KT/KS DESIGN CONSIDERATIONS

1. EPA TIMER RESET/WRITE CONFLICT

If the user writes to the EPA timer at the same time that the timer is reset, it is indeterminate which will take precedence. Users should not write to a timer if using EPA signals to reset it.

2. VALID TIME MATCHES

The timer must increment/decrement to the compare value for a match to occur. A match does not occur if the timer is loaded with a value equal to an EPA compare value. Matches also do not occur if a timer is reset and 0 is the EPA compare value.

3. P6__PIN.4-.7 NOT UPDATED IMMEDIATELY

Values written to P6__REG are temporarily held in a buffer. If P6__MODE is cleared, the buffer is loaded into P6__REG.x If P6__MODE is set, the value stays in the buffer and is loaded into P6__REG.x when P6__MODE.x is cleared. Since reading P6__REG returns the current value in P6__REG and not the buffer, changes to P6__REG cannot be read until/unless P6__MODE.x is cleared.

4. WRITE CYCLE DURING RESET

If RESET occurs during a write cycle, the contents of the external memory device may be corrupted.

5. INDIRECT SHIFT INSTRUCTION

The upper 3 bits of the byte register holding the shift count are not masked completely. If the shift count register has the value 32 × n, where n = 1, 3, 5, or 7, the operand will be shifted 32 times. This should have resulted in no shift taking place.

6. PORT 4 ADDRESS BEHAVIOR

For bus timing Modes 1 and 2, specified only on the 87C196KT/KS C-step, Port 4 does not retain the address during the data portion of the bus cycle. *Designs using an 8-bit external memory system in bus Mode 1 or Mode 2 require an external latch on Port 4 to retain the address during the data portion of the bus cycle.* Designs using an 8-bit external memory system in the **KR** or **KR + 1 Wait** bus timing modes do not require an external latch. Designs using 16-bit external memory systems require an external latch on both Port 3 and Port 4 in all bus timing modes.

7. EPA Overruns

EPA ''lock-up'' can occur if overruns are not handled correctly, refer to Intel Techbit #DB0459 *''Understanding EPA Capture Overruns''*, date 12-9-93. Applies to EPA channels with interrupts and overruns enabled (ON/RT bit set to 1).

8. Indirect Addressing with Auto-Increment

For the special case of a pointer pointing to itself using auto-increment, an incorrect access of the incremented pointer address will occur instead of an access to the original pointer address. All other indirect auto-increment accesses will not be effected. Please refer to Techbit #MCO593.

Incorrect sequence: Results in ax being incremented by 1 and the contents of the address pointed to by ax+1 to be loaded into bx.

```
ld  ax,#ax
ldb bx,[ax]+
```

Suggested sequence: Results in the contents of the address pointed to by ax to be loaded into bx and ax incremented by 1.

```
ld  ax,#bx; where ax does not equal
bx
ldb cx,[ax]+
```

DATA SHEET REVISION HISTORY

This is the (-003) version of the 20 MHz 8XC196KT/KS datasheet. The following differences exist between the -002 revision and the -003 revision.

1. V_{OL3} estimate added.

2. ‘‘Voltage on Analog Input Pin’’ removed. Parameter covered by Note 1: V_{REF} must be within 0.5V of V_{CC}.