ANALOG DEVICES

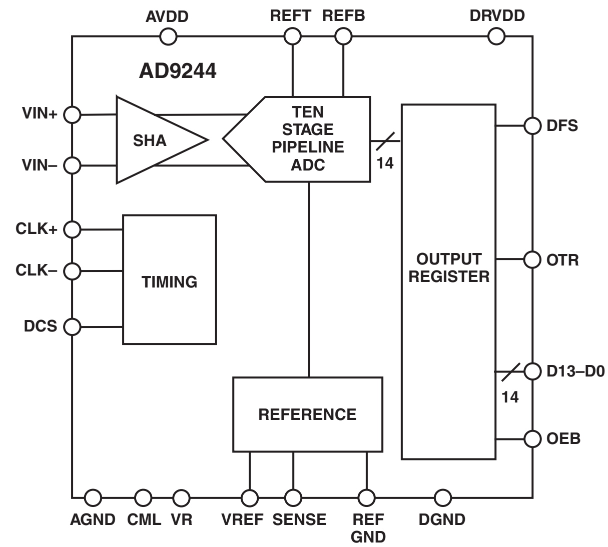
14-Bit, 40/65 MSPS A/D Converter

AD9244

FEATURES
14-Bit, 40/65 MSPS ADC
Low Power:
  550 mW at 65 MSPS
  300 mW at 40 MSPS
On-Chip Reference and Sample-and-Hold
750 MHz Analog Input Bandwidth
SNR > 73 dBc to Nyquist @ 65 MSPS
SFDR > 86 dBc to Nyquist @ 65 MSPS
Differential Nonlinearity Error = ±0.7 LSB
Guaranteed No Missing Codes over Full Temperature Range
1 V to 2 V p-p Differential Full-Scale Analog Input Range
Single 5 V Analog Supply, 3.3 V/5 V Driver Supply
Out-of-Range Indicator
Straight Binary or Twos Complement Output Data
Clock Duty Cycle Stabilizer
Output Enable Function
48-Lead LQFP Package

APPLICATIONS
Communications Subsystems (Microcell, Picocell)
Medical and High End Imaging Equipment
Ultrasound Equipment

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION
The AD9244 is a monolithic, single 5 V supply, 14-bit, 40 MSPS/65 MSPS analog-to-digital converter with an on-chip, high performance sample-and-hold amplifier and voltage reference. The AD9244 uses a multistage differential pipelined architecture with output error correction logic to provide 14-bit accuracy at 40 MSPS/65 MSPS data rates and guarantees no missing codes over the full operating temperature range.

The AD9244 has an on-board, programmable voltage reference. An external reference can also be used to suit the dc accuracy and temperature drift requirements of the application.

A differential or single-ended clock input is used to control all internal conversion cycles. The digital output data can be presented in straight binary or in twos complement format. An out-of-range (OTR) signal indicates an overflow condition that can be used with the most significant bit to determine low or high overflow.

Fabricated on an advanced CMOS process, the AD9244 is available in a 48-lead low profile quad flatpack package (LQFP) and is specified for operation over the industrial temperature range (–40°C to +85°C).

PRODUCT HIGHLIGHTS
Low Power—The AD9244, at 550 mW, consumes a fraction of the power of presently available ADCs in existing high speed solutions.

IF Sampling—The AD9244 delivers outstanding performance at input frequencies beyond the first Nyquist zone. Sampling at 65 MSPS with an input frequency of 100 MHz, the AD9244 delivers 71 dB SNR and 86 dB SFDR.

Pin Compatibility—The AD9244 offers a seamless migration from the 12-bit, 65 MSPS AD9226.

On-Board Sample-and-Hold (SHA)—The versatile SHA input can be configured for either single-ended or differential inputs.

Out-of-Range (OTR)—The OTR output bit indicates when the input signal is beyond the AD9244's input range.

Single Supply—The AD9244 uses a single 5 V power supply, simplifying system power supply design. It also features a separate digital output driver supply to accommodate 3.3 V and 5 V logic families.

REV. A

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AD9244–SPECIFICATIONS

DC SPECIFICATIONS

(AVDD = 5 V, DRVDD = 3 V, f_{SAMPLE} = 65 MSPS (–65) or 40 MSPS (–40), Differential Clock Inputs, VREF = 2 V, External Reference, Differential Analog Inputs, unless otherwise noted.)

Parameter	Temp	Test Level	AD9244BST-65 Min	AD9244BST-65 Typ	AD9244BST-65 Max	AD9244BST-40 Min	AD9244BST-40 Typ	AD9244BST-40 Max	Unit
RESOLUTION	Full	VI	14			14			Bits
DC ACCURACY									
No Missing Codes	Full	VI		Guaranteed			Guaranteed		Bits
Offset Error	Full	VI		±0.3	±1.4		±0.3	±1.4	% FSR
Gain Error[1]	Full	VI		±0.6	±2.0		±0.6	±2.0	% FSR
Differential Nonlinearity (DNL)[2]	Full	VI			±1.0			±1.0	LSB
	25°C	V		±0.7			±0.6		LSB
Integral Nonlinearity (INL)[2]	Full	V		±1.4			±1.3		LSB
TEMPERATURE DRIFT									
Offset Error	Full	V		±2.0			±2.0		ppm/°C
Gain Error (EXT VREF)[1]	Full	V		±2.3			±2.3		ppm/°C
Gain Error (INT VREF)[3]	Full	V		±25			±25		ppm/°C
INTERNAL VOLTAGE REFERENCE									
Output Voltage Error (2 VREF)	Full	VI			±29			±29	mV
Load Regulation @ 1 mA	Full	V		0.5			0.5		mV
Output Voltage Error (1 VREF)	Full	IV			±15			±15	mV
Load Regulation @ 0.5 mA	Full	V		0.25			0.25		mV
Input Resistance	Full	V		5			5		kΩ
INPUT REFERRED NOISE									
VREF = 2 V	25°C	V		0.8			0.8		LSB rms
VREF = 1 V	25°C	V		1.5			1.5		LSB rms
ANALOG INPUT									
Input Voltage Range (Differential)									
VREF = 2 V	Full	V		2			2		V p-p
VREF = 1 V	Full	V		1			1		V p-p
Common-Mode Voltage	Full	V	0.5		4	0.5		4	V
Input Capacitance[4]	25°C	V		10			10		pF
Input Bias Current[5]	25°C	V		500			500		µA
Analog Bandwidth (Full Power)	25°C	V		750			750		MHz
POWER SUPPLIES									
Supply Voltages									
AVDD	Full	IV	4.75	5	5.25	4.75	5	5.25	V
DRVDD	Full	IV	2.7		5.25	2.7		5.25	V
Supply Current									
IAVDD	Full	V		109			64		mA
IDRVDD	Full	V		12			8		mA
PSRR	Full	V		±0.05			±0.05		% FSR
POWER CONSUMPTION									
DC Input[6]	Full	V		550			300		mW
Sine Wave Input	Full	VI		590	640		345	370	mW

NOTES

[1] Gain error is based on the ADC only (with a fixed 2.0 V external reference).

[2] Measured at maximum clock rate, f_{IN} = 2.4 MHz, full-scale sine wave, with approximately 5 pF loading on each output bit.

[3] Includes internal voltage reference error.

[4] Input capacitance refers to the effective capacitance between one differential input pin and AGND. Refer to Figure 2d for the equivalent analog input structure.

[5] Input bias current is due to the inputs looking like a resistor that is dependent on the clock rate.

[6] Measured with dc input at maximum clock rate.

Specifications subject to change without notice.

AC SPECIFICATIONS

(AVDD = 5 V, DRVDD = 3 V, f_{SAMPLE} = 65 MSPS (–65) or 40 MSPS (–40), Differential Clock Inputs, VREF = 2 V, External Reference, A_{IN} = –0.5 dBFS, Differential Analog Inputs, unless otherwise noted.)

Parameter	Temp	Test Level	AD9244BST-65 Min	AD9244BST-65 Typ	AD9244BST-65 Max	AD9244BST-40 Min	AD9244BST-40 Typ	AD9244BST-40 Max	Unit
SNR									
f_{IN} = 2.4 MHz	Full	VI	72.4			73.4			dBc
	25°C	I		74.8			75.3		dBc
f_{IN} = 15.5 MHz (–1 dBFS)	Full	IV	72.0						dBc
	25°C	V		73.7					dBc
f_{IN} = 20 MHz	Full	VI				72.1			dBc
	25°C	I					74.7		dBc
f_{IN} = 32.5 MHz	Full	IV	70.8						dBc
	25°C	I		73.0					dBc
f_{IN} = 70 MHz	Full	IV	69.9						dBc
	25°C	V		72.2					dBc
f_{IN} = 100 MHz	25°C	V		71.2			72.8		dBc
f_{IN} = 200 MHz	25°C	V		67.2			68.3		dBc
SINAD									
f_{IN} = 2.4 MHz	Full	VI	72.2			73.2			dBc
	25°C	I		74.7			75.1		dBc
f_{IN} = 20 MHz	Full	VI				72			dBc
	25°C	I					74.4		dBc
f_{IN} = 32.5 MHz	Full	IV	70.6						dBc
	25°C	I		72.6					dBc
f_{IN} = 70 MHz	Full	IV	69.7						dBc
	25°C	V		71.9					dBc
f_{IN} = 100 MHz	25°C	V		71			72.4		dBc
f_{IN} = 200 MHz	25°C	V		59.8			56.3		dBc
ENOB									
f_{IN} = 2.4 MHz	Full	VI	11.7			11.9			Bits
	25°C	I		12.1			12.2		Bits
f_{IN} = 20 MHz	Full	VI				11.7			Bits
	25°C	I					12.1		Bits
f_{IN} = 32.5 MHz	Full	IV	11.4						Bits
	25°C	I		11.8					Bits
f_{IN} = 70 MHz	Full	IV	11.3						Bits
	25°C	V		11.7					Bits
f_{IN} = 100 MHz	25°C	V		11.5			11.7		Bits
f_{IN} = 200 MHz	25°C	V		9.6			9.1		Bits
THD									
f_{IN} = 2.4 MHz	Full	VI			–78.4			–80.7	dBc
	25°C	I		–90.0			–89.7		dBc
f_{IN} = 20 MHz	Full	VI						–80.4	dBc
	25°C	I					–89.4		dBc
f_{IN} = 32.5 MHz	Full	IV			–79.2				dBc
	25°C	I		–84.6					dBc
f_{IN} = 70 MHz	Full	IV			–78.7				dBc
	25°C	V		–84.1					dBc
f_{IN} = 100 MHz	25°C	V		–83.0			–83.2		dBc
f_{IN} = 200 MHz	25°C	V		–60.7			–56.6		dBc
WORST 2 or 3									
f_{IN} = 2.4 MHz	25°C	V		–94.5			–93.7		dBc
f_{IN} = 20 MHz	25°C	V					–92.8		dBc
f_{IN} = 32.5 MHz	25°C	V		–86.5					dBc
f_{IN} = 70 MHz	25°C	V		–86.1					dBc
f_{IN} = 100 MHz	25°C	V		–86.2			–84.5		dBc
f_{IN} = 200 MHz	25°C	V		–60.7			–56.6		dBc

AC SPECIFICATIONS (continued)

Parameter	Temp	Test Level	AD9244BST-65 Min	AD9244BST-65 Typ	AD9244BST-65 Max	AD9244BST-40 Min	AD9244BST-40 Typ	AD9244BST-40 Max	Unit
SFDR									
f_{IN} = 2.4 MHz	Full	VI	78.6			82.5			dBc
	25°C	I		94.5			93.7		dBc
f_{IN} = 15.5 MHz (–1 dBFS)	Full	IV	83						dBc
	25°C	V		90					dBc
f_{IN} = 20 MHz	Full	IV				81.4			dBc
	25°C	I					91.8		dBc
f_{IN} = 32.5 MHz	Full	IV	80.0						dBc
	25°C	I		86.4					dBc
f_{IN} = 70 MHz	Full	IV	79.5						dBc
	25°C	V		86.1					dBc
f_{IN} = 100 MHz	25°C	V		86.2			84.5		dBc
f_{IN} = 200 MHz	25°C	V		60.7			56.6		dBc

DIGITAL SPECIFICATIONS (AVDD = 5 V, DRVDD = 3 V, VREF = 2 V, External Reference, unless otherwise noted.)

Parameter	Temp	Test Level	AD9244BST-65 Min	AD9244BST-65 Typ	AD9244BST-65 Max	AD9244BST-40 Min	AD9244BST-40 Typ	AD9244BST-40 Max	Unit
DIGITAL INPUTS									
Logic 1 Voltage (OEB, DRVDD = 3 V)	Full	IV	2			2			V
Logic 1 Voltage (OEB, DRVDD = 5 V)	Full	IV	3.5			3.5			V
Logic 0 Voltage (OEB)	Full	IV			0.8			0.8	V
Logic 1 Voltage (DFS, DCS)	Full	IV	3.5			3.5			V
Logic 0 Voltage (DFS, DCS)	Full	IV			0.8			0.8	V
Input Current	Full	IV			10			10	µA
Input Capacitance	Full	V		5			5		pF
CLOCK INPUT PARAMETERS									
Differential Input Voltage	Full	IV	0.4			0.4			V p-p
CLK–Voltage[1]	Full	IV	0.25			0.25			V
Internal Clock Common-Mode	Full	V		1.6			1.6		V
Single-Ended Input Voltage									
Logic 1 Voltage	Full	IV	2			2			V
Logic 0 Voltage	Full	IV			0.8			0.8	V
Input Capacitance	Full	V		5			5		pF
Input Resistance	Full	V		100			100		kΩ
DIGITAL OUTPUTS (DRVDD = 5 V)[2]									
Logic 1 Voltage (I_{OH} = 50 µA)	Full	IV	4.5			4.5			V
Logic 0 Voltage (I_{OL} = 50 µA)	Full	IV			0.1			0.1	V
Logic 1 Voltage (I_{OH} = 0.5 mA)	Full	IV	2.4			2.4			V
Logic 0 Voltage (I_{OL} = 1.6 mA)	Full	IV			0.4			0.4	V
DIGITAL OUTPUTS (DRVDD = 3 V)[2]									
Logic 1 Voltage (I_{OH} = 50 µA)	Full	IV	2.95			2.95			V
Logic 0 Voltage (I_{OL} = 50 µA)	Full	IV			0.05			0.05	V
Logic 1 Voltage (I_{OH} = 0.5 mA)	Full	IV	2.8			2.8			V
Logic 0 Voltage (I_{OL} = 1.6 mA)	Full	IV			0.4			0.4	V

NOTES
[1]See Clock section of Theory of Operation for more details.
[2]Output voltage levels measured with 5 pF load on each output.
Specifications subject to change without notice.

SWITCHING SPECIFICATIONS (AVDD = 5 V, DRVDD = 3 V, unless otherwise noted.)

Parameter	Temp	Test Level	AD9244BST-65 Min	AD9244BST-65 Typ	AD9244BST-65 Max	AD9244BST-40 Min	AD9244BST-40 Typ	AD9244BST-40 Max	Unit
CLOCK INPUT PARAMETERS									
Maximum Conversion Rate	Full	VI	65			40			MHz
Minimum Conversion Rate	Full	V			500			500	kHz
Clock Period[1]	Full	V	15.4			25			ns
Clock Pulsewidth High[2]	Full	V	4			4			ns
Clock Pulsewidth Low[2]	Full	V	4			4			ns
Clock Pulsewidth High[3]	Full	V	6.9			11.3			ns
Clock Pulsewidth Low[3]	Full	V	6.9			11.3			ns
DATA OUTPUT PARAMETERS									
Output Delay (t_{PD})[4]	Full	V	3.5		7	3.5		7	ns
Pipeline Delay (Latency)	Full	V		8			8		Clock Cycles
Aperture Delay (t_A)	Full	V		1.5			1.5		ns
Aperture Uncertainty (Jitter)	Full	V		0.3			0.3		ps rms
Output Enable Delay	Full	V		15			15		ns
OUT-OF-RANGE RECOVERY TIME	Full	V		2			1		Clock Cycles

NOTES
[1]The clock period may be extended to 2 µs with no degradation in specified performance at 25°C.
[2]With duty cycle stabilizer enabled.
[3]With duty cycle stabilizer disabled.
[4]Measured from clock 50% transition to data 50% transition with 5 pF load on each output.
Specifications subject to change without notice

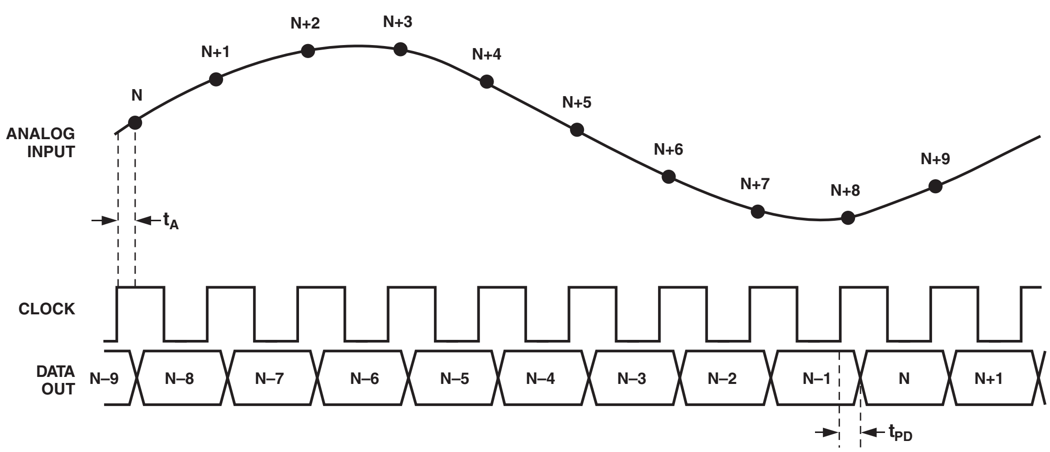


Figure 1. Input Timing

ABSOLUTE MAXIMUM RATINGS[1]

Mnemonic	With Respect to	Min	Max	Unit
ELECTRICAL				
AVDD	AGND	–0.3	+6.5	V
DRVDD	DGND	–0.3	+6.5	V
AGND	DGND	–0.3	+0.3	V
AVDD	DRVDD	–6.5	+6.5	V
REFGND	AGND	–0.3	+0.3	V
CLK+, CLK–, DCS	AGND	–0.3	AVDD + 0.3	V
DFS	AGND	–0.3	AVDD + 0.3	V
VIN+, VIN–	AGND	–0.3	AVDD + 0.3	V
VREF	AGND	–0.3	AVDD + 0.3	V
SENSE	AGND	–0.3	AVDD + 0.3	V
REFB, REFT	AGND	–0.3	AVDD + 0.3	V
CML	AGND	–0.3	AVDD + 0.3	V
VR	AGND	–0.3	AVDD + 0.3	V
OTR	DGND	–0.3	DRVDD + 0.3	V
D0–D13	DGND	–0.3	DRVDD + 0.3	V
OEB	DGND	–0.3	DRVDD + 0.3	V
ENVIRONMENTAL[2]				
Junction Temperature			150	°C
Storage Temperature		–65	+150	°C
Operating Temperature		–40	+85	°C
Lead Temperature (10 sec)			300	°C

NOTES

[1]Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

[2]Typical thermal impedances; θ_{JA} = 50.0°C/W; θ_{JC} = 17.0°C/W. These measurements were taken on a 4-layer board in still air, in accordance with EIA/JESD51-7.

EXPLANATION OF TEST LEVELS

Test Level

I. 100% production tested.

II. 100% production tested at 25°C and sample tested at specified temperatures.

III. Sample tested only.

IV. Parameter is guaranteed by design and characterization testing.

V. Parameter is a typical value only.

VI. 100% production tested at 25°C; guaranteed by design and characterization testing for industrial temperature range; 100% production tested at temperature extremes for military devices.

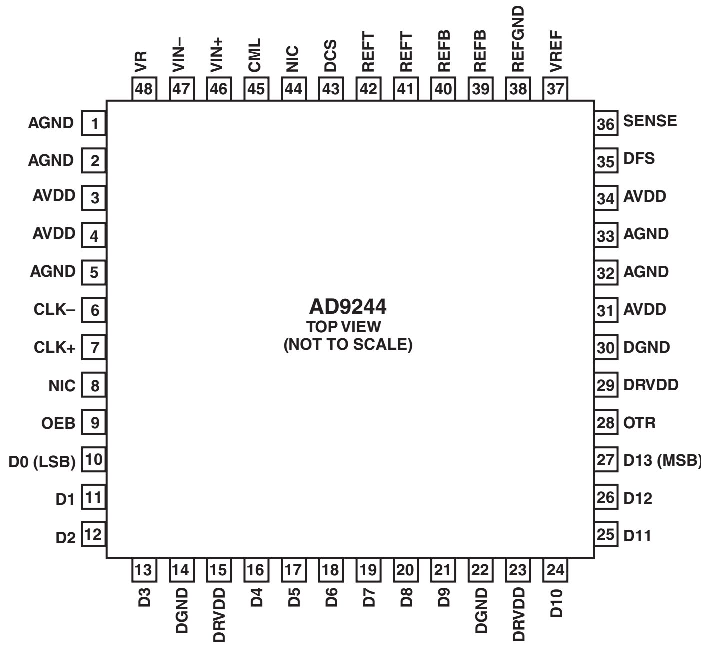
ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD9244BST-65	–40°C to +85°C	48-Lead Low Profile Quad Flatpack Package	ST-48
AD9244BST-40	–40°C to +85°C	48-Lead Low Profile Quad Flatpack Package	ST-48
AD9244BSTRL-65	–40°C to +85°C	48-Lead Low Profile Quad Flatpack Package	ST-48
AD9244BSTRL-40	–40°C to +85°C	48-Lead Low Profile Quad Flatpack Package	ST-48
AD9244-65PCB		Evaluation Board	
AD9244-40PCB		Evaluation Board	

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD9244 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION



PIN FUNCTION DESCRIPTIONS

Pin No.	Mnemonic	Description
1, 2, 5, 32, 33	AGND	Analog Ground.
3, 4, 31, 34	AVDD	Analog Supply Voltage.
6, 7	CLK–, CLK+	Differential Clock Inputs.
8, 44	NIC	No Internal Connection.
9	OEB	Digital Output Enable (Active Low).
10	D0 (LSB)	Least Significant Bit, Digital Output.
11–13, 16–21, 24–26	D1–D3, D4–D9, D10–D12	Digital Outputs.
14, 22, 30	DGND	Digital Ground.
15, 23, 29	DRVDD	Digital Supply Voltage.
27	D13 (MSB)	Most Significant Bit, Digital Output.
28	OTR	Out-of-Range Indicator (Logic 1 indicates OTR).
35	DFS	Data Format Select. Connect to AGND for straight binary, AVDD for twos complement.
36	SENSE	Internal Reference Control.
37	VREF	Internal Reference.
38	REFGND	Reference Ground.
39–42	REFB, REFT	Internal Reference Decoupling.
43	DCS	50% Duty Cycle Stabilizer. Connect to AVDD to activate 50% duty cycle stabilizer, AGND for external control of both clock edges.
45	CML	Common-Mode Reference (0.5 × AVDD).
46, 47	VIN+, VIN–	Differential Analog Inputs.
48	VR	Internal Bias Decoupling.

TERMINOLOGY

Analog Bandwidth (Full Power Bandwidth)
The analog input frequency at which the spectral power of the fundamental frequency (as determined by the FFT analysis) is reduced by 3 dB.

Aperture Delay
The delay between the 50% point of the rising edge of the clock and the instant at which the analog input is sampled.

Aperture Uncertainty (Jitter)
The sample-to-sample variation in aperture delay.

Differential Analog Input Voltage Range
The peak-to-peak differential voltage must be applied to the converter to generate a full-scale response. Peak differential voltage is computed by observing the voltage on a single pin and subtracting the voltage from the other pin, which is 180 degrees out of phase. Peak-to-peak differential is computed by rotating the input phase 180° and taking the peak measurement again. Then the difference is found between the two peak measurements.

Differential Nonlinearity (DNL, No Missing Codes)
An ideal ADC exhibits code transitions that are exactly 1 LSB apart. DNL is the deviation from this ideal value. Guaranteed no missing codes to 14-bit resolution indicates that all 16384 codes must be present over all operating ranges.

Dual Tone SFDR*
The ratio of the rms value of either input tone to the rms value of the peak spurious component. The peak spurious component may or may not be an IMD product.

Effective Number of Bits (ENOB)
The effective number of bits for a device for sine wave inputs at a given input frequency can be calculated directly from its measured SINAD using the following formula:

$$N = (SINAD - 1.76)/6.02$$

Gain Error
The first code transition should occur at an analog value 1/2 LSB above negative full scale. The last code transition should occur at an analog value 1 1/2 LSB below the nominal full scale. Gain error is the deviation of the actual difference between first and last code transitions and the ideal difference between first and last code transitions.

Common-Mode Rejection Ratio (CMRR)
Common-mode (CM) signals appearing on VIN+ and VIN– are ideally rejected by the differential front end of the ADC. With a full-scale CM signal driving both VIN+ and VIN–, CMRR is the ratio of the amplitude of the full-scale input CM signal to the amplitude of signal that is not rejected, expressed in dBFS.

IF Sampling
Due to the effects of aliasing, an ADC is not necessarily limited to Nyquist sampling. Higher sampled frequencies will be aliased down into the first Nyquist zone (DC–$f_{CLOCK}/2$) on the output of the ADC. Care must be taken that the bandwidth of the sampled signal does not overlap Nyquist zones and alias onto itself. Nyquist sampling performance is limited by the bandwidth of the input SHA and clock jitter (noise caused by jitter increases as the input frequency increases).

Integral Nonlinearity (INL)
INL refers to the deviation of each individual code from a line drawn from negative full scale through positive full scale. The point used as negative full scale occurs 1/2 LSB before the first code transition. Positive full scale is defined as a level 1 1/2 LSB beyond the last code transition. The deviation is measured from the middle of each particular code to the true straight line.

Minimum Conversion Rate
The clock rate at which the SNR of the lowest analog signal frequency drops by no more than 3 dB below the guaranteed limit.

Maximum Conversion Rate
The clock rate at which parametric testing is performed.

Nyquist Sampling
When the frequency components of the analog input are below the Nyquist frequency ($f_{CLOCK}/2$), this is often referred to as Nyquist sampling.

Out-of-Range Recovery Time
The time it takes for the ADC to reacquire the analog input after a transition from 10% above positive full scale to 10% above negative full scale, or from 10% below negative full scale to 10% below positive full scale.

Power Supply Rejection Ratio
The change in full scale from the value with the supply at its minimum limit to the value with the supply at its maximum limit.

Signal-to-Noise-and-Distortion (SINAD)*
The ratio of the rms signal amplitude to the rms value of the sum of all other spectral components below the Nyquist frequency, including harmonics but excluding dc.

Signal-to-Noise Ratio (SNR)*
The ratio of the rms signal amplitude to the rms value of the sum of all other spectral components below the Nyquist frequency, excluding the first six harmonics and dc.

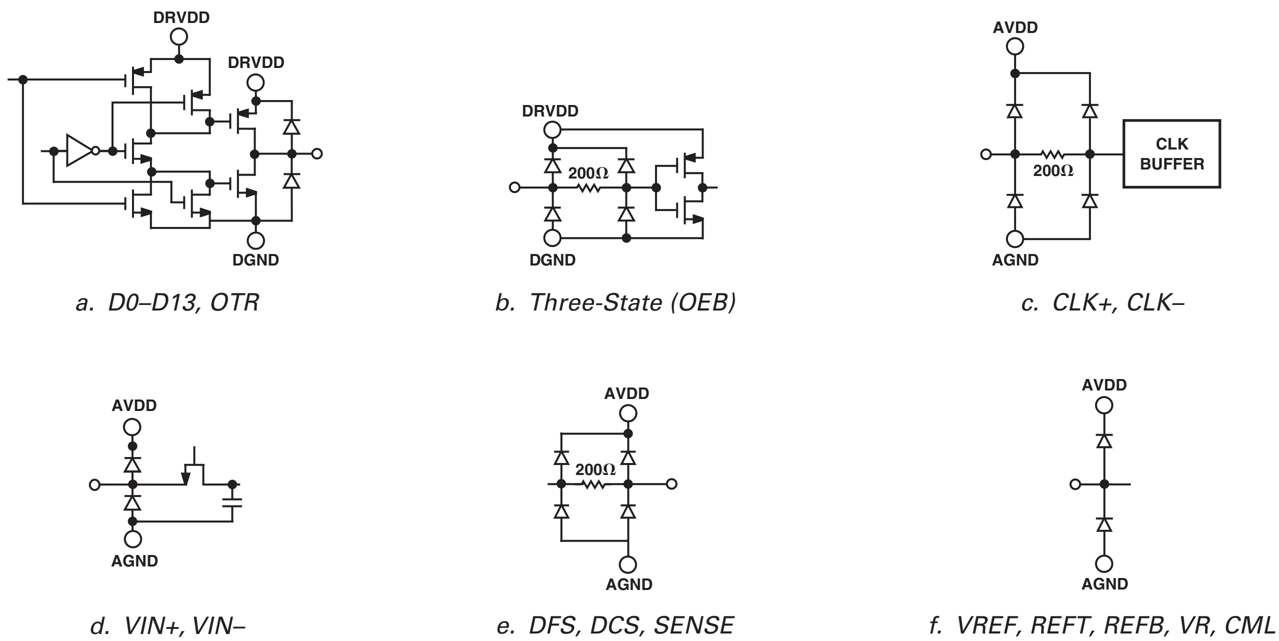
Spurious-Free Dynamic Range (SFDR)*
The difference in dB between the rms amplitude of the input signal and the peak spurious signal.

Temperature Drift
The temperature drift for offset error and gain error specifies the maximum change from the initial (25°C) value to the value at T_{MIN} or T_{MAX}.

Total Harmonic Distortion (THD)*
The ratio of the rms sum of the first six harmonic components to the rms value of the measured input signal.

Offset Error
The major carry transition should occur for an analog value 1/2 LSB below VIN+ = VIN–. Offset error is defined as the deviation of the actual transition from that point.

*AC specifications may be reported in dBc (degrades as signal levels are lowered) or in dBFS (always related back to converter full scale).



a. D0–D13, OTR

b. Three-State (OEB)

c. CLK+, CLK–

d. VIN+, VIN–

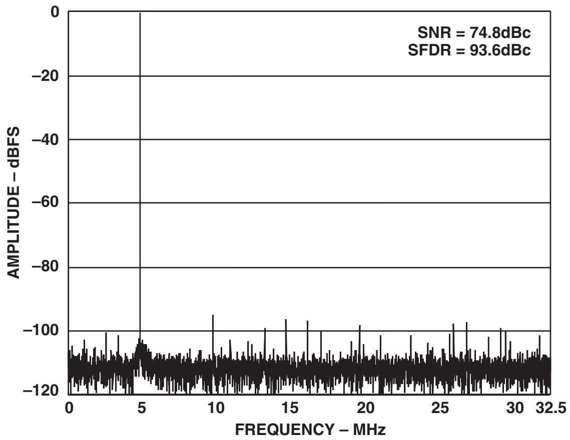
e. DFS, DCS, SENSE

f. VREF, REFT, REFB, VR, CML

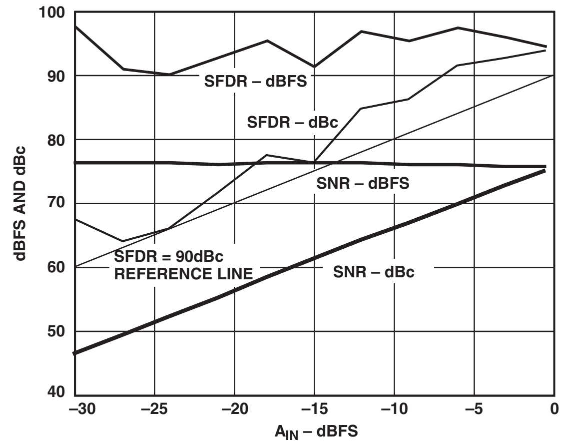
Figure 2. Equivalent Circuits

AD9244–Typical Performance Characteristics

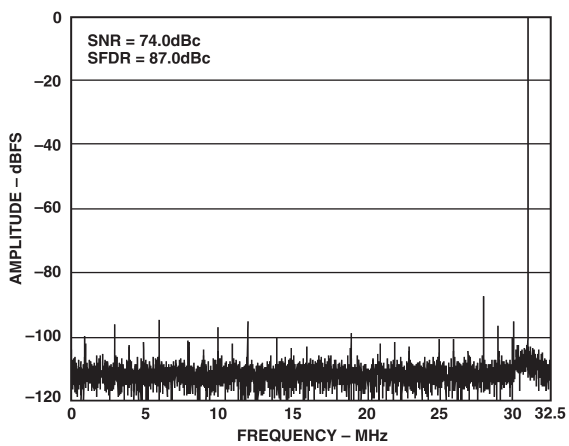
(AVDD = 5.0 V, DRVDD = 3.0 V, f_{SAMPLE} = 65 MSPS with CLK Duty Cycle Stabilizer Enabled, T_A = 25°C, Differential Analog Input, Common-Mode Voltage (VCM) = 2.5 V, Input Amplitude (A_{IN}) = –0.5 dBFS, VREF = 2.0 V External, FFT length = 8 K, unless otherwise noted.)



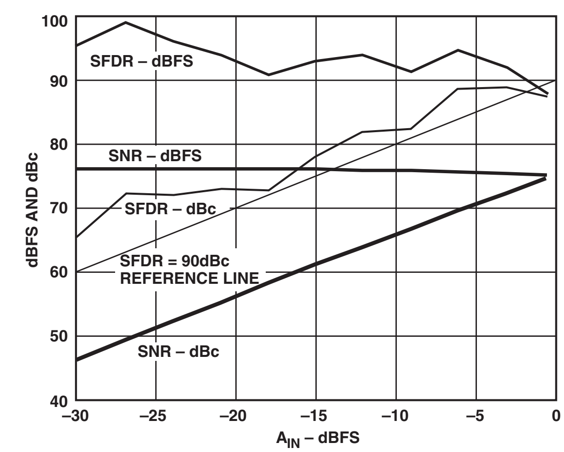
TPC 1. Single-Tone FFT, f_{IN} = 5 MHz



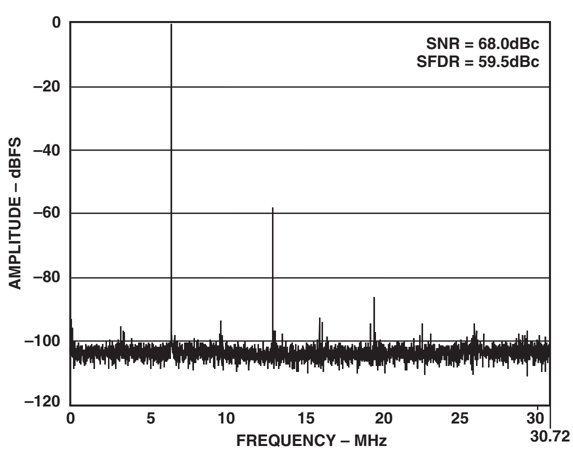
TPC 4. Single-Tone SNR/SFDR vs. A_{IN}, f_{IN} = 5 MHz



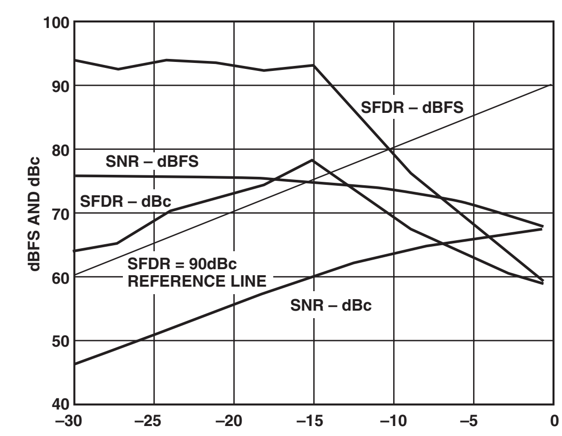
TPC 2. Single-Tone FFT, f_{IN} = 31 MHz



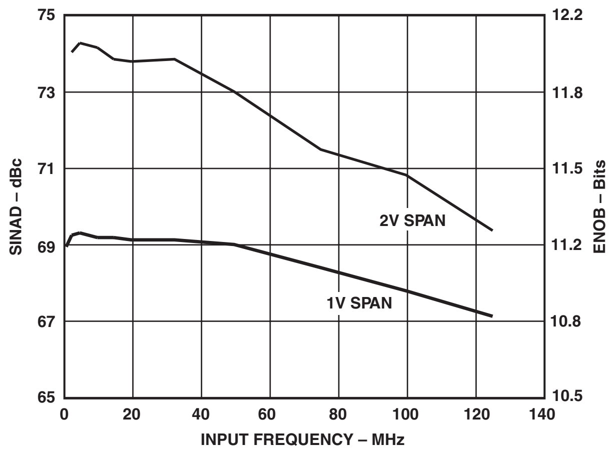
TPC 5. Single-Tone SNR/SFDR vs A_{IN}, f_{IN} = 31 MHz



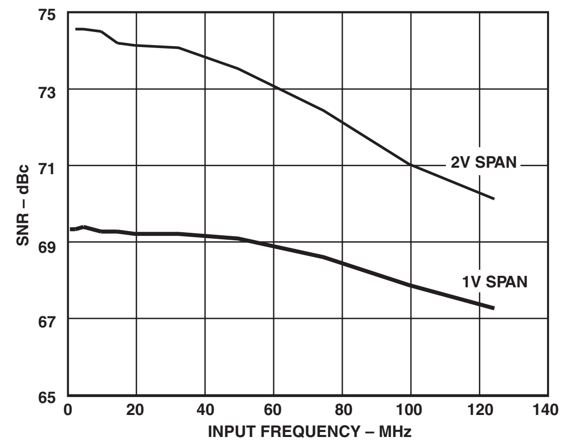
TPC 3. Single-Tone FFT, f_{IN} = 190 MHz, f_{SAMPLE} = 61.44 MSPS



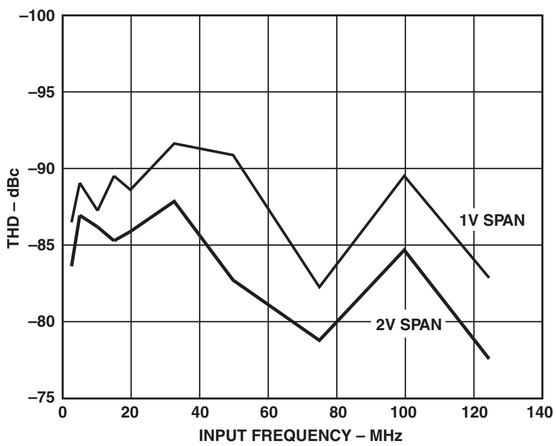
TPC 6. Single-Tone SNR/SFDR vs. A_{IN}, f_{IN} = 190 MHz, f_{SAMPLE} = 61.44 MSPS



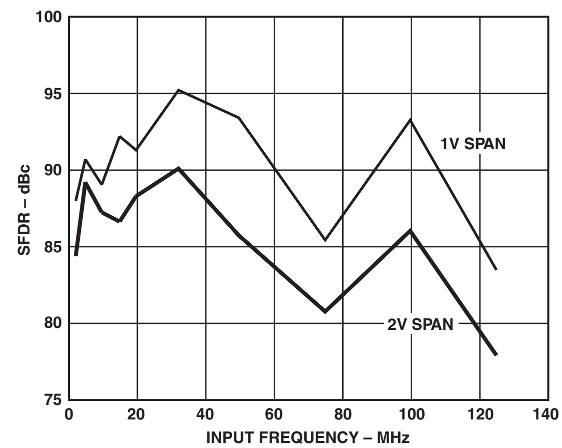
TPC 7. SINAD/ENOB vs. Input Frequency



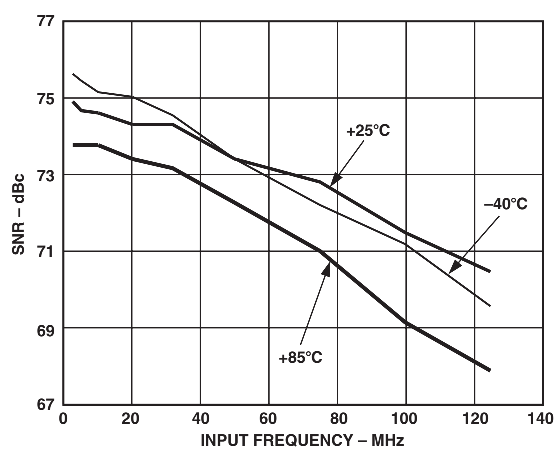
TPC 10. SNR vs. Input Frequency



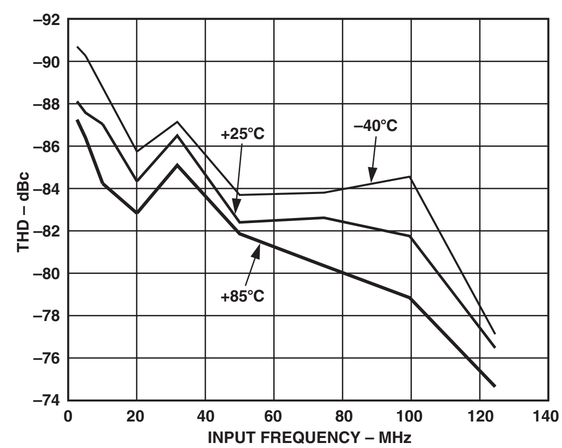
TPC 8. THD vs. Input Frequency



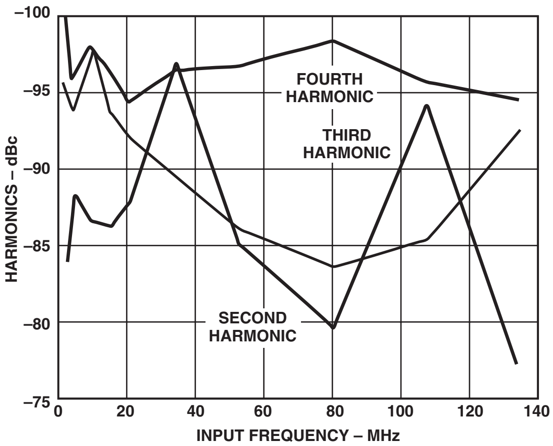
TPC 11. SFDR vs. Input Frequency



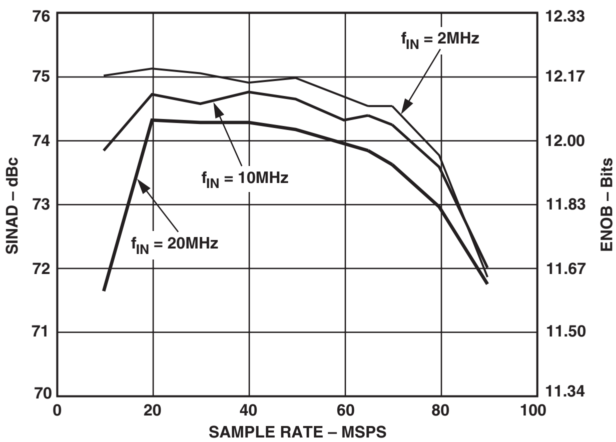
TPC 9. SNR vs. Temperature and Input Frequency



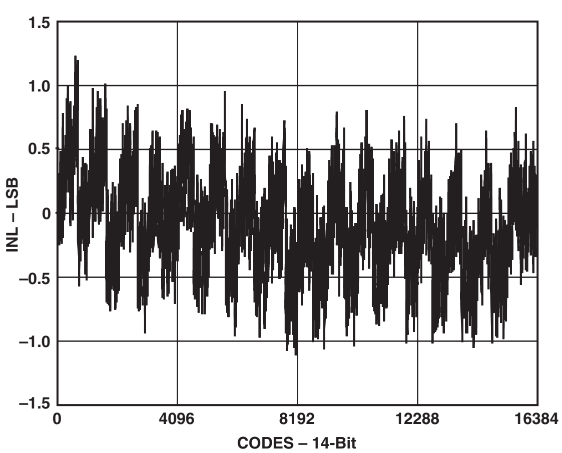
TPC 12. THD vs. Temperature and Input Frequency



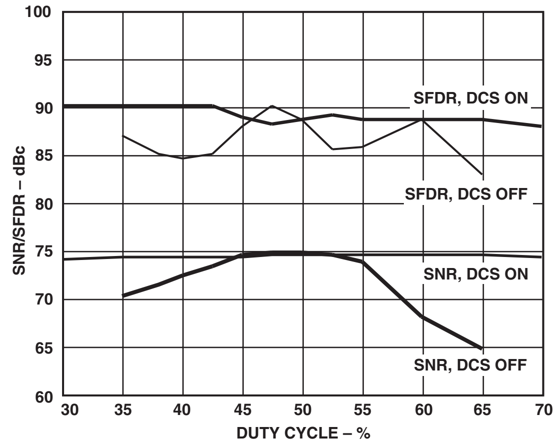
TPC 13. Harmonics vs. Input Frequency



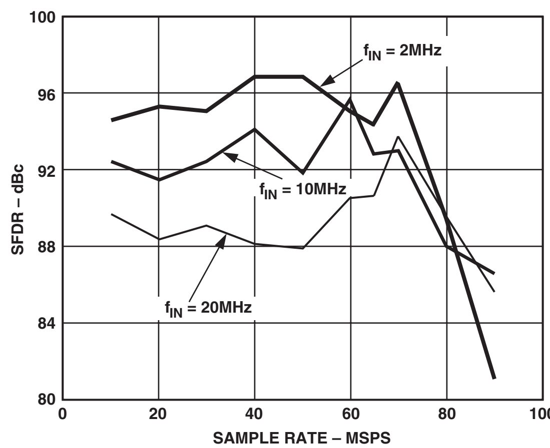
TPC 14. SINAD vs. Sample Rate



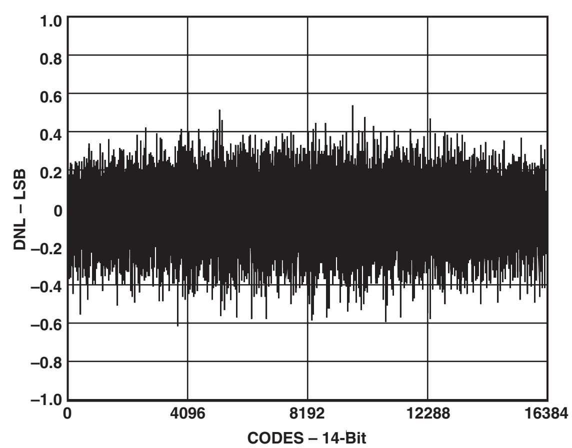
TPC 15. Typical INL



TPC 16. SNR/SFDR vs. Duty Cycle, f_{IN} = 2.5 MHz

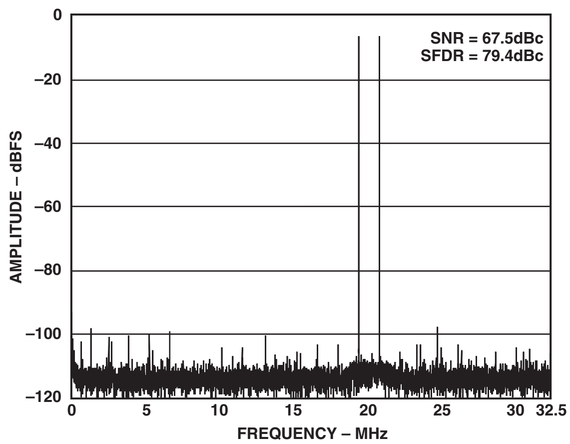


TPC 17. SFDR vs. Sample Rate

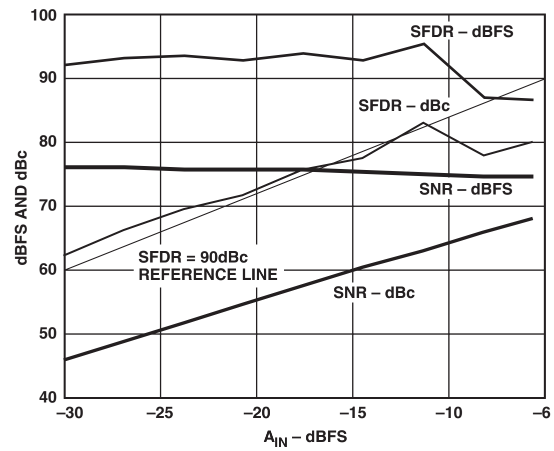


TPC 18. Typical DNL

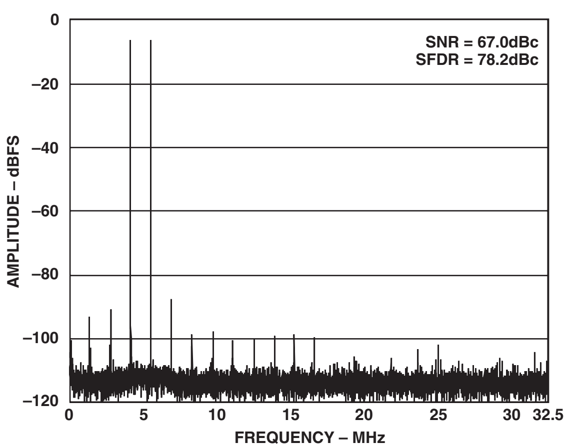
TYPICAL IF SAMPLING PERFORMANCE



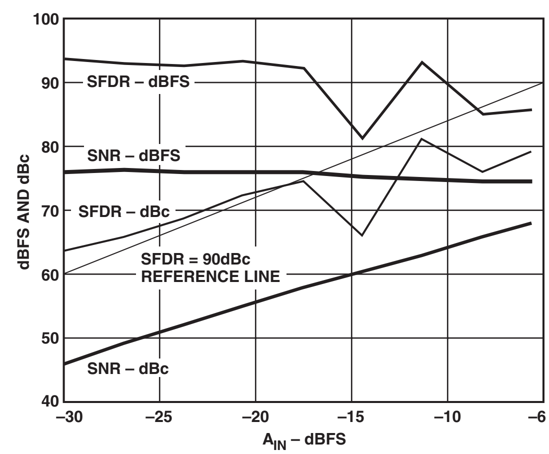
TPC 19. Dual-Tone FFT with f_{IN-1} = 44.2 MHz and f_{IN-2} = 45.6 MHz (A_{IN1} = A_{IN2} = –6.5 dBFS)



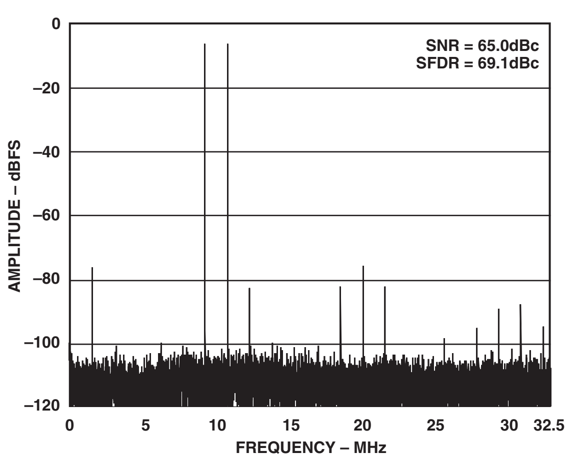
TPC 22. Dual-Tone SNR/SFDR vs. A_{IN} with f_{IN-1} = 44.2 MHz and f_{IN-2} = 45.6 MHz



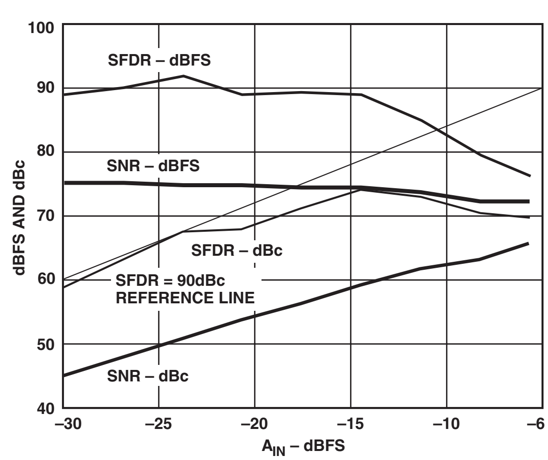
TPC 20. Dual-Tone FFT with f_{IN-1} = 69.2 MHz and f_{IN-2} = 70.6 MHz (A_{IN1} = A_{IN2} = –6.5 dBFS)



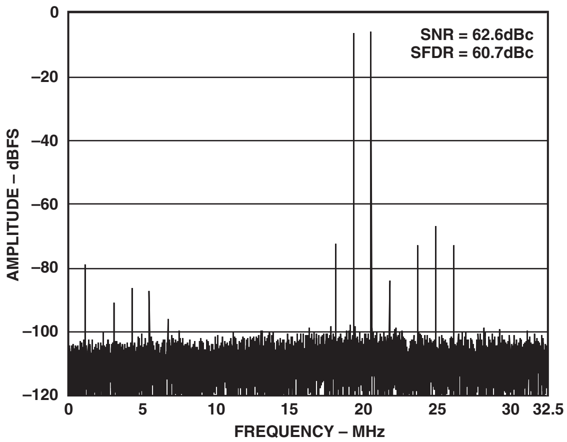
TPC 23. Dual-Tone SNR/SFDR vs. A_{IN} with f_{IN-1} = 69.2 MHz and f_{IN-2} = 70.6 MHz



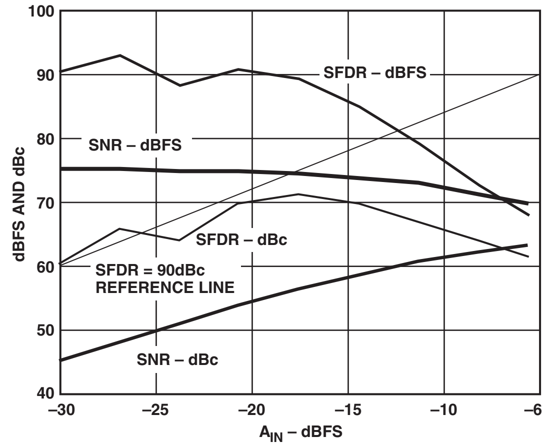
TPC 21. Dual-Tone FFT with f_{IN-1} = 139.2 MHz and f_{IN-2} = 140.7 MHz (A_{IN1} = A_{IN2} = –6.5 dBFS)



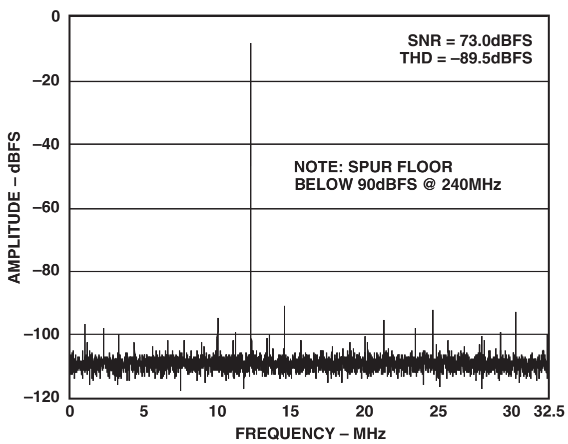
TPC 24. Dual-Tone SNR/SFDR vs. A_{IN} with f_{IN-1} = 139.2 MHz and f_{IN-2} = 140.7 MHz



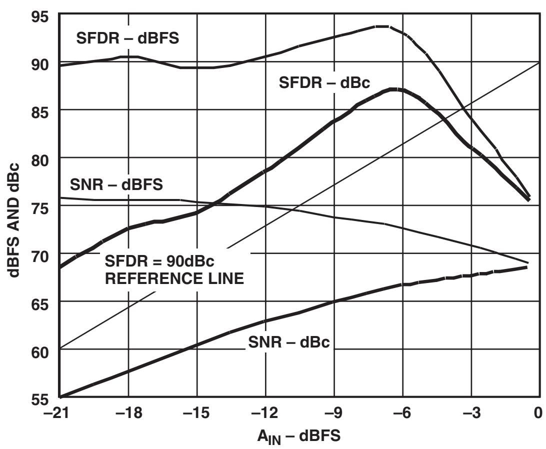
TPC 25. Dual-Tone FFT with f_{IN-1} = 239.1 MHz and f_{IN-2} = 240.7 MHz (A_{IN-1} = A_{IN2} = –6.5 dBFS)



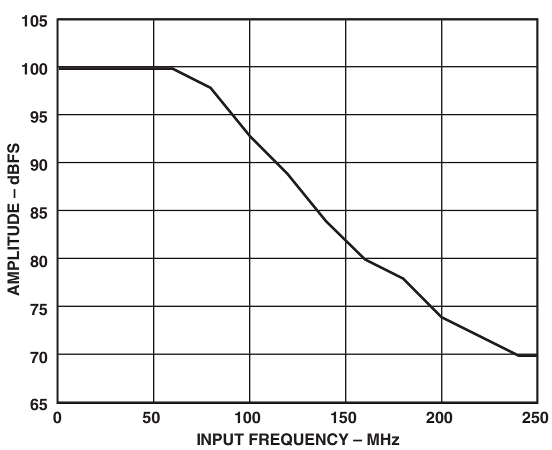
TPC 28. Dual-Tone SNR/SFDR vs. A_{IN} with f_{IN-1} = 239.1 MHz and f_{IN-2} = 240.7 MHz



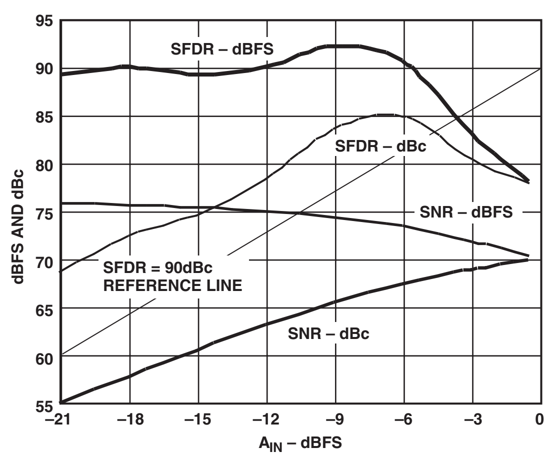
TPC 26. Driving ADC Inputs with Transformer and Balun, f_{IN} = 240 MHz, A_{IN} = –8.5 dBFS



TPC 29. Driving ADC Inputs with Transformer and Balun SNR/SFDR vs. A_{IN}, f_{IN} = 240 MHz



TPC 27. CMRR vs. Input Frequency (A_{IN} = 0 dBFS and CML = 2.5 V)



TPC 30. Driving ADC Inputs with Transformer and Balun SNR/SFDR vs. A_{IN}, f_{IN} = 190 MHz

THEORY OF OPERATION

The AD9244 is a high performance, single-supply 14-bit ADC. In addition to high dynamic range Nyquist sampling, it is designed for excellent IF undersampling performance with an analog input as high as 240 MHz.

The AD9244 uses a calibrated 10-stage pipeline architecture with a patented wideband, input sample-and-hold amplifier (SHA) implemented on a cost-effective CMOS process. Each stage of the pipeline, excluding the last, consists of a low resolution flash ADC along with a switched capacitor DAC and interstage residue amplifier (MDAC). The MDAC amplifies the difference between the reconstructed DAC output and the flash input for the next stage in the pipeline. One bit of redundancy is used in each of the stages to facilitate digital correction of flash errors. The last stage simply consists of a flash ADC.

The pipeline architecture allows a greater throughput rate at the expense of pipeline delay or latency. While the converter captures a new input sample every clock cycle, it takes eight clock cycles for the conversion to be fully processed and appear at the output as illustrated in Figure 1. This latency is not a concern in many applications. The digital output, together with the OTR indicator, is latched into an output buffer to drive the output pins. The output drivers of the AD9244 can be configured to interface with 5 V or 3.3 V logic families.

The AD9244 has a duty clock stabilizer (DCS) that generates its own internal falling edge to create an internal 50% duty cycle clock, independent of the externally applied duty cycle. Control of straight binary or twos complement output format is accomplished with the DFS pin.

The ADC samples the analog input on the rising edge of the clock. While the clock is low, the input SHA is in sample mode. When the clock transitions to a high logic level, the SHA goes into the hold mode. System disturbances just prior to or immediately after the rising edge of the clock and/or excessive clock jitter may cause the SHA to acquire the wrong input value and should be minimized.

ANALOG INPUT AND REFERENCE OVERVIEW

The differential input span of the AD9244 is equal to the potential at the VREF pin. The VREF potential may be obtained from the internal AD9244 reference or an external source.

In differential applications, the center point of the input span is the common-mode level of the input signals. In single-ended applications, the center point is the dc potential applied to one input pin while the signal is applied to the opposite input pin. Figures 3a to 3c show various system configurations.

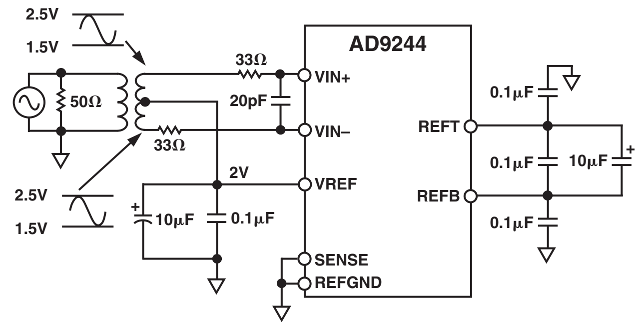


Figure 3a. 2 V p-p Differential Input, Common-Mode Voltage = 2 V

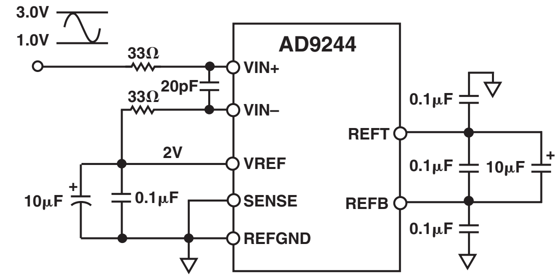


Figure 3b. 2 V p-p Single-Ended Input, Common-Mode Voltage = 2 V

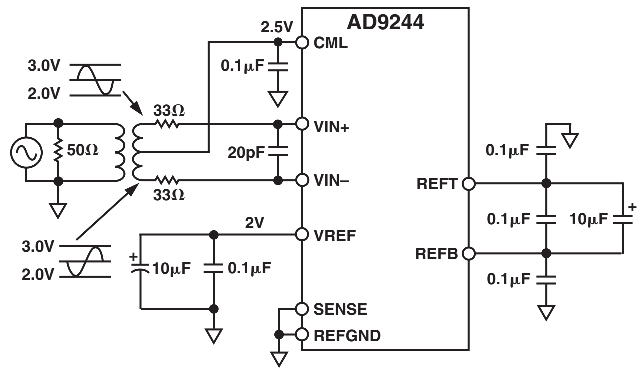


Figure 3c. 2 V p-p Differential Input, Common-Mode Voltage = 2.5 V

Figure 4 is a simplified model of the AD9244 analog input, showing the relationship between the analog inputs, VIN+, VIN–, and the reference voltage, VREF. Note that this is only a symbolic model and that no actual negative voltages exist inside the AD9244. Similar to the voltages applied to the top and bottom of the resistor ladder in a flash ADC, the value VREF/2 defines the minimum and maximum input voltages to the ADC core.

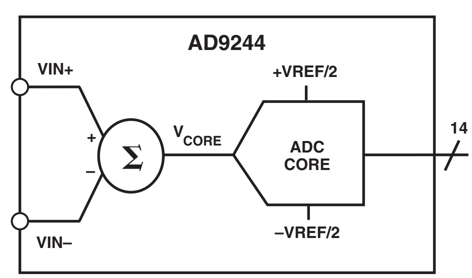


Figure 4. Equivalent Analog Input of AD9244

A differential input structure allows the user to easily configure the inputs for either single-ended or differential operation. The ADC's input structure allows the dc offset of the input signal to be varied independent of the input span of the converter. Specifically, the input to the ADC core can be defined as the difference of the voltages applied at the *VIN+* and *VIN–* input pins. Therefore, the equation

$$V_{CORE} = VIN+ - VIN- \tag{1}$$

defines the output of the differential input stage and provides the input to the ADC core. The voltage, V_{CORE}, must satisfy the condition

$$-VREF/2 < V_{CORE} < VREF/2 \tag{2}$$

where *VREF* is the voltage at the *VREF* pin.

In addition to the limitations placed on the input voltages *VIN+* and *VIN–* by Equations 1 and 2, boundaries on the inputs also exist based on the power supply voltages according to the conditions

$$\begin{aligned} &AGND - 0.3\,V < VIN+ < AVDD + 0.3\,V \\ &AGND - 0.3\,V < VIN- < AVDD + 0.3\,V \end{aligned} \tag{3}$$

where *AGND* is nominally 0 V and *AVDD* is nominally 5 V. The range of valid inputs for *VIN+* and *VIN–* is any combination that satisfies both Equations 2 and 3.

For additional information showing the relationship between *VIN+*, *VIN–*, *VREF,* and the analog input range of the AD9244, see Tables I and II.

ANALOG INPUT OPERATION

Figure 5 shows the equivalent analog input of the AD9244, which consists of a 750 MHz differential SHA. The differential input structure of the SHA is flexible, allowing the device to be configured for either a differential or single-ended input. The analog inputs VIN+ and VIN– are interchangeable, with the exception that reversing the inputs to the VIN+ and VIN– pins results in a data inversion (complementing the output word).

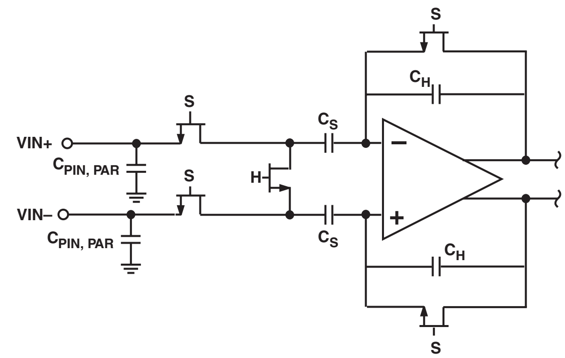


Figure 5. Analog Input of AD9244 SHA

Table I. Analog Input Configuration Summary

Input Connection	Coupling	Input Span (V)	Input Range (V) VIN+*	VIN–*	Input CM Voltage	Comments
Single-Ended	DC or AC	1.0	0.5 to 1.5	1.0	1.0	Best for stepped input response applications.
		2.0	1 to 3	2.0	2.0	Optimum noise performance for single-ended mode, often requires low distortion op amp with VCC > 5 V due to its headroom issues.
Differential	DC or AC	1.0	2.25 to 2.75	2.75 to 2.25	2.5	Optimum full-scale THD and SFDR performance well beyond the ADC's Nyquist frequency.
		2.0	2.0 to 3.0	3.0 to 2.0	2.5	Optimum noise performance for differential mode Preferred mode for applications.

*VIN+ and VIN– can be interchanged if data inversion is required.

Table II. Reference Configuration Summary

Reference Operating Mode	Connect	To	Resulting VREF (V)	Input Span (VIN+ – VIN–) (V p-p)
Internal	SENSE	VREF	1	1
Internal	SENSE	AGND	2	2
Internal	R1	VREF and SENSE	1 ≤ VREF ≤ 2.0	1 ≤ SPAN ≤ 2
	R2	SENSE and REFGND	VREF = (1 + R1/R2)	(SPAN = VREF)
External	SENSE	AVDD	1 ≤ VREF ≤ 2.0	SPAN = EXTERNAL REF
	VREF	EXTERNAL REF		

The optimum noise and dc linearity performance for either differential or single-ended inputs is achieved with the largest input signal voltage span (i.e., 2 V input span) and matched input impedance for VIN+ and VIN–. Only a slight degradation in dc linearity performance exists between the 2 V and 1 V input spans; however, the SNR is lower in the 1 V input span.

When the ADC is driven by an op amp and a capacitive load is switched onto the output of the op amp, the output will momentarily drop due to its effective output impedance. As the output recovers, ringing may occur. To remedy the situation, a series resistor, R_S, can be inserted between the op amp and the SHA input as shown in Figure 6. A shunt capacitance also acts like a charge reservoir, sinking or sourcing the additional charge required by the sampling capacitor, C_S, further reducing current transients seen at the op amp's output.

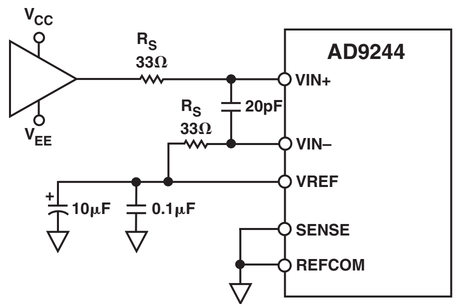


Figure 6. Resistors Isolating SHA Input from Op Amp

The optimum size of this resistor is dependent on several factors, including the ADC sampling rate, the selected op amp, and the particular application. In most applications, a 30 Ω to 100 Ω resistor is sufficient.

For noise sensitive applications, the very high bandwidth of the AD9244 may be detrimental and the addition of a series resistor and/or shunt capacitor can help limit the wideband noise at the ADC's input by forming a low-pass filter. The source impedance driving VIN+ and VIN– should be matched. Failure to provide matching may result in degradation of the SNR, THD, and SFDR performance.

Differentially Driving the Analog Inputs

The AD9244 has a very flexible input structure, allowing it to interface with single-ended or differential inputs.

The optimum mode of operation, analog input range, and associated interface circuitry will be determined by the particular application's performance requirements as well as power supply options.

Differential operation requires that VIN+ and VIN– be simultaneously driven with two equal signals that are 180° out of phase with each other.

Differential modes of operation (ac-coupled or dc-coupled input) provide the best SFDR performance over a wide frequency range. They should be considered for the most demanding spectral-based applications (i.e., direct IF conversion to digital).

Since not all applications have a signal precondition for differential operation, there is often a need to perform a single-ended-to-differential conversion. In systems that do not require dc coupling, an RF transformer with a center tap is the best method for generating differential input signals for the AD9244. This provides the benefit of operating the ADC in the differential mode without contributing additional noise or distortion. An RF transformer also has the added benefit of providing electrical isolation between the signal source and the ADC.

The differential input characterization for this data sheet was performed using the configuration in Figure 7. The circuit uses a Mini-Circuits® RF transformer, model T1–1T, which has an impedance ratio of 1:1. This circuit assumes that the signal source has a 50 Ω source impedance. The secondary center tap of the transformer allows a dc common-mode voltage to be added to the differential input signal. In Figure 7, the center tap is connected to a resistor divider providing a half supply voltage. It could also be connected to the CML pin of the AD9244. It is recommended for IF sampling applications (70 MHz < f_{IN} < 200 MHz) that the 20 pF differential capacitor between VIN+ and VIN– be reduced or removed.

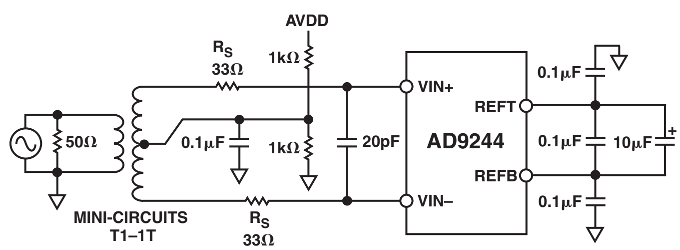


Figure 7. Transformer-Coupled Input

The circuit shown in Figure 8 shows a method for applying a differential direct-coupled signal to the AD9244. An AD8138 amplifier is used to derive a differential signal from a single-ended signal.

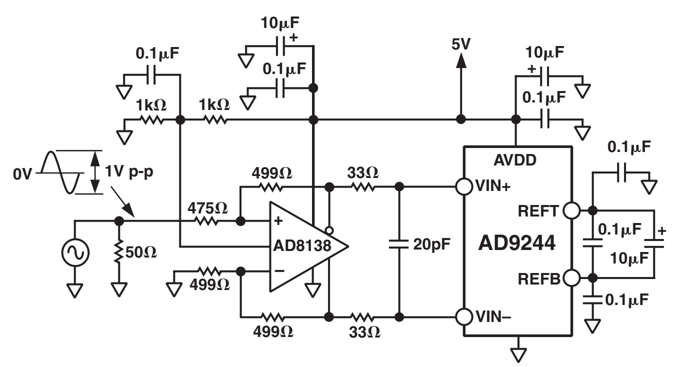


Figure 8. Direct-Coupled Drive Circuit with AD8138 Differential Op Amp

REFERENCE OPERATION

The AD9244 contains a band gap reference that provides a pin-strappable option to generate either a 1 V or 2 V output. With the addition of two external resistors, the user can generate reference voltages between 1 V and 2 V. Another alternative is to use an external reference for designs requiring enhanced accuracy and/or drift performance as described later in this section. Figure 9a shows a simplified model of the internal voltage reference of the AD9244. A reference amplifier buffers a 1 V fixed reference. The output from the reference amplifier, A1, appears on the VREF pin. As stated earlier, the voltage on the VREF pin determines the full-scale differential input span of the ADC.

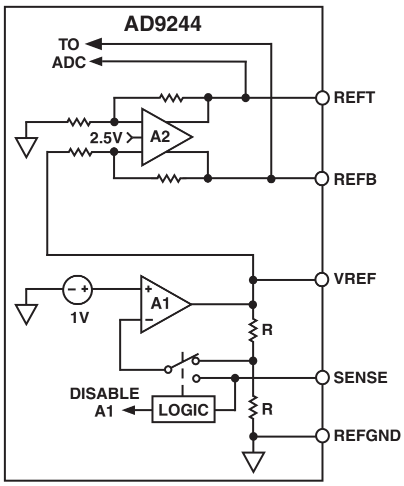


Figure 9a. Equivalent Reference Circuit

The voltage appearing at the VREF pin and the state of the internal reference amplifier, A1, are determined by the voltage present at the SENSE pin. The logic circuitry contains comparators that monitor the voltage at the SENSE pin. The various reference modes are summarized in Table II and are described in the next few sections.

The actual reference voltages used by the internal circuitry of the AD9244 appear on the REFT and REFB pins. The voltages on these pins are symmetrical about midsupply or CML. For proper operation, it is necessary to add a capacitor network to decouple these pins. Figure 9b shows the recommended decoupling network. The turn-on time of the reference voltage appearing between REFT and REFB is approximately 10 ms and should be taken into consideration in any power-down mode of operation. The VREF pin should be bypassed to the REFGND pin with a 10 µF tantalum capacitor in parallel with a low inductance 0.1 µF ceramic capacitor.

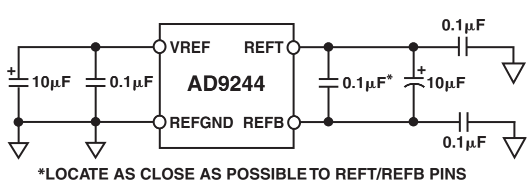


Figure 9b. Reference Decoupling

Pin Programmable Reference

By shorting the VREF pin directly to the SENSE pin, the internal reference amplifier is placed in a unity gain mode and the resulting VREF output is 1 V. By shorting the SENSE pin directly to the REFGND pin, the internal reference amplifier is configured for a gain of 2.0 and the resulting VREF output is 2.0 V.

Resistor Programmable Reference

Figure 10 shows an example of how to generate a reference voltage other than 1.0 V or 2.0 V with the addition of two external resistors. Use the equation

$$VREF = 1\ \ V \times \left(1 + R1/R2\right)$$

to determine the appropriate values for $R1$ and $R2$. These resistors should be in the 2 kΩ to 10 kΩ range. For the example shown, $R1$ equals 2.5 kΩ and $R2$ equals 5 kΩ. From the equation above, the resulting reference voltage on the VREF pin is 1.5 V. This sets the differential input span to 1.5 V p-p. The midscale voltage can also be set to VREF by connecting VIN– to VREF.

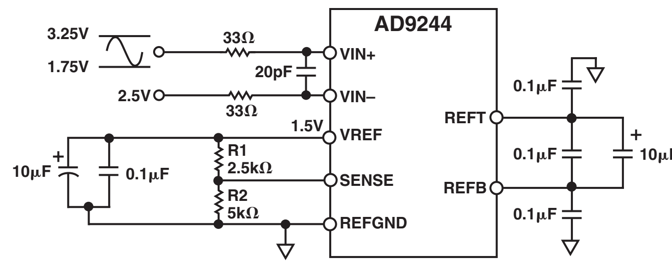


Figure 10. Resistor Programmable Reference (1.5 V p-p Input Span, Differential Input with VCM = 2.5 V)

Using an External Reference

To use an external reference, the internal reference must be disabled by connecting the SENSE pin to AVDD. The AD9244 contains an internal reference buffer, A2 (see Figure 9a), that simplifies the drive requirements of an external reference. The external reference must be able to drive a 5 kΩ (±20%) load. The bandwidth of the reference is deliberately left small to minimize the reference noise contribution. As a result, it is not possible to drive VREF externally with high frequencies.

Figure 11 shows an example of an external reference driving both VIN– and VREF. In this case, both the common-mode voltage and input span are directly dependent on the value of VREF. Both the input span and the center of the input span are equal to the external VREF. Thus the valid input range extends from (VREF + VREF/2) to (VREF – VREF/2). For example, if the precision reference part, REF191, a 2.048 V external reference, is used, the input span is 2.048 V. In this case, 1 LSB of the AD9244 corresponds to 0.125 mV. It is essential that a minimum of a 10 µF capacitor, in parallel with a 0.1 µF low inductance ceramic capacitor, decouple the reference output to AGND.

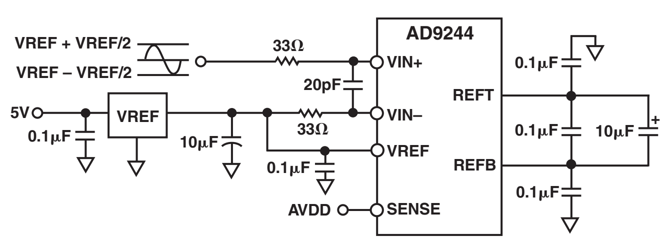


Figure 11. Using an External Reference

Table III. Output Data Format

Input (V)	Condition (V)	Binary Output Mode	Twos Complement Mode	OTR
VIN+ – VIN–	< –VREF – 0.5 LSB	00 0000 0000 0000	10 0000 0000 0000	1
VIN+ – VIN–	= –VREF	00 0000 0000 0000	10 0000 0000 0000	0
VIN+ – VIN–	= 0	10 0000 0000 0000	00 0000 0000 0000	0
VIN+ – VIN–	= +VREF – 1.0 LSB	11 1111 1111 1111	01 1111 1111 1111	0
VIN+ – VIN–	> +VREF – 0.5 LSB	11 1111 1111 1111	01 1111 1111 1111	1

DIGITAL INPUTS AND OUTPUTS

Digital Outputs

Table III details the relationship among the ADC input, OTR, and digital output format.

Data Format Select (DFS)

The AD9244 may be programmed for straight binary or twos complement data on the digital outputs. Connect the DFS pin to AGND for straight binary and to AVDD for twos complement.

Digital Output Driver Considerations

The AD9244 output drivers can be configured to interface with 5 V or 3.3 V logic families by setting DRVDD to 5 V or 3.3 V, respectively. The output drivers are sized to provide sufficient output current to drive a wide variety of logic families. However, large drive currents tend to cause glitches on the supplies and may affect converter performance. Applications requiring the ADC to drive large capacitive loads or large fanouts may require external buffers or latches.

Out-of-Range (OTR)

An out-of-range condition exists when the analog input voltage is beyond the input range of the ADC. OTR is a digital output that is updated along with the data output corresponding to the particular sampled input voltage. Thus, OTR has the same pipeline latency as the digital data. OTR is low when the analog input voltage is within the analog input range and high when the analog input voltage exceeds the input range as shown in Figure 12. OTR will remain high until the analog input returns to within the input range and another conversion is completed. By logically AND-ing OTR with the MSB and its complement, overrange high or underrange low conditions can be detected. Table IV is a truth table for the overrange/underrange range circuit in Figure 13, which uses NAND gates. Systems requiring programmable gain conditioning of the AD9244 can, after eight clock cycles, detect an out-of-range condition, thus eliminating gain selection iterations. Also, OTR can be used for digital offset and gain calibration.

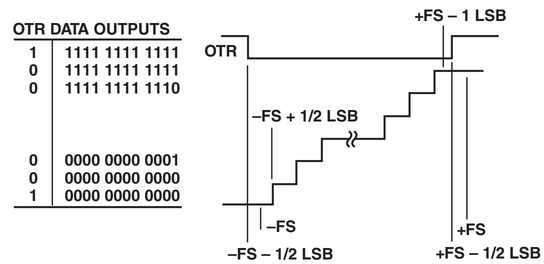


Figure 12. OTR Relation to Input Voltage and Output Data

Table IV. Output Data Format

OTR	MSB	Analog Input Is
0	0	Within Range
0	1	Within Range
1	0	Underrange
1	1	Overrange

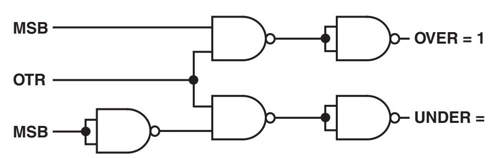


Figure 13. Overrange/Underrange Logic

Digital Output Enable Function (OEB)

The AD9244 has three-state ability. If the OEB pin is low, the output data drivers are enabled. If the OEB pin is high, the output data drivers are placed in a high impedance state. It is not intended for rapid access to the data bus. Note that OEB is referenced to the digital supplies (DRVDD) and should not exceed that supply voltage.

CLOCK OVERVIEW

The AD9244 has a flexible clock interface that accepts either a single-ended or differential clock. An internal bias voltage facilitates ac coupling using two external capacitors. To remain backward compatible with the single-pin clock scheme of the AD9226, the AD9244 can be operated with a dc-coupled, single-pin clock by grounding the CLK– pin and driving CLK+.

When the CLK– pin is not grounded, the CLK+ and CLK– pins function as a differential clock receiver. When CLK+ is greater than CLK–, the SHA is in hold mode; when CLK+ is less than CLK–, the SHA is in track mode (see timing in Figure 14). The rising edge of the clock (CLK+ – CLK–) switches the SHA from track to hold and timing jitter on this transition should be minimized, especially for high frequency analog inputs.

It is often difficult to maintain a 50% duty cycle to the ADC, especially when driving the clock with a single-ended or sine wave input. To ease the constraint of providing an accurate 50% clock, the ADC has an optional internal duty cycle stabilizer (DCS) that allows the rising clock edge to pass through with minimal jitter and interpolates the falling edge, independent of the input clock falling edge. The DCS is described in greater detail in a later section.

Clock Input Modes

Figures 15a to 15e illustrate the modes of operation of the clock receiver. Figure 15a shows a differential clock directly coupled to CLK+ and CLK–. In this mode, the common mode of the CLK+ and CLK– signals should be close to 1.6 V. Figure 15b illustrates a single-ended clock input. The capacitor decouples the internal bias voltage on the CLK– pin (about 1.6 V), establishing a threshold for the CLK+ pin. Figure 15c provides backward compatibility with the AD9226. In this mode, CLK– is grounded and the threshold for CLK+ is 1.5 V. Figure 15d shows a differential clock ac-coupled by connecting through two capacitors. AC coupling a single-ended clock can also be accomplished using the circuit in Figure 15e.

When using the differential clock circuits of Figure 15a or Figure 15d, if CLK– drops below 250 mV, the mode of the clock receiver may change, causing conversion errors. It is essential that CLK– remain above 250 mV when the clock is ac-coupled or dc-coupled.

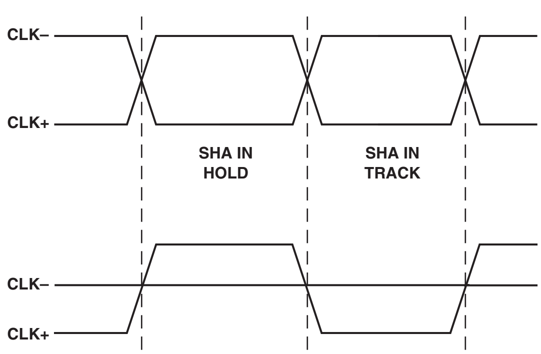


Figure 14. SHA Timing

Clock Input Considerations

The analog input is sampled on the rising edge of the clock. Timing variations, or jitter, on this edge causes the sampled input voltage to be in error by an amount proportional to the slew rate of the input signal and to the amount of the timing variation. Thus, to maintain the excellent high frequency SFDR and SNR characteristics of the AD9244, it is essential that the clock edge be kept as clean as possible.

The clock should be treated like an analog signal. Clock drivers should not share supplies with digital logic or noisy circuits. The clock traces should not run parallel to noisy traces. Using a pair of symmetrically routed, differential clock signals can help to provide immunity from common-mode noise coupled from the environment.

The clock receiver functions like a differential comparator. At the CLK inputs, a slowly changing clock signal will result in more jitter than a rapidly changing one. Driving the clock with a low amplitude sine wave input is not recommended. Running a high speed clock through a divider circuit will provide a fast rise/fall time, resulting in the lowest jitter in most systems.

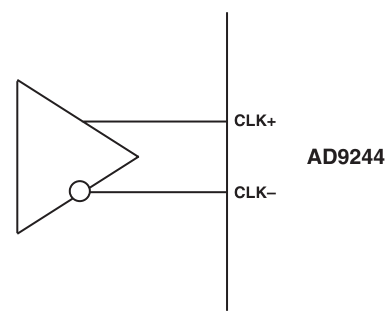


Figure 15a. Differential Clock Input—DC-Coupled

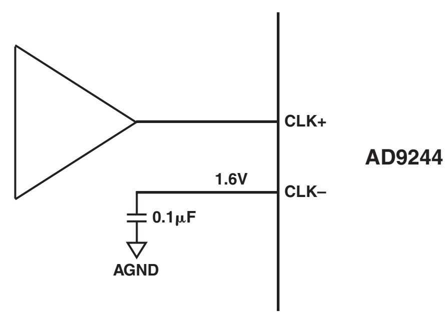


Figure 15b. Single-Ended Clock Input—DC-Coupled

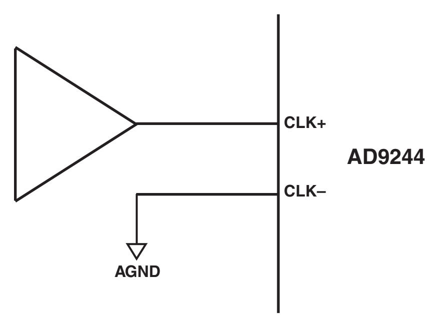


Figure 15c. Single-Ended Input—Retains Pin Compatibility with AD9226

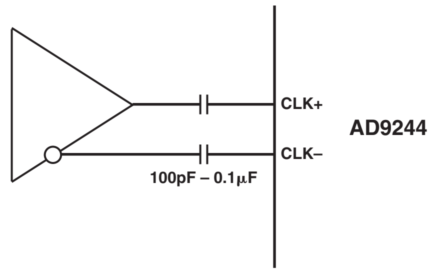


Figure 15d. Differential Clock Input—AC-Coupled

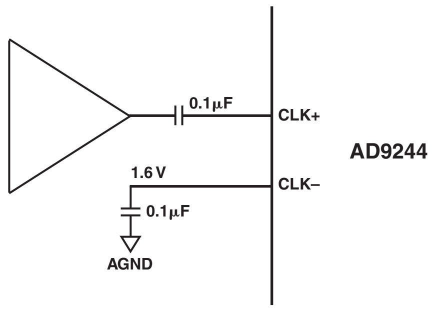


Figure 15e. Single-Ended Clock Input—AC-Coupled

Clock Power Dissipation

Most of the power dissipated by the AD9244 is from the analog power supplies. However, lower clock speeds will reduce digital supply current. Figure 16 shows the relationship between power and clock rate.

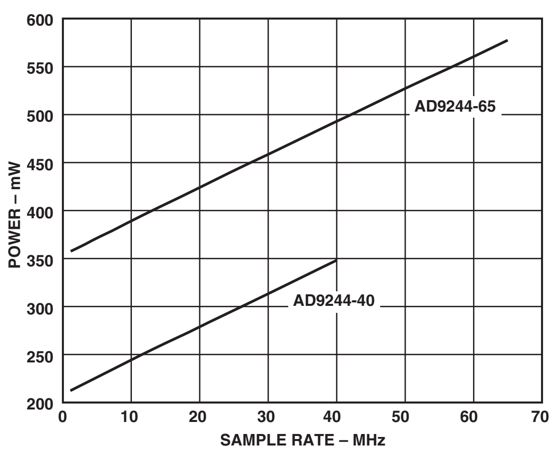


Figure 16. Power Consumption vs. Sample Rate

Clock Stabilizer (DCS)

The clock stabilizer circuit in the AD9244 desensitizes the ADC from clock duty cycle variations. System clock constraints are eased by internally restoring the clock duty cycle to 50%, independent of the clock input duty cycle. Low jitter on the rising edge (sampling edge) of the clock is preserved while the falling edge is generated on-chip.

It may be desirable to disable the clock stabilizer and may be necessary when the clock frequency is varied or completely stopped. Note that stopping the clock is not recommended with ac-coupled clocks. Once the clock frequency is changed, over 100 clock cycles may be required for the clock stabilizer to settle to the new speed. When the stabilizer is disabled, the internal switching will be directly affected by the clock state. If CLK+ is high, the SHA will be in hold mode; if CLK+ is low, the SHA will be in track mode. TPC 16 shows the benefits of using the clock stabilizer. Connecting the DCS pin to AVDD implements the internal clock stabilization function in the AD9244. If the DCS pin is connected to ground, the AD9244 will use both edges of the external clock in its internal timing circuitry (see Specifications for timing requirements).

GROUNDING AND DECOUPLING

Analog and Digital Grounding

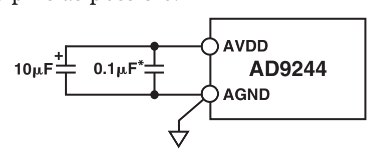
Proper grounding is essential in high speed, high resolution systems. Multilayer printed circuit boards (PCBs) are recommended to provide optimal grounding and power distribution. The use of power and ground planes offers distinct advantages, including:

- The minimization of the loop area encompassed by a signal and its return path.
- The minimization of the impedance associated with ground and power paths.
- The inherent distributed capacitor formed by the power plane, PCB material, and ground plane.

It is important to design a layout that minimizes noise from coupling onto the input signal. Digital input signals should not be run in parallel with input signal traces and should be routed away from the input circuitry. While the AD9244 features separate analog and digital ground pins, it should be treated as an analog component. The AGND and DGND pins must be joined together directly under the AD9244. A solid ground plane under the ADC is acceptable if the power and ground return currents are carefully managed.

Analog Supply Decoupling

The AD9244 features separate analog and digital supply and ground circuits, helping to minimize digital corruption of sensitive analog signals. In general, AVDD (analog power) should be decoupled to AGND (analog ground). The AVDD and AGND pins are adjacent to one another. Figure 17 shows the recommended decoupling for each pair of analog supplies; 0.1 µF ceramic chip and 10 µF tantalum capacitors should provide adequately low impedance over a wide frequency range. The decoupling capacitors (especially 0.1 µF) should be located as close to the pins as possible.



*LOCATE AS CLOSE AS POSSIBLE TO SUPPLY PINS

Figure 17. Analog Supply Decoupling

Digital Supply Decoupling

The digital activity on the AD9244 falls into two categories: correction logic and output drivers. The internal correction logic draws relatively small surges of current, mainly during the clock transitions. The output drivers draw large current impulses when the output bits change state. The size and duration of these currents are a function of the load on the output bits; large capacitive loads should be avoided.

For the digital decoupling shown in Figure 18, 0.1 µF ceramic chip and 10 µF tantalum capacitors are appropriate. The decoupling capacitors (especially 0.1 µF) should be located as close to the pins as possible. Reasonable capacitive loads on the data pins are less than 20 pF per bit. Applications involving greater digital loads should consider increasing the digital decoupling and/or using external buffers/latches.

A complete decoupling scheme will also include large tantalum or electrolytic capacitors on the power supply connector to reduce low frequency ripple to insignificant levels.

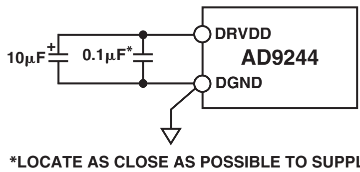


Figure 18. Digital Supply Decoupling

CML

The AD9244 has a midsupply reference point. This is used within the internal architecture of the AD9244 and must be decoupled with a 0.1 µF capacitor. It will source or sink a load of up to 300 µA. If more current is required, the CML pin should be buffered with an amplifier.

VR

VR is an internal bias point on the AD9244. It must be decoupled to AGND with a 0.1 µF capacitor.

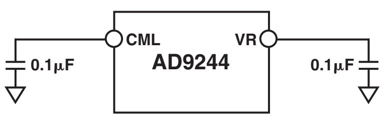


Figure 19. CML/VR Decoupling

EVALUATION BOARD

Analog Input Configuration

Table V provides a summary of the analog input configuration. The analog inputs of the AD9244 on the evaluation board can be driven differentially through a transformer via Connector S4, or the AD8138 amplifier via Connector S2, or driven single-ended directly via Connector S3. When using the transformer or AD8138 amplifier, a single-ended source may be used as both of these devices are configured on the AD9244 evaluation board to convert from single-ended signals to differential. Optimal AD9244 performance is achieved above 500 kHz by using the input transformer. To drive the AD9244 via the transformer, connect solderable Jumpers JP45 and JP46. DC bias is provided by the Resistors R8 and R28. The evaluation board has positions for through-hole and surface-mount transformers. For applications requiring lower frequencies or dc applications, the AD8138 can be used. The AD8138 will provide good distortion and noise performance, as well as input buffering, up to 30 MHz. For more information, refer to the AD8138 data sheet. To use the AD8138 to drive the AD9244, remove the transformer (T1 or T4) and connect solderable Jumpers JP42 and JP43. The AD9244 can be driven single-ended directly via S3 and can be ac-coupled or dc-coupled by removing or inserting JP5. To run the evaluation board in this way, remove the transformer (T1 or T4) and connect solderable Jumpers JP40 and JP41. The Resistors R40, R41, R8, and R28 are used to bias the AD9244 inputs to the correct common-mode levels in this application.

Reference Configuration

As described in the Analog Input and Reference Overview section earlier in this data sheet, the AD9244 can be configured to use its own internal or an external reference. An external reference, D3, and reference buffer, U5, are included on the AD9244 evaluation board. Jumpers JP8 and JP22–JP24 can be used to select the desired reference configuration (Table VI).

Clock Configuration

The AD9244 evaluation board was designed to achieve optimal performance as well as to be easily configurable by the user. To configure the clock input, begin by connecting the correct combination of solderable Jumpers JP11–JP15 (Table VII). The specific jumper configuration is dependent on the application and can be determined by referring to the clock input modes section. If the differential clock input mode is selected, an external sine wave generator applied to S5 can be used as the clock source. The clock buffer/drive MC10EL16 from ON Semiconductor is used on the evaluation board to buffer and square the clock input. If the single-ended clock configuration is used, an external clock source can be applied to S1.

The AD9244 evaluation board generates a buffered clock at TTL/CMOS levels for use with a data capture system, such as the HSC-ADC-EVAL-SC system. The clock buffering is provided by U4 and U7 and is configured by Jumpers JP3, JP4, JP9, and JP18 (Table VII).

Table V. Analog Input Jumper Configuration

	Input Connector	Jumpers	Notes
Differential: Transformer	S4	45, 46	R8, R28 Provide DC Bias. Optimal for 500 kHz+.
Differential: Amplifier	S2	42, 43	Remove T1 or T4. Used for low input frequencies.
Single-Ended	S3	5, 40, 41	Remove T1 or T4. JP5: connected for dc-coupled, not connected for ac-coupling.

Table VI. Reference Jumper Configuration

Reference	Voltage	Jumpers	Notes
Internal	2 V	23	JP8 Not Connected.
Internal	1 V	24	JP8 Not Connected.
Internal	1 V ≤ VREF ≤ 2 V	25	JP8 Not Connected. VREF = 1 + R1/R2.
External	1 V ≤ VREF ≤ 2 V	8, 22	Set VREF with R26.

Table VII. Clock Jumper Configuration

	Input Connector	Jumpers
DUT Clock		
Differential	S5	11, 13
Single-Ended	S1	12, 15
Data Capture Clock		
Internal		
Diff DUT Clock	NA	9, 18A
SE DUT Clock	NA	9, 18B
External	S6	3 or 4

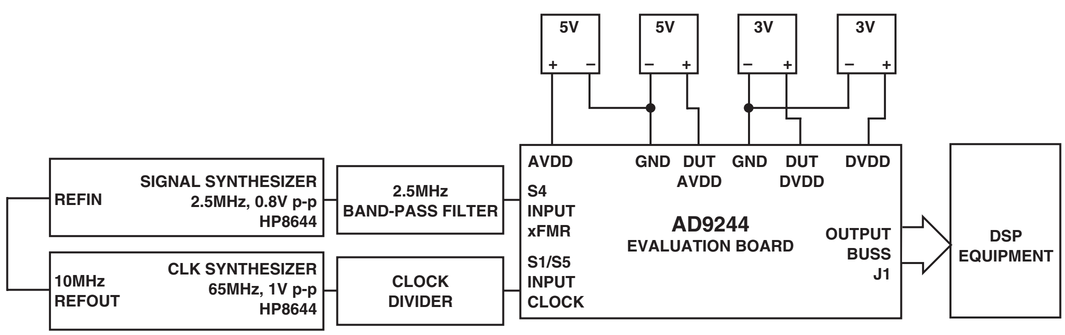


Figure 20. Evaluation Board Connections

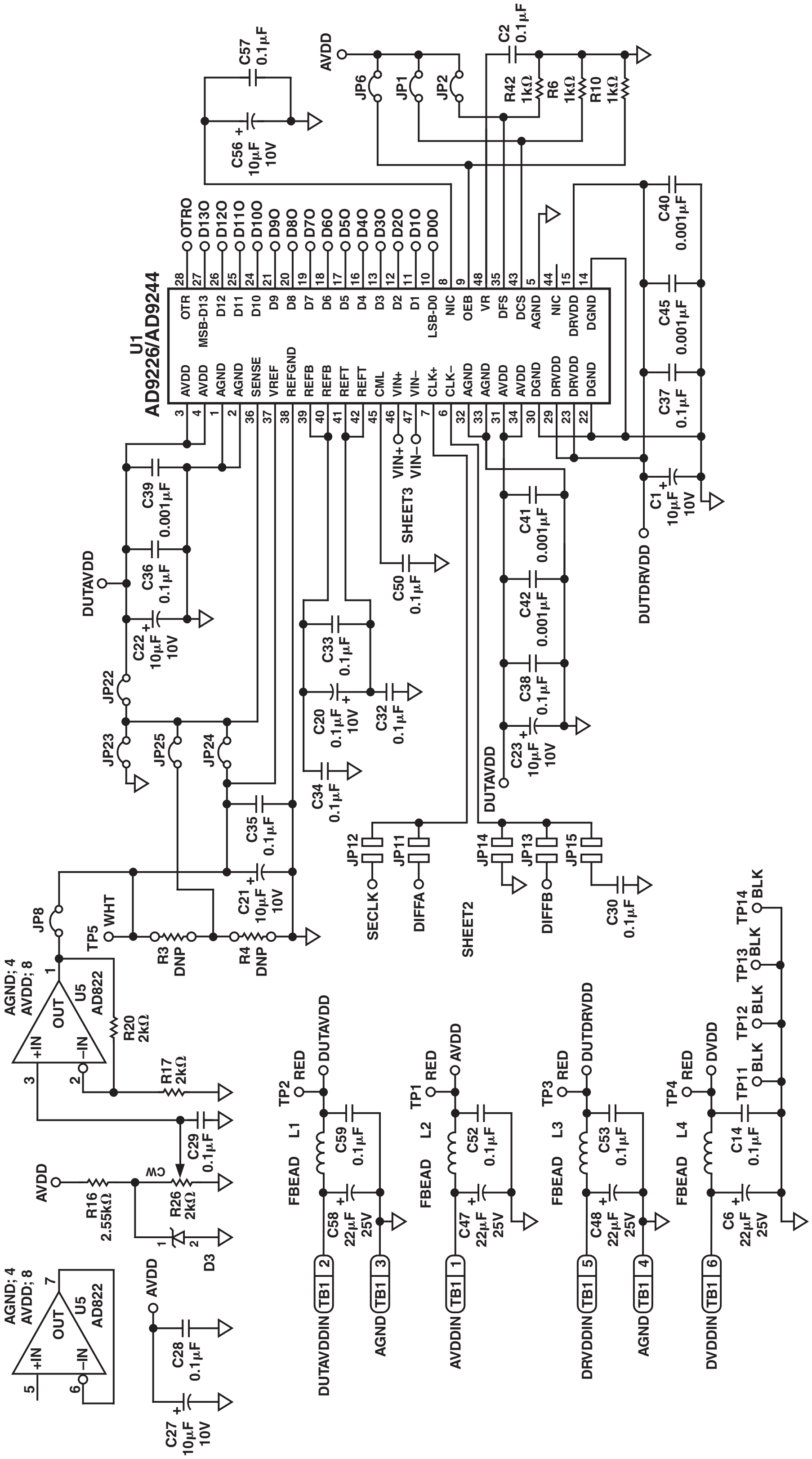


Figure 21. AD9244 Evaluation Board, ADC, External Reference, and Power Supply Circuitry

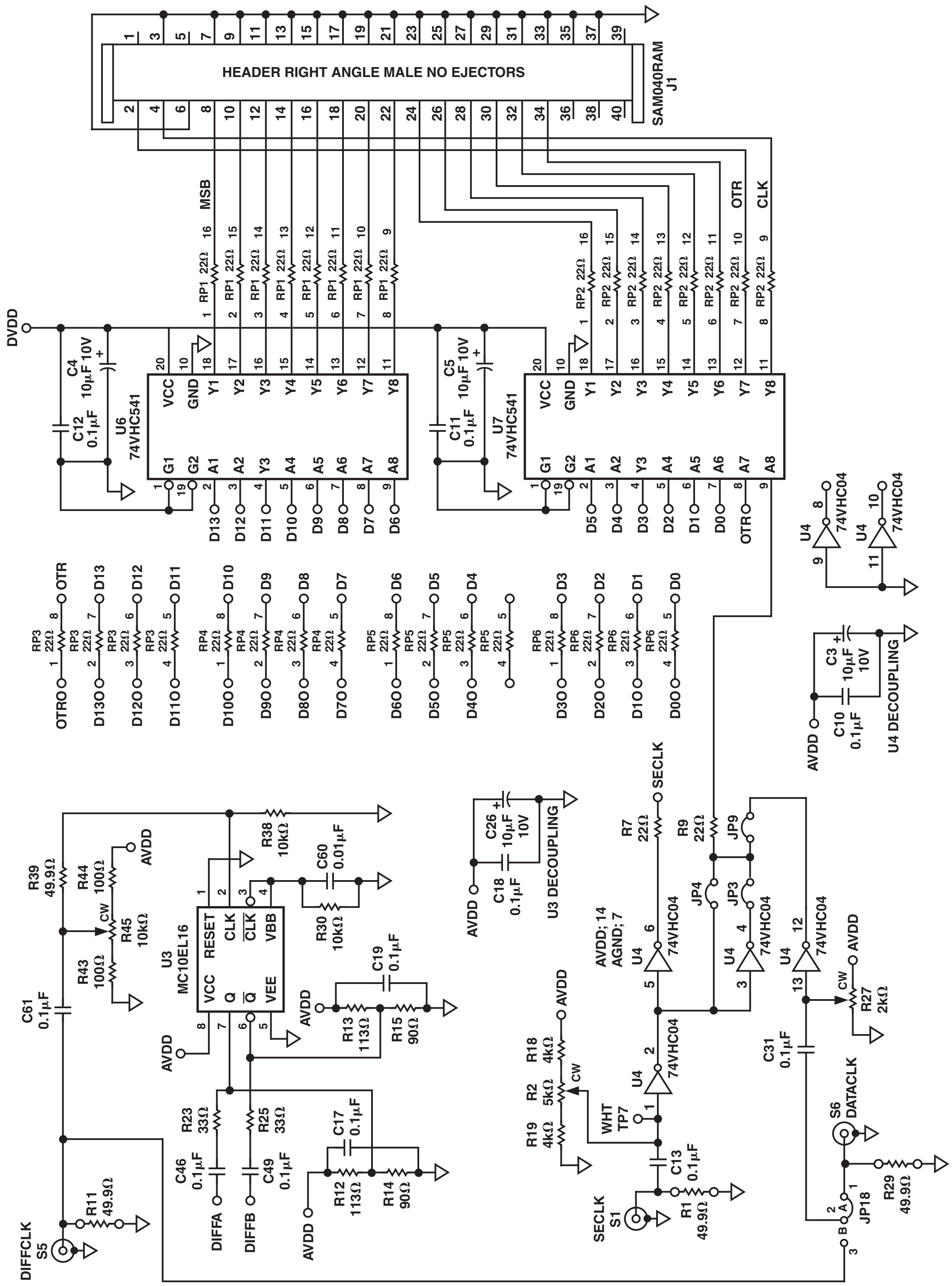


Figure 22. AD9244 Evaluation Board, Clock Input, and Digital Output Buffer Circuitry

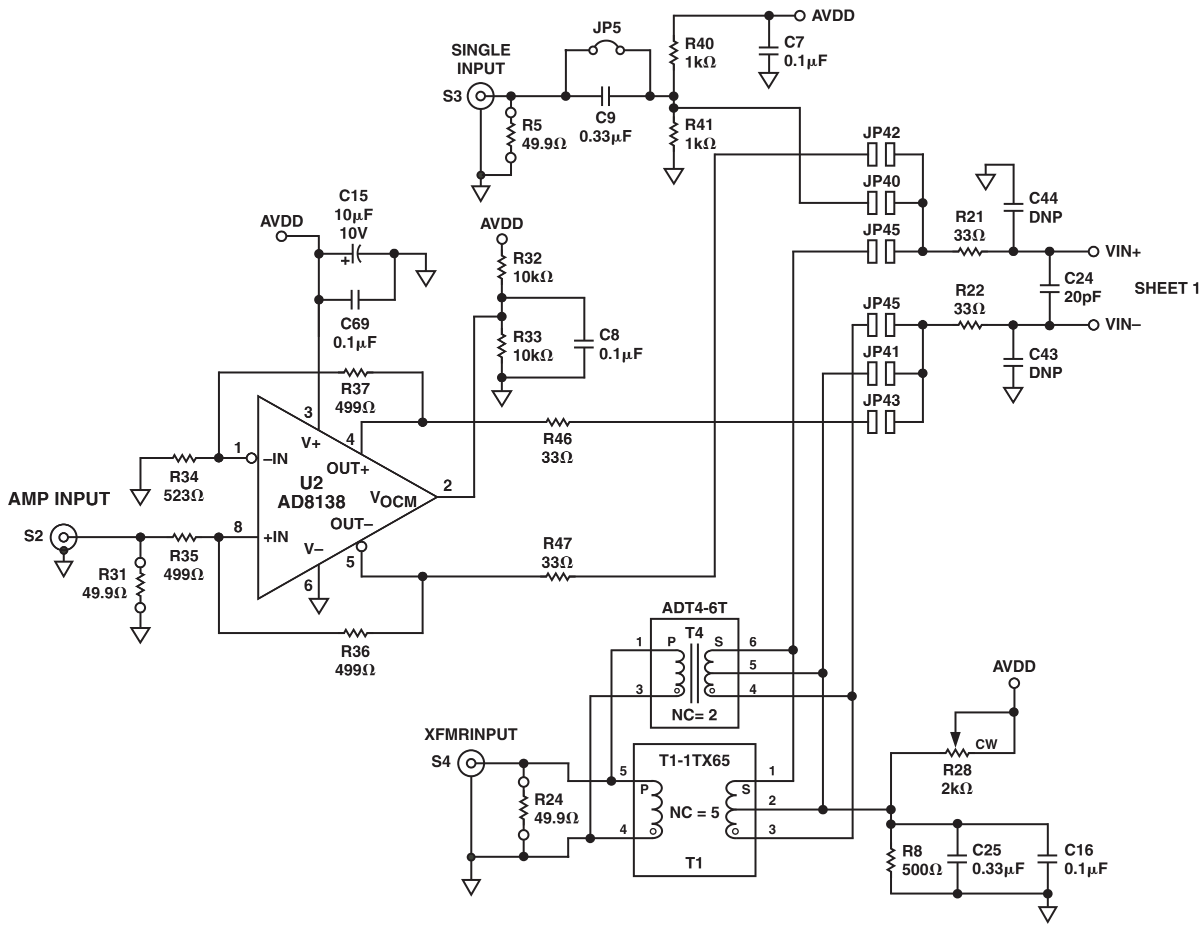


Figure 23. AD9244 Evaluation Board, Analog Input Circuitry

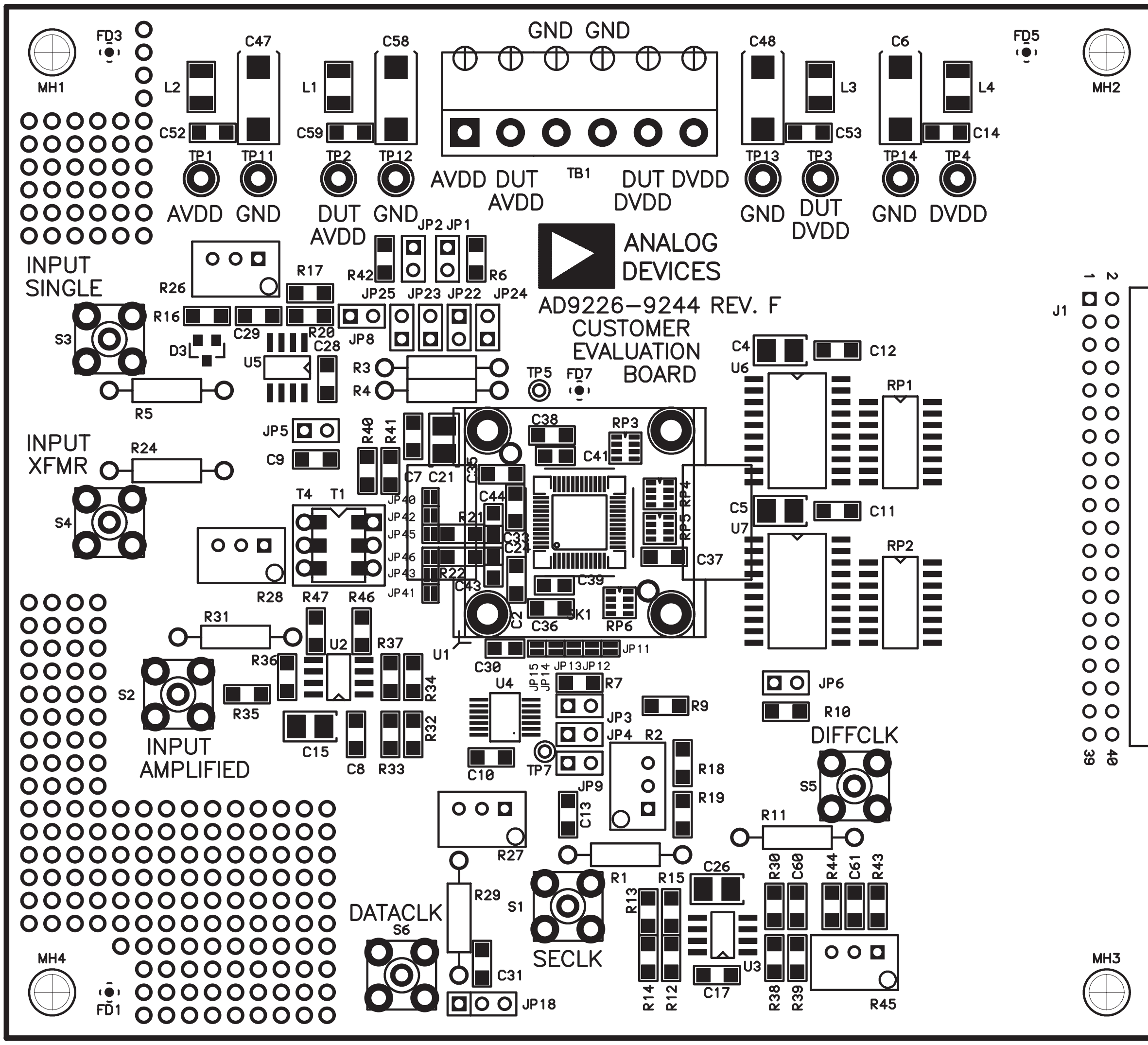


Figure 24. AD9244 Evaluation Board, PCB Assembly, Top

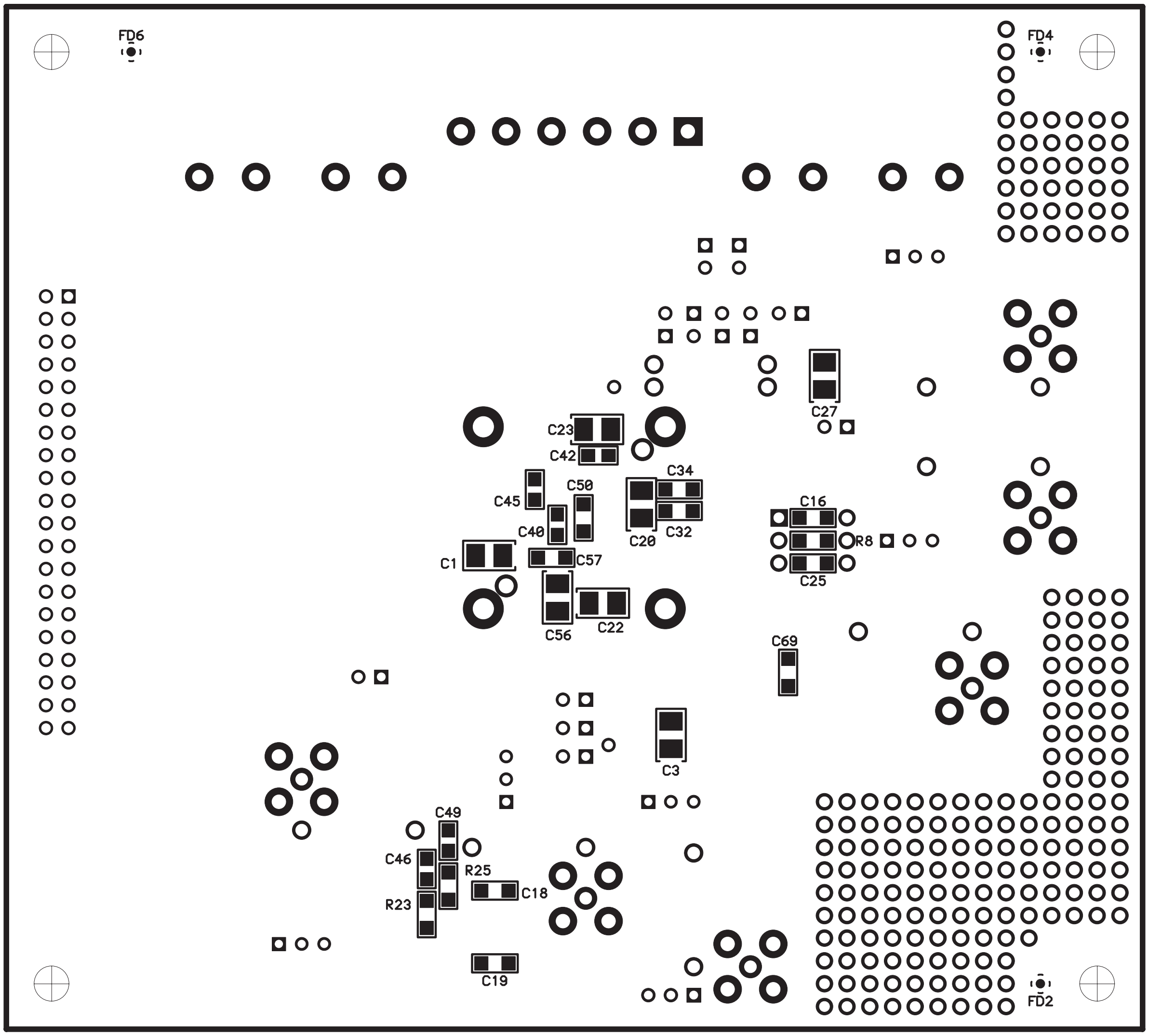


Figure 25. AD9244 Evaluation Board, PCB Assembly, Bottom

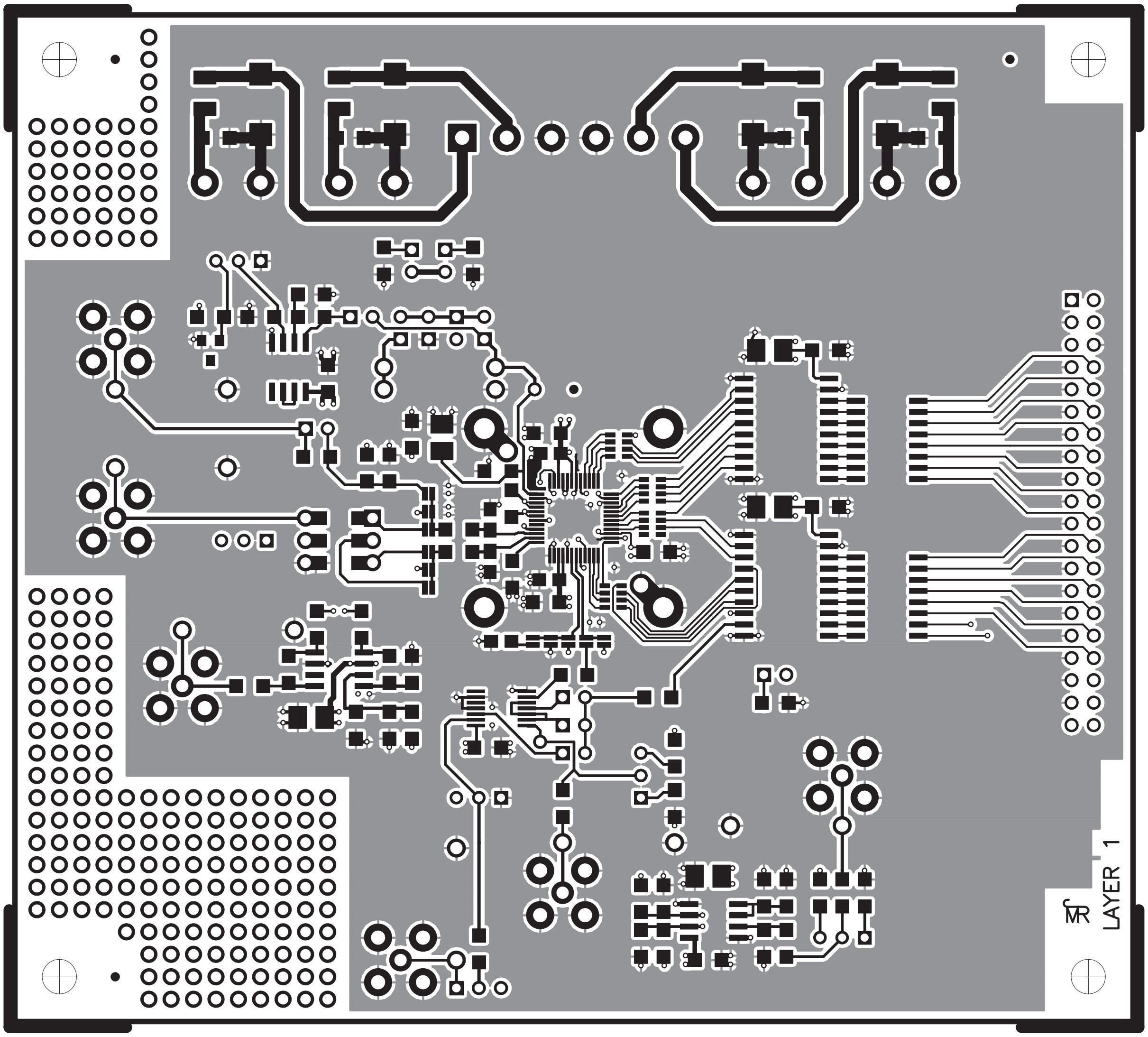


Figure 26. AD9244 Evaluation Board, PCB Layer 1 (Top)

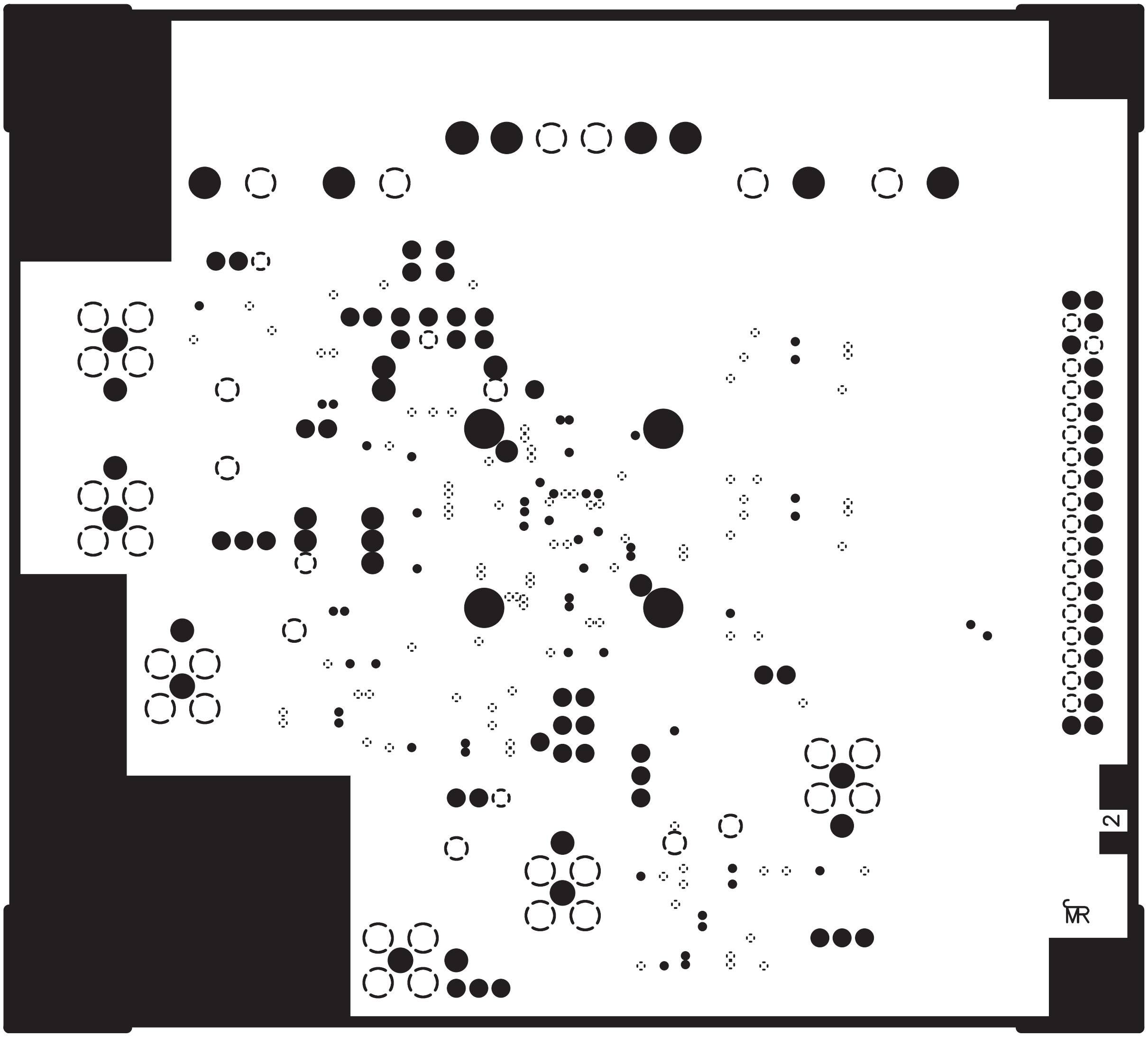


Figure 27. AD9244 Evaluation Board, PCB Layer 2 (Ground Plane)

Figure 28. AD9244 Evaluation Board, PCB Layer 3 (Power Plane)

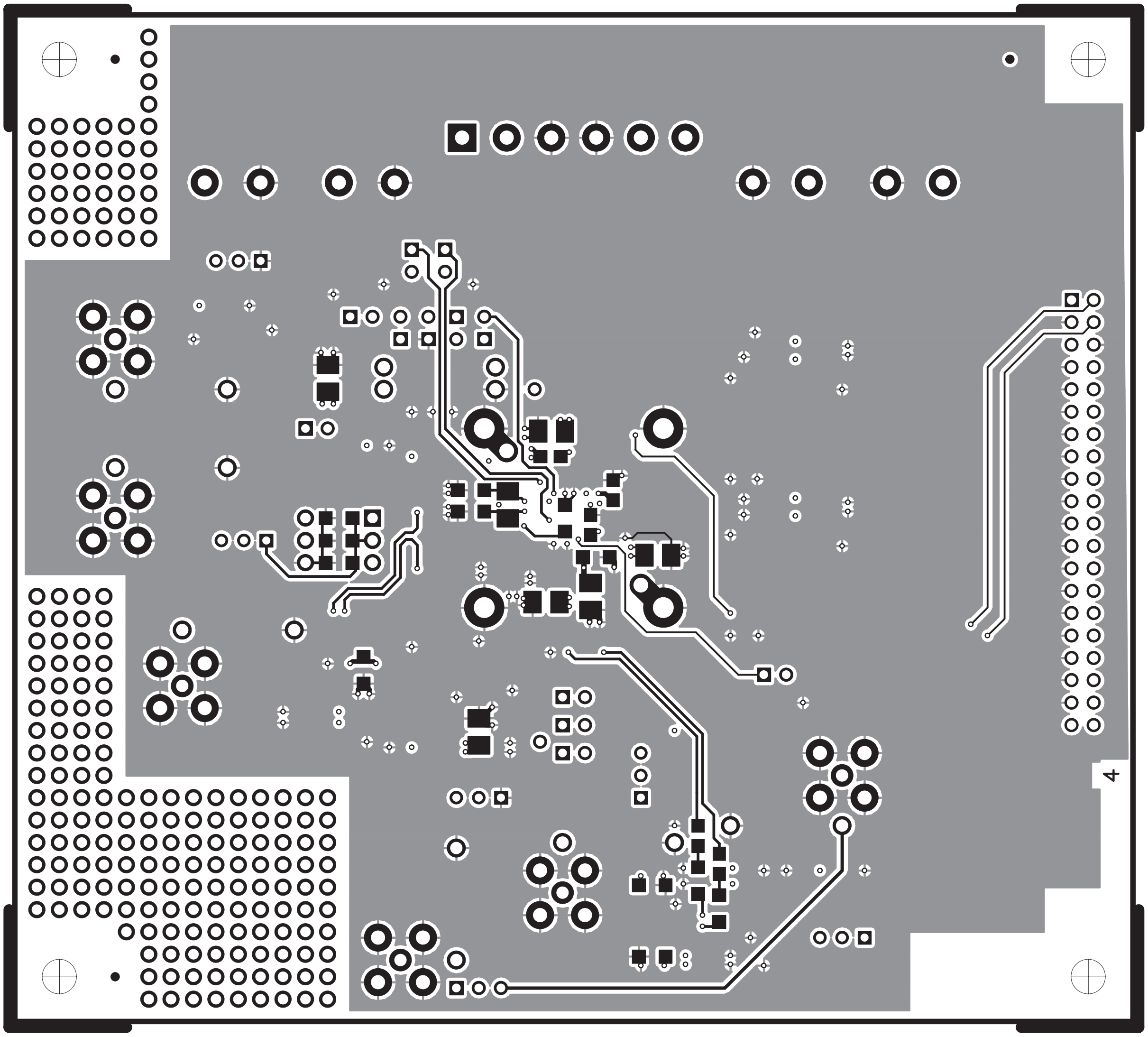
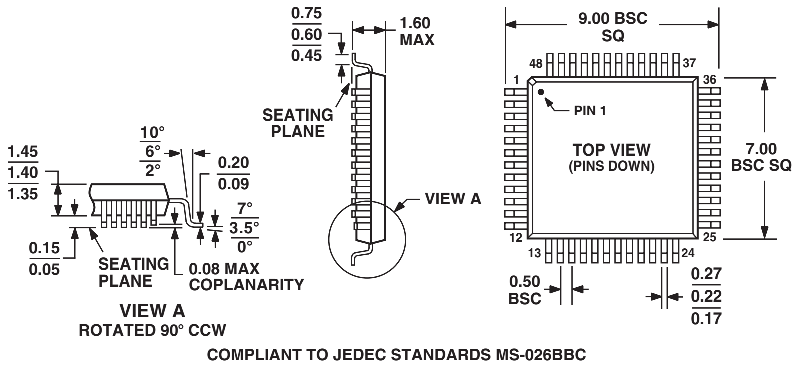


Figure 29. AD9244 Evaluation Board, PCB Layer 4 (Bottom)

OUTLINE DIMENSIONS

8-Lead Low Profile Quad Flat Package [LQFP] (ST-48)

Dimensions shown in millimeters



Revision History

C02404–0–6/03(A)