Integrated Device Technology, Inc.

COMPACT PCI SMART I/O 64 CARD

PRELIMINARY INFORMATION

IDT7M9535
IDT7M9536
IDT7M9537

FEATURES:

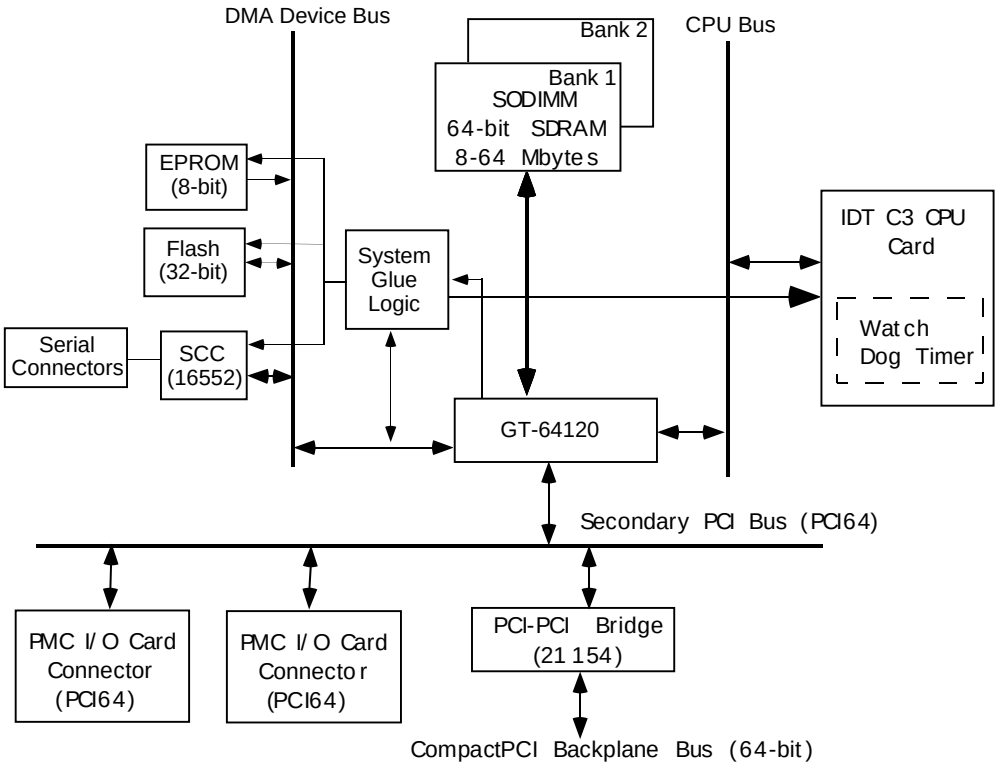
- High performance IDT Common-bus CPU Card (C3),
  - IDT MIPS processors RV4650, RV4700 or RV5000
  - Configurable with up to 1MB of L2 cache
- 6U size CompactPCI peripheral board
- Two 64-bit PCI Mezzanine Card (PMC) slots on board to support a wide range of PCI based I/O devices
- Digital 21154 PCI to PCI Bridge
  - Separates Secondary (on board) PCI bus traffic from backplane PCI bus traffic
  - 64-bit backplane and secondary PCI buses
- Galileo GT64120 single chip PCI system controller
  - Up to 75MHz CPU bus frequency
- Two 144 Pin SDRAM SODIMM sockets for DRAM
  - SDRAM
  - 64 bit DRAM data path
  - 8Mbyte to 128Mbyte of DRAM supported
- Flash
  - 32 bit Width
  - 4Mbyte standard configuration
  - Consult factory for 8 Mbyte option
- Boot Prom
  - 8-bit Width
  - Up to 512KB
- Dual serial interface ports
  - 16552D (16550A compatible)
  - 10 pin (2x5) headers
- Two General Purpose Registers
- On Board Reset Generation

DESCRIPTION:

The IDT7M9535/36/37 is a standard 6U CompactPCI Card which consists of an IDTC3 CPU Card based subsystem that can be used as an I/O processor in a CompactPCI based system.

It is designed to be plugged into any CPCI backplane peripheral slot that can accept a standard 6U size card. The card contains all of the features required of a typical CPU subsystem for embedded I/O processing applications.

FUNCTIONAL BLOCK DIAGRAM



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BOARD OVERVIEW

The IDT7M9535/36/37 consists of the following functional blocks: 21154 PCI to PCI Bridge, C3 processor, GT64120 PCI System Controller Chip, DRAM memory, system glue logic, Flash/EPROM and serial port controller. The IDT7M9535/36/37 CPU subsystem is designed to interface with its targeted system through a standard CompactPCI bus interface.

PCI TO PCI BRIDGE

The 21154 PCI to PCI Bridge is a high performance 64-bit to 64-bit PCI bridge that is compliant to PCI Revision 2.1. This chip isolates the primary (backplane) and on board secondary PCI busses. This isolation allows concurrent PCI traffic on the backplane and secondary PCI busses.

IDT C3 PROCESSOR CARD

The IDT C3 (Common-bus CPU Card) is a mezzanine based card that provides a common hardware interface for IDT's family of 64-bit MIPS processors (RV4650, RV4700 and RV5000). In addition, this card also has the following features:

- up to 1MB of optional L2 cache.
- 5V tolerant Inputs and I/Os.
- R4X00/R5000 bus interface.
- Watchdog Timer.

PCI SYSTEM CONTROLLER

The GT64120 from Galileo Technology, Inc. is designed to connect a high speed processor to peripheral devices. It is specifically designed to interface with the MIPS family of 64-bit processors. It connects the CPU to an asynchronous local device bus which is used to interface with the boot EPROM, Serial I/O, and Flash memory. It also has a built-in DRAM controller for interfacing the processor to the onboard SDRAM main memory with minimal glue logic. In addition, the chip provides a CPU bus to PCI bus bridge. The GT64120 can be configured as either a PCI bus master or a PCI bus slave device.

DRAM

The main memory consists of two 144 pin sockets which can be populated with standard 64-bit synchronous DRAM (SDRAM) SODIMMs. One or both SODIMM sockets may be populated, each occupying separate banks. Parity is not supported on the SDRAM.

Each SODIMM can support one or two banks of SDRAM dependent on the type of SODIMM being used. One bank is supported when single bank SDRAM SODIMMs are used (e.g., 1Meg x 64), and two banks are supported when double bank SDRAM SODIMMs are used (e.g., 2Meg x 64). The design can use any standard SDRAM DIMM containing 8MB (1Meg x 64), 16MB (2Meg x 64), 32MB (4Meg x 64), or 64MB (8Meg x 64) allowing the memory on the IDT7M9535/36/37 to be expanded up to a maximum of 128 Mbytes.

BOOT EPROM

The Boot EPROM is a JEDEC standard 32 pin PLCC EPROM socket which can support up to 512KB (512k x 8) which holds the boot code for the board.

SERIAL I/O

The IDT7M9535/36/37 has two 16550A compatible RS232 serial ports. The serial ports come out to two 10 pin headers (2x5).

The 10 pin headers have the following pinout/definition:

Header Pinout/Definition (Top View)			
DCD	1	2	DSR
RD	3	4	RTS
TD	5	6	CTS
DTR	7	8	RI
GND	9	10	NC

WATCHDOG RESET

The watchdog reset is generated from the watchdog timer included on the C3. It is used to generate a warm reset to the processor if it has not been strobed within 1 second.

SYSTEM GLUE LOGIC

The system glue logic is responsible for the following functions:

- Processor General Purpose Registers (GPR0, GPR1)
- Device Decoding
- Interrupt Masking/Mapping
- Primary PCI bus Interrupt Generation

INTERRUPTS

The processor on the IDT7M9535/36/37 supports the following onboard interrupt sources:

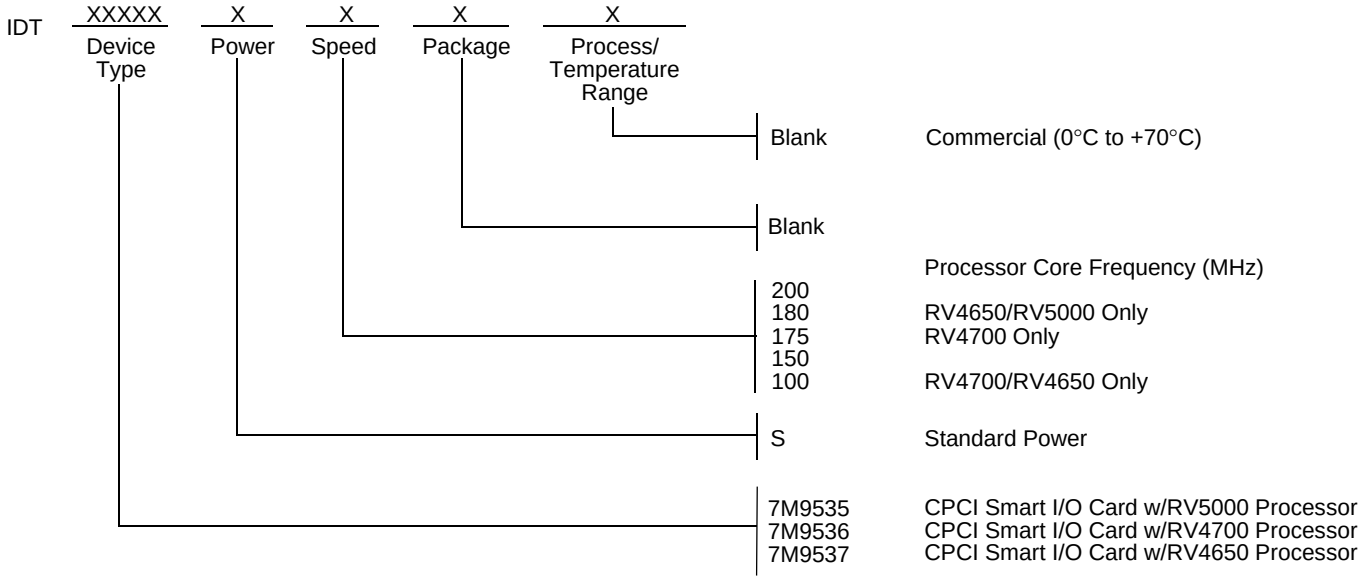
- GT64120 interrupt
- Serial I/O interrupts
- PMC Slot 1 interrupt
- PMC Slot 2 interrupt
- Processor internal timer interrupt

RESET

The IDT7M9535/36/37 supports several reset sources which include:

- Power on reset
- Manual Cold Reset (Front panel accessible)
- SW Warm Reset.
- Backplane CPCI Reset bus (Generates a Cold Reset to the card).
- Watchdog warm reset.

ORDERING INFORMATION



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Notes:
1. For other C3 options consult factory.