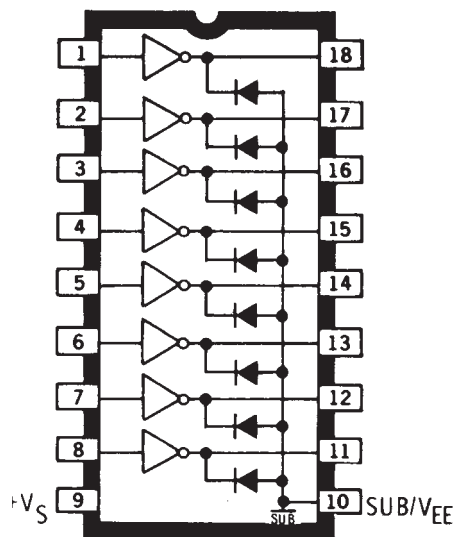


# SERIES 2580

## 8-CHANNEL SOURCE DRIVERS

UDN2580A and UDN2585A



Dwg. No. A-11,359

### ABSOLUTE MAXIMUM RATINGS

See next page.

This versatile family of integrated circuits will work with many combinations of logic- and load-voltage levels, meeting interface requirements beyond the capabilities of standard logic buffers. Series UDN2580A and A2580SLW source drivers can drive incandescent, LED, or vacuum fluorescent displays. Internal transient-suppression diodes permit the drivers to be used with inductive loads such as relays, solenoids, dc and stepping motors, and magnetic print hammers.

The Types UDN2580A and A2580SLW are high-current source drivers used to switch the ground ends of loads that are directly connected to a -50 V supply. Typical loads are telephone relays, PIN diodes, and LEDs.

The UDN2585A and A2585SLW are drivers designed for applications requiring low output saturation voltages. Typical loads are low-voltage LEDs and incandescent displays. The eight non-Darlington, 25 V outputs will simultaneously sustain continuous load currents of -120 mA at ambient temperatures to +70°C.

The UDN2588A and A2588SLW have separate logic and driver supply lines. Their eight drivers can serve as an interface between positive logic (TTL, CMOS, PMOS) or negative logic (NMOS) and either negative or split-load supplies to -80 V.

These drivers are packaged in plastic DIPs (suffix A) or surface-mountable wide-body SOICs (suffix LW), and are rated for operation over the temperature range of -20°C to +85°C.

### FEATURES

- TTL, CMOS, PMOS, NMOS Compatible
- High Output-Current Rating
- Internal Transient Suppression
- Efficient Input/Output Structure
- Through-Hole and Surface-Mount Packages

Always order by complete part number, e.g., **UDN2580A**.

# SERIES 2580

## 8-CHANNEL

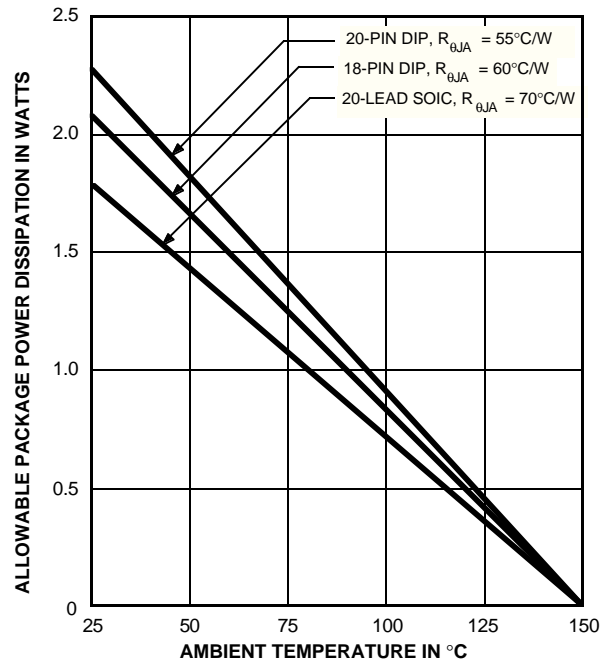
### SOURCE DRIVERS

#### ABSOLUTE MAXIMUM RATINGS

at 25°C Free-Air Temperature for any one driver (unless otherwise noted).

	UDN2580A A2580SLW	UDN2585A A2585SLW	UDN2588A A2588SLW
Output Voltage, $V_{CE}$	50 V	25 V	80 V
Supply Voltage, $V_S$ (ref. sub.)	50 V	25 V	80 V
Supply Voltage, $V_{CC}$ (ref. sub.)	—	—	80 V
Input Voltage, $V_{IN}$ (ref. $V_S$ )	-30 V	-20 V	-30 V
Total Output Current, ( $I_C + I_S$ )	-500 mA	-250 mA	-500 mA
Substrate Current $I_{SUB}$	3.0 A	2.0 A	3.0 A

Package Power Dissipation,  $P_D$  (single output) ..... 1.0 W  
 (total package) ..... See Graph  
 Operating Temperature Range,  $T_A$  ..... -20°C to +85°C  
 Storage Temperature Range,  $T_S$  ..... -55°C to +150°C



Dwg. GP-022-1



**SERIES 2580**  
**8-CHANNEL**  
**SOURCE DRIVERS**

For simplification, these devices are characterized on the following pages with specific voltages for inputs, logic supply ( $V_S$ ), load supply ( $V_{EE}$ ), and collector supply ( $V_{CC}$ ). Typical use of the UDN2580A and A2580SLW is with negative-referenced logic. The more common application of the UDN2585A, A2585SLW, UDN2588A and A2588SLW are with positive-referenced logic supplies. In application, the devices are capable of operation over a wide range of logic and supply voltage levels:

**TYPICAL OPERATING VOLTAGES**

$V_S$	$V_{IN(ON)}$	$V_{IN(OFF)}$	$V_{CC}$	$V_{EE(MAX)}$	Device Types
0 V	-15 V to -3.6 V	-0.5 V to 0 V	NA	-25 V	UDN2585A & A2585SLW
				-50 V	UDN2580A & A2580SLW
+5 V	0 V to +1.4 V	+4.5 V to +5 V	NA	-20 V	UDN2585A & A2585SLW
				-45 V	UDN2580A & A2580SLW
			$\leq 5$ V	-75 V	UDN2588A & A2588SLW
+12 V	0 V to +8.4 V	+11.5 V to +12 V	NA	-13 V	UDN2585A & A2585SLW
				-38 V	UDN2580A & A2580SLW
			$\leq 12$ V	-68 V	UDN2588A & A2588SLW
+15 V	0 V to +11.4 V	+14.5 V to +15 V	NA	-10V	UDN2585A & A2585SLW
				-35 V	UDN2580A & A2580SLW
			$\leq 15$ V	-65 V	UDN2588A & A2588SLW

NOTE: The substrate must be tied to the most negative point in the external circuit to maintain isolation between drivers and to provide for normal circuit operation.

# SERIES 2580 8-CHANNEL SOURCE DRIVERS

## UDN2580A and A2580SLW

ELECTRICAL CHARACTERISTICS at  $T_A = +25^\circ\text{C}$ ,  $V_S = 0\text{ V}$ ,  $V_{EE} = -45\text{ V}$  (unless otherwise noted).

Characteristic	Symbol	Test Conditions	Limits		
			Min.	Max.	Units
Output Leakage Current	$I_{CEX}$	$V_{IN} = -0.5\text{ V}$ , $V_{OUT} = V_{EE} = -50\text{ V}$	—	50	$\mu\text{A}$
		$V_{IN} = -0.4\text{ V}$ , $V_{OUT} = V_{EE} = -50\text{ V}$ , $T_A = 70^\circ\text{C}$	—	100	$\mu\text{A}$
Output Sustaining Voltage	$V_{CE(SUS)}$	$V_{IN} = -0.4\text{ V}$ , $I_{OUT} = -25\text{ mA}$ , Note 1	35	—	V
Output Saturation Voltage	$V_{CE(SAT)}$	$V_{IN} = -2.4\text{ V}$ , $I_{OUT} = -100\text{ mA}$	—	1.8	V
		$V_{IN} = -3.0\text{ V}$ , $I_{OUT} = -225\text{ mA}$	—	1.9	V
		$V_{IN} = -3.6\text{ V}$ , $I_{OUT} = -350\text{ mA}$	—	2.0	V
Input Current	$I_{IN(ON)}$	$V_{IN} = -3.6\text{ V}$ , $I_{OUT} = -350\text{ mA}$	—	-500	$\mu\text{A}$
		$V_{IN} = -15\text{ V}$ , $I_{OUT} = -350\text{ mA}$	—	-2.1	mA
	$I_{IN(OFF)}$	$I_{OUT} = -500\text{ }\mu\text{A}$ , $T_A = 70^\circ\text{C}$ , Note 3	-50	—	$\mu\text{A}$
Input Voltage	$V_{IN(ON)}$	$I_{OUT} = -100\text{ mA}$ , $V_{CE} \leq 1.8\text{ V}$ , Note 4	—	-2.4	V
		$I_{OUT} = -225\text{ mA}$ , $V_{CE} \leq 1.9\text{ V}$ , Note 4	—	-3.0	V
		$I_{OUT} = -350\text{ mA}$ , $V_{CE} \leq 2.0\text{ V}$ , Note 4	—	-3.6	V
	$V_{IN(OFF)}$	$I_{OUT} = -500\text{ }\mu\text{A}$ , $T_A = 70^\circ\text{C}$	-0.2	—	V
Clamp Diode Leakage Current	$I_R$	$V_R = 50\text{ V}$ , $T_A = 70^\circ\text{C}$	—	50	$\mu\text{A}$
Clamp Diode Forward Voltage	$V_F$	$I_F = 350\text{ mA}$	—	2.0	V
Input Capacitance	$C_{IN}$		—	25	pF
Turn-On Delay	$t_{PHL}$	$0.5 E_{IN}$ to $0.5 E_{OUT}$	—	5.0	$\mu\text{s}$
Turn-Off Delay	$t_{PLH}$	$0.5 E_{IN}$ to $0.5 E_{OUT}$	—	5.0	$\mu\text{s}$

NOTES: 1. Pulsed test,  $t_p \leq 300\text{ }\mu\text{s}$ , duty cycle  $\leq 2\%$ .

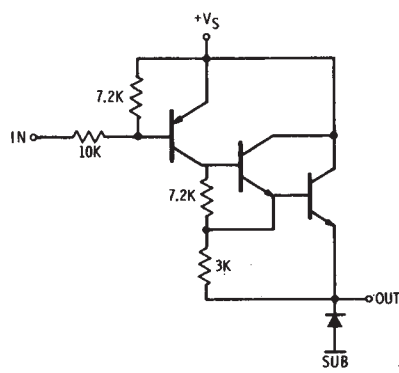
2. Negative current is defined as coming out of the specified device pin.

3. The  $I_{IN(OFF)}$  current limit guarantees against partial turn-on of the output.

4. The  $V_{IN(ON)}$  voltage limit guarantees a minimum output source current per the specified conditions.

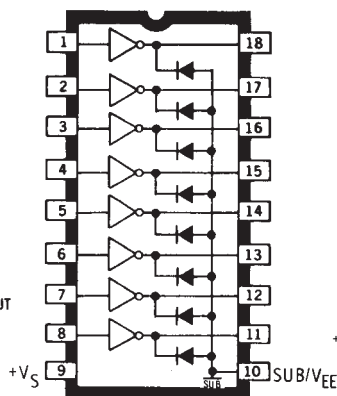
5. The substrate must always be tied to the most negative point and must be at least 4.0 V below  $V_S$ .

### PARTIAL SCHEMATIC



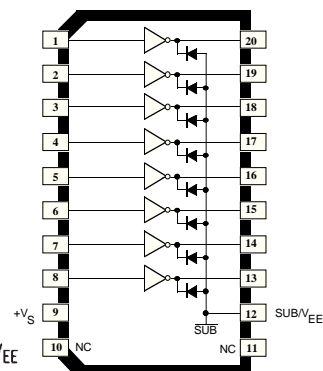
Dwg. No. A-11,358

### UDN2580A



Dwg. No. A-11,359

### A2580SLW



Dwg. PP-064



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# SERIES 2580

## 8-CHANNEL

### SOURCE DRIVERS

#### UDN2585A and A2585SLW

ELECTRICAL CHARACTERISTICS at  $T_A = +25^\circ\text{C}$ ,  $V_S = 0\text{ V}$ ,  $V_{EE} = -20\text{ V}$  (unless otherwise noted).

Characteristic	Symbol	Test Conditions	Limits		
			Min.	Max.	Units
Output Leakage Current	$I_{CEX}$	$V_{IN} = -0.5\text{ V}$ , $V_{OUT} = V_{EE} = -25\text{ V}$	—	50	$\mu\text{A}$
		$V_{IN} = -0.4\text{ V}$ , $V_{OUT} = V_{EE} = -25\text{ V}$ , $T_A = 70^\circ\text{C}$	—	100	$\mu\text{A}$
Output Sustaining Voltage	$V_{CE(SUS)}$	$V_{IN} = -0.4\text{ V}$ , $I_{OUT} = -25\text{ mA}$ , Note 1	15	—	V
Output Saturation Voltage	$V_{CE(SAT)}$	$V_{IN} = -4.6\text{ V}$ , $I_{OUT} = -60\text{ mA}$	—	1.1	V
		$V_{IN} = -4.6\text{ V}$ , $I_{OUT} = -120\text{ mA}$	—	1.2	V
Input Current	$I_{IN(ON)}$	$V_{IN} = -4.6\text{ V}$ , $I_{OUT} = -120\text{ mA}$	—	-1.6	mA
		$V_{IN} = -14.6\text{ V}$ , $I_{OUT} = -120\text{ mA}$	—	-5.0	mA
Input Voltage	$V_{IN(ON)}$	$I_{OUT} = -120\text{ mA}$ , $V_{CE} \leq 1.2\text{ V}$ , Note 3	—	-4.6	V
	$V_{IN(OFF)}$	$I_{OUT} = -100\text{ }\mu\text{A}$ , $T_A = 70^\circ\text{C}$	-0.4	—	V
Clamp Diode Leakage Current	$I_R$	$V_R = 25\text{ V}$ , $T_A = 70^\circ\text{C}$	—	50	$\mu\text{A}$
Clamp Diode Forward Voltage	$V_F$	$I_F = 120\text{ mA}$	—	2.0	V
Input Capacitance	$C_{IN}$		—	25	pF
Turn-On Delay	$t_{PHL}$	$0.5 E_{IN}$ to $0.5 E_{OUT}$	—	5.0	$\mu\text{s}$
Turn-Off Delay	$t_{PLH}$	$0.5 E_{IN}$ to $0.5 E_{OUT}$	—	5.0	$\mu\text{s}$

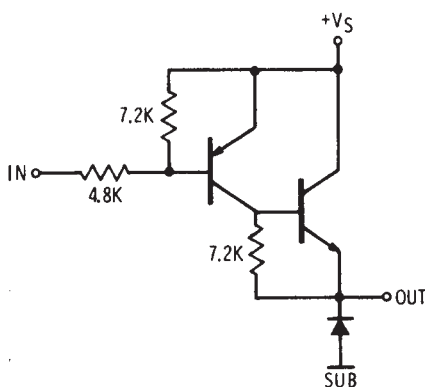
NOTES: 1. Pulsed test,  $t_p \leq 300\text{ }\mu\text{s}$ , duty cycle  $\leq 2\%$ .

2. Negative current is defined as coming out of the specified device pin.

3. The  $V_{IN(ON)}$  voltage limit guarantees a minimum output source current per the specified conditions.

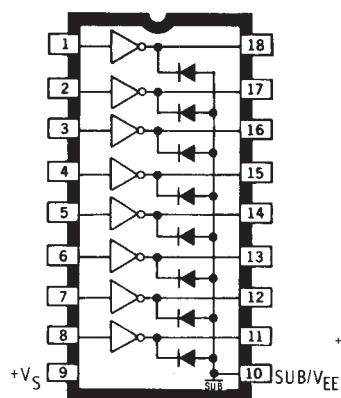
4. The substrate must always be tied to the most negative point and must be at least 4.0 V below  $V_S$ .

#### PARTIAL SCHEMATIC



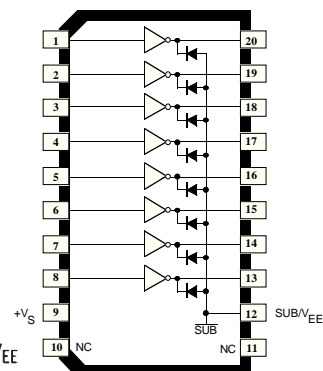
Dwg. No. A-11,360

#### UDN2585A



Dwg. No. A-11,359

#### A2585SLW



Dwg. PP-064

# SERIES 2580

## 8-CHANNEL

### SOURCE DRIVERS

#### UDN2588A and A2588SLW

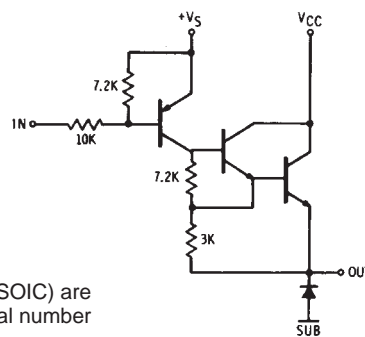
**ELECTRICAL CHARACTERISTICS at  $T_A = +25^\circ\text{C}$ ,  $V_S = 5.0\text{ V}$ ,  $V_{CC} = 5.0\text{ V}$ ,  $V_{EE} = -40\text{ V}$**

**(unless otherwise noted).**

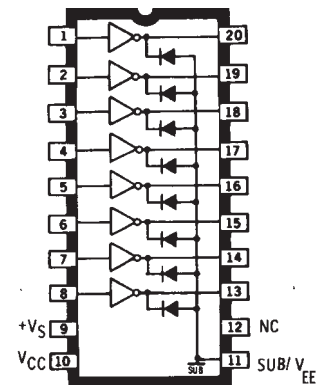
Characteristic	Symbol	Test Conditions	Limits		
			Min.	Max.	Units
Output Leakage Current	$I_{CEX}$	$V_{IN} \geq 4.5\text{ V}$ , $V_{OUT} = V_{EE} = -75\text{ V}$	—	50	$\mu\text{A}$
Output Sustaining Voltage	$V_{CE(SUS)}$	$V_{IN} \geq 4.6\text{ V}$ , $V_{EE} = -70\text{ V}$ , $I_{OUT} = -25\text{ mA}$ , Note 1	50	—	V
Output Saturation Voltage	$V_{CE(SAT)}$	$V_{IN} = 2.6\text{ V}$ , $I_{OUT} = -100\text{ mA}$ , Ref. $V_{CC}$	—	1.8	V
		$V_{IN} = 2.0\text{ V}$ , $I_{OUT} = -225\text{ mA}$ , Ref. $V_{CC}$	—	1.9	V
		$V_{IN} = 1.4\text{ V}$ , $I_{OUT} = -350\text{ mA}$ , Ref. $V_{CC}$	—	2.0	V
Input Current	$I_{IN(ON)}$	$V_{IN} = 1.4\text{ V}$ , $I_{OUT} = -350\text{ mA}$	—	-500	$\mu\text{A}$
		$V_S = 15\text{ V}$ , $V_{EE} = -30\text{ V}$ , $V_{IN} = 0\text{ V}$ , $I_{OUT} = -350\text{ mA}$	—	-2.1	mA
	$I_{IN(OFF)}$	$I_{OUT} = -500\text{ }\mu\text{A}$ , $T_A = 70^\circ\text{C}$ , Note 3	-50	—	$\mu\text{A}$
Input Voltage	$V_{IN(ON)}$	$I_{OUT} = -100\text{ mA}$ , $V_{CE} \leq 1.8\text{ V}$ , Note 4	—	2.6	V
		$I_{OUT} = -225\text{ mA}$ , $V_{CE} \leq 1.9\text{ V}$ , Note 4	—	2.0	V
		$I_{OUT} = -350\text{ mA}$ , $V_{CE} \leq 2.0\text{ V}$ , Note 4	—	1.4	V
	$V_{IN(OFF)}$	$I_{OUT} = -500\text{ }\mu\text{A}$	4.8	—	V
Clamp Diode Leakage Current	$I_R$	$V_R = 80\text{ V}$	—	50	$\mu\text{A}$
Clamp Diode Forward Voltage	$V_F$	$I_F = 350\text{ mA}$	—	2.0	V
Input Capacitance	$C_{IN}$		—	25	pF
Turn-On Delay	$t_{PLH}$	$0.5 E_{IN}$ to $0.5 E_{OUT}$	—	5.0	$\mu\text{s}$
Turn-Off Delay	$t_{PLH}$	$0.5 E_{IN}$ to $0.5 E_{OUT}$	—	5.0	$\mu\text{s}$

- NOTES:
1. Pulsed test,  $t_p \leq 300\text{ }\mu\text{s}$ , duty cycle  $\leq 2\%$ .
  2. Negative current is defined as coming out of the specified device pin.
  3. The  $I_{IN(OFF)}$  current limit guarantees against partial turn-on of the output.
  4. The  $V_{IN(ON)}$  voltage limit guarantees a minimum output source current per the specified conditions.
  5. The substrate must always be tied to the most negative point and must be at least 4.0 V below  $V_S$ .
  6.  $V_{CC}$  must be equal to or less positive than  $V_S$ .

#### PARTIAL SCHEMATIC



Dwg. No. A-11,361



Dwg. No. A-11,357

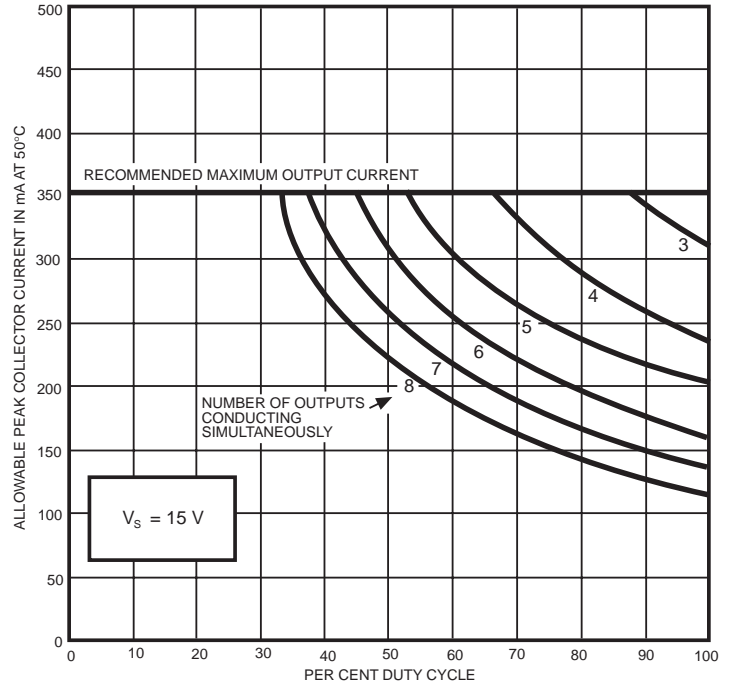
Note the UDN2588A (DIP) and the A2588SLW (SOIC) are electrically identical and share a common terminal number assignment.



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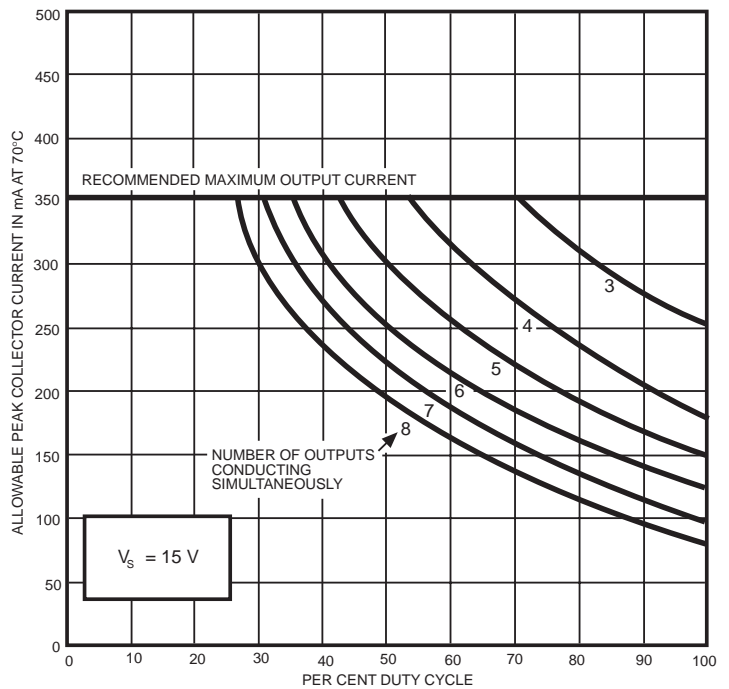
**SERIES 2580**  
**8-CHANNEL**  
**SOURCE DRIVERS**

**ALLOWABLE PEAK COLLECTOR CURRENT AT 50°C AS A FUNCTION OF DUTY CYCLE**



Dwg. No. A-11,107B

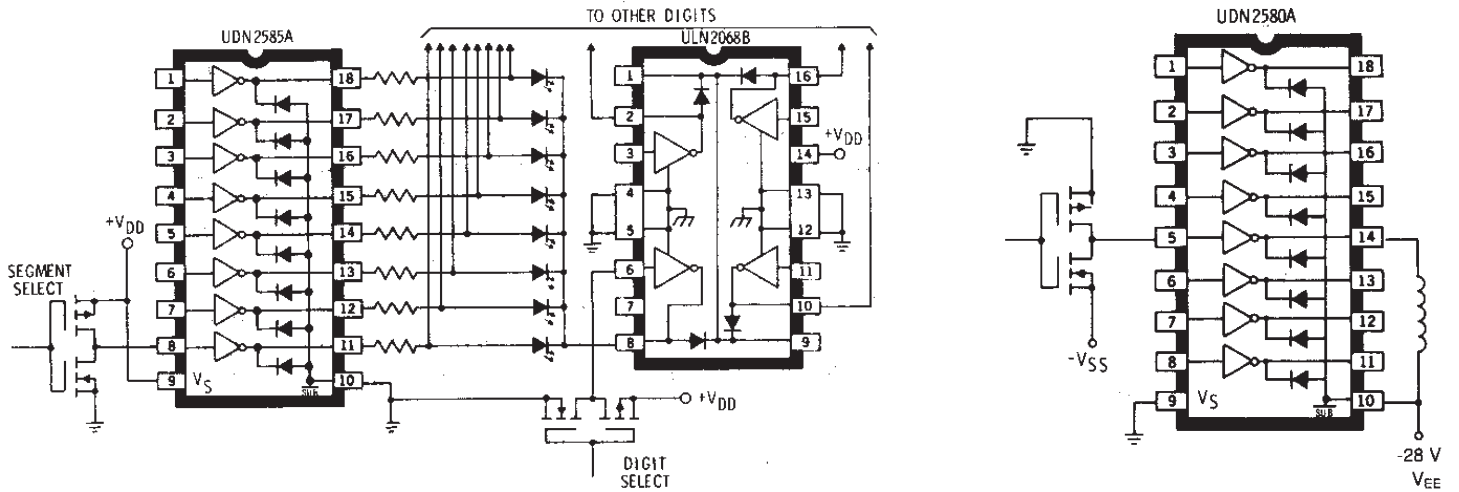
**ALLOWABLE PEAK COLLECTOR CURRENT AT 70°C AS A FUNCTION OF DUTY CYCLE**



Dwg. No. A-11,108B

# SERIES 2580 8-CHANNEL SOURCE DRIVERS

## TYPICAL APPLICATIONS

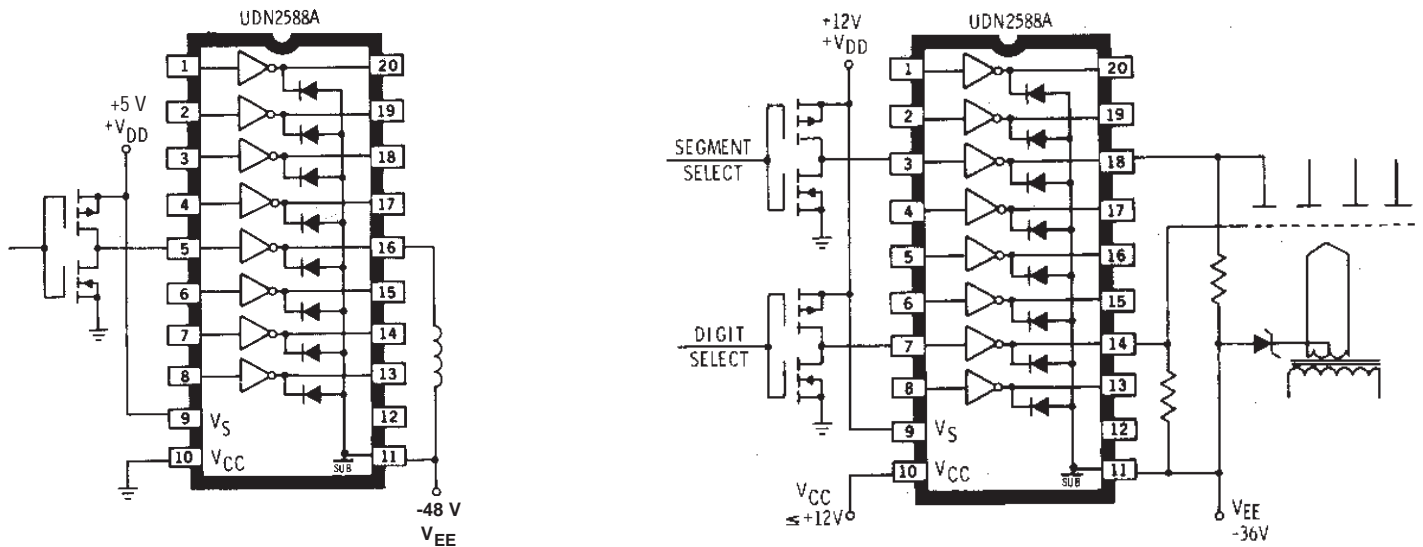


Dwg. No. B-1458A

Dwg. No. A-11,356

COMMON-CATHODE LED DRIVER

TELECOMMUNICATIONS  
RELAY DRIVER  
(Negative Logic)



Dwg. No. A-11,362A

Dwg. No. A-11,363

TELECOMMUNICATIONS RELAY DRIVER  
(Positive Logic)

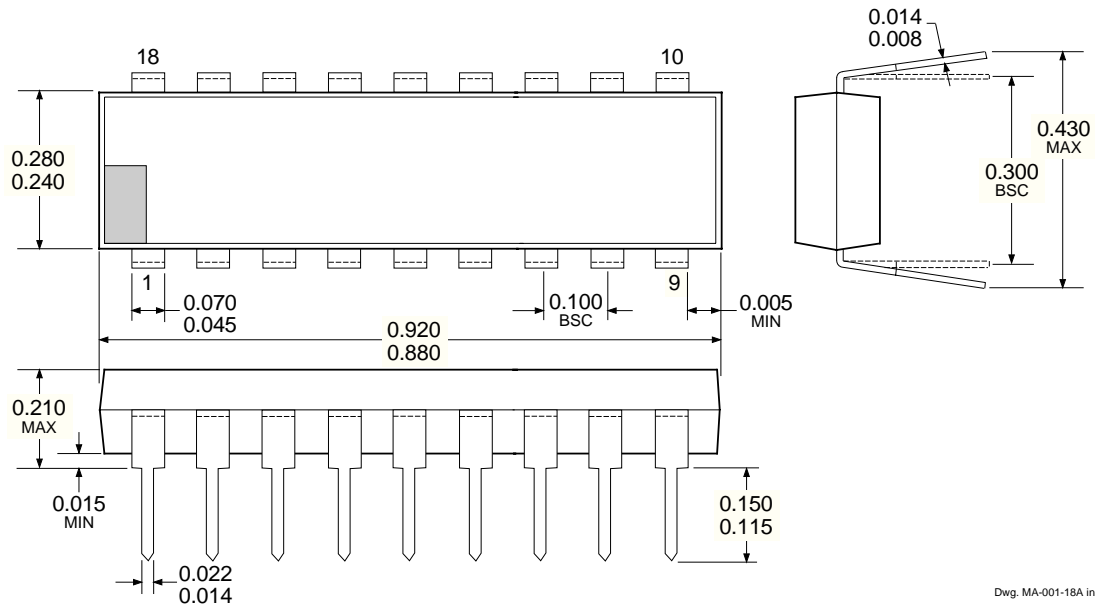
VACUUM-FLUORESCENT DISPLAY DRIVER  
(Split Supply)



**SERIES 2580**  
**8-CHANNEL**  
**SOURCE DRIVERS**

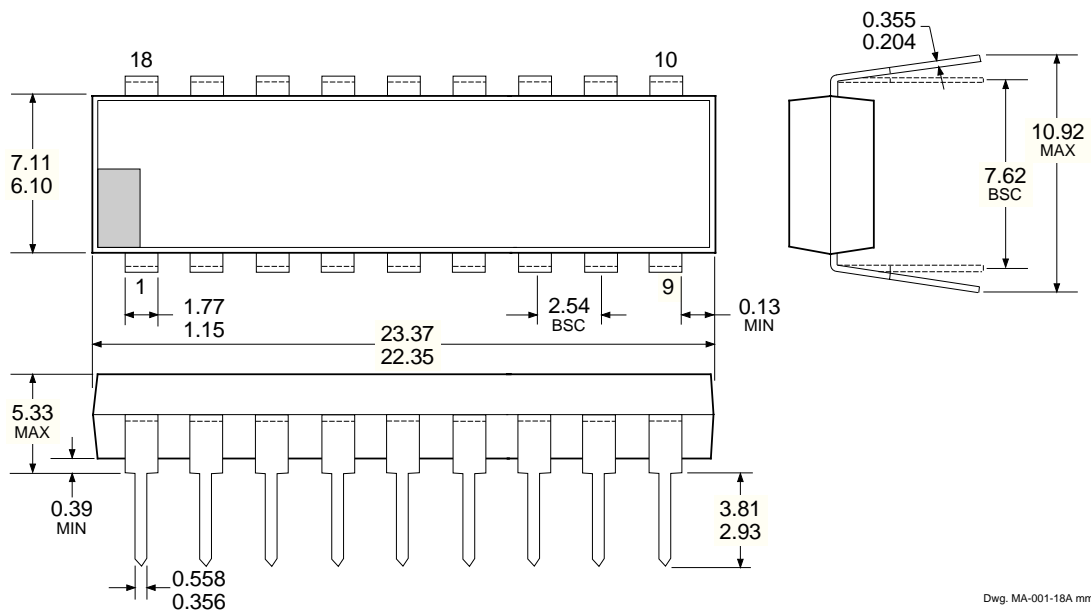
**UDN2580A and UDN2585A**

Dimensions in Inches  
 (controlling dimensions)



Dwg. MA-001-18A in

Dimensions in Millimeters  
 (for reference only)



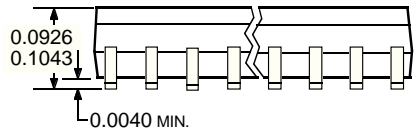
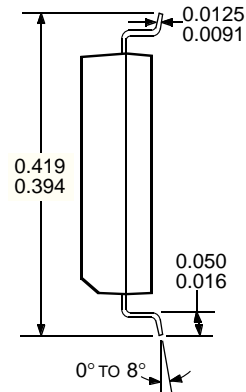
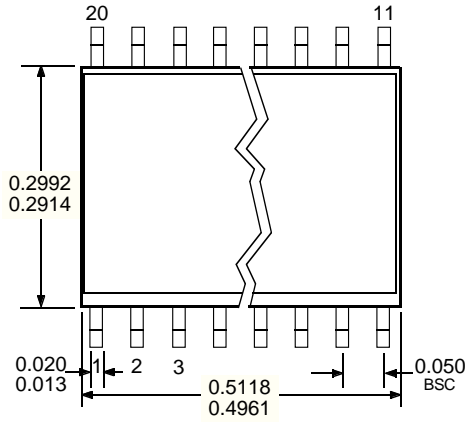
Dwg. MA-001-18A mm

- NOTES: 1. Exact body and lead configuration at vendor's option within limits shown.  
 2. Lead spacing tolerance is non-cumulative.  
 3. Lead thickness is measured at seating plane or below.

**SERIES 2580**  
**8-CHANNEL**  
**SOURCE DRIVERS**

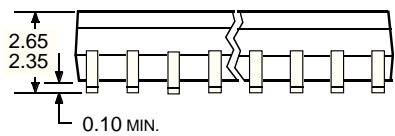
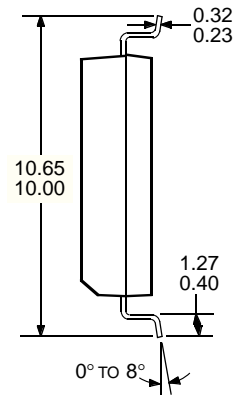
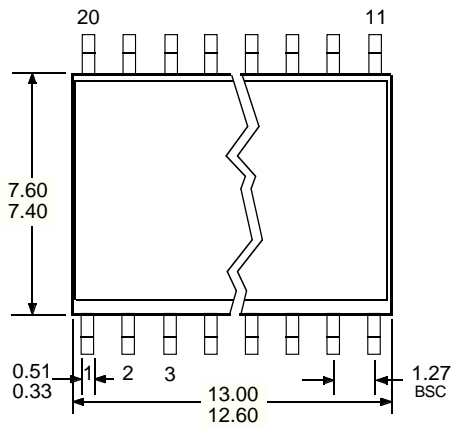
**A2580SLW and A2585SLW**

Dimensions in Inches  
 (for reference only)



Dwg. MA-008-20 in

Dimensions in Millimeters  
 (controlling dimensions)



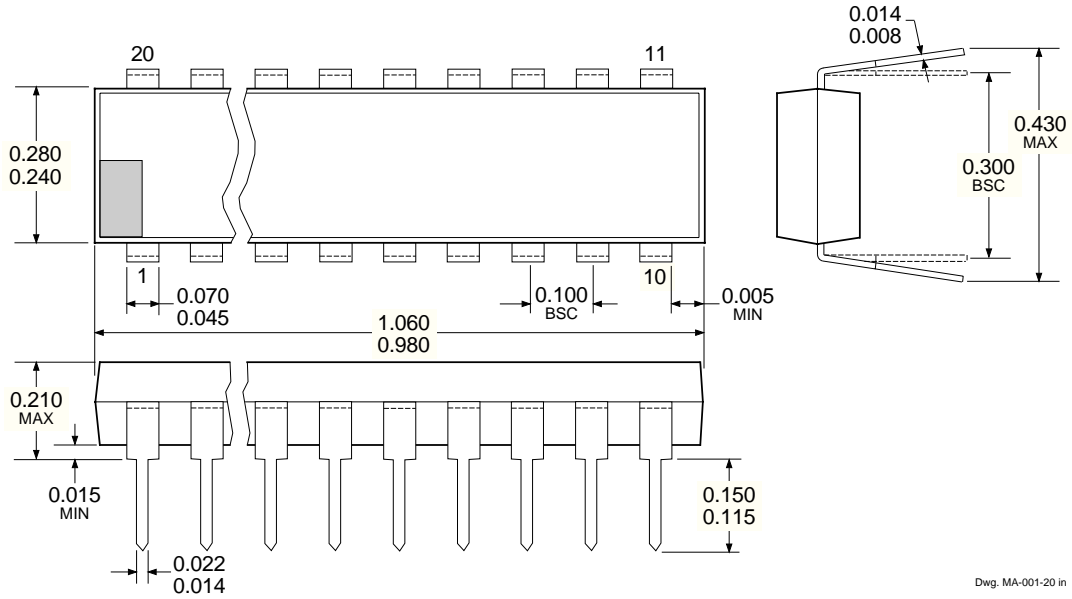
Dwg. MA-008-20 mm

- NOTES: 1. Exact body and lead configuration at vendor's option within limits shown.  
 2. Lead spacing tolerance is non-cumulative.

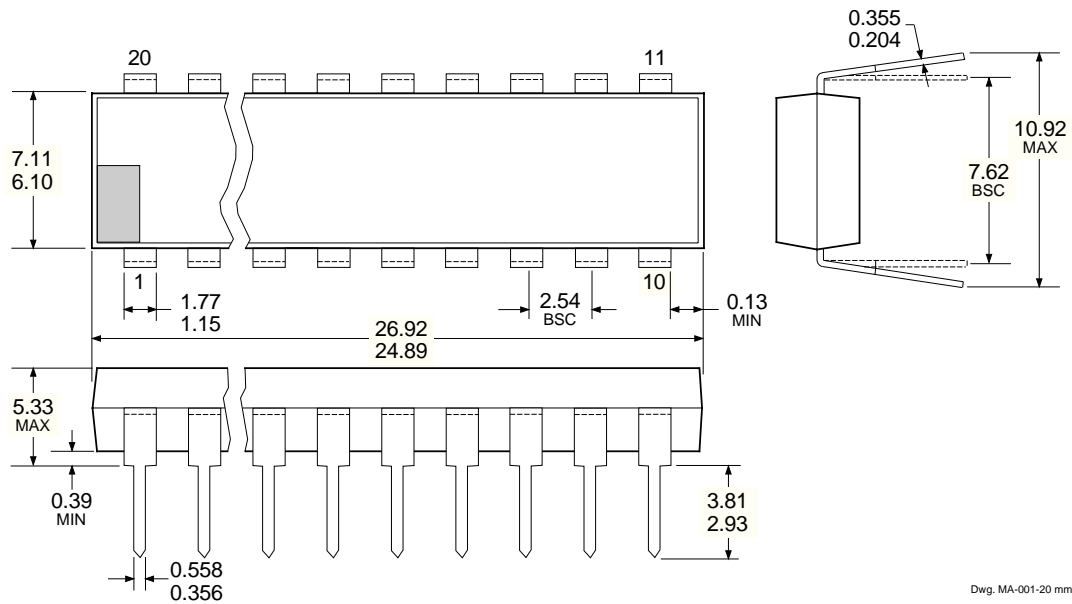
**SERIES 2580**  
**8-CHANNEL**  
**SOURCE DRIVERS**

**UDN2588A**

Dimensions in Inches  
 (controlling dimensions)



Dimensions in Millimeters  
 (for reference only)



- NOTES: 1. Exact body and lead configuration at vendor's option within limits shown.  
 2. Lead spacing tolerance is non-cumulative.  
 3. Lead thickness is measured at seating plane or below.

**SERIES 2580**  
**8-CHANNEL**  
**SOURCE DRIVERS**

**POWER SOURCE DRIVERS**  
**SELECTION GUIDE**

IN ORDER OF 1) OUTPUT CURRENT, 2) OUTPUT VOLTAGE, 3) NUMBER OF DRIVERS

Output Ratings *			Features					Part Number †
mA	V	#	Serial Input	Latched Drivers	Diode Clamp	Saturated Outputs	Internal Protection	
-25	60	8	–	X	–	–	–	5815
	60	10	X	X	Active Pull-Down	–	–	5810-F
	60	12	X	X	Active Pull-Down	–	–	5811
	60	20	X	X	Active Pull-Down	–	–	5812-F
	60	32	X	X	Active Pull-Down	–	–	5818-F
	85	8	–	–	–	–	–	6118
-120	-25	8	–	–	X	X	–	2585
	30	8	–	–	X	X	–	2985
	50	8	X	X	X	X	–	5895
-350	35	8	–	–	X	–	X	2987
	50	8	–	–	X	–	–	2981 and 2982
	50	8	X	X	X	–	–	5891
	-50	8	–	–	X	–	–	2580
	80	8	–	–	X	–	–	2983 and 2984
	80	8	X	X	X	–	–	5890
	-80	8	–	–	X	–	–	2588

\* Current is maximum specified test condition, voltage is maximum rating. See specification for sustaining voltage limits or over-current protection voltage limits.

† Complete part number includes additional characters to indicate operating temperature range and package style.

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