

F2F MAGNETIC STRIPE ENCODING CARD READER

DESCRIPTION

The M54910P is an I²L semiconductor integrated circuit consisting of an F2F demodulator for magnetic stripe card readers.

FEATURES

- Low power dissipation (18mA typ)
- Ignore bit select input (bits 2, 8)
- Open collector output
- Wide operating temperature range $T_a = -20 \sim +75^\circ\text{C}$

APPLICATION

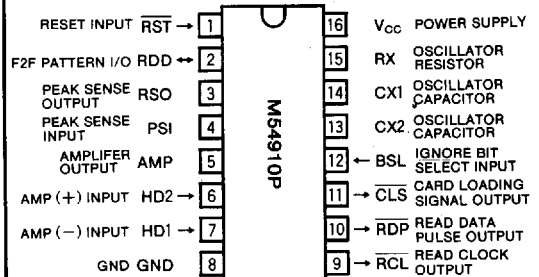
Magnetic stripe card readers

FUNCTION

The data signal from a magnetic stripe card is read by a magnetic head and enters the M54910P via inputs HD-1 and HD-2. The signal is analog processed by amplifier OP1, peak detector OP2 and waveform regenerator OP3 to demodulate the F2F pattern signal. The specific bit numbers set by input BSL are ignored, and the data is digitally processed to output card loading signal $\overline{\text{CLS}}$, demodulated clock signal $\overline{\text{RCL}}$, and demodulated data signal RDP.

$\overline{\text{CLS}}$ becomes low when two rising and falling edges of the F2F pattern signal RDD are counted (eight if BSL is high). If no input data is detected for a specified period, $\overline{\text{CLS}}$ returns to high. $\overline{\text{RCL}}$ is a clock signal whose period corre-

PIN CONFIGURATION (TOP VIEW)



Outline 16P4

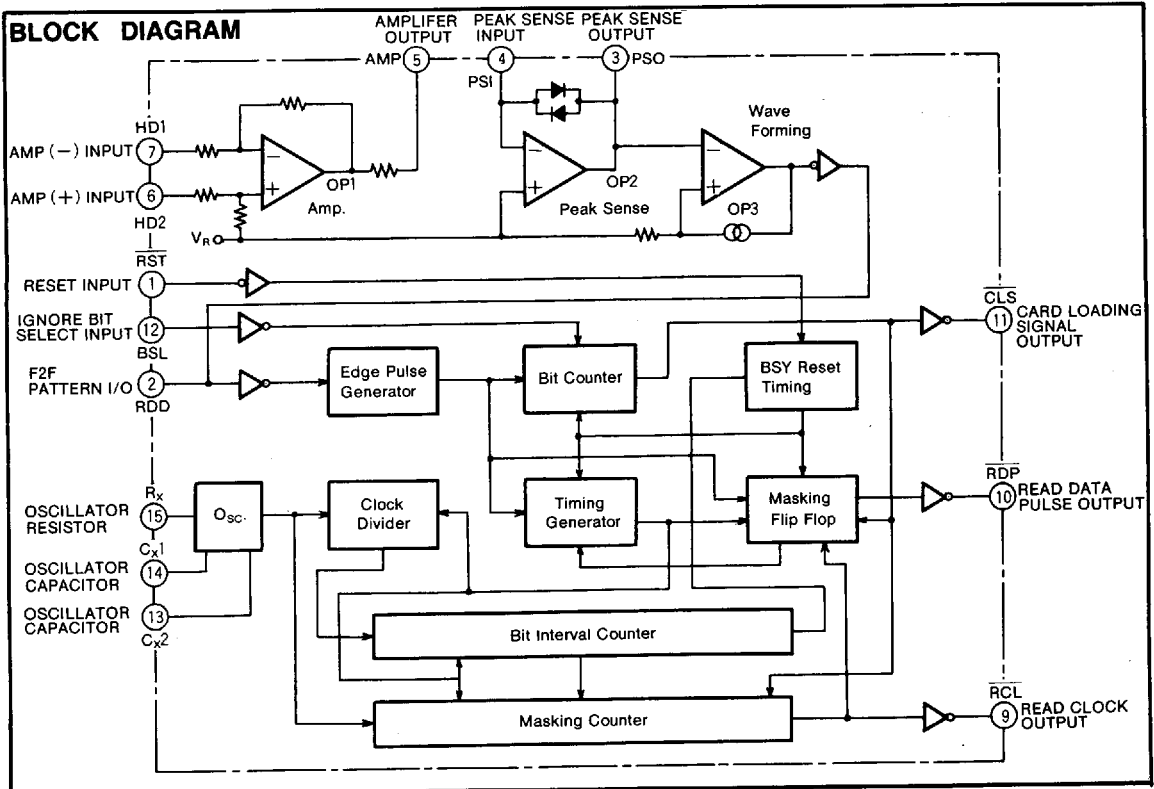
sponds to T_B , the duration of one data bit when the card speed is constant.

If T_{Bn} is the duration of a particular bit, $\overline{\text{RCL}}$ will be high for a period of $2/3 T_{Bn-1}$. When the bit value is 1, $\overline{\text{RDP}}$ is set low by the timing of RDD. In other words, while $\overline{\text{RCL}}$ is high, it can respond to a change of state in RDD. This means that even if the card speed changes, (typically $10 \sim 150\text{cm/s}$) where T_{Bn} satisfies the following formula.

$$2/3 T_{Bn-1} < T_{Bn} < 4/3 T_{Bn}$$

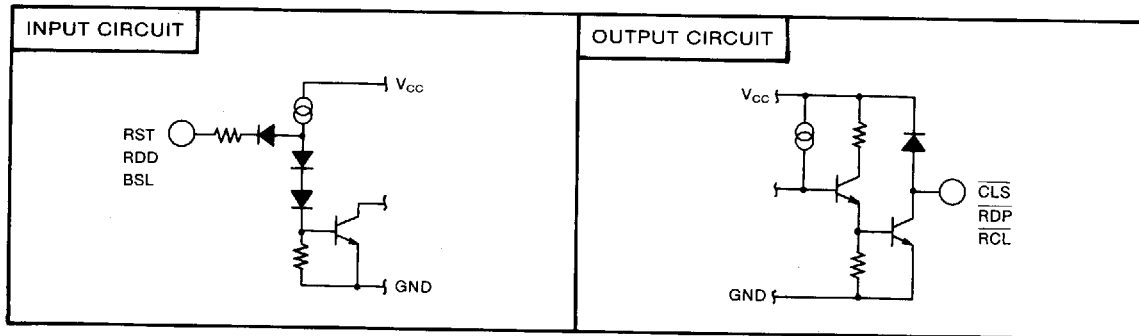
The T_B is counted by the oscillator period T_{Osc} .

BLOCK DIAGRAM



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I/O CIRCUIT CHART

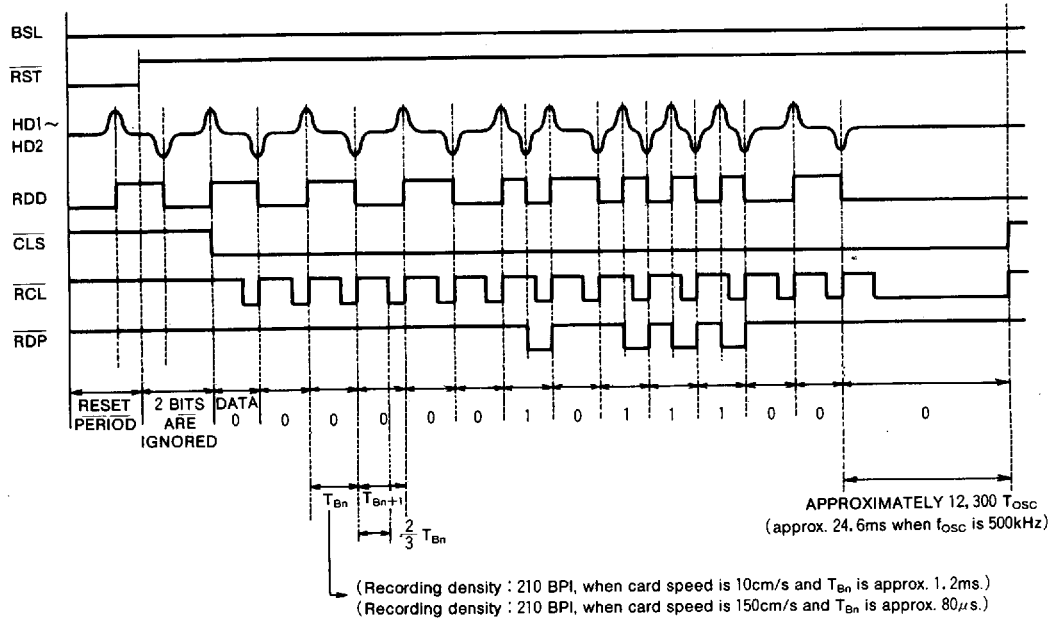


PIN DESCRIPTION

pin number	Symbol	Name	Description
1	$\overline{\text{RST}}$	Reset input	Resets when low. When not used, reset is performed as required by internal logic.
2	RDD	F2F pattern I/O	Monitor input/output of F2F pattern reformed magnetic head signal.
3	PSO	Peak sense output	A resistor and capacitor are connected in parallel between PSI and PSO to set the negative feedback impedance of the peak sense circuit.
4	PSI	Peak sense input	Refer to PSO and AMP
5	AMP	Amp output	A resistor and capacitor are connected between PSI and AMP to set the peak sense circuit.
6	HD2	Amp (+) input	The magnetic head is connected between HD1 and HD2.
7	HD1	Amp (-) input	Same as above.
8	GND	GND	
9	$\overline{\text{RCL}}$	Read clock output	Clock output after F2F demodulation.
10	$\overline{\text{RDP}}$	Read data pulse output	Data output after F2F demodulation.
11	$\overline{\text{CLS}}$	Card loading signal output	Becomes low while a card is running.
12	BSL	Ignore bit select input	2 bit are ignored when low, 8 bits when high.
13	CX2	Oscillator capacitance	A capacitor is connected between CX1 and CX2 to set the oscillator frequency.
14	CX1	Oscillator capacitance	Same as above
15	RX	Oscillator resistance	A resistor is connected between V _{CC} and RX to set the oscillator current.
16	V _{CC}	Power supply	

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TIMING DIAGRAM

ABSOLUTE MAXIMUM RATINGS ($T_a = -20 \sim +75^\circ\text{C}$, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
V_{cc}	Supply voltage		$-0.5 \sim +6$	V
V_i	Input voltage	RST, PDD, BSL	$-0.5 \sim V_{cc}$	V
V_o	Output voltage	When CLS, RDP and RCL are high	$-0.5 \sim V_{cc}$	V
P_d	Power dissipation		150	mW
T_{opr}	Operating temperature		$-20 \sim +75$	$^\circ\text{C}$
T_{stg}	Storage temperature		$-55 \sim +125$	$^\circ\text{C}$

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RECOMMENDED OPERATING CONDITIONS (T_a = -20~+75°C, unless otherwise noted)

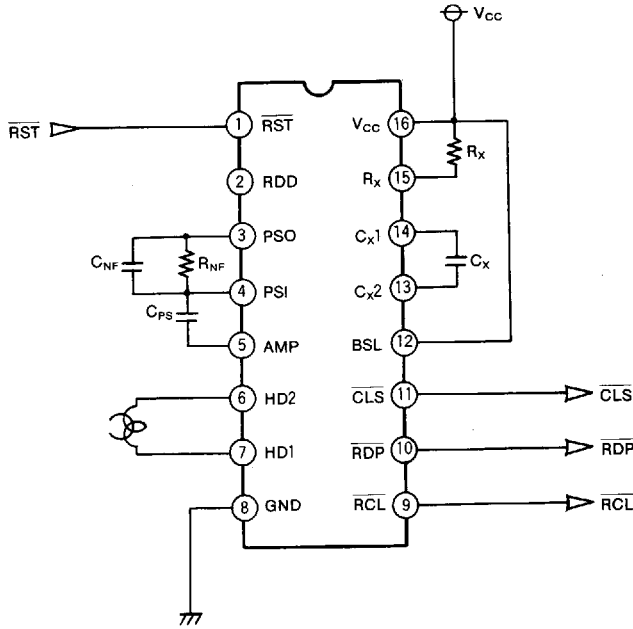
Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
V _{CC}	Supply voltage	4.5	5	5.5	V
V _{IH}	High-level input voltage	RST, RDD, BSL		V _{CC}	V
V _{IL}	Low-level input voltage	RST, RDD, BSL		0.8	V
I _{OL}	Low-level output current	CLS, RDP, RCL		16	mA
V _{OH}	High-level output voltage	When CLS, RDP and RCL are high.		V _{CC}	V
V _{ID}	Differential input voltage	HD1, HD2		80	mV _{PP}
f _{IN}	Input frequency	HD1, HD2		20	kHz
f _{OSC}	Oscillator frequency	$f_{osc} = \frac{1}{T_{osc}} = \frac{1}{2R_x C_x}$			kHz
R _X			15		kΩ
C _X	When recording density is 210 BPI		68		pF
C _{PS}	When recording density is 210 BPI		0.022		μF
C _{NF}	When recording density is 210 BPI		1000		pF
R _{NF}	When recording density is 210 BPI		680		kΩ

ELECTRICAL CHARACTERISTICS (T_a = -20~+75°C, unless otherwise noted)

Symbol	Parameter		Test conditions	Test circuit	Limits			Unit
					Min	Typ	Max	
I _{CC}	Circuit current	V _{CC}	V _{CC} =5.5V, V _{IN} =80mV _{PP} , f _{IN} =20kHz	1			25	mA
I _{IL}	Low-level input current	RST, RDD, BSL	V _{CC} =5.5V, V _{IL} =0.4V	5	-50		-200	μA
I _{IH}	High-level input current	RST, RDD, BSL	V _{CC} =5.5V, V _{IN} =5.5V	5			40	μA
V _{OL}	Low-level output voltage	CLS, RDP, RCL	V _{CC} =4.5, I _{OL} =16mA	6			0.4	V
I _{OL}	High-level output current	CLS, RDP, RCL	V _{CC} =5.5V, V _{OH} =5.5V	6			200	μA
R _{IN}	Input resistance	HD1, HD2	V _{CC} =5V, ΔV _{IN} =40mV	3	1.7		4.2	kΩ
V _R	Reference voltage	AMP	V _{CC} =5V	4	2.25		2.75	V
G _{V1}	Voltage gain 1	Amplifier circuit	V _{CC} =5V, V _{IN} =80mV _{PP} , f _{IN} =1kHz	2	24		30	V/V
G _{V2}	Voltage gain 2	Amplifier circuit	V _{CC} =5V, V _{IN} =80mV _{PP} , f _{IN} =20kHz	2	21		30	V/V
V _{OPP}	Maximum output voltage	Amplifier circuit	V _{CC} =5V, f _{IN} =20kHz	2	2.6			V _{PP}
I _{IB}	Input bias current	PSI	V _{CC} =5V	3			-0.2	μA
V _{CL}	Clamp voltage	Peak sense circuit	V _{CC} =5V, V _{IN} =80mV _{PP} , f _{IN} =1mkHz	1	0.8		2.4	V _{PP}
V _{TH}	Threshold voltage	Waveform regenerator circuit	V _{CC} =5V	4	±0.15		±0.26	V
DF	Duty factor	Peak sense circuit	V _{CC} =5V, V _{IN} =2.5mV _{PP} , f _{IN} =1kHz	1	40		60	%
f _{OSC}	Oscillator frequency	Oscillator circuit	V _{CC} =5V, R _X =15kΩ, C _X =68pF	4	380		600	kHz
T _{d1}	Delay time 1		V _{CC} =5V	7			T _{osc} +2	μs
T _{d2}	Delay time 2		V _{CC} =5V	7			3T _{osc} +2	μs
T _{d3}	Delay time 3		V _{CC} =5V	7			3T _{osc} +4	μs
T _{d4}	Delay time 4		V _{CC} =5V	7			12294T _{osc} +0.5	μs

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APPLICATION EXAMPLE

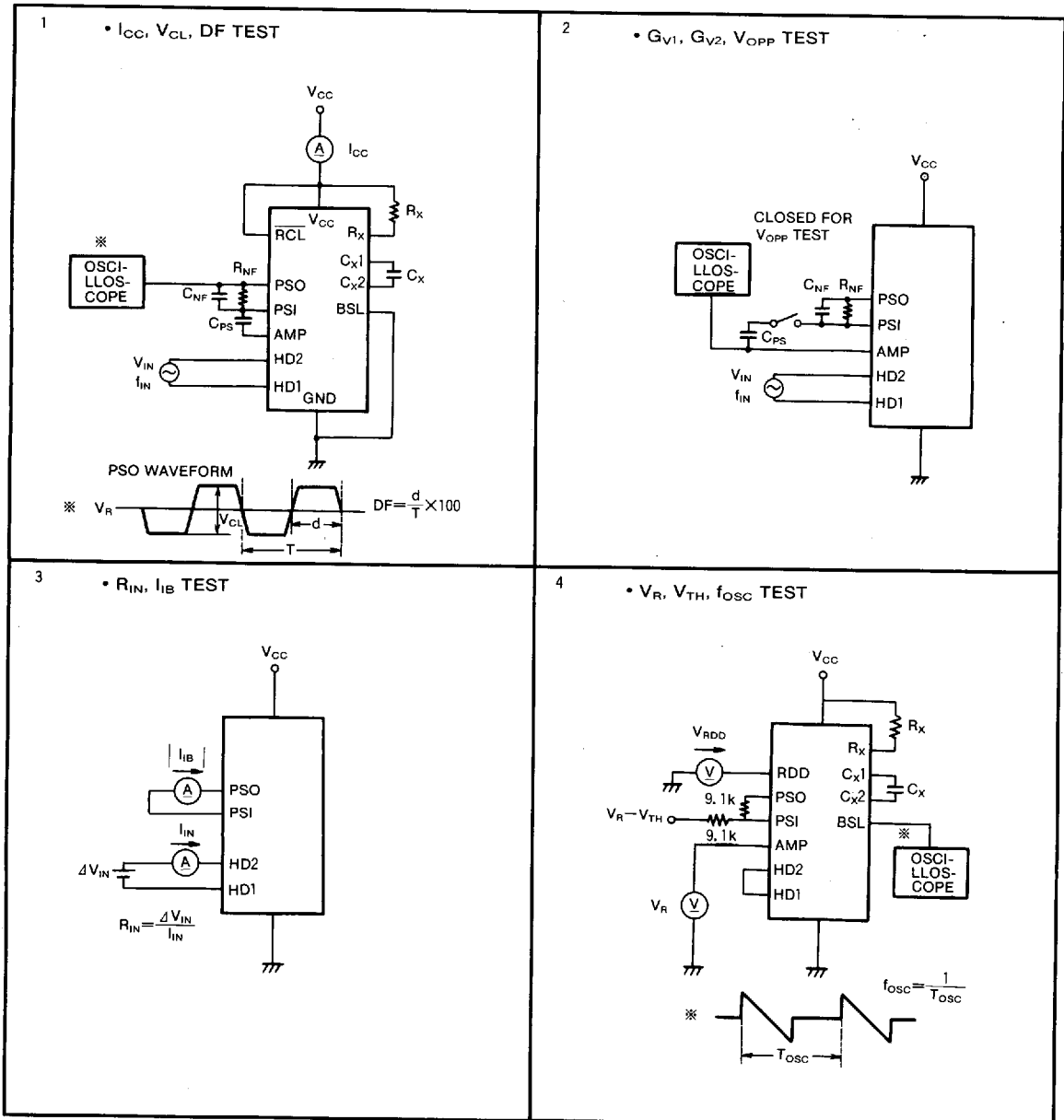


Note : The following procedure allows RDD to be used as an input.

- 1) Short circuit HD1 and HD2.
- 2) Leave AMP and PSO open.
- 3) Connect resistor R_{Pg} ($5k\Omega$ to $50k\Omega$) between PSI and GND.

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TEST CIRCUIT ($R_x=15k\Omega$, $C_x=68pF$, $C_{PS}=0.022\mu F$, $C_{NF}=1000pF$, $R_{NF}=680k\Omega$, unless otherwise noted)



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