TDA8939

Zero dead time Class-D 7.5 A power comparator

Rev. 01 — 22 April 2004 Objective data sheet

1. General description

Zero dead time Class-D 7.5 A power comparator

The TDA8939 is a power comparator designed for use in a high efficiency class-D audio power amplifier system.

It contains power switches, drive logic, protection circuitry, bias circuitry and a fully differential input stage (comparator).

This device is optimized for applications in fully digital open-loop class-D audio systems (in combination with a digital PWM controller).

The TDA8939 power comparator operates with high efficiency and low dissipation. The system operates over a wide supply voltage range from ±10 V up to ±30 V.

2. Features

- Zero dead time switching
- Maximum output current 7.5 A
- Standby mode
- High efficiency
- Operating voltage from ±10 V to ±30 V (symmetrical) or 20 V to 60 V (asymmetrical)
- Low quiescent current
- High output power
- Diagnostic output
- Thermal protection, current protection and voltage protection.

3. Applications

- Television sets
- Home-sound sets
- Multimedia systems
- All mains fed audio systems
- Car audio (boosters).

PHILIPS

4. Quick reference data

Table 1: Quick reference data

V_P = ±25 V; $f_{carrier}$ = 384 kHz.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_P	supply voltage	symmetrical supply voltage	[1]	±10	±25	±30	V
		asymmetrical supply voltage		20	50	60	V
$I_{q(tot)}$	total quiescent current	no load connected; no filters; no snubbers connected		-	50	70	mA
η	efficiency	P_{rated}		-	90	-	%

[1] When the supply voltage is below ±12.5 V the PWM outputs will not be able to switch to the high side at the first PWM cycle.

5. Ordering information

Table 2: Ordering information

Type number	Package		
	Name	Description	Version
TDA8939TH	HSOP24	plastic, heatsink small outline package; 24 leads; low stand-off height	SOT566-3

6. Block diagram

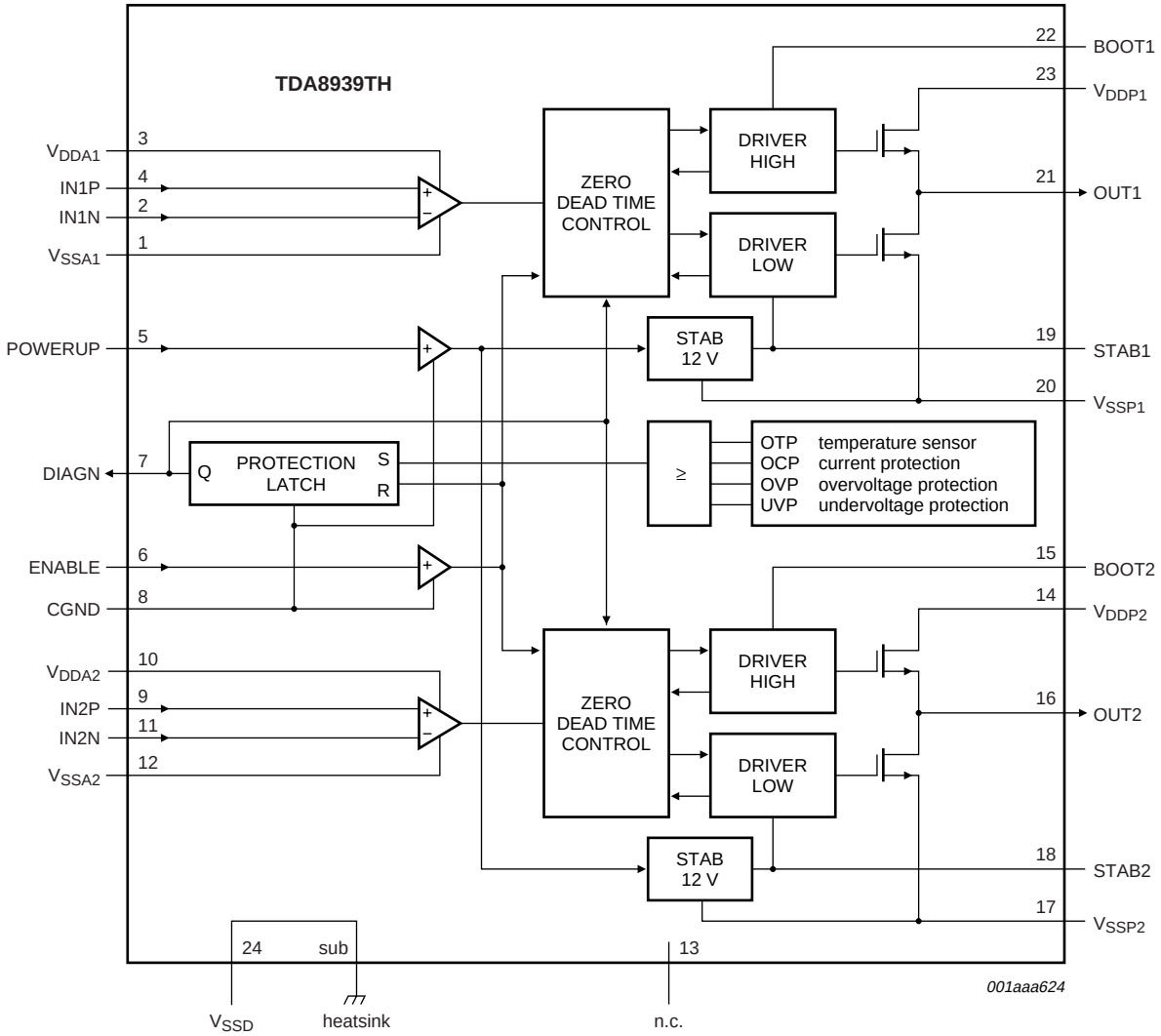


Fig 1. Block diagram.

7. Pinning information

7.1 Pinning

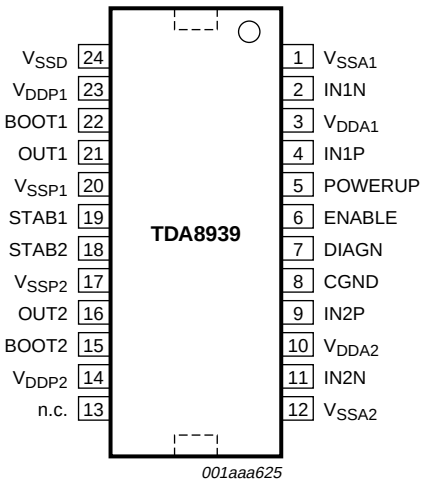


Fig 2. Pin configuration.

7.2 Pin description

Table 3: Pin description

Symbol	Pin	Description
V_{SSA1}	1	negative analog supply voltage for channel 1
IN1N	2	inverting input channel 1
V_{DDA1}	3	positive analog supply voltage for channel 1
IN1P	4	non-inverting input channel 1
POWERUP	5	enable input for switching on internal reference sources
ENABLE	6	digital enable input
DIAGN	7	digital open-drain diagnostic output for OTP, OCP, OVP and UVP (active LOW)
CGND	8	common ground, reference ground for diagnostic, enable and power-up
IN2P	9	non-inverting input channel 2
V_{DDA2}	10	positive analog supply voltage for channel 2
IN2N	11	inverting input channel 2
V_{SSA2}	12	negative analog supply voltage for channel 2
n.c.	13	not connected
V_{DDP2}	14	positive power supply voltage for channel 2
BOOT2	15	bootstrap capacitor 2
OUT2	16	PWM output channel 2
V_{SSP2}	17	negative power supply voltage for channel 2
STAB2	18	decoupling internal stabilizer for logic supply channel 2

Table 3: Pin description *...continued*

Symbol	Pin	Description
STAB1	19	decoupling internal stabilizer for logic supply channel 1
V_{SSP1}	20	negative power supply voltage for channel 1
OUT1	21	PWM output channel 1
BOOT1	22	bootstrap capacitor 1
V_{DDP1}	23	positive power supply voltage for channel 1
V_{SSD}	24	negative digital supply voltage
SUB	-	heat spreader of package; internally connected to V_{SSD}

8. Functional description

8.1 General

The TDA8939 class-D power comparator is designed for use in fully digital open-loop class-D audio applications. Excellent timing accuracy with respect to delay times and rise and fall times is achieved and one of the most important sources of distortion in a full digital open-loop audio amplifier is eliminated; the zero dead time switching concept is included. The TDA8939 contains two independent class-D output stages with high power D-MOS switches, drivers, timing and control logic. For protection a temperature sensor, a maximum current detection and overvoltage detection circuit are integrated. An internal protection latch keeps the power comparator in shut-down mode after a fault condition has been detected. External reset of the latch is required via the enable input.

8.2 Protections

Overtemperature, overcurrent and overvoltage sensors are included in the TDA8939 power comparator. In the event that the maximum temperature, maximum current or maximum supply voltage is exceeded the diagnostic output is activated (open-drain output pulled-down via external pull-up resistor).

The diagnostic output pin is activated (active LOW) in case of:

1. Overtemperature (OTP): the junction temperature (T_j) exceeds a threshold level.

2. Overcurrent (OCP): the output current exceeds the maximum output current threshold level (e.g. when the loudspeaker terminals are short-circuited it will be detected by the current protection).

3. Overvoltage (OVP): the supply voltage applied to the power comparator exceeds the maximum supply voltage threshold level.

The TDA8939 is self-protecting. If a fault condition (OTP, OCP or OVP) is detected it will pull-down the diagnostic output (pin 7), while at the same time shutting down the power stage. In case of a fault condition in one of the half-bridges or output channel the other half-bridge and output channel will also shut down. All protections trigger a latch which ensures that the power stage remains deactivated until the latch is reset again.

The latch is reset by switching the enable voltage of the power stage to LOW level. Both set (S) and reset (R) inputs of the protection latch trigger on a negative falling slope.

The block diagram of diagnostic output including OTP, OCP and OVP is illustrated in Figure 3. The diagnostic output (pin 7) is an open-drain output; a pull-up resistor connected to $+V_{pull-up}$ has to be applied externally.

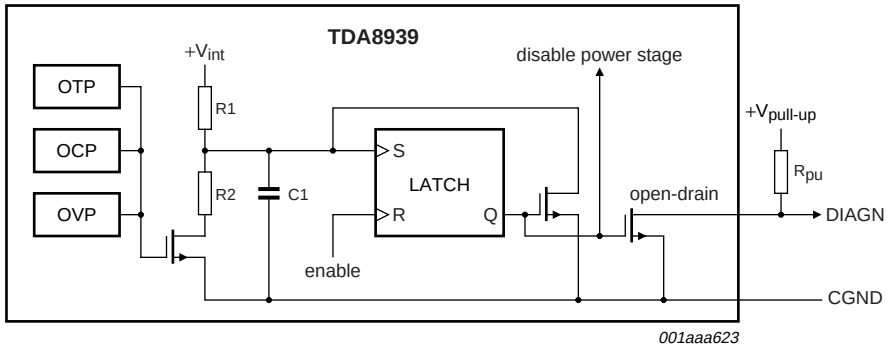


Fig 3. OCP, OTP and OVP protection: S/R latch.

8.3 Interfacing between controller and the TDA8939

For interfacing with a digital PWM controller IC or microcontroller in the final system application the following inputs and outputs are available see Table 4 and 5.

8.3.1 Inputs

Table 4: Inputs

Pin name	Pin number	Description
IN1P and IN1N	4 and 2	full differential input for output channel 1; referenced with respect to each other; common mode referenced to V_{SSD}
IN2P and IN2N	9 and 11	full differential input for output channel 2; referenced with respect to each other; common mode referenced to V_{SSD}
POWERUP	5	standby switch; reference to CGND; at a LOW level the device is in standby mode and consumes a very low standby current. At HIGH level the device is DC-biased (switch-on of internal reference voltages and currents). The device can only be switched to full operating mode by the enable input, if the power-up input is at HIGH level.
ENABLE	6	mode switch; reference to CGND; at a LOW level the power D-MOS switches are open and the PWM output is floating; all internal logic circuits are in reset condition. At a HIGH level the power comparator is fully operational if the power-up input is also at a HIGH level. In this condition the power comparator outputs are controlled by the input pins (IN1P, IN1N, IN2P and IN2N); see also Figure 6. The enable input signal is also used to reset the protection latch.

8.3.2 Outputs

Table 5: Outputs

Pin name	Pin number	Description
DIAGN	7	Digital open-drain output; referenced to CGND; output indicates the following fault conditions: OTP, OCP, OVP and UVP. In the event of a fault condition the output is pulled to the CGND voltage (active LOW). If the diagnostic output functionality is used in the application, an external pull-up resistor is required.

8.3.3 Reference voltages

Table 6: Reference voltages

Pin name	Pin number	Description
CGND	8	common ground; reference ground for diagnostic output, enable input and power-up input
V_{SSD}	24	negative digital supply; reference ground digital circuits. The V_{SSD} pin should be connected to V_{SS} voltage in the application. Internally the V_{SSD} pin is connected to the V_{SSAx} and V_{SSPx} (e.g. V_{SSA1} and V_{SSP1}) via an ESD protection diode.

8.4 Start-up timing

Power comparator mode selection:

- Standby mode: when pin POWERUP is LOW, the power comparator is in standby mode, independent of the signal on the enable input
- Reset mode: when pin POWERUP is HIGH, the status of the power comparator is controlled by pin ENABLE; if pin ENABLE is LOW, the status of the power stage is reset and the outputs are floating
- Operating mode: when pin ENABLE is HIGH, the power stage is in operating mode.

To ensure correct start-up of the power stage, the enable input should never be HIGH when the power-up input is LOW. Before switching to operating mode, the amplifier should first be switched to reset mode.

Remark: It is possible to directly connect the power-up input to the positive supply line (e.g. V_{DDA1}). As soon as the supply voltage is applied the device will be DC-biased (reset mode).

Table 7: Mode selection

Pin		Mode
POWERUP	**ENABLE**	
LOW	X	standby
HIGH	LOW	reset
HIGH	HIGH	operating

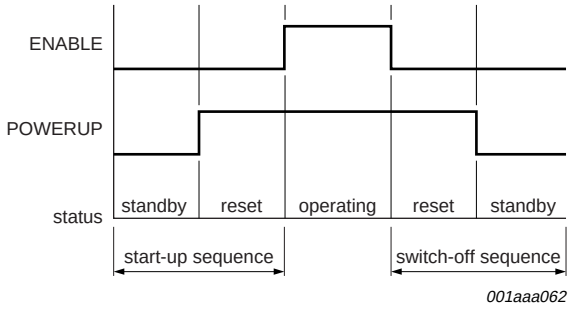


Fig 4. Mode selection timing diagram.

9. Limiting values

Table 8: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_p	supply voltage		-	60	V
I_{ORM}	repetitive peak current on output pins		-	7.5	A
T_{stg}	storage temperature		–55	+150	°C
T_{amb}	ambient temperature		–40	+85	°C
T_{vj}	virtual junction temperature		-	150	°C

10. Thermal characteristics

Table 9: Thermal characteristics

Symbol	Parameter	Conditions	Value	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	40	K/W
$R_{th(j-c)}$	thermal resistance from junction to case		1.3	K/W

11. Static characteristics

Table 10: Static characteristics

V_P = ±25 V; $f_{carrier}$ = 384 kHz; T_{amb} = 25 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Supplies							
V_P	supply voltage	symmetrical supply voltage	[1]	±10	±25	±30	V
		asymmetrical supply voltage		20	50	60	V
I_q	quiescent current	no load; no filters; no snubbers connected		-	50	70	mA
		reset mode		-	10	20	mA
I_{stb}	standby current	standby mode		-	120	170	µA
Internal stabilizer logic supplies							
V_{STAB1}, V_{STAB2}	stabilizer output voltage			11	12	15	V
Comparator full differential input stage: pins IN1P, IN1N, IN2P and IN2N							
$V_{i(diff)}$	differential input voltage range			1	3.3	12	V
$V_{i(com)}$	common mode input voltage			V_{SSA1}	-	V_{DDA1} − 7.5	V
$I_{i(bias)}$	input bias current			-	-	10	µA
Common ground: pin CGND							
V_{CGND}	common ground reference voltage	asymmetrical supply		-	0	-	V
Diagnostic output: pin DIAGN							
V_{OL}	LOW-level output voltage	referenced to CGND; I_{DIAGN} = 1 mA	[2]	0	-	1	V
$V_{pu(max)}$	maximum pull-up voltage	referenced to CGND		-	-	12	V
I_L	leakage current	no error condition		-	-	50	µA
Enable input: pin ENABLE							
V_{IL}	LOW-level input voltage	referenced to CGND		0	-	1	V
V_{IH}	HIGH-level input voltage	referenced to CGND		3	-	12	V
I_I	input current	V_{ENABLE} = 12 V		-	70	140	µA
Power-up input: pin POWERUP							
V_{IL}	LOW-level input voltage	referenced to CGND		0	-	0.5	V
V_{IH}	HIGH-level input voltage	referenced to CGND		3	-	V_{DDA}	V
V_{hys}	hysteresis voltage			-	0.3	-	V
I_I	input current	$V_{POWERUP}$ = 12 V		-	70	140	µA

Table 10: Static characteristics *...continued*

V_P = ±25 V; $f_{carrier}$ = 384 kHz; T_{amb} = 25 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Temperature protection						
T_{diag}	diagnostic trigger temperature	$V_{DIAGN} = V_{OL}$	150	-	-	°C
Overcurrent protection						
I_{prot}	diagnostic and protection trigger current	$V_{DIAGN} = V_{OL}$	7.5	-	-	A
Overvoltage protection						
$V_{DD(max)}$	diagnostic and protection trigger maximum supply voltage	$V_{DIAGN} = V_{OL}$	±30	±33	-	V

[1] When the supply voltage is below ±12.5 V the PWM outputs will not be able to switch to the high side at the first PWM cycle.

[2] OTP, OCP and/or OVP protection activated.

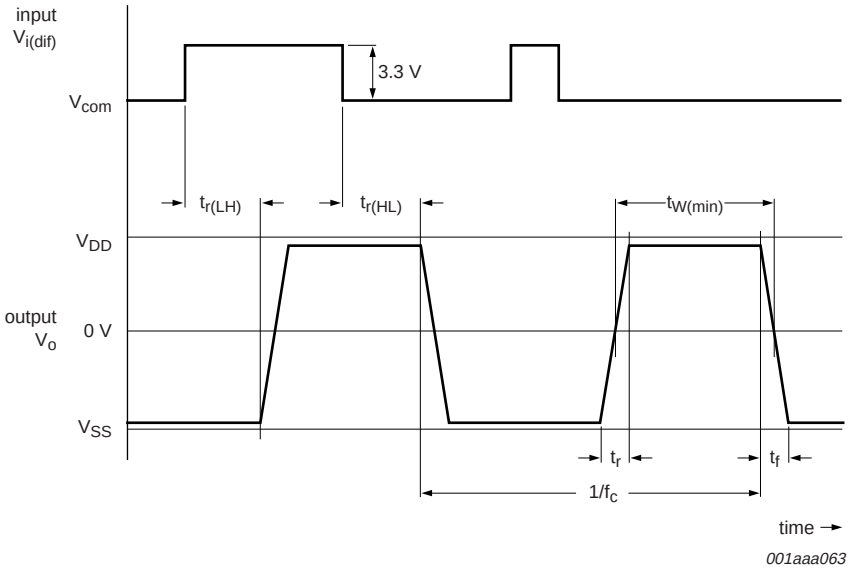
12. Dynamic characteristics

Table 11: Dynamic characteristics

V_P = ±25 V; T_{amb} = 25 °C; $f_{carrier}$ = 384 kHz; see also Figure 8 for definitions.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
PWM output							
t_r	rise time output voltage			-	20	-	ns
t_f	fall time output voltage			-	20	-	ns
t_{dead}	dead time			-	0	-	ns
$t_{r(LH)}$	large signal response time LOW-to-HIGH transition at output	input amplitude = 3.3 V		-	90	-	ns
$t_{r(HL)}$	large signal response time HIGH-to-LOW transition at output	input amplitude = 3.3 V		-	90	-	ns
$t_{W(min)}$	minimal pulse width			-	150	-	ns
R_{DS_ON}	R_{DS_ON} output transistors			-	0.2	0.3	Ω
η	efficiency	$P_o = P_{rated}$	[1]	-	-	90	-

[1] Output power measured across the loudspeaker load. Power measurement based on indirect measurement by measuring the R_{DS_ON}.



$V_{common} = V_{SSA1}$ to $(V_{DDA1} - 7.5\ V)$.

t_{dead} cannot be represented in the figure.

Response times depend on input signal amplitude.

The second input pulse is not reproduced with same pulse width by the output due to minimum pulse width limitation.

Fig 5. Timing diagram PWM output.

13. Output power estimation

The maximum achievable output power is not only determined by the power comparator characteristics, but by the total system application.

The following application blocks determine the maximum achievable output power:

Power comparator:

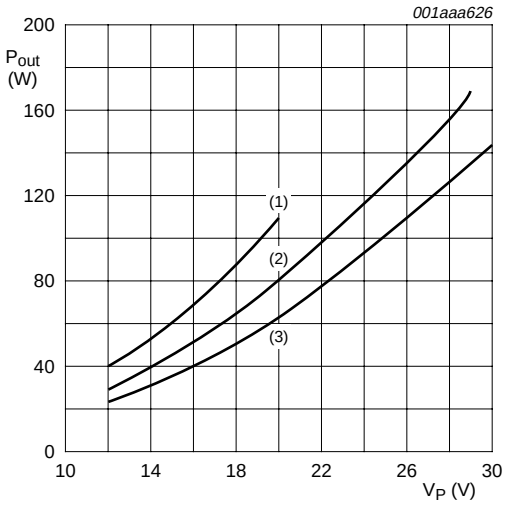
- Minimum pulse width
- Series resistances: R_{DS_ON}, bond wires, printed-circuit board tracks, series resistance of the coil, etc.

System application:

- Power supply voltage
- Load impedance
- Controller characteristics: maximum modulation depth and carrier frequency.

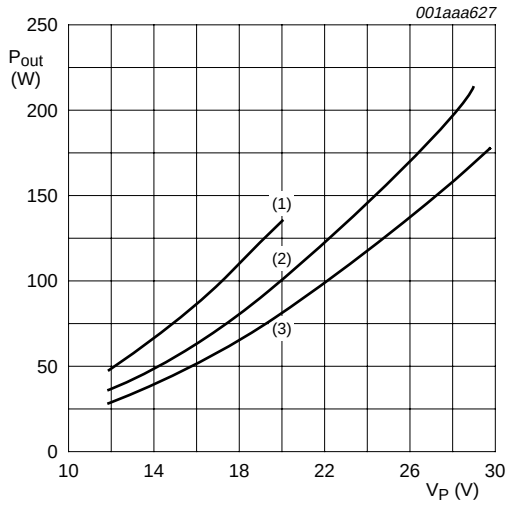
In Figure 6 an estimate is given for the output power in full-bridge application as function of the (symmetrical) supply voltage for different values of the load-impedance. The following variables are taken into account:

- Minimum pulse width: 150 ns
- Total series resistance: 0.4 Ω
- Carrier frequency: 384 kHz.



(1) Z_L = 4 Ω.
(2) Z_L = 6 Ω.
(3) Z_L = 8 Ω.

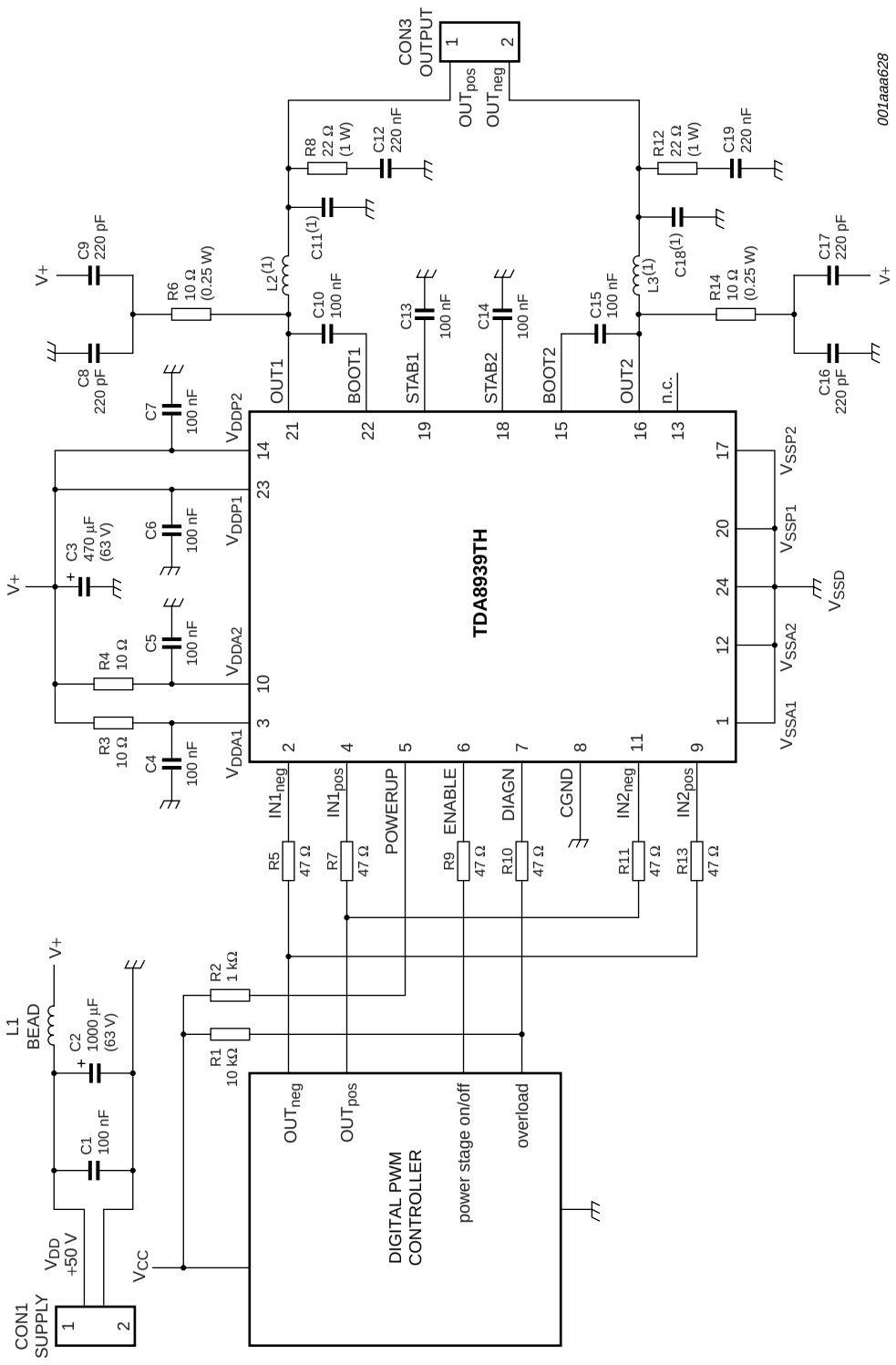
Fig 6. Output power estimation as a function of (symmetrical) supply voltage for THD = 1 %.



(1) Z_L = 4 Ω.
(2) Z_L = 6 Ω.
(3) Z_L = 8 Ω.

Fig 7. Output power estimation as a function of (symmetrical) supply voltage for THD = 10 %.

14. Application information



(1) For 8 Ω BTL and f_{corner} = 40.2 kHz: L2 = L3 = 27 µH; C11 = C18 = 470 nF.
For 8 Ω BTL and f_{corner} = 44.5 kHz: L2 = L3 = 22 µH; C11 = C18 = 470 nF.
For 4 Ω BTL and f_{corner} = 47.7 kHz: L2 = L3 = 10 µH; C11 = C18 = 1 µF.

Fig 8. Typical application diagram using a single (asymmetrical) supply voltage.

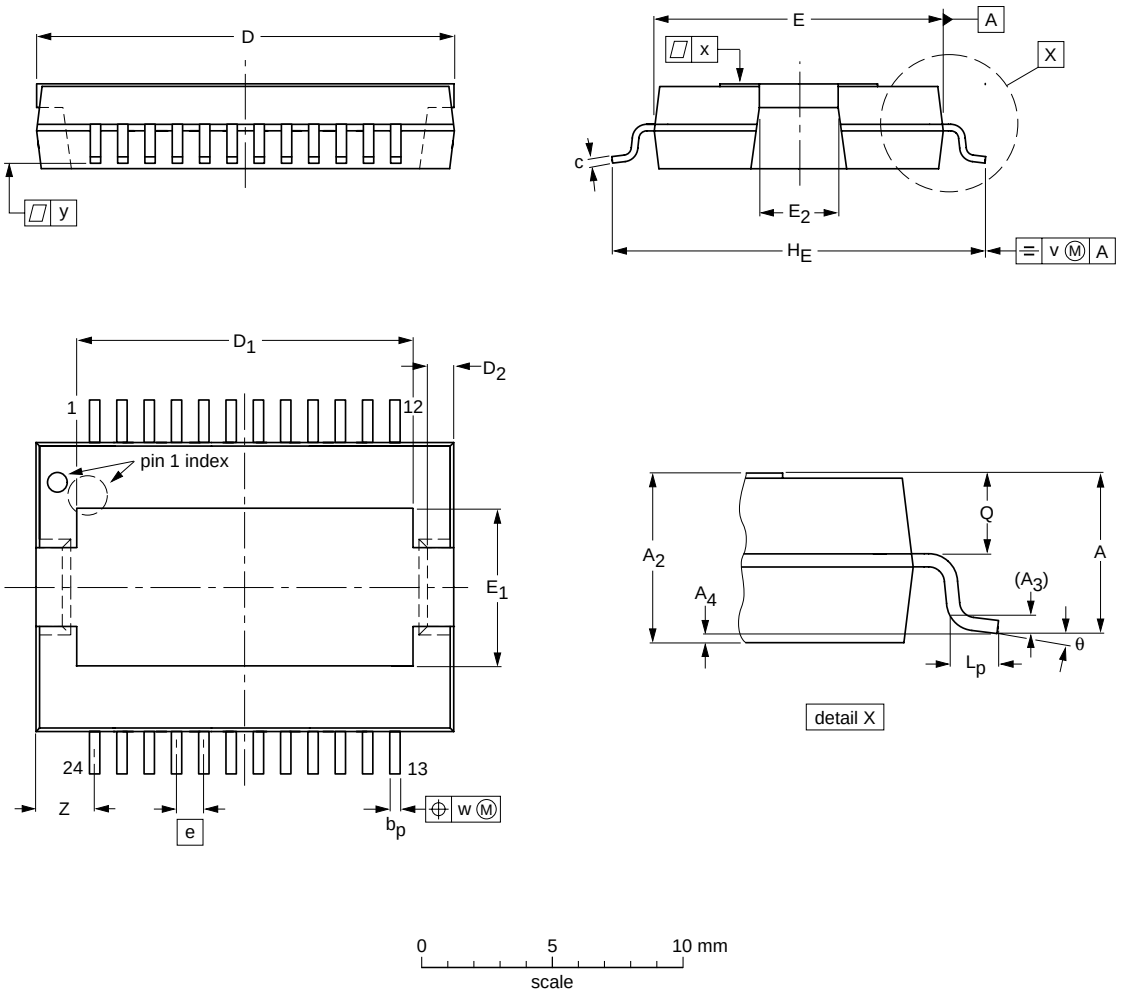
15. Test information

15.1 Quality information

The *General Quality Specification for Integrated Circuits, SNW-FQ-611* is applicable.

16. Package outline

HSOP24: plastic, heatsink small outline package; 24 leads; low stand-off height **SOT566-3**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_2	A_3	A_4(1)	b_p	c	D(2)	D_1	D_2	E(2)	E_1	E_2	e	H_E	L_p	Q	v	w	x	y	Z	θ
mm	3.5	3.5 3.2	0.35	+0.08 –0.04	0.53 0.40	0.32 0.23	16.0 15.8	13.0 12.6	1.1 0.9	11.1 10.9	6.2 5.8	2.9 2.5	1	14.5 13.9	1.1 0.8	1.7 1.5	0.25	0.25	0.03	0.07	2.7 2.2	8° 0°

Notes

1. Limits per individual lead.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT566-3						~~03-02-18~~ 03-07-23

Fig 9. Package outline.

17. Soldering

17.1 Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *Data Handbook IC26; Integrated Circuit Packages* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

17.2 Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement. Driven by legislation and environmental forces the worldwide use of lead-free solder pastes is increasing.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 270 °C depending on solder paste material. The top-surface temperature of the packages should preferably be kept:

- below 225 °C (SnPb process) or below 245 °C (Pb-free process)
  - for all BGA, HTSSON..T and SSOP..T packages
  - for packages with a thickness ≥ 2.5 mm
  - for packages with a thickness < 2.5 mm and a volume ≥ 350 mm^3 so called thick/large packages.
- below 240 °C (SnPb process) or below 260 °C (Pb-free process) for packages with a thickness < 2.5 mm and a volume < 350 mm^3 so called small/thin packages.

Moisture sensitivity precautions, as indicated on packing, must be respected at all times.

17.3 Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;

– smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

The footprint must incorporate solder thieves at the downstream end.

- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time of the leads in the wave ranges from 3 to 4 seconds at 250 °C or 265 °C, depending on solder material applied, SnPb or Pb-free respectively.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

17.4 Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

17.5 Package related soldering information

Table 12: Suitability of surface mount IC packages for wave and reflow soldering methods

Package [1]	Soldering method	
	Wave	Reflow [2]
BGA, HTSSON..T [3], LBGA, LFBGA, SQFP, SSOP..T [3], TFBGA, USON, VFBGA	not suitable	suitable
DHVQFN, HBCC, HBGA, HLQFP, HSO, HSOP, HSQFP, HSSON, HTQFP, HTSSOP, HVQFN, HVSON, SMS	not suitable [4]	suitable
PLCC [5], SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended [5] [6]	suitable
SSOP, TSSOP, VSO, VSSOP	not recommended [7]	suitable
CWQCCN..L [8], PMFP [9], WQCCN..L [8]	not suitable	not suitable

[1] For more detailed information on the BGA packages refer to the *(LF)BGA Application Note* (AN01026); order a copy from your Philips Semiconductors sales office.

[2] All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods*.

[3] These transparent plastic packages are extremely sensitive to reflow soldering conditions and must on no account be processed through more than one soldering cycle or subjected to infrared reflow soldering with peak temperature exceeding 217 °C ± 10 °C measured in the atmosphere of the reflow oven. The package body peak temperature must be kept as low as possible.

[4] These packages are not suitable for wave soldering. On versions with the heatsink on the bottom side, the solder cannot penetrate between the printed-circuit board and the heatsink. On versions with the heatsink on the top side, the solder might be deposited on the heatsink surface.

[5] If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.

[6] Wave soldering is suitable for LQFP, QFP and TQFP packages with a pitch (e) larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.

[7] Wave soldering is suitable for SSOP, TSSOP, VSO and VSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

[8] Image sensor packages in principle should not be soldered. They are mounted in sockets or delivered pre-mounted on flex foil. However, the image sensor package can be mounted by the client on a flex foil by using a hot bar soldering process. The appropriate soldering profile can be provided on request.

[9] Hot bar soldering or manual soldering is suitable for PMFP packages.

18. Revision history

Table 13: Revision history

Document ID	Release date	Data sheet status	Change notice	Order number	Supersedes
TDA8939_1	20040422	Objective data sheet	-	9397 750 13023	-

19. Data sheet status

Level	Data sheet status [1]	Product status [2] [3]	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
III	Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN).

[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

20. Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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22. Contact information

For additional information, please visit: **http://www.semiconductors.philips.com**

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23. Contents

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