PM5315

SPECTRA-2488

SONET/SDH PAYLOAD EXTRACTOR/ALIGNER FOR 2488 MBIT/S

Data Sheet

Proprietary and Confidential

Released

Issue 4: November, 2001

Legal Information

Copyright

PMC-1990821 (R4)

Disclaimer

Trademarks

Patents

The technology discussed is protected by one or more of the following Patents

U.S. Patent No. 5,640,398

Canadian. Patent No. 2,161,921

Relevant patent applications and other patents may also exist.

Contacting PMC-Sierra

PMC-Sierra
8555 Baxter Place Burnaby, BC
Canada V5A 4V7

Tel: +1(604) 415-6000
Fax: +1(604) 415-6200

Document Information: document@pmc-sierra.com
Corporate Information: info@pmc-sierra.com
Technical Support: apps@pmc-sierra.com
Web Site: http://www.pmc-sierra.com

Table of Contents

List of Registers

List of Figures

List of Tables

1 Definitions

The following table defines the abbreviations for the SPECTRA-2488.

SRLI	SONET/SDH Receive Line Interface
RRMP	Receive Regenerator Multiplexer Processor
RHPP	Receive High order Path Processor
RTTP	Received Tail Trace Processor
STLI	SONET/SDH Transmit Line Interface
TRMP	Transmit Regenerator Multiplexer Processor
THPP	Transmit High order Path Processor
TTTP	Transmit Tail Trace Processor
SVCA	SONET/SDH Virtual Container Aligner
STSI	SONET/SDH Time Slot Interchange
PRGM	PRBS Generator and Monitor
TAPI	Transmit Add bus Pointer Interpreter
SARC	SONET/SDH Alarm Reporting Controller
SBER	SONET/SDH Bit Error Rate

2 Features

2.1 General

- Single channel STS-48/STM-16 or four channel STS-12/STM-4 SONET/SDH PAYLOAD EXTRACTOR/ALIGNER.

- Monolithic SONET/SDH PAYLOAD EXTRACTOR/ALIGNER for use in
  single STS-48c (STM-16/AU4-16c) or
  single STS-48 (STM-16/AU4-12c/AU4-8c/AU4-4c/AU4/AU3/TU3) or
  quad STS-12c (STM-4/AU4-4c) or
  quad STS-12 (STM-4/AU4/AU3/TU3)
  interface applications, operating at serial interface speeds of up to 2488 Mbit/s.

- In single STS-48/STM-16 mode supports a duplex 16-bit 155.52 MHz differential PECL line side interface for direct connection to external clock recovery, clock synthesis and serializer-deserializer components.

- In quad STS-12/STM-4 mode supports four duplex 8-bit 77.76 MHz TTL compatible line side interface for direct connection to external clock recovery, clock synthesis and serializer-deserializer components.

- Provides termination for SONET Section, Line and Path overhead or SDH Regenerator Section, Multiplexer Section and High Order Path overhead.

- Translate AU4/3x(TUG3/TU3/VC3) into 3x(AU3/VC3) from the receive side to the DROP TelecomBus.

- Translate 3x(AU3/VC3) into AU4/3x(TUG3/TU3/VC3) from the ADD TelecomBus to the transmit side.

- In single STS-48/STM-16 mode provides a 32-bit 77.76 MHz ADD and DROP TelecomBus.

- In quad STS-12/STM-4 mode provides four 8-bit 77.76 MHz ADD and DROP TelecomBuses.

- Maps SONET/SDH payloads to system timing, accommodating plesiochronous timing offsets between the line and system timing references, through pointer processing.

- Provides Time Slot Interchange (TSI) function at the ADD and DROP TelecomBuses for grooming any legal mix of SONET/SDH paths.

- Supports line loopback from the line side receive stream to the transmit stream and diagnostic loopback from the ADD TelecomBus interface to the DROP TelecomBus interface.

- Provides a standard 5 signal IEEE 1149.1 JTAG test port for boundary scan board test purposes.

- Provides a generic 16-bit microprocessor bus interface for configuration, control, and status monitoring.
- Low power 1.8 V CMOS core logic with 3.3 V CMOS/TTL compatible digital inputs and digital outputs. PECL inputs and outputs are 3.3V compatible.
- 520 pin Super BGA package.

2.2 SONET Section and Line / SDH Regenerator and Multiplexer Section

- Frames to the SONET/SDH receive stream and inserts the framing bytes (A1, A2) and the section trace byte (J0) into the transmit stream; descrambles the receive stream and scrambles the transmit stream.
- Calculates and compares the bit interleaved parity (BIP) error detection codes (B1, B2) for the receive stream. Calculates and inserts B1, B2 in the transmit stream. Accumulates near end errors (B1, B2) and far end errors (M1). Inserts line remote error indications (REI) into the M1 byte based on received B2 errors.
- Detects signal degrade (SD) and signal fail (SF) threshold crossing alarms based on received B2 errors.
- The entire SONET/SDH transport overhead is extracted to and inserted from dedicated pins. The transport overhead bytes may be sourced from internal registers or from bit serial transport overhead input stream. Transport overhead insertion may also be disabled.
- In single STS-48/STM-16 mode, extracts and serializes on dedicated pins the data communication channels (D1-D3, D4-D12) and inserts the corresponding signals into the transmit stream.
- In quad STS-12/STM-4 mode, extracts and serializes on dedicated pins the data communication channels (D1-D3, D4-D12) and inserts the corresponding signals into the transmit stream for one of the four stream.
- Extracts and filters the automatic protection switch (APS) channel (K1, K2) bytes into internal registers. Inserts the APS channel into the transmit stream.
- Extracts and filters the synchronization status message (S1) byte into an internal register. Inserts the synchronization status message byte into the transmit stream.
- Extracts a 16 or 64 byte section trace (J0) message using an internal register bank for the receive stream. Detects an unstable message or mismatch message with an expected message. Provides access to the accepted message via the microprocessor port. Inserts a 16 byte or 64 byte section trace (J0) message using an internal register bank for the transmit stream.
- Detects loss of signal (LOS), out of frame (OOF), loss of frame (LOF), line remote defect indication (RDI), line alarm indication signal (AIS), and protection switching byte failure alarms on the receive stream.

- Provides a transmit and receive ring control port, allowing alarms and status to be passed between mate SPECTRA-2488's for ring-based add drop multiplexer and line multiplexer applications.
- Configurable to force Line AIS in the transmit stream.
- Provides automatic transmit line RDI insertion following detection of various received alarms (LOS, LOF, LAIS, SD, SF, STIM, STIU).
- Provides automatic DROP bus line AIS insertion following detection of various received alarms (LOS, LOF, LAIS, SD, SF, STIM, STIU).

2.3 SONET Path / SDH High Order Path

- Interprets any legal mix of STS (AU and TU3) pointer bytes (H1, H2, and H3), extracts the synchronous payload envelope(s) and processes the path overhead for the receive stream.
- Generates any legal mix of STS (AU and TU3) pointer bytes (H1, H2, and H3) and inserts the path overhead for the transmit stream.
- Detects loss of pointer (LOP), path alarm indication signal (PAIS) and path (normal and enhanced) remote defect indication (RDI) for the receive stream. Optionally inserts path alarm indication signal (PAIS) and path remote defect indication (RDI) in the transmit stream.
- Extracts and insert the entire SONET/SDH path overhead to and from dedicated pins. The path overhead bytes may be sourced from internal registers or from bit serial path overhead input stream. Path overhead insertion may also be disabled.
- Extracts the received path payload label (C2) byte into an internal register and detects for payload label unstable (PLU), payload label mismatch (PLM), payload unequipped (UNEQ) and payload defect indication (PDI). Inserts the path payload label (C2) byte from an internal register for the transmit stream.
- Extracts a 16 byte or 64 byte path trace (J1) message using an internal register bank for the receive stream. Detects an unstable message or mismatch message with an expected message. Provides access to the captured, accepted and expected message via the microprocessor port. Inserts a 16 byte or 64 byte path trace (J1) message using an internal register bank for the transmit stream.
- Calculates received path BIP-8 and counts received path BIP-8 errors for performance monitoring purposes. BIP-8 errors are selectable to be treated on a bit basis or block basis. Optionally calculates and inserts path BIP-8 error detection codes for the transmit stream.
- Counts received path remote error indications (REI) for performance monitoring purposes. Optionally inserts the path REI count into the path status byte (G1) based on bit or block BIP-8 errors detected in the receive path.
- Provides access via path overhead ports to all the overhead bytes needed to implement Tandem Connections.
- Ring control port provides communication of path REI and path RDI alarms to the transmit stream of a mate SPECTRA-2488 in the returning direction.

- Provides automatic transmit path RDI and path Enhanced RDI insertion following detection of various received alarms (LAIS, LOP, LOPC, PAIS, PAISC, PTIM, PTIU, PLM, PLU, UNEQ, PDI).
- Provides automatic DROP bus path AIS insertion following detection of various received alarms (LAIS, LOP, LOPC, PAIS, PAISC, PTIM, PTIU, PLM, PLU, UNEQ, PDI).

2.4 System Side Interfaces

- In single STS-48/STM-16 mode provides a single 32-bit 77.76 MHz TelecomBus interface.
- In quad STS-12/STM-4 mode provides four 8-bit 77.76 MHz TelecomBus interfaces.
- TelecomBus interfaces indicates/accepts the location of the section trace byte (J0), optionally the path trace byte(s) (J1) and all synchronous payload envelope bytes in the byte serial stream.
- TelecomBus accommodates phase and frequency differences between the receive/transmit streams and the DROP/ADD busses via pointer adjustments.
- Provides TSI function to interchange or groom paths at the Telecom ADD and DROP buses.

3 Applications

- SONET/SDH Add Drop Multiplexers
- SONET/SDH Terminal Multiplexers
- SONET/SDH Line Multiplexers
- SONET/SDH Cross Connects
- SONET/SDH Tandem Path Termination Equipment
- SONET/SDH Test Equipment
- Switches and Hubs
- Routers

4 References

1. American National Standard for Telecommunications - Digital Hierarchy - Optical Interface Rates and Formats Specification, ANSI T1.105-1991.

2. American National Standard for Telecommunications - Layer 1 In-Service Digital Transmission Performance Monitoring, T1X1.3/93-005R1, April 1993.

3. American National Standard for Telecommunications – Synchronous Optical Network (SONET) – Tandem Connection Maintenance, ANSI T1.105.05-1994.

4. Committee T1 Contribution, "Draft of T1.105 - SONET Rates and Formats", T1X1.5/94-033R2-1994.

5. Bell Communications Research - GR-253-CORE “SONET Transport Systems: Common Generic Criteria”, Issue 2 Revision 2, January 1999.

6. Bell Communications Research - GR-436-CORE “Digital Network Synchronization Plan”, Issue 1 Revision 1, June 1996.

7. ETS 300 417-1-1, "Generic Functional Requirements for Synchronous Digital Hierarchy (SDH) Equipment", January, 1996.

8. ITU-T Recommendation G.703 - "Physical/Electrical Characteristics of Hierarchical Digital Interfaces", 1991.

9. ITU-T Recommendation G.704 - "General Aspects of Digital Transmission Systems; Terminal Equipment - Synchronous Frame Structures Used At 1544, 6312, 2048, 8488 and 44 736 kbit/s Hierarchical Levels", July, 1995.

10. ITU, Recommendation G.707 - "Network Node Interface For The Synchronous Digital Hierarchy", 1996.

11. ITU Recommendation G.781, - “Structure of Recommendations on Equipment for the Synchronous Digital Hierarchy (SDH)”, January, 1994.

12. ITU Recommendation G.783, “Characteristics of Synchronous Digital Hierarchy (SDH) Equipment Functional Blocks”, 28 October, 1996.

13. ITU Recommendation O.151, “Error Performance measuring Equipment Operating at the Primary Rate and Above”, October, 1992.

14. ITU Recommendation I.432, “ISDN User Network Interfaces”, March 93.

5 Application Examples

The SPECTRA-2488™ device can be used in SONET/SDH network elements including switches, terminal multiplexers, and add-drop multiplexers. In such applications, the SPECTRA-2488 line interface typically interfaces to a serdes module. On the system side interface, the SPECTRA-2488 connects directly to a TelecomBus. Figure 1 shows how the SPECTRA-2488 is used to implement a 2488 Mbit/s aggregate interface. In this application, the SPECTRA-2488 performs SONET/SDH section, line and path termination and the PM5363 TUPP-622 performs tributary pointer processing and performance monitoring.

Figure 1 STS-48/STM-16 Application with 77.76 MHz Byte TelecomBus Interface

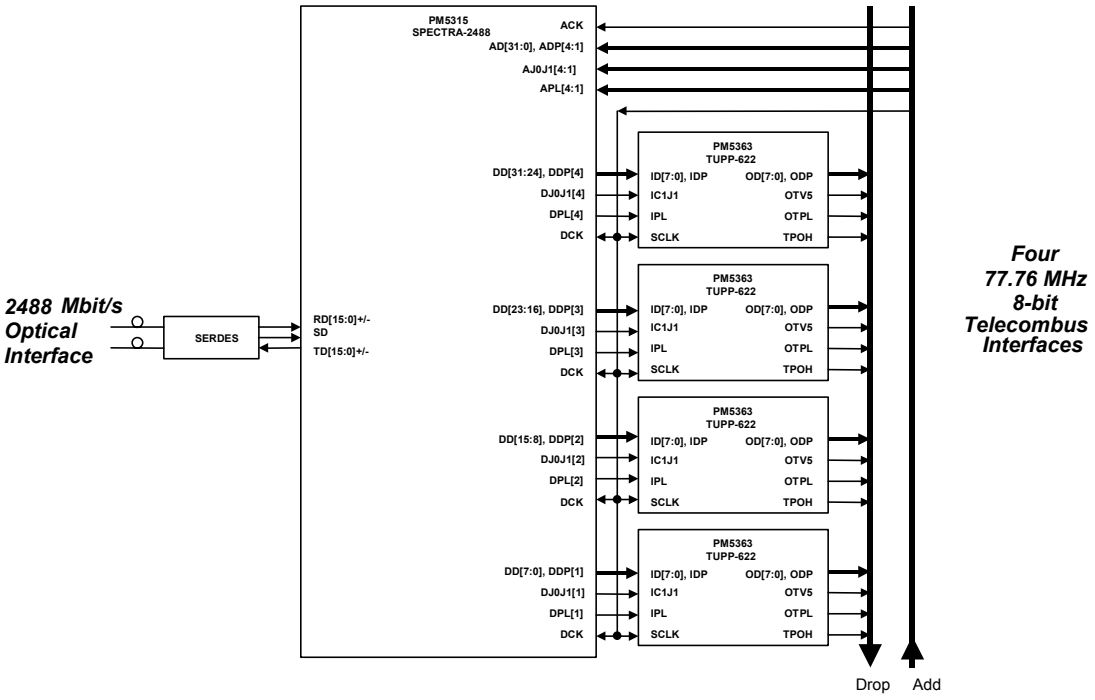
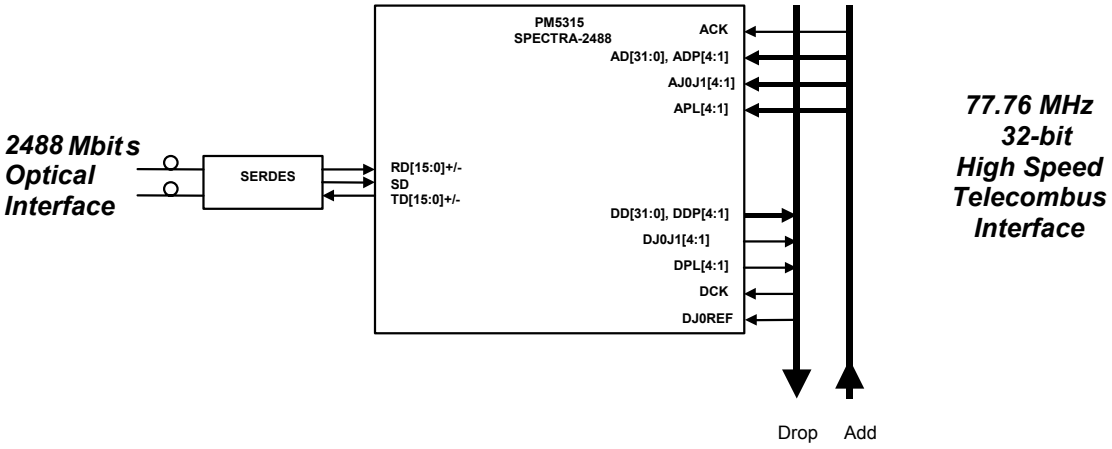


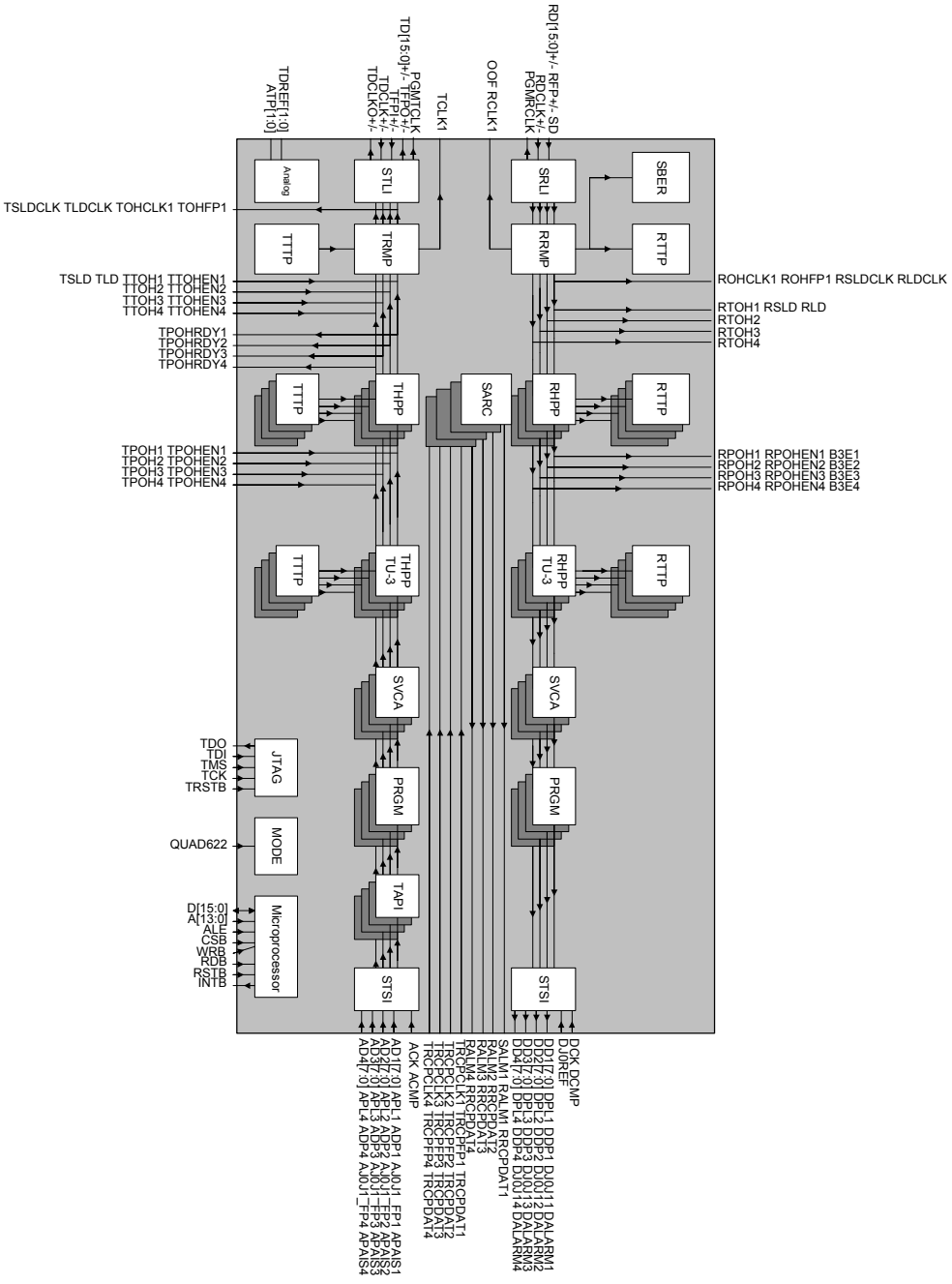
Figure 2 shows how the SPECTRA-2488 is used to implement a 2488 Mbit/s aggregate interface using a single 77.76 MHz 32 bit TelecomBus on the system side interface. In this application, the SPECTRA-2488 performs SONET/SDH section, line and path termination.

Figure 2 STS-48/STM-16 Application with 77.76 MHz 32-Bit TelecomBus Interface

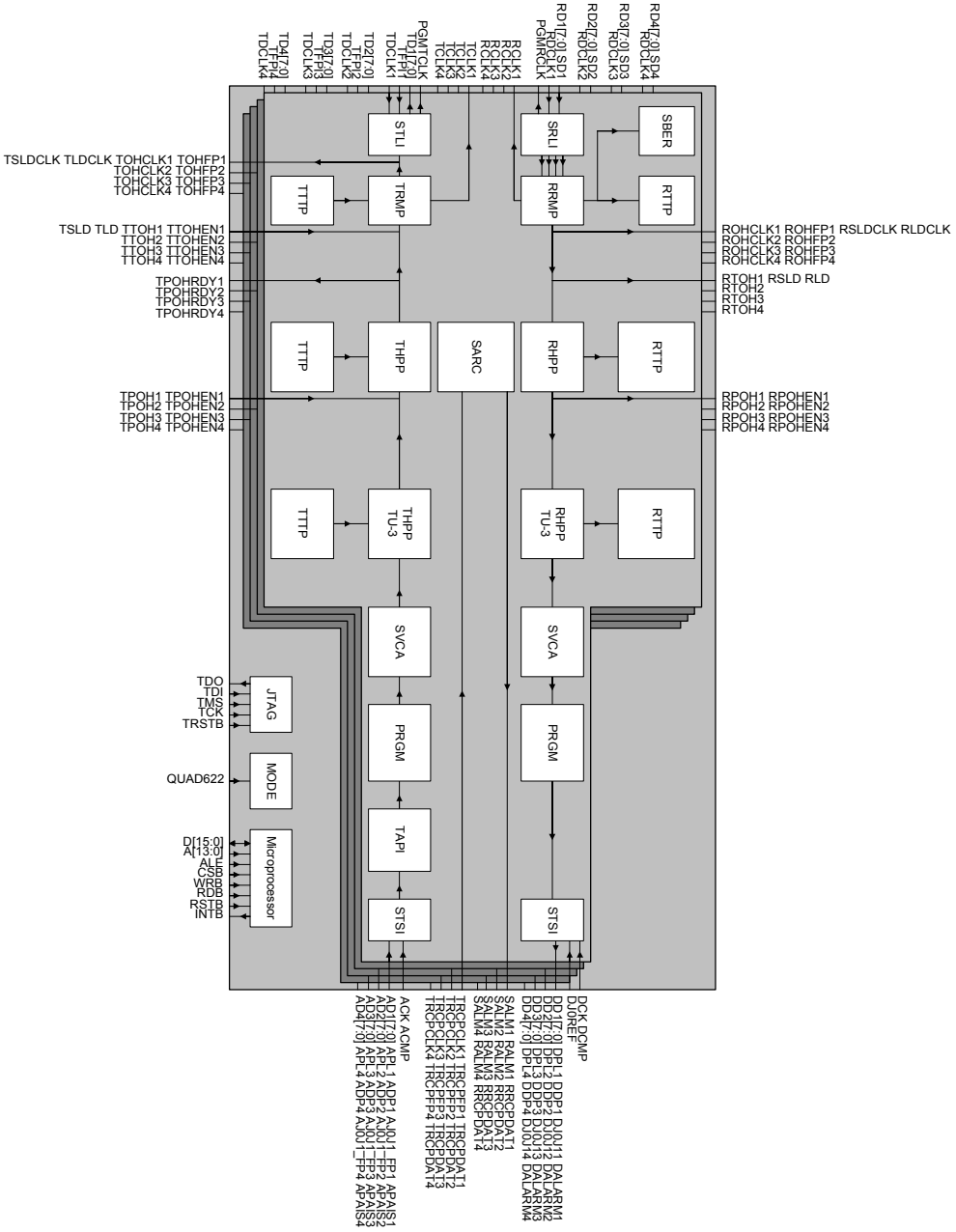


6 Block Diagram

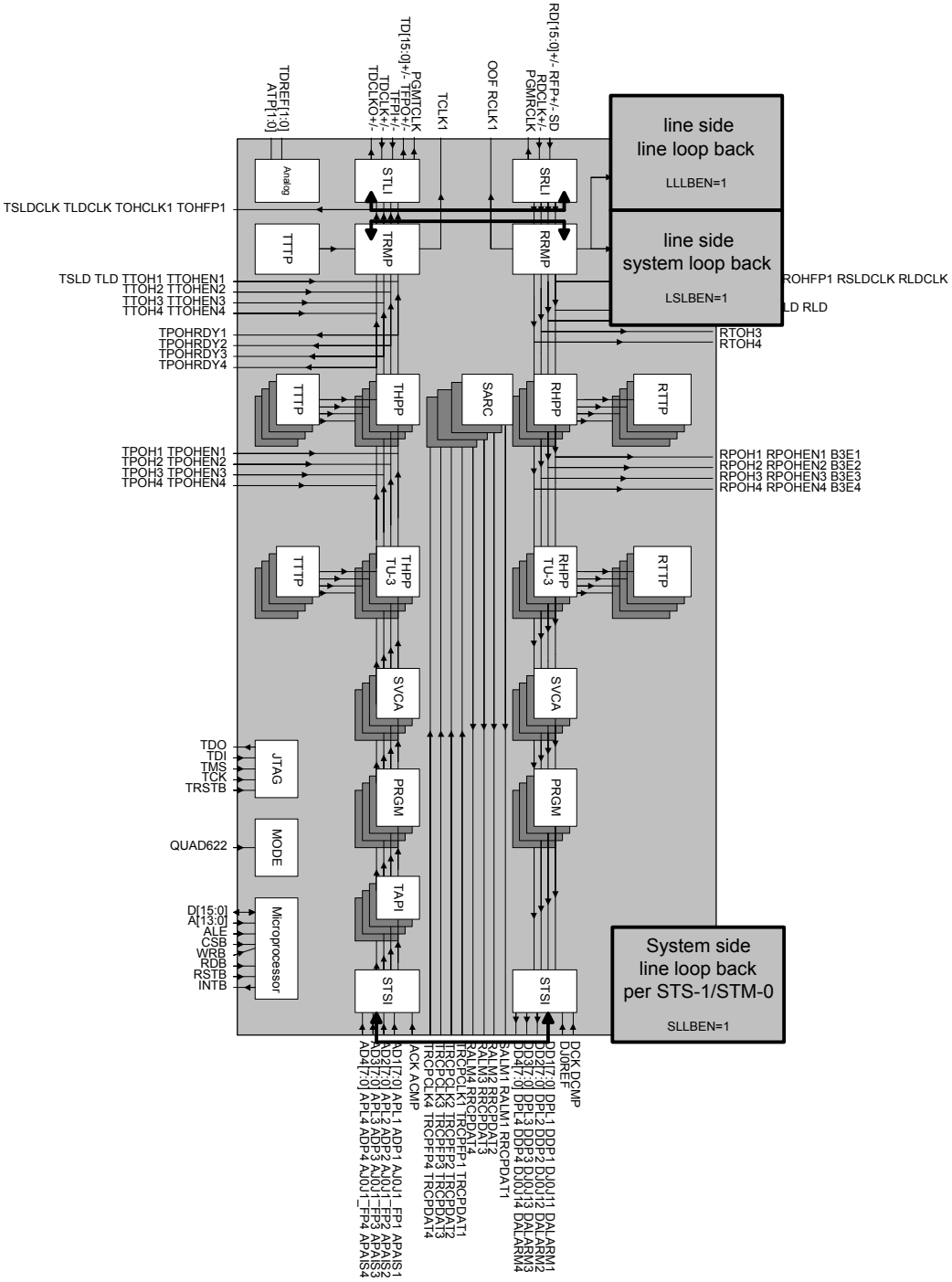
6.1 Block Diagram Single STS-48/STM-16 Mode



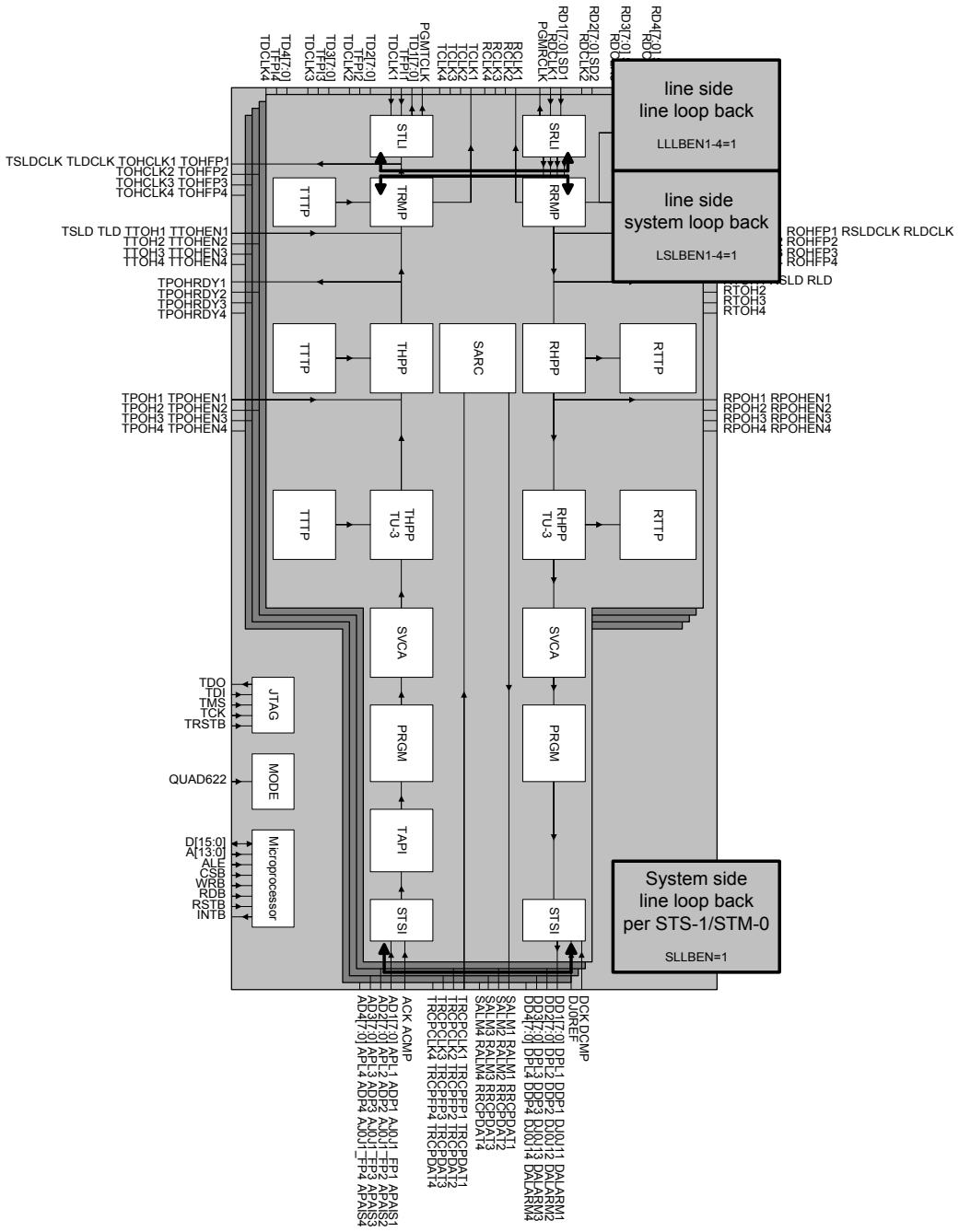
6.2 Block Diagram Quad STS-12/STM-4 Mode



6.3 Loopback Modes SINGLE STS-48/STM-16 Mode



6.4 Loopback Modes Quad STS-12/STM-4 Mode



7 Description

The PM5315 SONET/SDH PAYLOAD EXTRACTOR/ALIGNER (SPECTRA-2488) terminates the transport and path overhead of a single STS-48 (STM-16/AU4-12c/AU4-8c/AU4-4c/AU4/AU3/TU3), a single STS-48c (STM-16/AU4-16c), a quad STS-12 (STM-4/AU4/AU3/TU3) or a quad STS-12c (STM-4-4c) data streams at 2488 Mbit/s. The SPECTRA-2488 implements significant functions for a SONET/SDH compliant line interface.

In single STS-48/STM-16 mode, the SPECTRA-2488 receives SONET/SDH frames via a 16 bit serial interface at 155.52 MHz. In quad STS-12/STM-4 mode, the SPECTRA-2488 receives SONET/SDH frames via four 8 bit serial interfaces at 77.76 MHz. The Spectra-2488 terminates the SONET section, line and path or the SDH regenerator section, multiplexer section and high order path overhead. It performs framing (A1, A2), descrambling, detects section and line alarm conditions, and monitors section and line bit interleaved parity (BIP) (B1, B2), accumulating error counts at each level for performance monitoring purposes. B2 errors are also monitored to detect signal fail and signal degrade threshold crossing alarms. Line remote error indications (M1) are also accumulated. A 16 or 64 byte section trace (J0) message may be buffered and compared against an expected message. In addition, the SPECTRA-2488 interprets the received payload pointers (H1, H2), detects path alarm conditions, detects and accumulates path BIPs (B3), monitors and accumulates path Remote Error Indications (REIs), accumulates and compares the 16 or 64 byte path trace (J1) message against an expected result and extracts the synchronous payload envelope (virtual container). All transport and path overhead bytes are extracted and serialized on lower rate interfaces, allowing additional external processing of overhead, if desired.

The extracted SPE (VC) is placed on a 32 bit Telecom DROP bus at 77.76 MHz. For TelecomBus applications, frequency offsets (e.g., due to plesiochronous network boundaries, or the loss of a primary reference timing source) and phase differences (due to normal network operation) between the received data stream and the DROP bus are accommodated by pointer adjustments in the DROP bus.

In STS-48/STM-16 mode, the SPECTRA-2488 transmits SONET/SDH frames via a 16 bit serial interface at 155.52 MHz. In quad STS-12/STM-4 mode, the SPECTRA-2488 transmits SONET/SDH frames via four 8 bit serial interfaces at 77.76 MHz. The SPECTRA-2488 formats the SONET section, line and path or the SDH regenerator section, multiplexer section and high order path overhead. It performs framing pattern insertion (A1, A2), scrambling, section and line alarm insertion, and section and line BIPs (B1, B2) calculation as required to allow performance monitoring at the far end. Line remote error indications (M1) are optionally inserted. A 16 or 64 byte section trace (J0) message may be inserted. In addition, the SPECTRA-2488 generates the transmit payload pointers (H1, H2), creates and inserts the path BIPs (B3), optionally inserts a 16 or 64 byte path trace (J1) message, optionally inserts the path status byte (G1). In addition to its basic processing of the transmit SONET/SDH overhead, the SPECTRA-2488 provides convenient access to all overhead bytes, which are inserted serially on lower rate interfaces, allowing additional external sourcing of overhead, if desired. The SPECTRA-2488 also supports the insertion of a large variety of errors into the transmit stream, such as framing pattern errors, pointer errors and BIP errors, which are useful for system diagnostics and tester applications.

The inserted SPE (VC) is sourced from a 32 bit Telecom ADD bus at 77.76 MHz. For TelecomBus applications, frequency offsets (e.g., due to plesiochronous network boundaries, or the loss of a primary reference timing source) and phase differences (due to normal network operation) between the transmit data stream and the ADD bus are accommodated by pointer adjustments in the transmit data stream.

The SPECTRA-2488 supports Time-Slot Interchange (TSI) on the Telecom ADD and DROP buses. On the DROP side, the TSI views the receive stream as twelve independent time-division multiplexed columns of data (i.e. twelve constituent STS-1 (STM-0) or equivalent streams or time-slots or columns). Any column can be connected to any time-slot on the DROP bus. Both column swapping and broadcast are supported. Time-Slot Interchange is independent of the underlying payload mapping formats. Similarly, on the ADD side, data from the ADD bus is treated as twelve independent time-division multiplexed columns. Assignment of data columns to transmit time-slots (STS-1 (STM-0) or equivalent streams) is arbitrary.

The transmitter and receiver are independently configurable to allow for asymmetric interfaces. Ring control ports are provide to pass control and status information between mate transceivers. The SPECTRA-2488 is configured, controlled and monitored via a generic 16-bit microprocessor bus interface.

The SPECTRA-2488 is implemented in low power 1.8 Volt CMOS core logic with 3.3 Volt CMOS/TTL compatible digital inputs and digital outputs. It has pseudo ECL (PECL) compatible inputs and outputs and is packaged in a 520 pin SBGA package.

8 PIN DIAGRAMS

The SPECTRA-2488 is packaged in a 520 balls SBGA.

Left Side

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
VDD	VSS	VSS	VSS	AD1[2]	VSS	TRCPDATV[1]	TRCPCLKV[3]	TRCPDATV[4]	TMS	VSS	ALE	A[2]	A[7]	A[12]	VSS
VSS	VDD	VSS	AD1[7]	AD1[4]	APLV[1]	TRCPCLKV[1]	TRCPDATV[2]	TRCPCLKV[4]	TRSTB	INTB	RDB	A[1]	A[6]	A[11]	VSS
VSS	VSS	VDD	VDD	AD1[6]	AD1[1]	NC	TRCPFPV[2]	TRCPDATV[3]	TCK	TDO	WRB	A[0]	A[5]	A[10]	VDD
VSS	ADPV[1]	VDD	VDD	NC	AD1[3]	AJOJ1_FPV[1]	TRCPCLKV[2]	TRCPFPV[3]	NC	TDI	RSTB	NC	A[4]	A[9]	VDD
DD1[1]	DPLV[1]	APAISV[1]	NC	VDD	AD1[5]	AD1[0]	TRCPFPV[1]	VDDI[51]	TRCPFPV[4]	VDD	QUAD622	CSB	A[3]	A[8]	VDD
VSS	DD1[4]	DD1[2]	DD1[0]	DJOJ1V[1]											
DDPV[1]	DD1[7]	DD1[6]	DD1[5]	DD1[3]											
AD2[1]	APLV[2]	AJOJ1_FPV[2]	DALARMV[1]	VDDI[0]											
AD2[6]	AD2[4]	AD2[3]	AD2[2]	AD2[0]											
DJOJ1V[2]	APAISV[2]	ADPV[2]	AD2[7]	AD2[5]											
VSS	DD2[0]	NC	DPLV[2]	VDD											
DD2[5]	DD2[4]	DD2[3]	DD2[2]	DD2[1]											
AJOJ1_FPV[3]	DALARMV[2]	DDPV[2]	DD2[7]	DD2[6]											
AD3[3]	AD3[2]	AD3[1]	AD3[0]	APLV[3]											
AD3[7]	AD3[6]	AD3[5]	AD3[4]	VDDI[1]											
VSS	VSS	VDD	VDD	VDD											
ADPV[3]	APAISV[3]	DJOJ1V[3]	DPLV[3]	DD3[0]											
DD3[1]	DD3[2]	DD3[3]	DD3[4]	DD3[5]											
DD3[6]	DD3[7]	VDDI[2]	DDPV[3]	DALARMV[3]											
AJOJ1_FPV[4]	APLV[4]	AD4[0]	AD4[1]	AD4[2]											
VSS	AD4[3]	AD4[4]	AD4[5]	VDD											
AD4[6]	AD4[7]	ADPV[4]	APAISV[4]	DPLV[4]											
DJOJ1V[4]	DD4[0]	NC	DD4[1]	DD4[3]											
DD4[2]	DD4[4]	DD4[5]	DD4[6]	DDPV[4]											
DD4[7]	DALARMV[4]	VDDI[3]	ACK	DJOREF											
VSS	ACMP	DCMP	NC	B3E1											
DCK	SALM1	RALMV[1]	ROHFPV[1]	VDD	RRCPDATV[1]	ROHCLKV[2]	RRCPDATV[2]	ROHCLKV[3]	RRCPDATV[3]	VDD	RPOHENV[4]	RSLD	TTOHV[1]	TPOHENV[1]	VDD
VSS	ROHCLKV[1]	VDD	VDD	RTOHV[1]	NC	RTOHV[2]	NC	RTOHV[3]	NC	ROHFPV[4]	RRCPDATV[4]	RLDCLK	NC	TPOHRDYV[1]	VDD
VSS	VSS	VDD	VDD	RPOHENV[1]	RALMV[2]	RPOHV[2]	SALM3_B3E3	RPOHV[3]	SALM4_B3E4	RTOHV[4]	VDDI[17]	RLD	NC	NC	VDD
VSS	VDD	VSS	RPOHV[1]	NC	ROHFPV[2]	RPOHENV[2]	RALMV[3]	RPOHENV[3]	RALMV[4]	RPOHV[4]	NC	TOHCLKV[1]	TTOHENV[1]	NC	VSS
VDD	VSS	VSS	VSS	SALM2_B3E2	VSS	VDDI[15]	ROHFPV[3]	NC	ROHCLKV[4]	VSS	RSLDCLK	TOHFPV[1]	TPOHV[1]	TOHCLKV[2]	VSS

Right Side

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
A[13]	D[3]	D[7]	D[12]	VSS	RFPN	RDP14_RD15	RDN13_RD12	SDV[1]	VSS	VDDI[39]	VSS	VSS	VSS	VDD	A
VDDI[45]	D[4]	D[8]	D[13]	RDCLKP	RAVSL[3]	RAVDL[3]	RDN12_RD10	RCLKV[1]	RDN11_TD16	RAVSH[2]	RDP8_TD11	VSS	VDD	VSS	B
D[0]	D[5]	D[9]	D[14]	RDCLKN	RDP15_RD17	RAVSH[3]	RAVDH[3]	RAVSL[2]	RDN10_TD14	RDN9_TD12	VDD	VDD	VSS	VSS	C
D[1]	D[6]	D[10]	D[15]	RFPP	RDN15_RD16	RDP13_RD13	RDCLKV[1]	RDP11_TD17	RAVDL[2]	RDN8_TD10	VDD	VDD	RDP7_RD27	VSS	D
D[2]	VDDI[44]	D[11]	VDDI[42]	VDD	RDN14_RD14	RDP12_RD11	OOF	RDP10_TD15	RDP9_TD13	VDD	RAVDH[2]	RDN7_RD26	RDN6_RD24	TDCLKV[1]	E
										RDP6_RD25	RAVSL[1]	NC	RAVDL[1]	VSS	F
										TCLKV[1]	NC	NC	RAVSH[1]	RDN5_RD22	G
										RDP5_RD23	RDP4_RD21	RDN4_RD20	RAVDH[1]	SDV[2]	H
										RDCLKV[2]	VDDI[35]	RCLKV[2]	RAVSL[0]	RDN3_TD26	J
										RDP3_TD27	RDP2_TD25	RDN2_TD24	RAVDL[0]	NC	K
										VDD	NC	RAVSH[0]	RDP1_TD23	VSS	L
										RDN1_TD22	RDP0_TD21	RDN0_TD20	RAVDH[0]	TDCLKV[2]	M
										NC	TCLKV[2]	NC	VDDI[32]	PGMRCLK	N
										ATP[0]	ATP[1]	QAVS	QAVD	CAVSH	P
										CAVDH	TDREF[0]	TDREF[1]	NC	NC	R
										VDD	VDD	VDD	VSS	VSS	T
										TAVSL[3]	TFPIN_TFPI2	TFPIP_TFPI1	TDCLKN	TDCLKP	U
										TDN14_RD34	TDP14_RD35	NC	TDN15_RD36	TDP15_RD37	V
										TDP13_RD33	TAVSH[3]	VDDI[32]	NC	TAVDL[3]	W
										RDCLKV[3]	TAVDH[3]	TDN12_RD30	TDP12_RD31	TDN13_RD32	Y
										VDD	RCLKV[3]	NC	SDV[3]	VSS	AA
										TAVDL[2]	TDP10_TD35	TDN11_TD36	TDP11_TD37	TAVSL[2]	AB
										TDN9_TD32	TAVSH[2]	NC	NC	TDN10_TD34	AC
										NC	TAVDH[2]	TDN8_TD30	TDP8_TD31	TDP9_TD33	AD
											TDP7_RD47	TAVSL[1]	TCLKV[3]	TDCLKV[3]	AE
										TAVSH[1]	NC	TDN6_RD44	TDN7_RD46	VSS	AF
TPOHENV[2]	TTOHV[3]	TOHCLKV[4]	TPOHV[4]	VDD	TFPOP_TFPI3	TDCLKV[4]	TDP1_TD43	TDN3_TD46	RDCLKV[4]	VDD	TAVDH[1]	TDP5_RD43	VDDI[25]	TAVDL[1]	AG
TPOHV[2]	TOHFPV[3]	TPOHRDYV[3]	TTOHENV[4]	TSLDCLK	PGMTCLK	TCLKV[4]	TDP0_TD41	TDN2_TD44	RCLKV[4]	NC	VDD	VDD	TDN5_RD42	VSS	AH
TTOHENV[2]	VDDI[20]	TPOHENV[3]	TTOHV[4]	TPOHRDYV[4]	TLD	TDCLKOP	TDN0_TD40	TAVDL[0]	TDP3_TD47	TDN4_RD40	VDD	VDD	VSS	VSS	AJ
TTOHV[2]	TOHCLKV[3]	TPOHV[3]	NC	TPOHENV[4]	TLDCLK	TDCLKON	TAVDH[0]	TAVSH[0]	TDP2_TD45	SDV[4]	TDP4_RD41	VSS	VDD	VSS	AK
TOHFPV[2]	TPOHRDYV[2]	TTOHENV[3]	TOHFPV[4]	VSS	TSLD	TFPON_TFPI4	VDDI[23]	TDN1_TD42	VSS	TAVSL[0]	VSS	VSS	VSS	VDD	AL

9 Pin Description

9.1 Configuration Pin Signals

Pin Name	Type	Pin No.	Function
QUAD622	TTL Input	E20	The **quad 622 Mbit/s mode select** (QUAD622) signal selects between the single STS-48/STM-16 mode or the quad STS-12/STM-4 mode. When QUAD622 is low, the device is in single STS-48/STM-16 mode. When QUAD622 is high, the device is in quad STS-12/STM-4 mode.

9.2 STS-48/STM-16 Line Side Interface Signals

Pin Name	Type	Pin No.	Function
RDCLK+ RDCLK-	PECL Input	B11 C11	The differential **receive data clock** (RDCLK+/-) signal provides timing for the receive line side interface when the device is configured in STS-48/STM-16 mode. RDCLK+/- is a nominal 155.52 MHz 50 % duty cycle clock. SD, RD[15:0]+/- and RFP+/- are sampled on the rising edge of RDCLK+/-. Please refer to the Operation section for a discussion of PECL interfacing issues.
SD	TTL Input	A7	The active high **receive signal detect** (SD) signal indicates the presence of valid receive signal power from the Optical Physical Medium Dependent Device. SD is set to logic one to indicate valid data on RD[15:0]+/- bus. SD is set to logic zero to indicate a loss of signal. When SD is logic zero, the receive data on RD[15:0]+/- is forced to all zeros. SD is sample on the rising edge of RDCLK+/-.

Pin Name	Type	Pin No.	Function
RD[15]+ RD[15]- RD[14]+ RD[14]- RD[13]+ RD[13]- RD[12]+ RD[12]- RD[11]+ RD[11]- RD[10]+ RD[10]- RD[9]+ RD[9]- RD[8]+ RD[8]- RD[7]+ RD[7]- RD[6]+ RD[6]- RD[5]+ RD[5]- RD[4]+ RD[4]- RD[3]+ RD[3]- RD[2]+ RD[2]- RD[1]+ RD[1]- RD[0]+ RD[0]-	PECL Input	C10 D10 A9 E10 D9 A8 E9 B8 D7 B6 E7 C6 E6 C5 B4 D5 D2 E3 F5 E2 H5 G1 H4 H3 K5 J1 K4 K3 L2 M5 M4 M3	The differential **receive data** (RD[15:0]+/-) bus carries the 16-bit serial data stream when the device is configured in STS-48/STM-16 mode. RD[15]+/- is the most significant bit (corresponding to the first bit received). RD[0]+/- is the least significant bit (corresponding to the last bit received). RD[15:0]+/- is sampled on the rising edge of RDCLK+/-. Please refer to the Operation section for a discussion of PECL interfacing issues.
RFP+ RFP-	PECL Input	D11 A10	The differential active high **receive framing position** (RFP+/-) signal indicates the SONET/SDH frame alignment on the RD[15:0]+/- bus. RFP+/- is asserted for one RDCLK+/- clock cycle to indicate the first payload bytes after the J0/Z0 bytes on the RD[15:0]+/- bus. The operation of the RFP+/- input is controlled by the DISFRM bit in the SRLI 0040H register. When DISFRM is set to logic one, the SRLI is disable and an external framing device must byte and frame align the data on RD[15:0]+/-. When DISFRM is set to logic zero, RFP+/- is ignored and the SRLI will byte and frame align the data on RD[15:0]+/-. RFP+/- is sampled on the rising edge of RDCLK+/-. Please refer to the Operation section for a discussion of PECL interfacing issues.

Pin Name	Type	Pin No.	Function
OOF	TTL Output	E8	The active high **out of frame** (OOF) signal indicates when an out of frame condition is declared by the framing block. OOF is set high while the framing block is out of frame. An out of frame condition is declared when bit errors are detected in four consecutive framing pattern (A1 and A2 bytes). OOF is set low while the framing block is in frame. OOF forces an external framing device to start looking for the framing pattern in order to find a new byte and frame alignment. OOF is updated on the rising edge of RCLK1.
TDCLK+ TDCLK-	PECL Input	U1 U2	The differential **transmit data clock** (TDCLK+/-) signal provides timing for the transmit line side interface when the device is configured in STS-48/STM-16 mode. TDCLK+/- is a nominal 155.52 MHz 50 % duty cycle clock. Please refer to the Operation section for a discussion of PECL interfacing issues. TFPI+/- is sampled on the rising edge of TDCLK+/-.
TDCLKO+ TDCLKO-	PECL Output	AJ9 AK9	The differential **transmit data clock output reference** (TDCLKO+/-) signal provides timing reference for the output signals of the transmit line side interface when the device is configured in STS-48/STM-16 mode. TDCLKO+/- is a buffered version of TDCLK+/-. TDCLKO+/- output can be disabled and held low by programming the TDCLKOEN bit in the STLI 1040H register. TD[15:0]+/- and TFPO+/- are updated on the rising edge of TDCLKO+/- Current steered differential PECL drivers. Please refer to the Operation section for a discussion of PECL interfacing issues.7

Pin Name	Type	Pin No.	Function
TD[15]+ TD[15]- TD[14]+ TD[14]- TD[13]+ TD[13]- TD[12]+ TD[12]- TD[11]+ TD[11]- TD[10]+ TD[10]- TD[9]+ TD[9]- TD[8]+ TD[8]- TD[7]+ TD[7]- TD[6]+ TD[6]- TD[5]+ TD[5]- TD[4]+ TD[4]- TD[3]+ TD[3]- TD[2]+ TD[2]- TD[1]+ TD[1]- TD[0]+ TD[0]-	PECL Output	V1 V2 V4 V5 W5 Y1 Y2 Y3 AB2 AB3 AB4 AC1 AD1 AC5 AD2 AD3 AE4 AF2 AE5 AF3 AG3 AH2 AK4 AJ5 AJ6 AG7 AK6 AH7 AG8 AL7 AH8 AJ8	The differential **transmit data** (TD[15:0]+/-) bus carries the 16-bit serial data stream when the device is configured in STS-48/STM-16 mode. TD[15]+/- is the most significant bit (corresponding to the first bit transmitted). TD[0]+/- is the least significant bit (corresponding to the last bit transmitted). TD[15:0]+/- is updated on the rising edge of TDCLKO+/-. Current steered differential PECL drivers. Please refer to the Operation section for a discussion of PECL interfacing issues.
TFPI+ TFPI-	PECL Input	U3 U4	The differential active high **transmit framing position input** (TFPI+/-) signal synchronizes the SONET/SDH frame alignment on the TD[15:0]+/- bus when the device is configured in STS-48/STM-16 mode. TFPI+/- must be asserted for one TDCLK+/- clock cycle to synchronize TD[15:8]+/-. TFPI+/- must be present at every frame. TFPI+/- may be set low if such synchronization is not required. TFPI+/- is sampled on the rising edge of TDCLK+/-. Please refer to the Operation section for a discussion of PECL interfacing issues.

Pin Name	Type	Pin No.	Function
TFPO+ TFPO-	PECL Output	AG10 AL9	The differential active high **transmit framing position output** (TFPO+/-) signal indicates the SONET/SDH frame alignment on the TD[15:0]+/- bus when the device is configured in STS-48/STM-16 mode. TFPO+/- is asserted for one TDCLKO+/- clock cycle to indicate the first payload byte after the J0/Z0 bytes on TD[15:8]+/-. TFPO+/- is updated on the rising edge of TDCLKO+/-. Current steered differential PECL drivers. Please refer to the Operation section for a discussion of PECL interfacing issues.

9.3 Quad STS-12/STM-4 Line Side Interface Signals

Pin Name	Type	Pin No.	Function
RDCLK1 RDCLK2 RDCLK3 RDCLK4	TTL Schmidt Input	D8 J5 Y5 AG6	The **receive data clock** (RDCLK1-4) signal provides timing for the receive line side interface when the device is configured in quad STS-12/STM-4 mode. RDCLK1-4 is a nominal 77.76 MHz 50% duty cycle clock. RDCLK1-4 is a Schmidt triggered input. SD1-4 and RD1-4[7:0] are sampled on the rising-edge of RDCLK1-4.
SD1 SD2 SD3 SD4	TTL Input	A7 H1 AA2 AK5	The active high **receive signal detect** (SD1-4) signal indicates the presence of valid receive signal power from the Optical Physical Medium Dependent Device. SD1-4 is set to logic one to indicate valid data on RD1-4[7:0] bus. SD1-4 is set to logic zero to indicate a loss of signal. When SD1-4 is logic zero, the receive data on RD1-4[7:0] is forced to all zeros. SD1-4 is sampled on the rising edge of RDCLK1-4.

Pin Name	Type	Pin No.	Function
RD1[7] RD1[6] RD1[5] RD1[4] RD1[3] RD1[2] RD1[1] RD1[0] RD2[7] RD2[6] RD2[5] RD2[4] RD2[3] RD2[2] RD2[1] RD2[0] RD3[7] RD3[6] RD3[5] RD3[4] RD3[3] RD3[2] RD3[1] RD3[0] RD4[7] RD4[6] RD4[5] RD4[4] RD4[3] RD4[2] RD4[1] RD4[0]	TTL Input	C10 D10 A9 E10 D9 A8 E9 B8 D2 E3 F5 E2 H5 G1 H4 H3 V1 V2 V4 V5 W5 Y1 Y2 Y3 AE4 AF2 AE5 AF3 AG3 AH2 AK4 AJ5	The **receive data** (RD1-4[7:0]) bus carries the byte serial data stream when the device is configured in quad STS-12/STM-4 mode. RD1-4[7] is the most significant bit (corresponding to bit 1 of each serial word, the first bit received). RD1-4[0] is the least significant bit (corresponding to bit 8 of each serial word, the last bit received). RD1-4[7:0] is sampled on the rising edge of RDCLK1-4.
TDCLK1 TDCLK2 TDCLK3 TDCLK4	TTL Schmidt Input	E1 M1 AE1 AG9	The **transmit data clock** (TDCLK1-4) signal provides timing for the transmit line side interface when the device is configured in quad STS-12/STM-4 mode. TDCLK1-4 is a nominal 77.76 MHz 50% duty cycle clock. TDCLK1-4 is a Schmidt triggered input. TFPI1-4 is sampled on the rising edge of TDCLK1-4.

Pin Name	Type	Pin No.	Function
TD1[7] TD1[6] TD1[5] TD1[4] TD1[3] TD1[2] TD1[1] TD1[0] TD2[7] TD2[6] TD2[5] TD2[4] TD2[3] TD2[2] TD2[1] TD2[0] TD3[7] TD3[6] TD3[5] TD3[4] TD3[3] TD3[2] TD3[1] TD3[0] TD4[7] TD4[6] TD4[5] TD4[4] TD4[3] TD4[2] TD4[1] TD4[0]	TTL Output	D7 B6 E7 C6 E6 C5 B4 D5 K5 J1 K4 K3 L2 M5 M4 M3 AB2 AB3 AB4 AC1 AD1 AC5 AD2 AD3 AJ6 AG7 AK6 AH7 AG8 AL7 AH8 AJ8	The **transmit data** (TD1-4[7:0]) bus carries the byte serial data stream when the device is configured in quad STS-12/STM-4 mode. TD1-4[7] is the most significant bit (corresponding to bit 1 of each serial word, the first bit transmitted). TD1-4[0] is the least significant bit (corresponding to bit 8 of each serial word, the last bit transmitted). TD1-4[7:0] is updated on the rising edge of TCLK1-4.
TFPI1 TFPI2 TFPI3 TFPI4	TTL Input	U3 U4 AG10 AL9	The active high **transmit framing position input** (TFPI1-4) signal synchronizes the SONET/SDH frame alignment on the TD1-4[7:0] bus when the device is configured in quad STS-12/STM-4 mode. TFPI1-4 must be asserted for one TDCLK1-4 clock cycle to synchronize TD1-4[7:0]. It is not necessary for TFPI1-4 to be present at every frame, an internal counter fly-wheels based on the most recent TFPI1-4 assertion. TFPI1-4 may be set low if such synchronization is not required. TFPI1-4 is sampled on the rising edge of TDCLK1-4.

9.4 Receive and Transmit Reference (single and quad mode)

Pin Name	Type	Pin No.	Function
PGMRCLK	TTL Output	N1	The **programmable receive clock** (PGMRCLK) signal provides timing reference for the receive line interface. In single STS-48 mode, PGMRCLK is a divided version of RDCLK+/- clock. When PGMRCLKSEL bit in the SRLI 0041H register is set low, PGMRCLK is a nominal 19.44 MHz, 50% duty cycle clock. When PGMRCLKSEL bit is set high, PGMRCLK is a nominal 8 KHz, 50% duty cycle clock. In quad STS-12 mode, PGMRCLK is a divided version of one of the RDCLK1-4 clocks. The PGMRCLKSRC[1:0] bits in the SRLI 0041H register are used to select which of the four clocks is muxed onto PRGMRCLK. When PGMRCLKSEL bit is set low, PGMRCLK is a nominal 19.44 MHz, 50% duty cycle clock. When PGMRCLKSEL bit is set high, PGMRCLK is a nominal 8 KHz, 50% duty cycle clock. PGMRCLK output can be disabled and held low by programming the PGMRCLKEN bit in the SRLI 0041H register.
RCLK1 RCLK2 RCLK3 RCLK4	TTL Output	B7 J3 AA4 AH6	The **receive clock** (RCLK1-4) signal provides timing reference for the receive interface. In STS-48/STM-16 mode, RCLK1 is a nominal 77.76 MHz 50 % duty cycle clock. RCLK1 is a buffered version of RDCLK+/- divided by two. RCLK2-4 are not defined. In quad STS-12/STM-4 mode, RCLK1-4 is a nominal 77.76 MHz 50 % duty cycle clock. RCLK1-4 is a buffered version of RDCLK1-4. RCLK1-4 output can be disabled and held low by programming the RCLKEN1-4 bit in the SRLI 0040H register. OOF is updated on the rising edge of RCLK1-4.
PGMTCLK	TTL Output	AH10	The **programmable transmit clock** (PGMTCLK) signal provides timing reference for the transmit line interface. In single STS-48 mode, PGMTCLK is a divided version of TDCLK+/- clock. When PGMTCLKSEL bit in the STLI 1041H register bit is set low, PGMTCLK is a nominal 19.44 MHz, 50% duty cycle clock. When PGMTCLKSEL bit is set high, PGMTCLK is a nominal 8 KHz, 50% duty cycle clock. In quad STS-12 mode, PGMTCLK is a divided version of one of the TDCLK1-4 clocks. The PGMTCLKSRC[1:0] bits in the STLI 0041H register are used to select which of the four clocks is muxed onto PRGMTCLK. When PGMTCLKSEL register bit is set low, PGMTCLK is a nominal 19.44 MHz, 50% duty cycle clock. When PGMTCLKSEL register bit is set high, PGMTCLK is a nominal 8 KHz, 50% duty cycle clock. PGMTCLK output can be disabled and held low by programming the PGMTCLKEN bit in the STLI 1041H register.

Pin Name	Type	Pin No.	Function
TCLK1 TCLK2 TCLK3 TCLK4	TTL Output	G5 N4 AE2 AH9	The **transmit clock** (TCLK1-4) signal provides timing reference for the transmit interface. In STS-48/STM-16 mode, TCLK1 is a nominal 77.76 MHz 50 % duty cycle clock. TCLK1 is a buffered version of TDCLK+/- divided by two. TCLK2-4 are not defined. In quad STS-12/STM-4 mode, TCLK1-4 is a nominal 77.76 MHz 50 % duty cycle clock. TCLK1-4 is a buffered version of TCLK1-4. TCLK1-4 output can be disabled and held low by programming the TCLKEN1-4 bit in the STLI 1040H register. TD1-4[7:0] is updated on the rising edge of TCLK1-4.

9.5 Section/Line/Path Status and Alarms Signals (single and quad mode)

Pin Name	Type	Pin No.	Function
RRCPDAT1 RRCPDAT2 RRCPDAT3 RRCPDAT4	TTL Output	AG26 AG24 AG22 AH20	The **receive ring control port data** (RRCPDAT1-4) signal contains the receive ring control port data stream. The receive ring control port data consists of all the section, line and path alarms and status: Out Of Frame Indication, Lost Of Frame indication, Loss Of Signal indication, the line AIS indication, the line RDI indication, the APS byte failure indication, the section TIU/TIM indication, the signal degrade/fail indication, the K1/K2 bytes insertion, the line REI insertion, the line RDI insertion, the path LOP indication, the path AIS indication, the path PLU/PLM indication, the path UNEQ indication, the path PDI indication, the path RDI indication, the path ERDI indication, the path TIU/TIM indication, the path REI insertion and the path ERDI insertion. RRCPDAT1-4 can be connected directly to the TRCPDAT1-4 input of a mate SPECTRA-2488 in ring-based add-drop multiplexer applications. RRCPDAT1-4 is updated on the falling edge of ROHCLK1-4.
TRCPCLK1 TRCPCLK2 TRCPCLK3 TRCPCLK4	TTL Schmidt Input	B25 D24 A24 B23	The **transmit ring control port clock** (TRCPCLK1-4) signal provides timing for the transmit ring control port. TRCPCLK1-4 is y a nominal 20.736 MHz clock, 33% high duty cycle and can be connected directly to the ROHCLK1-4 output of a mate SPECTRA-2488 in ring-based add-drop multiplexer applications. TRCPCLK1-4 is a Schmidt triggered input. TRCPFP1-4 and TRCPDAT1-4 are sampled on the rising edge of TRCPCLK1-4.

Pin Name	Type	Pin No.	Function
TRCPFP1 TRCPFP2 TRCPFP3 TRCPFP4	TTL Input	E24 C24 D23 E22	The **transmit ring control port frame pulse** (TRCPFP1-4) signal identifies bit positions in the transmit ring control port data (TRCPDAT1-4). TRCPFP1-4 is high to indicate the Out Of Frame indication in the TRCPDAT1-4 data stream. TRCPFP1-4 can be connected directly to the ROHFP1-4 output of a mate SPECTRA-2488 in ring-based add-drop multiplexer applications. TRCPFP1-4 is sampled on the rising edge of TRCPCLK1-4.
TRCPDAT1 TRCPDAT2 TRCPDAT3 TRCPDAT4	TTL Input	A25 B24 C23 A23	The **transmit ring control port data** (TRCPDAT1-4) signal contains the transmit ring control port data stream. The receive ring control port data consists of all the section, line and path alarms insertion: the K1/K2 bytes insertion, the line REI insertion, the line RDI insertion, the path REI insertion and the path ERDI insertion. TRCPDAT1-4 can be connected directly to the RRCPDAT1-4 output of a mate SPECTRA-2488 in ring-based add-drop multiplexer applications. TRCPDAT1-4 is sampled on the rising edge of TRCPCLK1-4.
SALM1 SALM2 SALM3 SALM4	TTL Output	AG30 AL27 AJ24 AJ22	The **section alarm** (SALM1-4) signal is set high when an out of frame (OOF), loss of signal (LOS), loss of frame (LOF), line alarm indication signal (AIS-L), line remote defect indication (RDI-L), APS byte failure, section trace identifier mismatch (TIM-S), section trace identifier unstable (TIU-S), signal fail (SF) or signal degrade (SD) alarm is detected. Each alarm indication can be independently enabled using bits in the SARC SALM registers. SALM1-4 is set low when none of the enabled alarms are active. SALM1-4 is updated on the falling edge of ROHCLK1-4.
RALM1 RALM2 RALM3 RALM4	TTL Output	AG29 AJ26 AK24 AK22	The **Receive Alarm** (RALM1-4) signal is a multiplexed output of individual alarms of the receive paths. RALM1-4 signal is set high for the corresponding path when a section alarm, pat loss of pointer (LOP-P), path alarm indication signal (AIS-P), path remote defect indication (RDI-P), path enhance remote defect indication (ERDI-P), path label mismatch (PLM), path label unstable (PLU), path unequipped (UNEQ), path payload defect indication (PDI-P), path trace identifier mismatch (TIM-P) or path trace identifier unstable (TIU-P) alarm is detected. Each alarm indication can be independently enabled using bits in the SARC RALM registers. RALM1-4 is set low when none of the enabled alarms are active. RALM1-4 is updated on the falling edge of ROHCLK1-4.

9.6 Receive Section/Line/Path Overhead Extraction Signals (single and quad mode)

Pin Name	Type	Pin No.	Function
ROHCLK1 ROHCLK2 ROHCLK3 ROHCLK4	TTL Output	AH30 AG25 AG23 AL22	The **receive overhead clock** (ROHCLK1-4) signal provides timing for the receive section, line and path overhead extraction. In STS-48/STM-16 mode, ROHCLK1 is a nominal 20.736 MHz clock generated by gapping a 25.92 MHz clock. ROHCLK1 has a 33% high duty cycle. ROHCLK2-4 are not defined. In quad STS-12/STM-4 mode, ROHCLK1-4 is a nominal 20.736 MHz clock generated by gapping a 25.92 MHz clock. ROHCLK1-4 has a 33% high duty cycle. ROHFP1-4, RTOH1-4, RPOH1-4, RPOHEN1-4, B3E1-4, SALM1-4 and RALM1-4 are updated on the falling edge of ROHCLK1-4.
ROHFP1 ROHFP2 ROHFP3 ROHFP4	TTL Output	AG28 AK26 AL24 AH21	The **receive overhead frame pulse** (ROHFP1-4) signal provides timing for the receive section, line and path overhead extraction. In STS-48/STM-16 mode, ROHFP1 is used to indicate the most significant bit (MSB) on RSLD, RLD, RTOH1-4, RPOH1-4 and the first possible path BIP error on B3E1-4. ROHFP2-4 are not defined. In quad STS-12/STM-4 mode, ROHFP1-4 is used to indicate the most significant bit (MSB) on RSLD, RLD, RTOH1-4, RPOH1-4 and the first possible path BIP error on B3E1-4. ROHFP1-4 is set high when the MSB of the: D1 or D4 byte is present on RSLD. D4 byte is present on RLD. First A1 byte is present on RTOH. First J1 byte is present on RPOH. ROHFP1-4 can be sampled on the rising edge of RSLDCLK, RLDCLK and ROHCLK1-4. ROHFP1-4 is updated on the falling edge of ROHCLK1-4.
RTOH1 RTOH2 RTOH3 RTOH4	TTL Output	AH27 AH25 AH23 AJ21	The **receive transport overhead** (RTOH1-4) signal contains the received transport overhead bytes (A1, A2, J0, Z0, B1, E1, F1, D1-D3, H1-H3, B2, K1, K2, D4-D12, Z1/S1, Z2/M1, and E2) extracted from the incoming stream. RTOH1-4 is updated on the falling edge of ROHCLK1-4.

Pin Name	Type	Pin No.	Function
RPOH1 RPOH2 RPOH3 RPOH4	TTL Output	AK28 AJ25 AJ23 AK21	The **receive path overhead** (RPOH1-4) signal contains the received path overhead bytes (J1, B3, C2, G1, F2, H4, Z3, Z4, and Z5) extracted from the STS-48c/STS-36c/STS-24c/STS-12c/STS-3c/STS-1 SONET path overhead or the AU4-16c/AU4-12c/AU4-8c/AU4-4c/AU4/AU3/TU3 SDH path overhead. The RPOHEN1-4 signal is set high to indicate valid path overhead bytes on RPOH1-4. RPOH1-4 is updated on the falling edge of ROHCLK1-4.
RPOHEN1 RPOHEN2 RPOHEN3 RPOHEN4	TTL Output	AJ27 AK25 AK23 AG20	The **receive path overhead enable** (RPOHEN1-4) signal indicates valid path overhead bytes on RPOH1-4 When RPOHEN1-4 signal is set high, the corresponding path overhead byte presented on RPOH1-4 is valid. When RPOHEN1-4 is set low, the corresponding path overhead byte presented on RPOH1-4 is invalid. RPOHEN1-4 is updated on the falling edge of ROHCLK1-4.

9.7 Transmit Section/Line/Path Overhead Insertion Signals (single and quad mode)

Pin Name	Type	Pin No.	Function
TOHCLK1 TOHCLK2 TOHCLK3 TOHCLK4	TTL Output	AK19 AL17 AK14 AG13	The **transmit overhead clock** (TOHCLK1-4) signal provides timing for the transmit section, line and path overhead insertion. In STS-48/STM-16 mode, TOHCLK1 is a nominal 20.736 MHz clock generated by gapping a 25.92 MHz clock. TOHCLK1 has a 33% high duty cycle. TOHCLK2-4 are not defined. In quad STS-12/STM-4 mode, TOHCLK1-4 is a nominal 20.736 MHz clock generated by gapping a 25.92 MHz clock. TOHCLK1-4 has a 33% high duty cycle. TOHFP1-4 and TPOHRDY1-4 are updated on the falling edge of TOHCLK1-4. TTOH1-4, TTOHEN1-4, TPOH1-4 and TPOHEN1-4 are sampled on the rising edge of TOHCLK1-4.

Pin Name	Type	Pin No.	Function
TOHFP1 TOHFP2 TOHFP3 TOHFP4	TTL Output	AL19 AL15 AH14 AL12	The **transmit overhead frame pulse** (TOHFP1-4) signal provides timing for the transmit section, line and path overhead insertion. In STS-48/STM-16 mode, TOHFP1 is used to indicate the most significant bit (MSB) on TSLD, TLD, TTOH1-4 and TPOH1-4. TOHFP2-4 are not defined. In quad STS-12/STM-4 mode, TOHFP1-4 is used to indicate the most significant bit (MSB) on TSLD, TLD, TTOH1-4 and TPOH1-4. TOHFP1-4 is set high when the MSB of the: D1 or D4 byte should be present on TSLD. D4 byte should be present on TLD. First A1 byte should be present on TTOH. First J1 byte should be present on TPOH TOHFP1-4 can be sampled on the rising edge of TSLDCLK, TLDCLK and TOHCLK1-4 TOHFP1-4 is updated on the falling edge of TOHCLK1-4.
TTOH1 TTOH2 TTOH3 TTOH4	TTL Input	AG18 AK15 AG14 AJ12	The **transmit transport overhead** (TTOH1-4) signal contains the transport overhead bytes (A1, A2, J0, Z0, B1, E1, F1, D1-D3, H1-H3, B2, K1, K2, D4-D12, Z1/S1, Z2/M1, and E2) to be transmitted and the error masks to be applied on B1, B2, H1 and H2. TTOH1-4 is sampled on the rising edge of TOHCLK1-4..
TTOHEN1 TTOHEN2 TTOHEN3 TTOHEN4	TTL Input	AK18 AJ15 AL13 AH12	The **transmit transport overhead insert enable** (TTOHEN1-4) signal controls the insertion of the transmit transport overhead data which is inserted in the outgoing stream. When TTOHEN1-4 is high during the most significant bit of a TOH byte on TTOH1-4, the sampled TOH byte is inserted into the corresponding transport overhead byte positions (A1, A2, J0, Z0, E1, F1, D1-D3, H3, K1, K2, D4-D12, Z1/S1, Z2/M1, and E2 bytes). When TTOHEN1-4 is low during the most significant bit of a TOH byte on TTOH1-4, that sampled byte is ignored and the default values are inserted into these transport overhead bytes. When TTOHEN1-4 is high during the most significant bit of the H1, H2, B1 or B2 TOH byte positions on TTOH1-4, the sampled TOH byte is logically XOR'ed with the associated incoming byte to force bit errors on the outgoing byte. A logic low bit in the TTOH1-4 byte allows the incoming bit to go through while a bit set to logic high will toggle the incoming bit. A low level on TTOHEN1-4 during the MSB of the TOH byte disables the error forcing for the entire byte. TTOHEN1-4 is sampled on the rising edge of TOHCLK1-4.

Pin Name	Type	Pin No.	Function
TPOH1 TPOH2 TPOH3 TPOH4	TTL Input	AL18 AH15 AK13 AG12	The **transmit path overhead** (TPOH1-4) signal contains the path overhead bytes (J1, C2, G1, F2, Z3, Z4, and Z5) to be transmitted in the STS-48c/STS-36c/STS-24c/STS-12c/STS-3c/STS-1 SONET path overhead or the AU4-16c/AU4-12c/AU4-8c/AU4-4c/AU4/AU3/TU3 SDH path overhead and the error masks to be applied on B3 and H4. A path overhead byte is accepted for transmission when the external source indicates a valid byte (TPOHEN1-4 set high) and the SPECTRA-2488 indicates ready (TPOHRDY1-4 set high). The SPECTRA-2488 will ignore the byte on TPOH1-4 when TPOHEN1-4 is set low. The TPOHRDY1-4 is set low to indicate the SPECTRA-2488 is not ready, and the byte must be re-presented at the next opportunity. TPOH1-4 is sampled on the rising edge of TOHCLK1-4.
TPOHRDY1 TPOHRDY2 TPOHRDY3 TPOHRDY4	TTL Output	AH17 AL14 AH13 AJ11	The **transmit path overhead insert ready** (TPOHRDY1-4) signal indicates if the SPECTRA-2488 is ready to accept the byte currently on TPOH1-4. TPOHRDY1-4 is set high during the most significant bit of a POH byte to indicate readiness to accept the byte on the TPOH1-4 input. This byte will be accepted if TPOHEN1-4 is also set high. If TPOHEN1-4 is set low, the byte is invalid and is ignored. TPOHRDY1-4 is set low to indicate that the SPECTRA-2488 is unable to accept the byte on TPOH1-4, and expects the byte to be re-presented at the next opportunity. TPOHRDY1-4 is updated on the falling edge of TOHCLK1-4.
TPOHEN1 TPOHEN2 TPOHEN3 TPOHEN4	TTL Input	AG17 AG15 AJ13 AK11	The **transmit path overhead insert enable** (TPOHEN1-4) signal controls the insertion of the transmit path overhead data which is inserted in the outgoing stream. TPOHEN1-4 shall be set high during the most significant bit of a POH byte to indicate valid data on the TPOH1-4 input. This byte will be accepted for transmission if TPOHRDY1-4 is also set high. If TPOHRDY1-4 is set low, the byte is rejected and must be re-presented at the next opportunity. Accepted bytes sampled on TPOH1-4 are inserted into the corresponding path overhead byte positions (for the J1, C2, G1, F2, Z3, Z4, and Z5 bytes). The byte on TPOH1-4 is ignored when TPOHEN1-4 is set low during the most significant bit position. When the byte at the B3 or H4 byte position on TPOH1-4 is accepted, it is used as an error mask to modify the corresponding transmit B3 or H4 path overhead byte, respectively. The accepted error mask is XOR'ed with the corresponding B3 or H4 byte before it is transmitted. TPOHEN1-4 is sampled on the rising edge of the TOHCLK1-4.

9.8 Receive Section/Line DCC Extraction Signals (single and quad mode)

Pin Name	Type	Pin No.	Function
RSLDCLK	TTL Tristate Output	AL20	The **receive section or line data communication channel clock** (RSLDCLK) signal is used to update the receive section or line DCC (RSLD). When section DCC is selected, RSLDCLK is a nominal 192 kHz clock 50 % duty cycle. When line DCC is selected, RSLDCLK is a nominal 576 kHz clock with 50 % duty cycle. RSLD is updated on the falling edge of RSLDCLK and ROHFP1-4 is used to identify the MSB of the D1 or the D4 byte on RSLD. The RSLDSEL bit in the RRMP 0080H, 0480H, 0880H and 0C80H registers selects the section or line DCC and the RSLDTS bit tri-states RSLDCLK and RSLD outputs. The RDCC[1:0] bits in the SPECTRA 0001H register select which channel is muxed onto RSLDCLK.
RSLD	TTL Tristate Output	AG19	The **receive section or line data communication channel** (RSLD) signal contains the received section DCC (D1-D3) or line DCC (D4-D12). RSLD is updated on the falling edge of RSLDCLK and should be sampled externally on the rising edge of RSLDCLK. ROHFP1-4 is used to identify the MSB of the D1 or the D4 byte on RSLD. The RSLDSEL bit in the RRMP 0080H, 0480H, 0880H and 0C80H registers selects the section or line DCC and the RSLDTS bit tri-states RSLDCLK and RSLD outputs. The RDCC[1:0] bits in the SPECTRA 0001H register select which channel is muxed onto RSLD.
RLDCLK	TTL Tristate Output	AH19	The **receive line data communication channel clock** (RLDCLK) signal is used to update the received line DCC (RLD). RLDCLK is a nominal 576 kHz clock 50 % duty cycle. RLD is updated on the falling edge of RLDCLK and ROHFP1-4 is used to identify the MSB of the D4 byte on RLD. The RLDTS bit in the RRMP 0080H, 0480H, 0880H and 0C80H registers tri-states RLDCLK and RLD outputs. The RDCC[1:0] bits in the SPECTRA 0001H register select which channel is muxed onto RLDCLK.

Pin Name	Type	Pin No.	Function
RLD	TTL Tristate Output	AJ19	The **receive line data communication channel** (RLD) signal contains the received line DCC (D4-D12). RLD is updated on the falling edge of RLDCLK and should be sampled externally on the rising edge of RLDCLK. ROHFP1-4 is used to identify the MSB of the D4 byte on RLD. The RLDTS bit in the RRMP 0080H, 0480H, 0880H and 0C80H register tri-states RLDCLK and RLD outputs. The RDCC[1:0] bits in the SPECTRA 0001H register select which channel is muxed onto RLD.

9.9 Transmit Section/Line DCC Insertion Signals (single and quad mode)

Pin Name	Type	Pin No.	Function
TSLDCLK	TTL Tristate Output	AH11	The **transmit section or line data communication channel clock** (TSLDCLK) signal is used to clock in the transmit section or line DCC (TSLD). When section DCC is selected, TSLDCLK is a nominal 192 kHz clock 50 % duty cycle. When line DCC is selected, TSLDCLK is a nominal 576 kHz clock 50 % duty cycle. TSLD is sampled on the rising edge of TSLDCLK and TOHFP1-4 is used to identify the MSB of the D1 or the D4 byte on TSLD. The TSLDSEL bit in the TRMP 1080H, 1480H, 1880H and 1C80H registers selects the section or line DCC and the TSLDTS bit tri-states TSLDCLK output. The TDCC[1:0] bits in the SPECTRA 0002H register select which channel is muxed onto TSLDCLK.
TSLD	TTL Input	AL10	The **transmit section or line data communication channel** (TSLD) signal contains the section DCC (D1-D3) or the line DCC (D4-D12) to be transmitted. TSLD is sampled on the rising edge of TSLDCLK and TOHFP1-4 is used to identify the MSB of the D1 or the D4 byte on TSLD. The TTOH and TTOHEN inputs take precedence over TSLD. The TSLDSEL bit in the TRMP 1080H, 1480H, 1880H and 1C80H registers selects the section or line DCC. The TDCC[1:0] bits in the SPECTRA 0002H register select which channel is muxed onto TSLD.

Pin Name	Type	Pin No.	Function
TLDCLK	TTL Tristate Output	AK10	The **transmit line data communication channel clock** (TLDCLK) signal is used to clock in the transmit line DCC (TLD). TLDCLK is a nominal 576 kHz clock 50 % duty cycle. TLD is sampled on the rising edge of TLDCLK and TOHFP1-4 is used to identify the MSB of the D4 byte on TLD. The TLDTS bit in the TRMP 1080H, 1480H, 1880H and 1C80H registers tri-states TLDCLK output. The TDCC[1:0] bits in the SPECTRA 0002H register select which channel is muxed onto TLDCLK.
TLD	TTL Input	AJ10	The **transmit line data communication channel** (TLD) signal contains the line DCC (D4-D12) to be transmitted. TLD is sampled on the rising edge of TLDCLK and TOHFP1-4 is used to identify the MSB of the D4 byte on TLD. The TTOH and TTOHEN inputs take precedence over TLD. The TDCC[1:0] bits in the SPECTRA 0002H register select which channel is muxed onto TLD.

9.10 Receive Path BIP-8 Error Signals (single mode only)

Pin Name	Type	Pin No.	Function
B3E1 B3E2 B3E3 B3E4	TTL Output	AF27 AL27 AJ24 AJ22	The **bit interleaved parity error** (B3E1-4) signal carries the path BIP-8 errors detected for each STS-48c/STS-36c/STS-24c/ STS-12c/STS-3c/STS-1 SONET payload or AU4-16c/AU4-12c/AU4-8c/AU4-4c/AU4/AU3/TU3 SDH payload. B3E1-4 is set high for one ROHCLK1-4 clock cycle for each path BIP-8 error detected (up to eight errors per path per frame). When BIP-8 errors are treated on a block basis, B3E1-4 is set high for one ROHCLK1-4 clock cycle for up to eight path BIP-8 errors detected (up to one error per path per frame). Path BIP-8 errors are detected by comparing the extracted path BIP-8 byte (B3) with the computed path BIP-8 byte of the previous frame. The FORCEB3E bit in the SPECTRA 0001H register force, in quad mode, the B3E2-4 outputs instead of the SALM2-4 outputs. B3E1-4 is updated on the falling edge of ROHCLK1.

9.11 Drop Bus Telecom Interface Signals (single and quad mode)

Pin Name	Pin Type	PIN No.	Function
DCK	TTL Schmidt Input	AG31	The **DROP bus clock** (DCK) signal provides timing for the DROP bus interface. DCK is nominally a 77.76 MHz 50 % duty cycle clock. Frequency offset between the receive line side clock and the DROP bus clock are accommodated by pointer justification events on the DROP bus. DCK is a Schmidt triggered input. DCMP and DJ0REF are sampled on the rising edge of DCK. DD1-4[7:0], DPL1-4, DJ0J11-4, DDP1-4 and DALARM1-4 are updated on the rising edge of DCK
DCMP	TTL Input	AF29	The **DROP Connection Memory Page (DCMP)** signal controls the selection of the connection memory page in the DROP Time-Slot Interchange block. DCMP is XORed with the PSEL bit in the DSTSI 0222H register. When DCMP xor PSEL is set high, connection memory page 1 is selected. When DCMP xor PSEL is set low, connection memory page 0 is selected. DCMP is sampled at the J0 byte location as defined by the DJ0J1 output. Changes to the connection memory page selection is synchronized to the transport frame boundary of the second next frame. DCMP is sampled on the rising edge of DCK
DJ0REF	TTL Input	AE27	The active high **DROP bus J0 position** (DJ0REF) signal synchronizes the SONET/SDH frame alignment on the DD1-4[7:0] buses. DJ0REF must be asserted for one DCK clock cycle to synchronize the section trace byte. In STS-48/STM-16 mode, the section trace byte is synchronized on DD1[7:0] bus. In the quad STS-12/STM-4 mode, the section trace bytes are synchronized on DD1-4[7:0] buses. It is not necessary for DJ0REF to be present at every frame, an internal counter fly-wheels based on the most recent DJ0REF assertion. The DFPEN bit in the SPECTRA 0014H register synchronizes the drop bus on the first byte after the J0/Z0 bytes instead of the section trace. DJ0REF is sampled on the rising edge of DCK.

Pin Name	Pin Type	PIN No.	Function
DD1[7] DD1[6] DD1[5] DD1[4] DD1[3] DD1[2] DD1[1] DD1[0] DD2[7] DD2[6] DD2[5] DD2[4] DD2[3] DD2[2] DD2[1] DD2[0] DD3[7] DD3[6] DD3[5] DD3[4] DD3[3] DD3[2] DD3[1] DD3[0] DD4[7] DD4[6] DD4[5] DD4[4] DD4[3] DD4[2] DD4[1] DD4[0]	TTL Output	G30 G29 G28 F30 G27 F29 E31 F28 N28 N27 M31 M30 M29 M28 M27 L30 W30 W31 V27 V28 V29 V30 V31 U27 AE31 AD28 AD29 AD30 AC27 AD31 AC28 AC30	The **DROP bus data** (DD1-4[7:0]) bus carries the 32-bit serial STS-48c/STS-36c/STS-24c/STS-12c/STS-3c/STS-1 SONET payload or AU4-16c/AU4-12c/AU4-8c/AU4-4c/AU4/AU3/TU3 SDH payload when the device is configured in STS-48/STM-16 mode or carries the four byte serial STS-12c/STS-3c/STS-1 SONET payload or AU4-4c/AU4/AU3/TU3 SDH payload when the device is configured in quad STS-12/STM-4 mode. When the DROP bus STSI functionality is disabled, the dropped payload multiplexing corresponds to that of the received SONET/SDH data. STSI may be used to reorder this multiplexing on the DROP bus. The transport overhead bytes, with the exception of the H1, H2 pointer bytes, are set to zeros. The framing pattern may be inserted in the A1 and A2 framing bytes. The fixed stuff columns in a tributary mapped SPE (VC) may also be optionally set to zero. DD1-4[7] are the most significant bit (corresponding to bit 1 of each serial word, the first bit received). DD1-4[0] are the least significant bit (corresponding to bit 8 of each serial word, the last bit received). DD1-4[7:0] is updated on the rising edge of DCK.
DPL1 DPL2 DPL3 DPL4	TTL Output	E30 L28 U28 AB27	The active high **DROP bus payload** (DPL1-4) signal indicates when the DD1-4[7:0] bus is carrying a payload byte. DPL1-4 is set high during path overhead and payload bytes and low during transport overhead bytes. DPL1-4 is set high during the H3 byte to indicate a negative pointer justification event and set low during the byte following the H3 byte to indicate a positive pointer justification event. DPL1-4 is updated on the rising edge of DCK.
DJ0J11 DJ0J12 DJ0J13 DJ0J14	TTL Output	F27 K31 U29 AC31	The active high **DROP bus composite timing** (DJ0J1-4) signal indicates the frame and payload boundaries on the DD1-4[7:0] bus. DJ0J11-4 pulses high with the DROP bus payload active signal DPL1-4 set low to mark the section trace byte (J0). DJ0J11-4 pulses high with DPL1-4 set high to mark all the path trace byte (J1). DJ0J11-4 is updated on the rising edge of DCK.

Pin Name	Pin Type	PIN No.	Function
DALARM1 DALARM2 DALARM3 DALARM4	TTL Output	H28 N30 W27 AE30	The active high **Drop bus Alarm** (DALARM1-4) signal indicates path AIS. DALARM1-4 is set high when the byte on DD1-4[7:0] is in path AIS and is set low when the byte is out of path AIS. DALARM1-4 is updated on the rising edge of DCLK.
DDP1 DDP2 DDP3 DDP4	TTL Output	G31 N29 W28 AD27	The **DROP bus data parity** (DDP1-4) signal indicates the parity of the DROP bus signals. The DD1-4[7:0] data bus is always included in parity calculations. The DPLPAREN, DJ0J1PAREN, D32PAREN and DODDPAREN bits in the SPECTRA 0014H register control the inclusion of the DPL1-4, DJ0J11-4, DD1-4 signals in parity calculation and the sense (odd/even) of the parity. DDP1-4 is updated on the rising edge of DCK.

9.12 Add Bus Telecom Interface Signals (single and quad mode)

Pin Name	Pin Type	PIN No.	Function
ACK	TTL Schmidt Input	AE28	The **ADD bus clock** (ACK) signal provides timing for the ADD bus interface. ACK is nominally a 77.76 MHz 50 % duty cycle clock. Frequency offset between the transmit line side clock and the ADD bus clock are accommodated by pointer justification events on the transmit line side. ACK is a Schmidt triggered input. ACMP, AD1-4[7:0], APL1-4, AJ0J1_AFP1-4, ADP1-4 and APAIS1-4 are sampled on the rising edge of ACK.
ACMP	TTL Input	AF30	The **ADD Connection Memory Page (ACMP)** signal controls the selection of the connection memory page in the ADD Time-Slot Interchange block. ACMP is XORed with the PSEL bit in the ASTSI 1222H register. When ACMP xor PSEL is set high, connection memory page 1 is selected. When ACMP xor PSEL is set low, connection memory page 0 is selected. ACMP is sampled at the J0 byte location as defined by the AJ0J1 input. Changes to the connection memory page selection is synchronized to the transport frame boundary of the second next frame. ACMP is sampled on the rising edge of ACK

Pin Name	Pin Type	PIN No.	Function
AD1[7] AD1[6] AD1[5] AD1[4] AD1[3] AD1[2] AD1[1] AD1[0] AD2[7] AD2[6] AD2[5] AD2[4] AD2[3] AD2[2] AD2[1] AD2[0] AD3[7] AD3[6] AD3[5] AD3[4] AD3[3] AD3[2] AD3[1] AD3[0] AD4[7] AD4[6] AD4[5] AD4[4] AD4[3] AD4[2] AD4[1] AD4[0]	TTL Input	B28 C27 E26 B27 D26 A27 C26 E25 K28 J31 K27 J30 J29 J28 H31 J27 R31 R30 R29 R28 P31 P30 P29 P28 AB30 AB31 AA28 AA29 AA30 Y27 Y28 Y29	The **ADD bus data** (AD1-4[7:0]) bus carries the 32-bit serial STS-48c/STS-36c/STS-24c/STS-12c/STS-3c/STS-1 SONET payload or AU4-16c/AU4-12c/ AU4-8c/AU4-4c/AU4/AU3/TU3 SDH payload to be transmitted when the device is configured in STS-48/STM-16 mode or carries the four byte serial STS-12c/STS-3c/STS-1 SONET payload or AU4-4c/AU4/AU3/TU3 SDH payload to be transmitted when the device is configured in quad STS-12/STM-4 mode. When the ADD bus STSI functionality is disabled, the transmit SONET/SDH payload multiplexing corresponds to that of the ADD bus. STSI may be used to reorder this multiplexing on the transmit SONET/SDH payload. The transport overhead bytes are ignored with the programmable exception of H1 and H2 pointer bytes. The phase relation of the SPE (VC) to the transport frame is determined by the ADD bus composite timing signal AJ0J1_FP1-4 or optionally by interpreting the H1 and H2 pointer bytes. A V1 pulse in the AJ0J1_FP1-4 composite signal is tolerated but is not used to insert the multi-frame indication in the H4 byte. A valid H4 byte must be provided on the ADD bus to indicate the multi-frame alignment in a tributary structure SPE (VC). AD1-4[7] are the most significant bit (corresponding to bit 1 of each serial word, the first bit transmitted). AD1-4[0] are the least significant bit (corresponding to bit 8 of each serial word, the last bit transmitted). AD1-4[7:0] is sampled on the rising edge of ACK.
APL1 APL2 APL3 APL4	TTL Input	B26 H30 P27 Y30	The active high **ADD bus payload** (APL1-4) signal indicates when the AD1-4[7:0] bus is carrying a payload byte. APL1-4 is set high during path overhead and payload bytes and low during transport overhead bytes. APL1-4 is set high during the H3 byte to indicate a negative pointer justification event and set low during the byte following the H3 byte to indicate a positive pointer justification event. APL1-4 is sampled on the rising edge of ACK.

Pin Name	Pin Type	PIN No.	Function
AJ0J1_FP1 AJ0J1_FP2 AJ0J1_FP3 AJ0J1_FP4	TTL Input	D25 H29 N31 Y31	The active high **ADD bus composite timing** (AJ0J1_FP1-4) signal indicates the frame and optionally payload boundaries on the AD1-4[7:0] bus. AJ0J11-4 is defined when the AFPEN bit in the SPECTRA 0016H register is set low. AJ0J11-4 pulses high with the ADD bus payload active signal APL1-4 set low to mark the section trace byte (J0). Optionally, AJ0J11-4 pulses high with APL1-4 set high to mark all the path trace byte (J1). Setting TAPIDIS bit low in the SPECTRA 0002H register enables pointer interpretation on the ADD bus. Valid H1 and H2 pointer bytes must be provided on the ADD bus to allow the J1 position to be identified. The AD1-4[7:0] buses must be frame aligned to have the J0 pulses of the AJ0J11-4 composite signals high simultaneously. AJ0J1_FP1-4 is sampled on the rising edge of ACK.
			The active high **ADD bus framing position** (AJ0J1_FP1-4) signal indicates when the first byte of the payload after the J0/Z0 bytes is available on the AD1-4[7:0] bus. AFP1-4 is defined when the AFPEN bit in the SPECTRA 0016H register is set high. In STS-48/STM-16 mode, AFP1-4 pulses high to mark the first payload byte after the J0/Z0 bytes on the AD1[7:0] bus. In the quad STS-12/STM-4 mode, AFP1-4 pulses high to mark the first payload bytes after the J0/Z0 bytes on the AD1-4[7:0] buses. Note that AFP1-4 has a fixed relationship to the SONET/SDH frame but the start of the payload is determined by the STS/AU/TU pointer and may change relative to AFP1-4. The TAPIDIS bit in the SPECTRA 0002H register must be set low in this mode to enable pointer interpretation on the ADD bus. Valid H1 and H2 pointer bytes must be provided on the ADD buses to allow the J1 position to be identified. The AD1-4[7:0] buses must be frame aligned to have the FP pulses of the AFP1-4 composite signals high simultaneously. AJ0J1_FP1-4 is sampled on the rising edge of ACK.
APAIS1 APAIS2 APAIS3 APAIS4	TTL Input	E29 K30 U30 AB28	The active high **ADD bus Path AIS** (ADDPAIS1-4) signal indicates path AIS. APAIS1-4 is set high when the byte on AD1-4[7:0] is in path AIS and is set low when the byte is out of path AIS. APAIS1-4 is sampled on the rising edge of ACLK.

Pin Name	Pin Type	PIN No.	Function
ADP1 ADP2 ADP3 ADP4	TTL Input	D30 K29 U31 AB29	The **ADD bus data parity** (ADP1-4) signal indicates the parity of the ADD bus signals. The AD1-4[7:0] data bus is always included in parity calculations. The APLPAREN, AJ0J1PAREN, A32PAREN and AODDPAREN bits in the SPECTRA 0016H register control the inclusion of the APL1-4, AJ0J11-4, AD1-4 signals in parity calculation and the sense (odd/even) of the parity. ADP1-4 is sampled on the rising edge of ACK.

9.13 Microprocessor Interface Signals

Pin Name	Type	Pin No.	Function
CSB	TTL Schmidt Input	E19	The active low chip select (CSB) signal is low during SPECTRA-2488 register accesses. CSB is a Schmidt triggered input. Note that when not being used, CSB must be tied low. If CSB is not required (i.e. register accesses controlled using the RDB and WRB signals only), CSB must be connected to an inverted version of the RSTB input.
RDB	TTL Input	B20	The active low read enable (RDB) signal is low during a SPECTRA-2488 read access. The SPECTRA-2488 drives the D[15:0] bus with the contents of the addressed register while RDB and CSB are low.
WRB	TTL Input	C20	The active low write strobe (WRB) signal is low during a SPECTRA-2488 register write access. The D[15:0] bus contents are clocked into the addressed register on the rising WRB edge while CSB is low.
D[15] D[14] D[13] D[12] D[11] D[10] D[9] D[8] D[7] D[6] D[5] D[4] D[3] D[2] D[1] D[0]	TTL I/O	D12 C12 B12 A12 E13 D13 C13 B13 A13 D14 C14 B14 A14 E15 D15 C15	The bi-directional data bus, D[15:0], is used during SPECTRA-2488 read and write accesses.
A[13]	TTL Input	A15	The test register select signal (TRS) selects between normal and test mode register accesses. TRS is high during test mode register accesses, and is low during normal mode register accesses. TRS may be tied low.

Pin Name	Type	Pin No.	Function
A[12] A[11] A[10] A[9] A[8] A[7] A[6] A[5] A[4] A[3] A[2] A[1] A[0]	TTL Input	A17 B17 C17 D17 E17 A18 B18 C18 D18 E18 A19 B19 c19	The address bus (A[12:0]) selects specific registers during SPECTRA-2488 register accesses.
RSTB	TTL Schmidt Input	D20	The active low reset (RSTB) signal provides an asynchronous SPECTRA-2488 reset. RSTB is a Schmidt triggered input with an integral pull-up resistor.
ALE	TTL Input	A20	The address latch enable (ALE) is an active-high signal and latches the address bus A[13:0] when low. When ALE is high, the internal address latches are transparent. It allows the SPECTRA-2488 to interface to a multiplexed address/data bus. The ALE input has an integral pull up resistor.
INTB	TTL OD Output	B21	The active low interrupt (INTB) is set low when a SPECTRA-2488 enabled interrupt source is active. The SPECTRA-2488 may be enabled to report many alarms or events via interrupts. INTB is tri-stated when the interrupt is acknowledged via the appropriate register access. INTB is an open drain output.

9.14 Analog Miscellaneous Signals

Pin Name	Type	Pin No.	Function
TDREF[0] TDREF[1]	Analog	R4 R3	The transmit data reference (TDREF0 and TDREF1) analog pins are provided to create calibrated currents for the PECL output transceivers TD+/-. A 2.55 KOhm, 1% resistor is connected across TDREF0 and TDREF1 pins.
ATP[1] ATP[0]	Analog	P4 P5	Two analog test ports (ATP0, ATP1) are provided for production testing only. These pins must be tied to analog ground (AVS) during normal operation.

9.15 JTAG Test Access Port (TAP) Signals

Pin Name	Type	Pin No.	Function
TCK	TTL Schmidt Input	C22	The test clock (TCK) signal provides timing for test operations that can be carried out using the IEEE P1149.1 test access port. TCK is a Schmidt triggered input.
TMS	TTL Input	A22	The test mode select (TMS) signal controls the test operations that can be carried out using the IEEE P1149.1 test access port. TMS is sampled on the rising edge of TCK. TMS has an integral pull up resistor.

Pin Name	Type	Pin No.	Function
TDI	TTL Input	D21	When the SPECTRA-2488 is configured for JTAG operation, the test data input (TDI) signal carries test data into the SPECTRA-2488 via the IEEE P1149.1 test access port. TDI is sampled on the rising edge of TCK. TDI has an integral pull up resistor.
TDO	TTL Tristate Output	C21	The test data output (TDO) signal carries test data out of the SPECTRA-2488 via the IEEE P1149.1 test access port. TDO is updated on the falling edge of TCK. TDO is a tri-state output which is inactive except when scanning of data is in progress.
TRSTB	TTL Schmidt Input	B22	The active low test reset (TRSTB) signal provides an asynchronous SPECTRA-2488 test access port reset via the IEEE P1149.1 test access port. TRSTB is a Schmidt triggered input with an integral pull up resistor. In the event that TRSTB is not used, it must be connected to RSTB.

9.16 Power and Ground

Pin Name	Pin Type	PIN No.	Function
TAVDH	3.3 V Analog Power	AK8 AG4 AD4 Y4	The transmit analog power (TAVDH) pins for the analog core. The TAVDH pins should be connected through passive filtering networks to a well-decoupled +3.3V analog power supply. Please see the Operation section for detailed information.
TAVSH	Analog Ground	AK7 AF5 AC4 W4	The transmit analog ground (TAVSH) pins for the analog core. The TAVSH pins should be connected to the analog ground of the power supply. Please see the Operation section for detailed information.
TAVDL	1.8 V Analog Power	AJ7 AG1 AB5 W1	The transmit analog power (TAVDL) pins for the analog core. The TAVDL pins should be connected through passive filtering networks to a well-decoupled +1.8V analog power supply. Please see the Operation section for detailed information.
TAVSL	Analog Ground	AL5 AE3 AB1 U5	The transmit analog ground (TAVSL) pins for the analog core. The TAVSL pins should be connected to the analog ground of the power supply. Please see the Operation section for detailed information.
RAVDH	3.3 V Analog Power	M2 H2 E4 C8	The receive analog power (RAVDH) pins for the analog core. The RAVDH pins should be connected through passive filtering networks to a well-decoupled +3.3V analog power supply. Please see the Operation section for detailed information.
RAVSH	Analog Ground	L3 G2 B5 C9	The receive analog ground (RAVSH) pins for the analog core. The RAVSH pins should be connected to the analog ground of the power supply. Please see the Operation section for detailed information.
RAVDL	1.8 V Analog Power	K2 F2 D6 B9	The receive analog power (RAVDL) pins for the analog core. The RAVDL pins should be connected through passive filtering networks to a well-decoupled +1.8V analog power supply. Please see the Operation section for detailed information.

Pin Name	Pin Type	PIN No.	Function
RAVSL	Analog Ground	J2 F4 C7 B10	The receive analog ground (RAVSL) pins for the analog core. The RAVSL pins should be connected to the analog ground of the power supply. Please see the Operation section for detailed information.
CAVDH	3.3 V Analog Power	R5	The current reference analog power (CAVDH) pins for the analog core. The CAVDH pins should be connected through passive filtering networks to a well-decoupled +3.3V analog power supply. Please see the Operation section for detailed information.
CAVSH	Analog Ground	P1	The current reference analog ground (CAVSH) pins for the analog core. The CAVSH pins should be connected to the analog ground of the power supply. Please see the Operation section for detailed information.
QAVD	3.3 V Analog Power	P2	The quiet power (QAVD) pins for the analog core. QAVD should be connected to well-decoupled analog +3.3V supply. Please see the Operation section for detailed information.
QAVS	Analog Ground	P3	The quiet ground (QAVS) pins for the analog core. QAVS should be connected to analog ground of the QAVD supply. Please see the Operation section for detailed information.
VDDI[15:0]	1.8 V Digital Power		The core digital power (VDDI) pins should be connected to a well-decoupled +1.8V digital power supply. H27, R27, W29, AE29, AL25, AJ20, AJ14, AL8, AG2, W3, N2, J4, A5, E12, B15, E23
VDDO[47:0]	3.3 V Digital Power		The I/O digital power (VDDO) pins should be connected to a well-decoupled +3.3V digital power supply. A1, A31, B2, B30, C3, C4, C16, C28, C29, D3, D4, D16, D28, D29, E5, E11, E16, E21, E27, L5, L27, T3, T4, T5, T27, T28, T29, AA5, AA27, AG5, AG11, AG16, AG21, AG27, AH3, AH4, AH16, AH28, AH29, AJ3, AJ4, AJ16, AJ28, AJ29, AK2, AK30, AL1, AL31
VSS[55:0]	Digital Ground		The digital ground (VSS) pins should be connected to the digital ground of the digital power supply. A2, A3, A4, A6, A11, A16, A21, A26, A28, A29, A30, B1, B3, B16, B29, B31, C1, C2, C30, C31, D1, D31, F1, F31, L1, L31, T1, T2, T30, T31, AA1, AA31, AF1, AF31, AH1, AH31, AJ1, AJ2, AJ30, AJ31, AK1, AK3, AK16, AK29, AK31, AL2, AL3, AL4, AL6, AL11, AL16, AL21, AL26, AL28, AL29, AL30
NC	No Connect		The No Connect (NC) pins should be left unconnected. E28, L29, AC29, AF28, AK27, AH26, AH24, AL23, AH22, AK20, AH18, AJ18, AJ17, AK17, AK12, AH5, AF4, AD5, AC3, AC2, AA3, W2, V3, R1, R2, N3, N5, L4, K1, G3, G4, F3, E14, D19, D22, C25, D27

Notes on Pin Description

1. All SPECTRA-2488 inputs and bidirectionals present minimum capacitive loading and operate at TTL logic levels except: RDCLK, RD[15:0], RFP, TDCLK and TFPI inputs which operate at pseudo-ECL (PECL) logic levels.
2. All SPECTRA-2488 digital outputs and bidirectionals have 4 mA drive capability except D[15-0], INTB and TDO which have 6 mA drive capability and DJ0J11-4, DPL1-4, DD1-4[7:0], DDP1-4, DALARM1-4, PGMTCLK, TCLK1-4, TD1-4[7:0], PGMRCLK and RCLK1-4 which have 8 mA drive capability.
3. Inputs ALE, RSTB, TMS, TDI and TRSTB have internal pull-up resistors.
4. It is mandatory that every digital ground pin (VSS) be connected to the printed circuit board ground plane to ensure reliable device operation.
5. It is mandatory that every digital power pin (VDDI and VDDO) be connected to the printed circuit board power plane to ensure reliable device operation.
6. All analog power and ground pins can be sensitive to noise. They must be isolated from the digital power and ground. Care must be taken to correctly decouple these pins. Please refer to the Operations sections.
7. Due to ESD protection structures in the pads it is necessary to exercise caution when powering a device up or down. ESD protection devices behave as diodes between power supply pins and from I/O pins to power supply pins. Under extreme conditions it is possible to damage these ESD protection devices or trigger latch up. Please adhere to the recommended power supply sequencing as described in the Operation section of this document.
8. Do not exceed 100 mA of current on any pin during the power-up or power-down sequence. Refer to the Power Sequencing description in the Operations section.
9. Before any input activity occurs, ensure that the device power supplies are within their nominal voltage range.
10. Hold the device in the reset condition until the device power supplies are within their nominal voltage range.

10 Functional Description

10.1 SONET/SDH Receive Line Interface (SRLI)

The SONET/SDH receive line interface block performs byte and frame alignment on the incoming 2488 Mbit/s data stream based on the SONET/SDH A1/A2 framing pattern.

In single STS-48/STM-16 mode, the SRLI supports a 16 bit 155.52 MHz differential PECL line side interface for direct connection to external clock recovery, clock synthesis and serializer-deserializer components. In quad STS-12/STM-4 mode, the SRLI supports four independent 8 bit 77.76 MHz TTL compatible line side interface for direct connection to external clock recovery, clock synthesis and serializer-deserializer components.

Note: In both modes, an external Serial to Parallel Converter (SIPO) must be used. In single STS-48/STM-16 mode, an external or the internal framer (SRLI) can be used. In quad STS-12/STM-4 mode only the internal framer (SRLI) can be used.

While out of frame, the SRLI monitors the receive data stream for an occurrence of the A1/A2 framing pattern. The SRLI adjusts its byte and frame alignment when three consecutive A1 bytes followed by three consecutive A2 bytes occur in the data stream. The SRLI informs the RRMP framer block when the framing pattern has been detected to reinitialize to the new transport frame alignment. While in frame, the SRLI maintains the same byte and frame alignment until the RRMP declares out of frame.

10.2 Receive Regenerator and Multiplexer Processor (RRMP)

The Receive Regenerator and Multiplexer Processor (RRMP) block extracts and process the transport overhead of the received data stream.

The RRMP frames to the data stream by operating with an upstream pattern detector (SRLI) that searches for occurrences of the A1/A2 framing pattern. Once the SRLI has found an A1/A2 framing pattern, the RRMP monitors for the next occurrence of the framing pattern 125µs later. Two framing pattern algorithms are provided to improve performance in the presence of bit errors. In algorithm 1, the RRMP declares frame alignment (removes OOF defect) when 12 A1 and 12 A2 bytes are seen error-free. In algorithm 2, the RRMP declares frame alignment (removes OOF defect) when one A1 byte and the first four bits of one A2 byte are seen error-free. Once in frame, the RRMP monitors the framing pattern and declares OOF when one or more bit errors in the framing pattern are detected for four consecutive frames. Again, depending upon the algorithm either 24 framing bytes or 12 framing bits are examined for bit errors in the framing pattern.

The performance of these framing algorithms in the presence of bit errors and random data is robust. When looking for frame alignment the performance of each algorithm is dominated by the alignment algorithm used in the SRLI which always examines 3 A1 and 3 A2 framing bytes. The probability of falsely framing to random data is less than 0.00001% for either algorithm. Once in frame alignment, the RRMP continuously monitors the framing pattern. When the incoming stream contains a 10^{-3} BER, the first algorithm provides a 99.75% probability that the mean time between OOF occurrences is 1.3 seconds and the second algorithm provides a 99.75% probability that the mean time between OOF occurrences is 7 minutes.

Table 1 A1/A2 Bytes Used For Out Of Frame Detection

SONET/SDH	Algorithm 1	Algorithm 2
STS-12/STM-4	All A1 & A2 bytes	First A1 byte Last A2 byte (first four bits only)
STS-48/STM-16	STS-12 #1 All A1 bytes STS-12 #4 All A2 bytes	STS-12 #1 First A1 byte STS-12 #4 Last A2 byte (first four bits only)

Table 2 A1/A2 Bytes Used For In Frame Detection

SONET/SDH	Algorithm 1	Algorithm 2
STS-12/STM-4	All A1 & A2 bytes	First A1 byte Last A2 byte (first four bits only)
STS-48/STM-16	STS-12 #1 All A1 bytes STS-12 #1 All A2 bytes	STS-12 #1 First A1 byte STS-12 #1 Last A2 byte (first four bits only)

The RRMP also detects loss of frame (LOF) defect and loss of signal (LOS) defect. LOF is declared when an out of frame (OOF) condition exists for a total period of 3ms during which there is no continuous in frame period of 3 ms. LOF output is removed when an in frame condition exists for a continuous period of 3 ms. LOS is declared when a continuous period of 20 µs without transitions on the received data stream is detected. LOS is removed when two consecutive framing patterns are found (based on algorithm 1 or algorithm 2) and during the intervening time (one frame) there are no continuous periods of 20 µs without transitions on the received data stream.

The RRMP calculates the section BIP-8 error detection code on the scrambled data of the complete frame. The section BIP-8 code is based on a bit interleaved parity calculation using even parity. The calculated BIP-8 code is compared with the BIP-8 code extracted from the B1 byte of STS-1 (STM-0) #1 of the following frame after de-scrambling. Any difference indicates a section BIP-8 error. The RRMP accumulates section BIP-8 errors in a microprocessor readable 16 bits saturating counter (up to 1 second accumulation time). Optionally, block section BIP-8 errors can be accumulated.

The RRMP optionally de-scrambles the received data stream.

The RRMP calculates the line BIP-8 error detection codes on the de-scrambled line overhead and synchronous payload envelope bytes of the constituent STS-1 (STM-0). The line BIP-8 code is based on a bit interleaved parity calculation using even parity. The calculated BIP-8 codes are compared with the BIP-8 codes extracted from the B2 byte of the constituent STS-1 (STM-0) of the following frame after de-scrambling. Any difference indicates a line BIP-8 error. The RRMP accumulates line BIP-8 errors in a microprocessor readable 24 bits saturating counter (up to 1 second accumulation time). Optionally, block BIP-24 errors can be accumulated.

The RRMP extracts the line remote error indication (REI-L) errors from the M1 byte of STS-1 (STM-0) #3 and accumulates them in a microprocessor readable 24 bits saturating counter (up to 1 second accumulation time). Optionally, block line REI errors can be accumulated.

The RRMP extracts and filters the K1/K2 APS bytes for three frames. The filtered K1/K2 APS bytes are accessible through microprocessor readable registers. The RRMP also monitors the unfiltered K1/K2 APS bytes to detect APS byte failure (APSBF-L) defect, line alarm indication signal (AIS-L) defect and line remote defect indication (RDI-L) defect. APS byte failure is declared when twelve consecutive frames have been received where no three consecutive frames contain identical K1 bytes. The APS byte failure is removed upon detection of three consecutive frames containing identical K1 bytes. The detection of invalid APS codes must be done is done in software by polling the K1/K2 APS register. Line AIS is declared when the bit pattern 111 is observed in bits 6, 7, and 8 of the K2 byte for three or five consecutive frames. Line AIS is removed when any pattern other than 111 is observed for three or five consecutive frames. Line RDI is declared when the bit pattern 110 is observed in bits 6, 7, and 8 of the K2 byte for three or five consecutive frames. Line RDI is removed when any pattern other than 110 is observed for three or five consecutive frames.

The RRMP extracts and filters the synchronization status message (SSM) for eight frames. The filtered SSM is accessible through microprocessor readable registers.

RRMP optionally inserts line alarm indication signal (AIS-L).

The RRMP extracts and serially outputs all the transport overhead (TOH) bytes on the RTOH port. The TOH bytes are output in the same order that they are received (A1, A2, J0/Z0, B1, E1, F1, D1-D3, H1-H3, B2, K1, K2, D4-D12, S1/Z1, Z2/M1/Z2 and E2). RTOHCLK is the generated output clock used to provide timing for the RTOH port. RTOHCLK is a nominal 20.736 MHz clock generated by gapping a 25.92 MHz clock. Sampling RTOHFP high with the rising edge of RTOHCLK identifies the MSB of the first A1 byte.

Figure 3 STS-12 (STM-4) on RTOH 1-4or STS-48 (STM-16) on RTOH1

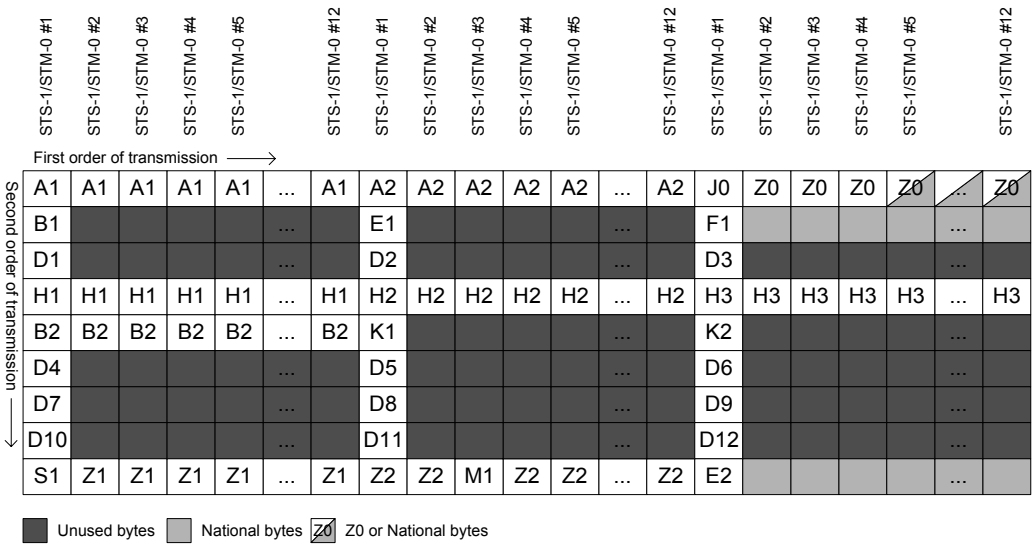
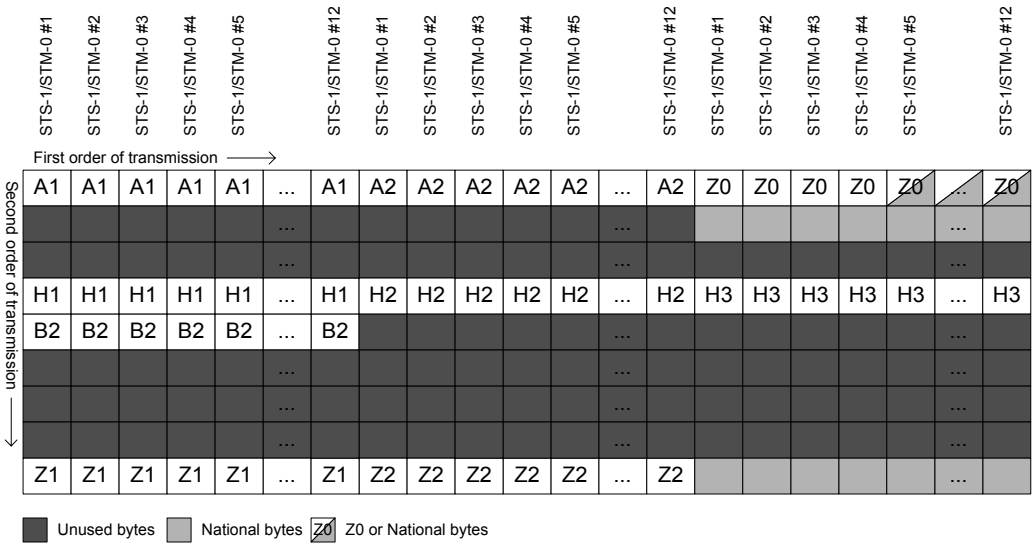


Figure 4 STS-48 (STM-16) on RTOH2-4



The RRMP serially outputs the line DCC bytes on the RLD and the RSLD ports. The line DCC bytes (D4-D12) are output on RLD. RSLD is selectable to output either the section DCC bytes (D4-D12) or the line DCC bytes (D1-D3). RLDCLK is the generated output clock used to provide timing for the RLD port. RLDCLK is a nominal 576 kHz clock. RSLDCLK is the generated output clock used to provide timing for the RSLD port. If RSLD carries the line DCC, RSLDCLK is a nominal 576 kHz clock or if RSLD carries the section DCC, RSLDCLK is a nominal 192 kHz clock. Sampling RTOHFP high identifies the MSB of the first DCC byte on RLD (D4) and RSLD (D1 or D4).

A maskable interrupt is activated to indicate any change in the status of out of frame (OOF), loss of frame (LOF), loss of signal (LOS), line remote defect indication (RDI-L), line alarm indication signal (AIS-L), synchronization status message (COSSM), APS bytes (COAPS) and APS byte failure (APSBF) or any errors in section BIP-8, line BIP-8 and line remote error indication (REI-L).

The RRMP block provides de-scrambled data and frame alignment indication signals for use by the RHPP.

10.3 Receive Tail Trace Processor (RTTP)

The Receive Tail Trace Processor (RTTP) block monitors the tail trace messages of the receive data stream for trace identifier unstable (TIU) defect and trace identifier mismatch (TIM) defect. Three tail trace algorithms are defined.

The first algorithm is BELLCORE compliant. The algorithm detects trace identifier mismatch (TIM) defect on a 16 or 64 byte tail trace message. A TIM defect is declared when none of the last 20 messages matches the expected message. A TIM defect is removed when 16 of the last 20 messages match the expected message. The expected tail trace message is a static message written in the expected page of the RTTP by an external microprocessor. Optionally, the expected message is matched when the tail trace message is all zeros.

The second algorithm is ITU compliant. The algorithm detects trace identifier unstable (TIU) defect and trace identifier mismatch (TIM) defect on a 16 or 64 byte tail trace message. The current tail trace message is stored in the captured page of the RTTP. If the length of the message is 16 bytes, the RTTP synchronizes on the MSB of the message. The byte with the MSB set high is placed in the first location of the captured page. If the length of the message is 64 bytes, the RTTP synchronizes on the CR/LF (CR = 0Dh, LF = 0Ah) characters of the message. The following byte is placed in the first location of the captured page.

A persistent tail trace message is declared when an identical message is receive for 3 or 5 consecutive multi-frames (16 or 64 frames). A persistent message becomes the accepted message. The accepted message is stored in the accepted page of the RTTP. A TIU defect is declared when one or more erroneous bytes are detected in a total of 8 messages without any persistent message in between. A TIU defect is removed when a persistent message is received.

A TIM defect is declared when the accepted message does not match the expected message. A TIM defect is removed when the accepted message matches the expected message. The expected message is a static message written in the expected page of the RTTP by an external microprocessor. Optionally, the algorithm declares a match tail trace message when the accepted message is all zeros.

The third algorithm is not BELLCORE/ITU compliant. The algorithm detects trace identifier unstable (TIU) on a single continuous tail trace byte. A TIU defect is declared when one or more erroneous bytes are detected in three consecutive 16 byte windows. The first window starts on the first erroneous byte. A TIU defect is removed when an identical byte is received for 48 consecutive frames. A maskable interrupt is activated to indicate any change in the status of trace identifier unstable (TIU) and trace identifier mismatch (TIM).

10.4 Receive High Order Path Processor (RHPP)

The Receive High Order Path Processor (RHPP) provides pointer interpretation, extraction of path overhead, extraction of the synchronous payload envelope (virtual container), and path level alarm and performance monitoring.

10.4.1 Pointer Interpreter

The pointer interpreter extracts and validates the H1 and H2 bytes in order to identify the location of the path overhead byte (J1) and all the synchronous payload envelop bytes (SPE) of the constituent STS-1/3c/12c/48c (VC3/4/4-4c/4-16c) payloads. The pointer interpreter is a time multiplexed finite state machine that can process any mixed of STS-1/3c/12c/48c (AU3/4/4-4c/4-16c) pointers. Within the pointer interpretation algorithm three states are defined as shown below

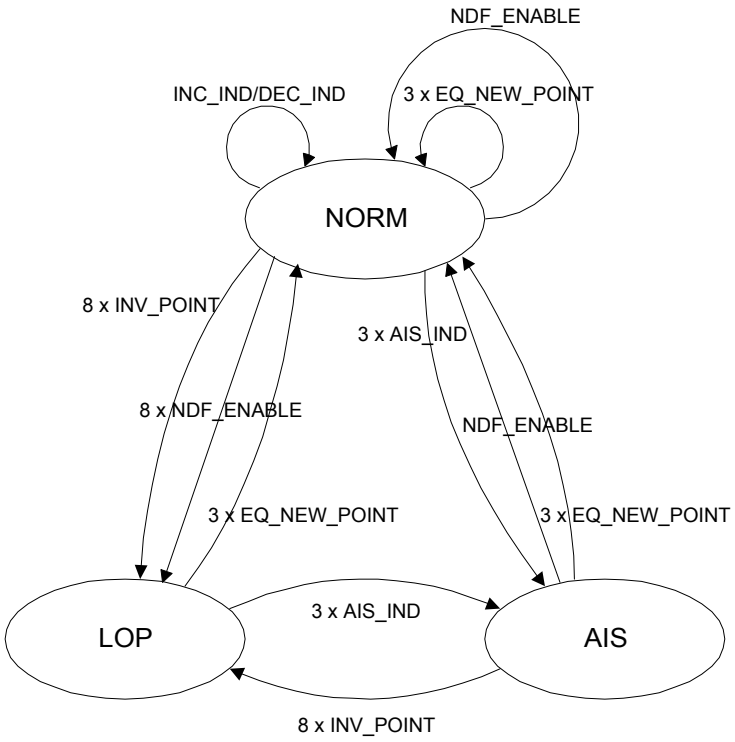
NORM_state (NORM)

AIS_state (AIS)

LOP_state (LOP)

The transition between states will be consecutive events (indications), e.g., three consecutive AIS indications to go from the NORM_state to the AIS_state. The kind and number of consecutive indications activating a transition is chosen such that the behavior is stable and insensitive to low BER. The only transition on a single event is the one from the AIS_state to the NORM_state after receiving a NDF enabled with a valid pointer value. It should be noted that, since the algorithm only contains transitions based on consecutive indications, this implies that, for example, non-consecutively received invalid indications do not activate the transitions to the LOP_state.

Figure 5 Pointer interpretation state diagram



The following events (indications) are defined

NORM_POINT: disabled NDF + ss + offset value equal to active offset.

NDF_ENABLE: enabled NDF + ss + offset value in range of 0 to 782.

AIS_IND: H1 = FFh + H2 = FFh.

INC_IND: disabled NDF + ss + majority of I bits inverted + no majority of D bits inverted + previous NDF_ENABLE, INC_IND or DEC_IND more than 3 frames ago.

DEC_IND: disabled NDF + ss + majority of D bits inverted + no majority of I bits inverted + previous NDF_ENABLE, INC_IND or DEC_IND more than 3 frames ago.

INV_POINT: not any of the above (i.e.: not NORM_POINT, not NDF_ENABLE, not AIS_IND, not INC_IND and not DEC_IND).

NEW_POINT: disabled NDF + ss + offset value in range of 0 to 782 but not equal to active offset.

Note 1: active offset is defined as the accepted current phase of the SPE (VC) in the NORM_state and is undefined in the other states.

Note 2: enabled NDF is defined as the following bit patterns: 1001, 0001, 1101, 1011 and 1000.

Note 3: disabled NDF is defined as the following bit patterns: 0110, 1110, 0010, 0100 and 0111.

Note 4: the remaining six NDF bit patterns (0000, 0011, 0101, 1010, 1100, 1111) result in an INV_POINT indication.

Note 5: ss bits are unspecified in SONET and have bit pattern 10 in SDH.

Note 6: the use of ss bits in definition of indications may be optionally disabled.

Note 7: the requirement for previous NDF_ENABLE, INC_IND or DEC_IND be more than 3 frames ago may be optionally disabled.

Note 8: NEW_POINT is also an INV_POINT.

Note 9: the requirement for the pointer to be within the range of 0 to 782 in 8 X NDF_ENABLE may be optionally disabled.

Note 10: LOP is not declared if all the following conditions exist:
- the received pointer is out of range (>782),
- the received pointer is static,
- the received pointer can be interpreted, according to majority voting on the I and D bits, as a positive or negative justification indication, after making the requested justification, the received pointer continues to be interpretable as a pointer justification.
- When the received pointer returns to an in-range value, the SPECTRA-2488 will interpret it correctly.

The transitions indicated in the state diagram are defined as follows

INC_IND/DEC_IND: offset adjustment (increment or decrement indication)

3 x EQ_NEW_POINT: three consecutive equal NEW_POINT indications

NDF_ENABLE: single NDF_ENABLE indication

3 x AIS_IND: three consecutive AIS indications

8 x INV_POINT: eight consecutive INV_POINT indications

8 x NDF_ENABLE: eight consecutive NDF_ENABLE indications

Note 1: the transitions from NORM_state to NORM_state do not represent state changes but imply offset changes.

Note 2: 3 x EQ_NEW_POINT takes precedence over other events and may optionally reset the INV_POINT count.

Note 3: all three offset values received in 3 x EQ_NEW_POINT must be identical.

Note 4: "consecutive event counters" are reset to zero on a change of state (except the INV_POINT counter).

LOP is declared on entry to the LOP_state after eight consecutive invalid pointers or eight consecutive NDF enabled indications. Path AIS is optionally inserted in the DROP bus when LOP is declared. The alarm condition is reported in the ring control port and is optionally returned to the source node by signaling the corresponding Transmit High Order Path Processor in the local SPECTRA-2488 to insert a path RDI indication. Alternatively, if in-band error reporting is enabled, the path RDI bit in DROP bus G1 byte is set to indicate the LOP alarm to the THPP in a remote SPECTRA-2488.

PAIS is declared on entry to the AIS_state after three consecutive AIS indications. Path AIS is inserted in the DROP bus when AIS is declared. The alarm condition reported in the ring control port and is optionally returned to the source node by signaling the corresponding Transmit High Order Path Processor in the local SPECTRA-2488 to insert a path RDI indication. Alternatively, if in-band error reporting is enabled, the path RDI bit in DROP bus G1 byte is set to indicate the PAIS alarm to the THPP in a remote SPECTRA-2488.

10.4.2 Concatenation Pointer Interpreter State Machine

The concatenation pointer interpreter extracts and validates the H1 and H2 concatenation bytes. The concatenation pointer interpreter is a time multiplexed finite state machine that can process any mixed of STS-1/3c/12c/48c (AU3/4/4-4c/4-16c) pointers. Within the pointer interpretation algorithm three states are defined as shown below.

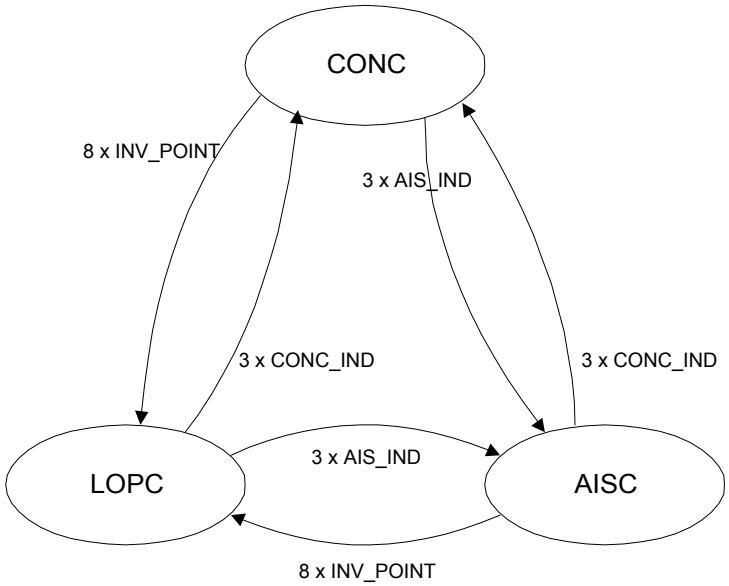
CONC_state (CONC)

AISC_state (AISC)

LOPC_state (LOPC)

The transitions between the states will be consecutive events (indications), e.g. three consecutive AIS indications to go from the CONC_state to the AISC_state. The kind and number of consecutive indications activating a transition is chosen such that the behavior is stable and insensitive to low BER.

Figure 6 Concatenation Pointer Interpretation State Diagram



The following events (indications) are defined

CONC_IND: enabled NDF + dd + "1111111111"

AIS_IND: H1 = FFh + H2 = FFh

INV_POINT: not any of the above (i.e.: not CONC_IND and not AIS_IND)

Note 1: enabled NDF is defined as the following bit patterns: 1001, 0001, 1101, 1011 and 1000.

Note 2: the remaining eleven NDF bit patterns (0000, 0010, 0011, 0100, 0101, 0110, 0111, 1010, 1100, 1110, 1111) result in an INV_POINT indication.

Note 3: dd bits are unspecified in SONET/SDH.

The transitions indicated in the state diagram are defined as follows

3 X CONC_IND: three consecutive CONC indications

3 x AIS_IND: three consecutive AIS indications

8 x INV_POINT: eight consecutive INV_POINT indications

Note 1: "consecutive event counters" are reset to zero on a change of state.

LOPC is declared on entry to the LOPC_state after eight consecutive pointers with values other than concatenation indications. Path AIS is optionally inserted in the DROP bus when LOPC is declared. The alarm condition is reported in the ring control port and is optionally returned to the source node by signaling the corresponding Transmit High Order Path Processor in the local SPECTRA-2488 to insert a path RDI indication. Alternatively, if in-band error reporting is enabled, the path RDI bit in DROP bus G1 byte is set to indicate the LOP alarm to the THPP in a remote SPECTRA-2488.

PAISC is declared on entry to the AISC_state after three consecutive AIS indications. Path AIS is optionally inserted in the DROP bus when AISC is declared. The alarm condition reported in the ring control port and is optionally returned to the source node by signaling the corresponding Transmit High Order Path Processor in the local SPECTRA-2488 to insert a path RDI indication. Alternatively, if in-band error reporting is enabled, the path RDI bit in DROP bus G1 byte is set to indicate the PAIS alarm to the THPP in a remote SPECTRA-2488.

10.4.3 Error Monitoring

The RHPP calculates the path BIP-8 error detection codes on the STS-1/3c/12c/48c (VC-3/4/4-4c/4-16c) payloads. When processing a VC-3 payload, the two fixed stuff columns can be excluded of the BIP-8 calculation if the FSBIPDIS register bit is set. The path BIP-8 code is based on a bit interleaved parity calculation using even parity. The calculated BIP-8 codes are compared with the BIP-8 codes extracted from the B3 byte of each constituent STS (VC) payload of the following frame. Any differences indicate a path BIP-8 error. The RHPP accumulates path BIP-8 errors in a microprocessor readable 16 bits saturating counter (up to 1 second accumulation time). Optionally, block BIP-8 errors can be accumulated.

The RHPP extracts the path remote error indication (REI-P) errors from bits 1, 2, 3 and 4 of the path status byte (G1) and accumulates them in a microprocessor readable 16 bits saturating counter (up to 1 second accumulation time). Optionally, block block REI errors can be accumulated.

The RHPP monitors the path signal label byte (C2) payload to validate change in the accepted path signal label (APSL). The same PSL byte must be received for three or five consecutive frames (selectable by the PSL5 bit in the configuration register) before being considered accepted.

The RHPP also monitors the path signal label byte (C2) to detect path payload label unstable (PLU-P) defect. A PSL unstable counter is increment every time the received PSL differs from the previously received PSL (an erroneous PSL will cause the counter to be increment twice, once when the erroneous PSL is received and once when the error free PSL is received). The PSL unstable counter is reset when the same PSL value is received for three or five consecutive frames (selectable by the PSL5 bit in the configuration register). PLU-P is declared when the PSL unstable counter reaches five. PLU-P is removed when the PSL unstable counter is reset.

The RHPP also monitors the path signal label byte (C2) to detect path payload label mismatch (PLM-P) defect. PLM-P is declared when the accepted PSL does not match the expected PSL according to Table 3. PLM-P is removed when the accepted PSL match the expected PSL according to Table 3. The accepted PSL is the same PSL value received for three or five consecutive frames (selectable by the PSL5 bit in the configuration register). The expected PSL is a programmable PSL value.

The RHPP also monitors the path signal label byte (C2) to detect path unequipped (UNEQ-P) defect. UNEQ-P is declared when the accepted PSL is 00H and the expected PSL is not 00H. UNEQ-P is removed when the accepted PSL is not 00H or when the accepted PSL is 00H and the expected PSL is 00H. The accepted PSL is the same PSL value received for three or five consecutive frames (selectable by the PSL5 bit in the configuration register). The expected PSL is a register programmable PSL value.

The RHPP also monitors the path signal label byte (C2) to detect path payload defect indication (PDI-P) defect. PDI-P is declared when the accepted PSL is a PDI defect that matches the expected PDI defect. PPDI is removed when the accepted PSL is not a PDI defect or when the accepted PSL is a PDI defect that does not match the expected PDI defect. The accepted PSL is the same PSL value received for three or five consecutive frames (selectable by the PSL5 bit in the configuration register). Table 4 gives the expected PDI defect based on the programmable PDI and PDI range register values.

Table 3 PLM-P, UNEQ-P and PDI-P Defects Declaration

Expected PSL		Accepted PSL			PLM-P	UNEQ-P	PDI-P
00	Unequipped	00	Unequipped		Match	Inactive	Inactive
		01	Equipped non specific		Mismatch	Inactive	Inactive
		02-E0 FD-FF	Equipped specific		Mismatch	Inactive	Inactive
		E1-FC	PDI	$=_{exp}$PDI	Mismatch	Inactive	Active
				$!=_{exp}$PDI	Mismatch	Inactive	Inactive
01	Equipped non specific	00	Unequipped		Mismatch	Active	Inactive
		01	Equipped non specific		Match	Inactive	Inactive
		02-E0 FD-FF	Equipped specific		Match	Inactive	Inactive
		E1-FC	PDI	$=_{exp}$PDI	Match	Inactive	Active
				$!=_{exp}$PDI	Mismatch	Inactive	Inactive
02-FF	Equipped specific PDI	00	Unequipped		Mismatch	Active	Inactive
		01	Equipped non specific		Match	Inactive	Inactive
		02-E0 FD-FF	Equipped specific	$=_{exp}$PSL	Match	Inactive	Inactive
				$!=_{exp}$PSL	Mismatch	Inactive	Inactive
		E1-FC	PDI	$=_{exp}$PDI	Match	Inactive	Active
				$!=_{exp}$PDI	Mismatch	Inactive	Inactive

Table 4 Expected PDI Defect Based On PDI and PDI Range Values

PDI Register Value	PDI Range Register Value	Exp PDI	PDI Register Value	PDI Range Register Value	Exp PDI
00000	Disable	None	01111	Disable	EF
	Enable			Enable	E1-EF
00001	Disable	E1	10000	Disable	F0
	Enable	E1-E1		Enable	E1-F0
00010	Disable	E2	10001	Disable	F1
	Enable	E1-E2		Enable	E1-F1
00011	Disable	E3	10010	Disable	F2
	Enable	E1-E3		Enable	E1-F2
00100	Disable	E4	10011	Disable	F3
	Enable	E1-E4		Enable	E1-F3
00101	Disable	E5	10100	Disable	F4
	Enable	E1-E5		Enable	E1-F4
00110	Disable	E6	10101	Disable	F5
	Enable	E1-E6		Enable	E1-F5
00111	Disable	E7	10110	Disable	F6
	Enable	E1-E7		Enable	E1-F6
01000	Disable	E8	10111	Disable	F7
	Enable	E1-E8		Enable	E1-F7
01001	Disable	E9	11000	Disable	F8
	Enable	E1-E9		Enable	E1-F8
01010	Disable	EA	11001	Disable	F9
	Enable	E1-EA		Enable	E1-F9
01011	Disable	EB	11010	Disable	FA
	Enable	E1-EB		Enable	E1-FA
01100	Disable	EC	11011	Disable	FB
	Enable	E1-EC		Enable	E1-FB
01101	Disable	ED	11100	Disable	FC
	Enable	E1-ED		Enable	E1-FC
01110	Disable	EE			
	Enable	E1-EE			

The RHPP monitors bits 5, 6 and 7 of the path status byte (G1) to detect to detect path remote defect indication (RDI-P) and path enhanced remote defect indication (ERDI-P) defects.

RDI-P is declared when bit 5 of the G1 byte is set high for five or ten consecutive frames (selectable by the PRDI10 bit in the configuration register). RDI-P is removed when bit 5 of the G1 byte is set low for five or ten consecutive frames. ERDI-P is declared when the same 010, 100, 101, 110 or 111 pattern is detected in bits 5, 6 and 7 of the G1 byte for five or ten consecutive frames (selectable by the PRDI10 bit in the configuration register). ERDI-P is removed when the same 000, 001 or 011 pattern is detected in bits 5, 6 and 7 of the G1 byte for five or ten consecutive frames.

The RHPP extracts and serially outputs all the path overhead (POH) bytes on the time multiplexed RPOH port. The POH bytes are output in the same order that they are received (J1, B3, C2, G1, F2, H4, Z3, Z4 and N1). RPOHCLK is the generated output clock used to provide timing for the RPOH port. RPOHCLK is a nominal 20.736 MHz clock generated by gapping a 25.92 MHz clock. Sampling RPOHFP high with the rising edge of RPOHCLK identifies the MSB of the first J1 byte.

10.5 SONET/SDH Transmit Line Interface (STLI)

The SONET/SDH transmit line interface block properly formats the outgoing 2488 Mbit/s data stream.

In single STS-48/STM-16 mode, the STLI supports a 16 bit 155.52 MHz differential PECL line side interface for direct connection to external clock recovery, clock synthesis and serializer-deserializer components. In quad STS-12/STM-4 mode, the STLI supports four independent 8 bit 77.76 MHz TTL compatible line side interface for direct connection to external clock recovery, clock synthesis and serializer-deserializer components.

10.6 Transmit Regenerator Multiplexer Processor (TRMP)

The Transmit Regenerator and Multiplexer Processor (TRMP) block inserts the transport overhead bytes in the transmit data stream.

The TRMP accumulates the line BIP-8 errors detected by the RRMP during the last receive frame. The line BIP-8 errors are returned to the far end as line remote error indication (REI-L) during the next transmit frame. Because the RRMP and the TRMP are in two different clock domains, none, one or two line BIP-8 errors can be accumulated per transmit frame. The minimum value between the maximum REI-L given in Table 5 and the accumulator count is returned as the line REI-L in the M1 byte of STS-1 (STM-0) #3. Optionally, block BIP-24 errors can be accumulated.

Table 5 Maximum Line REI Errors Per Transmit Frame

SONET/SDH	Maximum Single BIP-8 Errors LREIBLK=0	Maximum Block BIP-24 Errors LREIBLK=1
STS-3/STM-1	0001 1000	0000 0001
STS-12/STM-4	0110 0000	0000 0100
STS-48/STM-16	1111 1111	0001 0000
STS-192/STM-64	1111 1111	0100 0000

The TRMP serially inputs all the transport overhead (TOH) bytes from the TTOH port. The TOH bytes must be input in the same order that they are transmitted (A1, A2, J0/Z0, B1, E1, F1, D1-D3, H1-H3, B2, K1, K2, D4-D12, S1/Z1, Z2/M1/Z2 and E2). TTOHCLK is the generated output clock used to provide timing for the TTOH port. TTOHCLK is a nominal 20.736 MHz clock generated by gapping a 25.92 MHz clock. Sampling TTOHFP high with the rising edge of TTOHCLK identifies the MSB of the first A1 byte. TTOHEN port is used to validate the byte insertion on a byte per byte basis. When TTOHEN is sampled high on the MSB of the serial byte, the serial byte is inserted. When TTOHEN is sampled low on the MSB of the serial byte, the serial byte is discarded.

Figure 7 STS-12 (STM-4) on TTOH 1-4or STS-48 (STM-16) on TTOH1

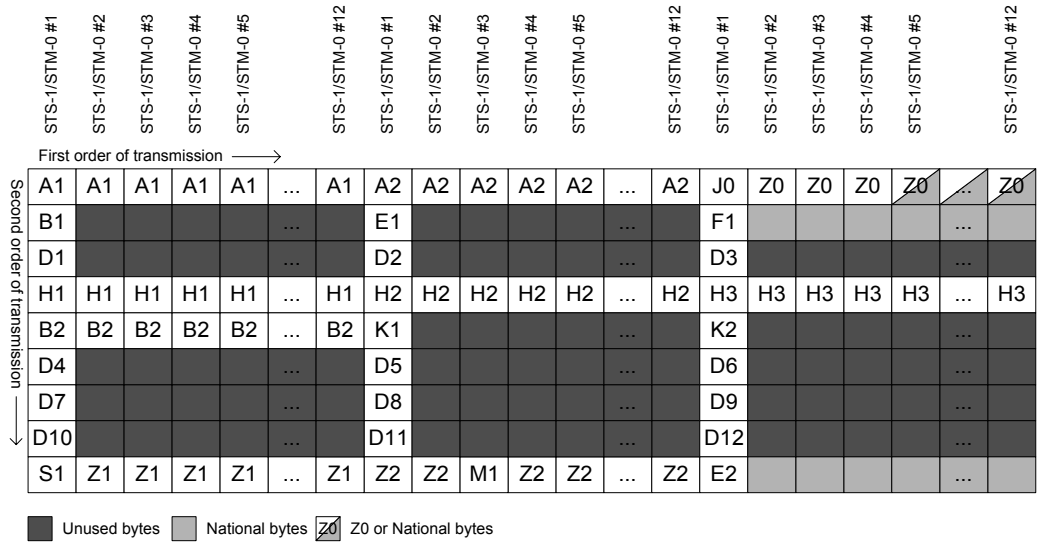
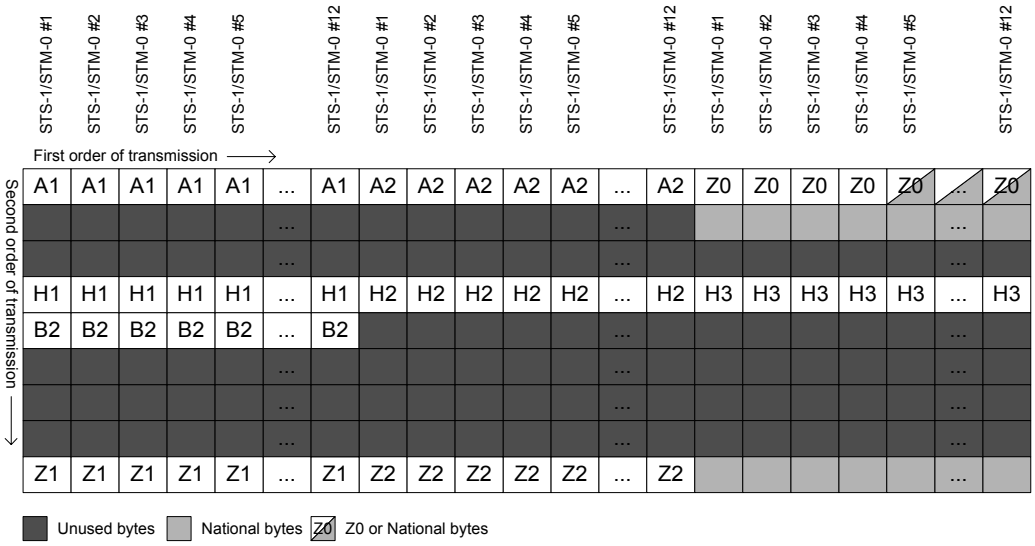


Figure 8 STS-48 (STM-16) on TTOH2-4



The TRMP serially inputs the line DCC bytes from the TLD and the TSLD ports. The line DCC bytes (D4-D12) are input from TLD. TSLD is selectable to input either the section DCC bytes (D4-D12) or the line DCC bytes (D1-D3). TLDCLK is the generated output clock used to provide timing for the TLD port. TLDCLK is a nominal 576 kHz clock. TSLDCLK is the generated output clock used to provide timing for the TSLD port. If TSLD carries the line DCC, TSLDCLK is a nominal 576 kHz clock or if TSLD carries the section DCC, TSLDCLK is a nominal 192 kHz clock. Sampling TTOHFP high identifies the MSB of the first DCC byte on TLD (D4) and TSLD (D1 or D4).

The TRMP also inserts most of the transport overhead bytes from internal registers. Since there is multiple sources for the same overhead byte, the TOH bytes must be prioritized according to Table 6 before being inserted into the data stream.

Table 6 TOH Insertion Priority

BYTE	HIGHEST priority						LOWEST priority
A1		76h (A1ERR=1)	F6h (A1A2EN=1)	TTOH (TTOHEN=1)			A1 pass through
A2			28h (A1A2EN=1)	TTOH (TTOHEN=1)			A2 pass through
J0	STS-1/STM-0 # (J0Z0INCEN=1)	J0[7:0] (TRACEEN=1)	J0V (J0REGEN=1)	TTOH (TTOHEN=1)			J0 pass through
Z0	STS-1/STM-0 # (J0Z0INCEN=1)		Z0V (Z0REGEN=1)	TTOH (TTOHEN=1)			Z0 pass through
B1				Calculated B1 xor TTOH (TTOHEN=1 & B1MASKEN=1)			Calculated B1 xor B1MASK
				TTOH (TTOHEN=1 & B1MASKEN=0)			

BYTE	HIGHEST priority						LOWEST priority
E1			E1V (E1REGEN=1)	TTOH (TTOHEN=1)			E1 pass through
F1			F1V (F1REGEN=1)	TTOH (TTOHEN=1)			F1 pass through
D1-D3			D1D3V (D1D3REGEN=1)	TTOH (TTOHEN=1)	TSLD (TSLDSEL=0 & TSLDEN=1)		D1-D3 pass through
H1				H1 pass through xor TTOH (TTOHEN=1 & HMASKEN=1)			H1 pass through xor H1MASK
				TTOH (TTOHEN=1 & HMASKEN=0)			
H2				H2 pass through xor TTOH (TTOHEN=1 & HMASKEN=1)			H2 pass through xor H2MASK
				TTOH (TTOHEN=1 & HMASKEN=0)			
H3				TTOH (TTOHEN=1)			H3 pass through
B2				Calculated B2 xor TTOH (TTOHEN=1 & B2MASKEN=1)			Calculated B2 xor B2MASK
				TTOH (TTOHEN=1 & B2MASKEN=0)			
K1		APS[15:8] (APSEN=1)	K1V (K1K2REGEN=1)	TTOH (TTOHEN=1)			K1 pass through
K2		APS[7:0] (APSEN=1)	K2V (K1K2REGEN=1)	TTOH (TTOHEN=1)			K2 pass through
D4-D12			D4D12V (D4D12REGEN=1)	TTOH (TTOHEN=1)	TSLD (TSLDSEL=1 & TSLDEN=1)	TLD (TLDEN=1)	D4-D12 pass through
S1			S1V (S1REGEN=1)	TTOH (TTOHEN=1)			S1 pass through
Z1			Z1V (Z1REGEN=1)	TTOH (TTOHEN=1)			Z1 pass through
Z2			Z2V (Z2REGEN=1)	TTOH (TTOHEN=1)			Z2 pass through
M1			LREI[7:0] (LREIEN=1)	TTOH (TTOHEN=1)			M1 pass through
E2			E2V (E2REGEN=1)	TTOH (TTOHEN=1)			E2 pass through
National			NATIONALV (NATIONALEN=1)	TTOH (TTOHEN=1)			National pass through
Unused			UNUSEDV (UNUSEDEN=1)	TTOH (TTOHEN=1)			Unused pass through
PLD							PLD pass through

The Z0DEF register bit defines the Z0/NATIONAL growth bytes for row #1. When Z0DEF is set to logic one, the Z0/NATIONAL bytes are defined according to ITU. When Z0DEF is set to logic zero, the Z0/NATIONAL bytes are defined according to BELLCORE.

Table 7 Z0/National Growth Bytes Definition For Row #1

TRMP Mode	Type	Z0DEF = 1	Z0DEF = 0
STS-3/STM-1	Z0	None	From STS-1/STM-0 #2 to #3
	National	From STS-1/STM-0 #2 to #3	None
STS-12/STM-4 master mode	Z0	From STS-1/STM-0 #2 to #4	From STS-1/STM-0 #2 to #12
	National	From STS-1/STM-0 #5 to #12	None
STS-48/STM-16 slave mode	Z0	From STS-1/STM-0 #1 to #4	From STS-1/STM-0 #1 to #12
	National	From STS-1/STM-0 #5 to #12	None

The H1, H2, B1 and B2 bytes input from the TTOH port are inserted or are used as a mask to toggle bits in the corresponding H1, H2, B1 and B2 bytes depending on the HMASK B1MASK and B2MASK register bits. When the HMASK, B1MASK or B2MASK register bit is set low and TTOHEN is sampled high on the MSB of the serial H1, H2, B1 or B2 byte, the serial byte is inserted in place of the corresponding byte. When the HMASK, B1MASK or B2MASK register bit is set high and TTOHEN is sampled high on the MSB of the serial H1, H2, B1 or B2 byte, the serial byte is XORed with the corresponding path payload pointer (already in the data stream) or the calculated BIP-8 byte before being inserted.

The TRMP inserts the APS bytes detected by the RRMP during the last receive frame. The APS bytes are returned to the far end by the TRMP during the next transmit frame. Because the RRMP and the TRMP are in two different clock domains, none, one or two APS bytes can be sampled per transmit frame. The last received APS bytes are transmitted.

The TRMP inserts the line remote defect indication (RDI-L) into the data stream. When line RDI must be inserted, the 110 pattern is inserted in bits 6, 7 and 8 of the K2 byte of STS-1 (STM-0) #1. Line RDI insertion has priority over TOH byte insertion. The TRMP also inserts the line alarm indication signal (AIS-L) into the data stream. When line AIS must be inserted, all ones are inserted in the line overhead and in the payload (all bytes of the frame except the section overhead bytes). Line AIS insertion has priority over line RDI insertion and TOH byte insertion.

The TRMP calculates the line BIP-8 error detection codes on the transmit data stream. One line BIP-8 error detection code is calculated for each of the constituent STS-1 (STM-0). The line BIP-8 byte is calculated on the unscrambled bytes of the STS-1 (STM-0) except for the 9 SOH bytes. The line BIP-8 byte is based on a bit interleaved parity calculation using even parity. For each STS-1 (STM-0), the calculated BIP-8 error detection code is inserted in the B2 byte of the following frame before scrambling.

The TRMP optionally scrambles the transmit data stream.

The TRMP calculates the section BIP-8 error detection code on the transmit data stream. The section BIP-8 byte is calculated on the scrambled bytes of the complete frame. The section BIP-8 byte is based on a bit interleaved parity calculation using even parity. The calculated BIP-8 error detection code is inserted in the B1 byte of STS-1 (STM-0) #1 of the following frame before scrambling.

10.7 Transmit Tail Trace Processor (TTTP)

The Transmit Tail Trace Processor (TTTP) block generates the tail trace messages to be transmitted. byte. The TTTP can generate a 16 or 64 byte tail trace message. The message is source from an internal RAM and must have been previously written by an external micro processor. Optionally, the tail trace message can be reduced to a single continuous tail trace byte.

The tail trace message must include synchronization because the TTTP does not add synchronization. The synchronization mechanism is different for a 16 bytes message and for a 64 bytes message. When the message is 16 bytes, the synchronization is based on the MSB of the tail trace byte. Only one of the 16 bytes has is MSB set high. The byte with its MSB set high is considered the first byte of the message. When the message is 64 bytes, the synchronization is based on the CR/LF (CR = 0Dh, LF = 0Ah) characters of tail trace message. The byte following the CR/LF bytes is considered the first byte of the message.

To avoid generating an unstable/mismatch message, the TTTP forces the message to all zeros while the microprocessor updates the internal RAM.

10.8 Transmit High Order Path Processor (THPP)

The Transmit High Order Path Processor (THPP) block inserts the path overhead bytes in the transmit data stream.

The THPP accumulates the path BIP-8 errors detected by the RHPP during the last receive frame. The path BIP-8 errors are returned to the far end as path remote error indication (REI-P) during the next transmit frame. Because the RHPP and the THPP are in two different clock domains, none, one or two path BIP-8 errors can be accumulated per transmit frame. The minimum value between the maximum REI-P and the accumulator count is returned as the path REI in the G1 byte. Optionally, block BIP-8 errors can be accumulated.

The THPP serially inputs all the path overhead (POH) bytes from the TPOH port. The POH bytes must be input in the same order that they are transmitted (J1, B3, C2, G1, F2, H4, F3, K3 and N1). TPOHCLK is the generated output clock used to provide timing for the TPOH port. TPOHCLK is a nominal 20.736 MHz clock generated by gapping a 25.92 MHz clock. Sampling TPOHFP high with the rising edge of TPOHCLK identifies the MSB of the first J1 byte. TPOHEN port is used to validate the byte insertion on a byte per byte basis. When TPOHEN is sampled high on the MSB of the serial byte, the serial byte is inserted. When TPOHEN is sampled low on the MSB of the serial byte, the serial byte is discarded.

The THPP calculates the path BIP-8 error detection code on the transmit data stream. The path BIP-8 byte is calculated on all the payload bytes. The path BIP-8 byte is based on a bit interleaved parity calculation using even parity. The calculated BIP-8 error detection code is inserted in the B3 byte of the following frame.

Table 8 POH Insertion Priority

Byte	Highest Priority					Lowest Priority
J1	J1 pass through (TDIS=1 OR PAIS=1)	Path trace buffer (PTBJ1=1)	J1 ind. reg. (SRCJ1=1)		TPOH (TPOHEN=1)	J1 pass through
B3	B3 pass through (TDIS=1 OR PAIS=1)			Calculated B3 XOR TPOH (TPOHEN=1 AND B3MASKEN=1)	TPOH (TPOHEN=1)	Calculated B3 XOR B3MASK
C2	C2 pass through (TDIS=1 OR PAIS=1)	C2 ind. reg. (SRCC2=1)			TPOH (TPOHEN=1)	C2 pass through
G1	G1 pass through (TDIS=1 OR PAIS=1 OR IBER=1)	PRDI[2:0] and PREI[3:0] (ENG1REC=1)	G1 ind. reg. (SRCG1=1)		TPOH (TPOHEN=1)	G1 pass through
F2	F2 pass through (TDIS=1 OR PAIS=1)	F2 ind. reg. (SRCF2=1)			TPOH (TPOHEN=1)	F2 pass through
H4	H4 pass through (TDIS=1 OR PAIS=1)	H4 pass through XOR H4 ind. reg. (SRCH4=1 AND ENH4MASK=1)	H4 ind. reg. (SRCH4=1)	H4 pass through XOR TPOH (TPOHEN=1 AND H4MASK=1)	TPOH (TPOHEN=1)	H4 pass through
Z3	Z3 pass through (TDIS=1 OR PAIS=1)	Z3 ind. reg. (SRCZ3=1)			TPOH (TPOHEN=1)	Z3 pass through
Z4	Z4 pass through (TDIS=1 OR PAIS=1)	Z4 ind. reg. (SRCZ4=1)			TPOH (TPOHEN=1)	Z4 pass through
Z5	Z5 pass through (TDIS=1 OR PAIS=1)	Z5 ind. reg. (SRCZ5=1)			TPOH (TPOHEN=1)	Z5 pass through

10.9 Transmit Add Telecom Bus Pointer Interpreter (TAPI)

The Transmit Add Telecom Bus Pointer Interpreter (TAPI) block takes a SONET/SDH data stream from the ADD TelecomBus bus, interprets the STS-1/3c/12c/48c (AU3/4/4-4c/4-16c) pointers, indicates the J1 byte locations and detects alarm conditions (e.g. PAIS).

The TAPI block allows the SPECTRA-2488 to operate with TelecomBus like back plane systems which do not indicate the J1 byte positions. The TAPI block can be enabled using the TAPIDIS bit in the SPECTRA-2488 0x0002 register. When enabled, the TAPI takes a SONET/SDH data stream from the System Side Interface block, processes the stream and identifies the J1 byte locations.

10.10 SONET/SDH Virtual Container Aligner (SVCA)

The SONET/SDH Virtual Container Aligner (SVCA) block aligns the payload data from an incoming SONET/SDH data stream to a new transport frame reference. The alignment is accomplished by recalculating the STS (AU) payload pointer value based on the offset between the transport overhead of the incoming data stream and that of the outgoing data stream.

Frequency offsets (e.g., due to plesiochronous network boundaries, or the loss of a primary reference timing source) and phase differences (due to normal network operation) between the incoming data stream and the outgoing data stream are accommodated by pointer adjustments in the outgoing data stream.

Elastic Store

The Elastic Store performs rate adaptation between the line side interface and the system side interface. The entire incoming payload, including path overhead bytes, is written into a first-in-first-out (FIFO) buffer at the incoming byte rate. Each FIFO word stores a payload data byte and a one bit tag labeling the J1 byte. Incoming pointer justifications are accommodated by writing into the FIFO during the negative stuff opportunity byte or by not writing during the positive stuff opportunity byte. Data is read out of the FIFO in the Elastic Store block at the outgoing byte rate by the Pointer Generator. Analogously, outgoing pointer justifications are accommodated by reading from the FIFO during the negative stuff opportunity byte or by not reading during the positive stuff opportunity byte.

The FIFO read and write addresses are monitored. Pointer justification requests will be made to the Pointer Generator based on the proximity of the addresses relative to FIFO thresholds. The Pointer Generator schedules a pointer increment event if the FIFO depth is below the lower threshold and a pointer decrement event if the depth is above the upper threshold. FIFO underflow and overflow events are detected and path AIS is optionally inserted in the outgoing data stream for three frames to alert downstream elements of data corruption.

Pointer Generator

The Pointer Generator generates the H1 and H2 bytes in order to identify the location of the path overhead byte (J1) and all the synchronous payload envelop bytes (SPE) of the constituent STS-1/3c/12c/48c (VC3/4/4-4c/4-16c) payloads. The pointer generator is a time multiplexed finite state machine that can process any mixed of STS-1/3c/12c/48c (AU3/4/4-4c/4-16c) pointers. Within the pointer generator algorithm, five states are defined as shown below

NORM_state (NORM)

AIS_state (AIS)

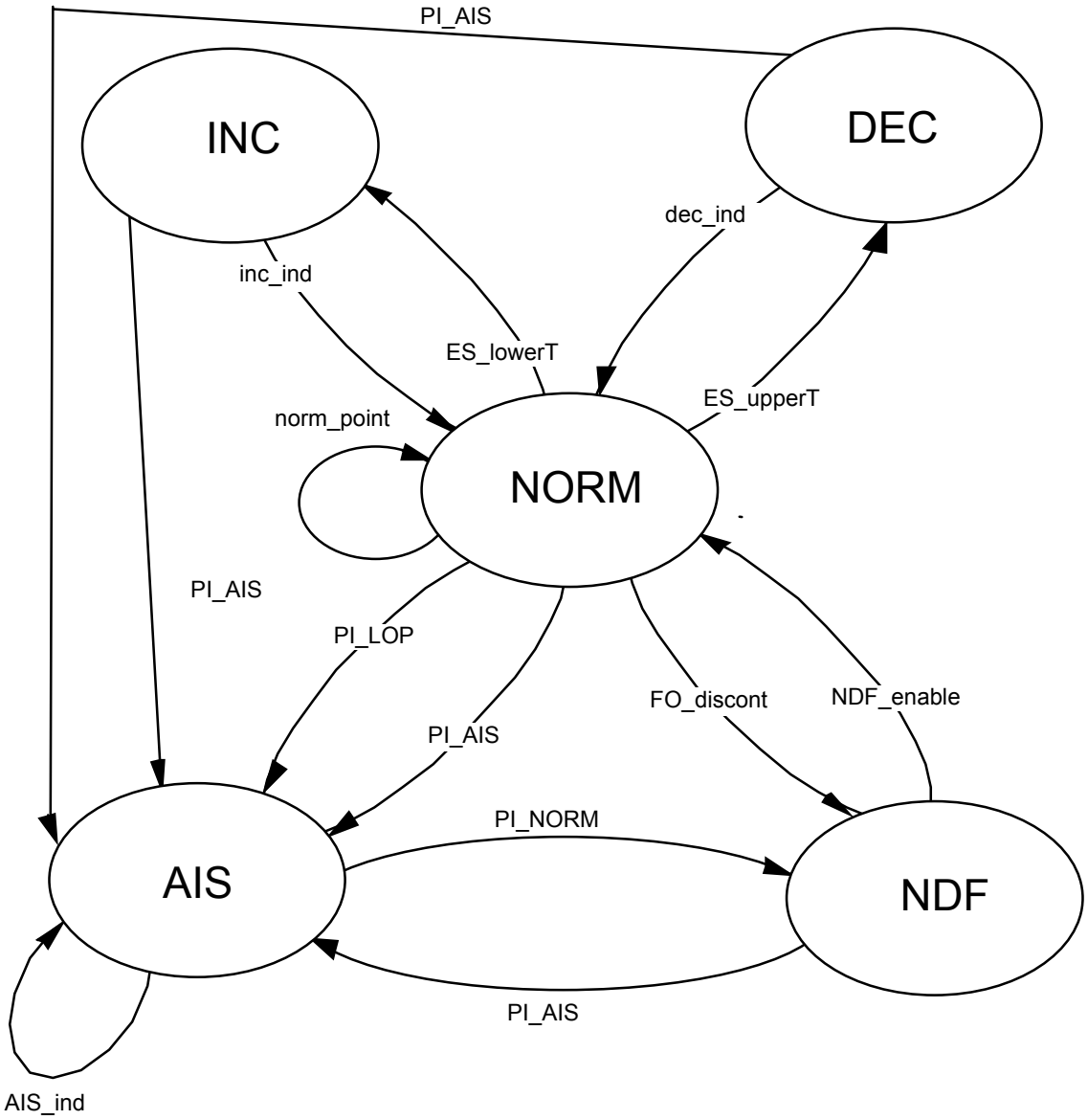
NDF_state (NDF)

INC_state (INC)

DEC_state (DEC)

The transition from the NORM to the INC, DEC, and NDF states are initiated by events in the Elastic Store (ES) block. The transition to/from the AIS state are controlled by the pointer interpreter (PI) in the Receive High Order Path Processor block. The transitions from INC, DEC, and NDF states to the NORM state occur autonomously with the generation of special pointer patterns.

Figure 9 Pointer Generation State Diagram



The following events, indicated in the state diagram, are defined

ES_lowerT: ES filling is below the lower threshold + previous inc_ind, dec_ind or NDF_enable more than three frames ago.

ES_upperT:	ES filling is above the upper threshold + previous inc_ind, dec_ind or NDF_enable more than three frames ago.
FO_discont:	frame offset discontinuity
PI_AIS:	PI in AIS state
PI_LOP:	PI in LOP state
PI_NORM:	PI in NORM state
Note 1	A frame offset discontinuity occurs if an incoming NDF enabled is received, or if an ES overflow/underflow occurred.

The autonomous transitions indicated in the state diagram are defined as follows

inc_ind:	transmit the pointer with NDF disabled and inverted I bits, transmit a stuff byte in the byte after H3, increment active offset.
dec_ind:	transmit the pointer with NDF disabled and inverted D bits, transmit a data byte in the H3 byte, decrement active offset.
NDF_enable:	accept new offset as active offset, transmit the pointer with NDF enabled and new offset.
norm_point:	transmit the pointer with NDF disabled and active offset.
AIS_ind:	active offset is undefined, transmit an all-1's pointer and payload.
Note 1	active offset is defined as the phase of the SPE (VC).
Note 2	the SS bits are undefined in SONET, and has bit pattern 10 in SDH
Note 3	enabled NDF is defined as the bit pattern 1001.
Note 4	disabled NDF is defined as the bit pattern 0110.

10.11 SONET/SDH PRBS Generator and Monitor (PRGM)

The SONET/SDH Pseudo-Random bit sequence Generator and Monitor (PRGM) block generates and monitors an unframed 2^{23}-1 payload test sequence on the TelecomBus ADD or DROP bus.

The PRGM can generate PRBS in an STS-1/3c/12c/48c (AU3/4/4—4c/4-16c) payload. The path overhead column, the fixed stuff columns #2 to #4 in an STS-12c (AU-4-4c) payload, the fixed stuff columns #2 to16 in an STS-48c (AU-4-16c) payload and the fixed stuff column #30 and #59 in an STS-1 (AU3) payload do not contain any PRBS data. The PRGM generator can be configured to preserve payload framing and overwrite the payload bytes or can be configured to autonomously generate payload framing and overwrite the payload bytes.

When processing a concatenated STS-48 (STM-16) payload, the master PRGM co-ordinates the distributed PRBS generation between itself and the slave PRGMs. Each PRGM generates one quarter of the complete PRBS sequence. To ensure that the slave PRGMs are synchronized with the master PRGM, a signature is continuously broadcast by the master PRGM to allow the slave PRGMs to check their relative states. A signature mis-match is flagged as an out-of-synch state by the slave PRGM. A re-synchronization of the PRBS generation must be initiated by the master PRGM (under software control).

The PRBS monitor of the PRGM block monitors the recovered payload data for the presence of an unframed 2^{23}-1 test sequence and accumulates pattern errors detected based on this pseudo-random pattern. The PRGM declares synchronization when a sequence of 32 correct pseudo-random patterns (bytes) are detected consecutively. Pattern errors are only counted when the PRGM is in synchronization with the input sequence. When 16 consecutive pattern errors are detected, the PRGM will fall out of synchronization and will continuously attempt to re-synchronize to the input sequence until it is successful.

When processing a concatenated STS-48 (STM-16) payload, the master PRGM and the slave PRGMs independently monitor one quarter of the complete PRBS sequence. To ensure that the slave PRGMs are synchronized with the master PRGM, the same signature matching will be performed as described for the PRBS generation.

A maskable interrupt is activated to indicate any change in the synchronization status.

10.12 SONET/SDH Time-Slot Interchange (STSI)

The SONET/SDH Time-Slot Interchange (STSI) block grooms the SONET/SDH data stream by performing STS-1 (STM-0) (time-slots) switching and TelecomBus buses (space-slots) switching. The TelecomBus ADD or DROP buses treat an STS-12/12c (STM-4/AU4-4c) data stream as twelve independent time-division multiplexed paths. The twelve time-slots correspond to the twelve constituent STS-1 (STM-0) paths. Table 9 show the relationship between the STS-1 (STM-0) path numbering and the STS-12/12c (STM-4/AU4-4c) data stream. The STS-1 (STM-0) paths are numbered according to the order of transmission (reception) and the STS-12/12c (STM-4/AU4-4c) data stream is numbered according to the STS-1/3c/12c (AU3/AU4/AU4-4c) groups.

Table 9 STS-1 (STM-0) Path Numbering for an STS-12/12c (STM-4/AU4-4c)

STS-1 (STM-0) path # (Tx/Rx Order)	TelecomBus	STS-12/12c (STM-4/AU4-4c)
1	1-4	STS-1 (AU3) #1 or STS-3c (AU4) #1 or STS-12 (AU4-4c) #1
2	1-4	STS-1 (AU3) #2 or STS-3c (AU4) #2 or STS-12 (AU4-4c) #1
3	1-4	STS-1 (AU3) #3 or STS-3c (AU4) #3 or STS-12 (AU4-4c) #1
4	1-4	STS-1 (AU3) #4 or STS-3c (AU4) #4 or STS-12 (AU4-4c) #1
5	1-4	STS-1 (AU3) #5 or STS-3c (AU4) #1 or STS-12 (AU4-4c) #1
6	1-4	STS-1 (AU3) #6 or STS-3c (AU4) #2 or STS-12 (AU4-4c) #1
7	1-4	STS-1 (AU3) #7 or STS-3c (AU4) #3 or STS-12 (AU4-4c) #1
8	1-4	STS-1 (AU3) #8 or STS-3c (AU4) #4 or STS-12 (AU4-4c) #1

STS-1 (STM-0) path # (Tx/Rx Order)	TelecomBus	STS-12/12c (STM-4/AU4-4c)
9	1-4	STS-1 (AU3) #9 or STS-3c (AU4) #1 or STS-12 (AU4-4c) #1
10	1-4	STS-1 (AU3) #10 or STS-3c (AU4) #2 or STS-12 (AU4-4c) #1
11	1-4	STS-1 (AU3) #11 or STS-3c (AU4) #3 or STS-12 (AU4-4c) #1
12	1-4	STS-1 (AU3) #12 or STS-3c (AU4) #4 or STS-12 (AU4-4c) #1

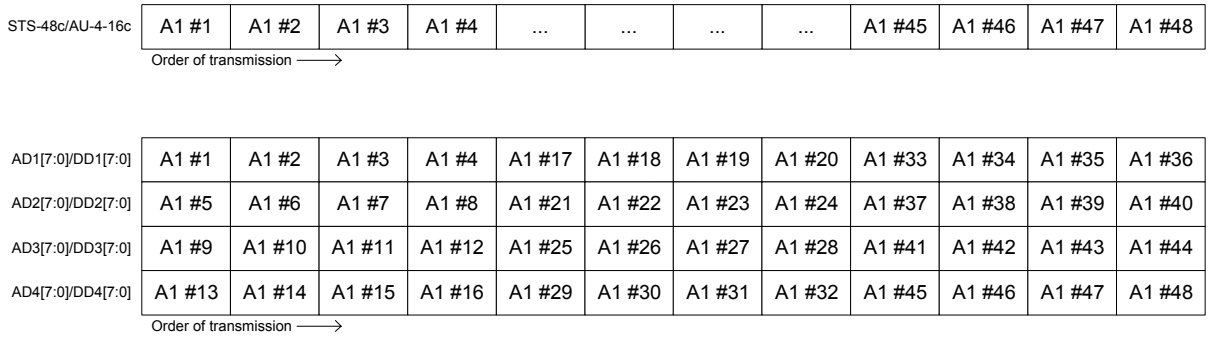
Switching of STS-1 (STM-0) (time-slots) and TelecomBus buses (space-slots) is arbitrary, thus any STS-1 (STM-0) can be switched to any of the time-slots and any TelecomBus buses can be switched to any of the space-slots. Concatenated streams such as STS-3c/12c (AU4/AU4-4c) should be switched as a group to keep the constituent STS-1 (STM-0) streams in the correct transmit or receive order within the group.

10.13 System Side Interfaces

In single STS-48/STM-16 mode, the line side interface supports a 77.76 MHz 32 bit TelecomBus interface.

For an STS-48 (STM-16) receive stream, the four constituent STS-12/STM-4 #1 - #4 are provided at the DD1[7:0], DD2[7:0], DD3[7:0] and DD4[7:0] TelecomBus DROP busses, respectively. For an STS-48c (AU4-4c) receive stream, the concatenated STS-48 (STM-16) is provided, 4 byte interleaved, at the DD1[7:0], DD2[7:0], DD3[7:0] and DD4[7:0] TelecomBus DROP busses. For an STS-48 (STM-16) transmit stream, the four constituent STS-12/STM-4 #1 - #4 are accepted at the AD1[7:0], AD2[7:0], AD3[7:0] and AD4[7:0] TelecomBus ADD busses, respectively. For an STS-48c (AU4-16c) transmit stream, the concatenated STS-48 (STM-16) is accepted, 4 byte interleaved, at the AD1[7:0], AD2[7:0], AD3[7:0] and AD4[7:0] TelecomBus ADD busses. Figure 10 shows the 4 byte interleaving for an STS-48c (AU4-16c).

Figure 10 STS-48C (AU4-16c) Four Byte Interleaving on the 32 bit TelecomBus



In quad STS-12/STM-4 mode, the line side interface supports four independent 77.76 MHz 8 bit TelecomBus interfaces. The four TelecomBus interfaces run on the same system clock.

For an STS-12/12c (STM-4/AU4-4c) receive stream, the four independent STS-12/12c (STM-4/AU4-4c) #1 - #4 are provided at the DD1[7:0], DD2[7:0], DD3[7:0] and DD4[7:0] TelecomBus DROP busses, respectively. For an STS-12/12c (STM-4/AU4-4c) transmit stream, the four independent STS-12/12c (STM-4/AU4-4c) #1 - #4 are accepted at the AD1[7:0], AD2[7:0], AD3[7:0] and AD4[7:0] TelecomBus ADD busses, respectively.

In both modes, the transport frame of the four TelecomBus DROP buses must be aligned with the DFP frame pulse. Only one DFP input is provided for the four TelecomBus DROP buses even in quad STS-12/STM-4 mode. In both modes, the transport frame of the four TelecomBus ADD buses must be aligned (coincident J0/AFP pulses on the associated AJ0J11-4/AFP1-4 signals). The payload data provided on the four TelecomBus ADD buses experience identical delays and the byte sequencing integrity is thus preserved.

The TelecomBus is very flexible and can support a wide range of system backplane architectures. Table 10 shows the system side ADD bus options

Table 10 System Side ADD Bus Configuration Options

AFPEN Bit	TAPIDIS Bit	APL1-4 Input Pin	AJ0J11-4/ AFP1-4 Input Pin	Comments
0	1	APL marks payload bytes	AJ0J1 marks J0 and J1 positions	TAPI block is bypassed. Ignores V1 indications
0	0	Tied to ground	AJ0J1 marks J0 position only	TAPI block interprets pointers for J1.
0	0	APL marks payload bytes	AJ0J1 marks J0 position only	TAPI block interprets pointers for J1.
0	0	APL marks payload bytes	AJ0J1 marks J0 and J1positions	TAPI block interprets pointers for J1. Ignores J1 and V1 indications on AJ0J1
1	1	-	-	Not Valid
1	0	Tied to ground	AFP marks first SPE byte position only	TAPI block interprets pointers for J1

10.14 JTAG Test Access Port Interface

The JTAG Test Access Port block provides JTAG support for boundary scan. The standard JTAG EXTEST, SAMPLE, BYPASS, IDCODE and STCTEST instructions are supported. The SPECTRA-2488 identification code is 053150CD hexadecimal.

10.15 Microprocessor Interface

The Microprocessor Interface Block provides the logic required to interface the generic microprocessor bus with the normal mode and test mode registers within the SPECTRA-2488. The normal mode registers are used during normal operation to configure and monitor the SPECTRA-2488. The test mode registers are used to enhance the testability of the SPECTRA-2488. The register set is accessed as shown in the Table 11. In the following section every register is documented and identified using the register numbers in Table 11. The corresponding memory map address is identified by the address column of the table. Addresses that are not shown are not used and must be treated as Reserved.

Table 11 Register Memory Map

REG #	A[12] RX/TX	A[11:10] QUAD	A[9:0]	Register Description
0000H	0	00	000H	SP2488 Master Configuration
0001H	0	00	001H	SP2488 Receive Configuration
0002H	0	00	002H	SP2488 Transmit Configuration
0003H	0	00	003H	SP2488 Loop Timing Configuration
0004H	0	00	004H	SP2488 Reserved
0005H	0	00	005H	SP2488 Reserved
0006H	0	00	006H	SP2488 Reserved
0007H	0	00	007H	SP2488 Reserved
0008H	0	00	008H	SP2488 System Side Line Loop Back #1
0009H	0	00	009H	SP2488 System Side Line Loop Back #2
000AH	0	00	00AH	SP2488 System Side Line Loop Back #3
000BH	0	00	00BH	SP2488 System Side Line Loop Back #4
000CH	0	00	00CH	SP2488 Line Side Loop Back
000DH	0	00	00DH	SP2488 Reserved
000EH	0	00	00EH	SP2488 Line Activity Monitor
000FH	0	00	00FH	SP2488 Unused
0010H	0	00	010H	SP2488 Interrupt Status #1
0011H	0	00	011H	SP2488 Interrupt Status #2
0012H	0	00	012H	SP2488 Interrupt Status #3
0013H	0	00	013H	SP2488 Interrupt Status #4
0014H	0	00	014H	SP2488 Drop System Configuration
0015H	0	00	015H	SP2488 Reserved
0016H	0	00	016H	SP2488 Add System Configuration
0017H	0	00	017H	SP2488 Add Parity Interrupt Status
0018H	0	00	018H	SP2488 System Activity Monitor
0019H	0	00	019H	SP2488 TAPI Path AIS Configuration
001AH	0	00	01AH	SP2488 JTAG ID (MSB)
001BH	0	00	01BH	SP2488 JTAG ID (LSB)

REG #	A[12] RX/TX	A[11:10] QUAD	A[9:0]	Register Description
001CH	0	00	001CH	SP2488 Unused
001DH	0	00	001DH	SP2488 Misc Config
001EH	0	00	01EH	SP2488 Reserved
001FH	0	00	01FH	SP2488 FREE Registers
0020-003FH	0	XX	020-03FH	SP2488 RX Slice Reserved
0040H	0	00	040H	SRLI Clock Configuration
0041H	0	00	041H	SRLI PGM Clock Configuration
0042-005FH	0	00	042-05FH	SRLI Reserved
0060H	0	XX	060H	SBER Configuration
0061H	0	XX	061H	SBER Status
0062H	0	XX	062H	SBER Interrupt Enable
0063H	0	XX	063H	SBER Interrupt Status
0064H	0	XX	064H	SBER SF BERM Accumulation Period (LSB)
0065H	0	XX	065H	SBER SF BERM Accumulation Period (MSB)
0066H	0	XX	066H	SBER SF BERM Saturation Threshold (LSB)
0067H	0	XX	067H	SBER SF BERM Saturation Threshold (MSB)
0068H	0	XX	068H	SBER SF BERM Declaring Threshold (LSB)
0069H	0	XX	069H	SBER SF BERM Declaring Threshold (MSB)
006AH	0	XX	06AH	SBER SF BERM Clearing Threshold (LSB)
006BH	0	XX	06BH	SBER SF BERM Clearing Threshold (MSB)
006CH	0	XX	06CH	SBER SD BERM Accumulation Period (LSB)
006DH	0	XX	06DH	SBER SD BERM Accumulation Period (MSB)
006EH	0	XX	06EH	SBER SD BERM Saturation Threshold (LSB)
006FH	0	XX	06FH	SBER SD BERM Saturation Threshold (MSB)
0070H	0	XX	070H	SBER SD BERM Declaring Threshold (LSB)
0071H	0	XX	071H	SBER SD BERM Declaring Threshold (MSB)
0072H	0	XX	072H	SBER SD BERM Clearing Threshold (LSB)
0073H	0	XX	073H	SBER SD BERM Clearing Threshold (MSB)
0074-007FH	0	XX	074-07FH	SBER Reserved
0080H	0	XX	080H	RRMP Configuration
0081H	0	XX	081H	RRMP Status
0082H	0	XX	082H	RRMP Interrupt Enable
0083H	0	XX	083H	RRMP Interrupt Status
0084H	0	XX	084H	RRMP Received APS
0085H	0	XX	085H	RRMP Received SSM
0086H	0	XX	086H	RRMP AIS enable
0087H	0	XX	087H	RRMP Section BIP Error Counter

REG #	A[12] RX/TX	A[11:10] QUAD	A[9:0]	Register Description
0088H	0	XX	088H	RRMP Line BIP Error Counter (LSB)
0089H	0	XX	089H	RRMP Line BIP Error Counter (MSB)
008AH	0	XX	08AH	RRMP Line REI Error Counter (LSB)
008BH	0	XX	08BH	RRMP Line REI Error Counter (MSB)
008C-009FH	0	XX	08C-09FH	RRMP Reserved
00A0H	0	XX	0A0H	RTTP SECTION Indirect Address
00A1H	0	XX	0A1H	RTTP SECTION Indirect Data
00A2H	0	XX	0A2H	RTTP SECTION Trace Unstable Status
00A3H	0	XX	0A3H	RTTP SECTION Trace Unstable Interrupt Enable
00A4H	0	XX	0A4H	RTTP SECTION Trace Unstable Interrupt Status
00A5H	0	XX	0A5H	RTTP SECTION Trace Mismatch Status
00A6H	0	XX	0A6H	RTTP SECTION Trace Mismatch Interrupt Enable
00A7H	0	XX	0A7H	RTTP SECTION Trace Mismatch Interrupt Status
00A8-00BFH	0	XX	0A8-0BFH	RTTP SECTION Reserved
00C0H	0	XX	0C0H	RTTP PATH Indirect Address
00C1H	0	XX	0C1H	RTTP PATH Indirect Data
00C2H	0	XX	0C2H	RTTP PATH Trace Unstable Status
00C3H	0	XX	0C3H	RTTP PATH Trace Unstable Interrupt Enable
00C4H	0	XX	0C4H	RTTP PATH Trace Unstable Interrupt Status
00C5H	0	XX	0C5H	RTTP PATH Trace Mismatch Status
00C6H	0	XX	0C6H	RTTP PATH Trace Mismatch Interrupt Enable
00C7H	0	XX	0C7H	RTTP PATH Trace Mismatch Interrupt Status
00C8-00DFH	0	XX	0C8-0DFH	RTTP PATH Reserved
00E0H	0	XX	0E0H	RTTP PATH TU3 Indirect Address
00E1H	0	XX	0E1H	RTTP PATH TU3 Indirect Data
00E2H	0	XX	0E2H	RTTP PATH TU3 Trace Unstable Status
00E3H	0	XX	0E3H	RTTP PATH TU3 Trace Unstable Interrupt Enable
00E4H	0	XX	0E4H	RTTP PATH TU3 Trace Unstable Interrupt Status
00E5H	0	XX	0E5H	RTTP PATH TU3 Trace Mismatch Status
00E6H	0	XX	0E6H	RTTP PATH TU3 Trace Mismatch Interrupt Enable
00E7H	0	XX	0E7H	RTTP PATH TU3 Trace Mismatch Interrupt Status
00E8-00FFH	0	XX	0E8-0FFH	RTTP PATH TU3 Reserved
0100H	0	XX	100H	RHPP Indirect Address
0101H	0	XX	101H	RHPP Indirect Data
0102H	0	XX	102H	RHPP Payload Configuration
0103H	0	XX	103H	RHPP Counter Update

REG #	A[12] RX/TX	A[11:10] QUAD	A[9:0]	Register Description
0104H	0	XX	104H	RHPP Path Interrupt Status
0105H	0	XX	105H	RHPP Pointer Concatenation Processing Disable
0106H	0	XX	106H	RHPP Unused
0107H	0	XX	107H	RHPP Unused
0108H	0	XX	108H	RHPP Pointer Interpreter Status STS-1/STM-0 #1
0109H	0	XX	109H	RHPP Pointer Interpreter Interrupt Enable STS-1/STM-0 #1
010AH	0	XX	10AH	RHPP Pointer Interpreter Interrupt Status STS-1/STM-0 #1
010BH	0	XX	10BH	RHPP Error Monitor Status STS-1/STM-0 #1
010CH	0	XX	10CH	RHPP Error Monitor Interrupt Enable STS-1/STM-0 #1
010DH	0	XX	10DH	RHPP Error Monitor Interrupt Status STS-1/STM-0 #1
010EH	0	XX	10EH	RHPP Reserved STS-1/STM-0 #1
010FH	0	XX	10FH	RHPP Reserved STS-1/STM-0 #1
…	…	…	…	…
0160H	0	XX	160H	RHPP Pointer Interpreter Status STS-1/STM-0 #12
0161H	0	XX	161H	RHPP Pointer Interpreter Interrupt Enable STS-1/STM-0 #12
0162H	0	XX	162H	RHPP Pointer Interpreter Interrupt Status STS-1/STM-0 #12
0163H	0	XX	163H	RHPP Error Monitor Status STS-1/STM-0 #12
0164H	0	XX	164H	RHPP Error Monitor Interrupt Enable STS-1/STM-0 #12
0165H	0	XX	165H	RHPP Error Monitor Interrupt Status STS-1/STM-0 #12
0166H	0	XX	166H	RHPP Reserved STS-1/STM-0 #12
0167H	0	XX	167H	RHPP Reserved STS-1/STM-0 #12
0168-017FH	0	XX	168-17FH	RHPP Reserved
0180H	0	XX	180H	RHPP TU3 Indirect Address
0181H	0	XX	181H	RHPP TU3 Indirect Data
0182H	0	XX	182H	RHPP TU3 Payload Configuration
0183H	0	XX	183H	RHPP TU3 Counter Update
0184H	0	XX	184H	RHPP TU3 Path Interrupt Status

REG #	A[12] RX/TX	A[11:10] QUAD	A[9:0]	Register Description
0185H	0	XX	185H	RHPP TU3 Pointer Concatenation Processing Disable
0186H	0	XX	186H	RHPP TU3 Unused
0187H	0	XX	187H	RHPP TU3 Unused
0188H	0	XX	188H	RHPP TU3 Pointer Interpreter Status STS-1/STM-0 #1
0189H	0	XX	189H	RHPP TU3 Pointer Interpreter Interrupt Enable STS-1/STM-0 #1
018AH	0	XX	18AH	RHPP TU3 Pointer Interpreter Interrupt Status STS-1/STM-0 #1
018BH	0	XX	18BH	RHPP TU3 Error Monitor Status STS-1/STM-0 #1
018CH	0	XX	18CH	RHPP TU3 Error Monitor Interrupt Enable STS-1/STM-0 #1
018DH	0	XX	18DH	RHPP TU3 Error Monitor Interrupt Status STS-1/STM-0 #1
018EH	0	XX	18EH	RHPP TU3 Reserved STS-1/STM-0 #1
018FH	0	XX	18FH	RHPP TU3 Reserved STS-1/STM-0 #1
…		…	…	…
01E0H	0	XX	1E0H	RHPP TU3 Pointer Interpreter Status STS-1/STM-0 #12
01E1H	0	XX	1E1H	RHPP TU3 Pointer Interpreter Interrupt Enable STS-1/STM-0 #12
01E2H	0	XX	1E2H	RHPP TU3 Pointer Interpreter Interrupt Status STS-1/STM-0 #12
01E3H	0	XX	1E3H	RHPP TU3 Error Monitor Status STS-1/STM-0 #12
01E4H	0	XX	1E4H	RHPP TU3 Error Monitor Interrupt Enable STS-1/STM-0 #12
01E5H	0	XX	1E5H	RHPP TU3 Error Monitor Interrupt Status STS-1/STM-0 #12
01E6H	0	XX	1E6H	RHPP TU3 Reserved STS-1/STM-0 #12
01E7H	0	XX	1E7H	RHPP TU3 Reserved STS-1/STM-0 #12
01E8-01FFH	0	XX	1E8-1FFH	RHPP TU3 Reserved
0200H	0	XX	200H	RSVCA Indirect Address
0201H	0	XX	201H	RSVCA Indirect Data
0202H	0	XX	202H	RSVCA Payload Configuration
0203H	0	XX	203H	RSVCA Positive Justification Interrupt Status
0204H	0	XX	204H	RSVCA Negative Justification Interrupt Status
0205H	0	XX	205H	RSVCA FIFO Overflow Interrupt Status

REG #	A[12] RX/TX	A[11:10] QUAD	A[9:0]	Register Description
0206H	0	XX	206H	RSVCA FIFO Underflow Interrupt Status
0207H	0	XX	207H	RSVCA Pointer Justification Interrupt Enable
0208H	0	XX	208H	RSVCA FIFO Interrupt Enable
0209H	0	XX	209H	RSVCA Reserved
020AH	0	XX	20AH	RSVCA Misc
020BH	0	XX	20BH	RSVCA Counter Update
020C-021FH	0	XX	20C-21FH	RSVCA Reserved
0220H	0	00	220H	DSTSI Indirect Address
0221H	0	00	221H	DSTSI Indirect Data
0222H	0	00	222H	DSTSI Configuration
0223H	0	00	223H	DSTSI Interrupt Status
0223-023FH	0	00	223-23FH	DSTSI Reserved
0240H	0	XX	240H	DPRGM Indirect Address
0241H	0	XX	241H	DPRGM Indirect Data
0242H	0	XX	242H	DPRGM Generator Payload Configuration
0243H		XX	243H	DPRGM Monitor Payload Configuration
0244H	0	XX	244H	DPRGM Monitor Byte Error Interrupt Status
0245H	0	XX	245H	DPRGM Monitor Byte Error Interrupt Enable
0246H	0	XX	246H	DPRGM Monitor B1/E1 Bytes Interrupt Status
0247H	0	XX	247H	DPRGM Monitor B1/E1 Bytes Interrupt Enable
0248H	0	XX	248H	DPRGM Reserved
0249H	0	XX	249H	DPRGM Monitor Synchronization Interrupt Status
024AH	0	XX	24AH	DPRGM Monitor Synchronization Interrupt Enable
024BH	0	XX	24BH	DPRGM Monitor Synchronization Status
024CH	0	XX	24CH	DPRGM Counter Update
024D-025FH	0	XX	24D-25FH	DPRGM Reserved
0260H	0	XX	260H	SARC Indirect Address
0261H	0	XX	261H	SARC Unused
0262H	0	XX	262H	SARC Section Configuration
0263H	0	XX	263H	SARC Section SALM enable
0264H	0	XX	264H	SARC Section RLAISINS enable
0265H	0	XX	265H	SARC Section TLRDIINS enable
0266H	0	XX	266H	SARC Unused
0267H	0	XX	267H	SARC Unused
0268H	0	XX	268H	SARC Path Configuration
0269H	0	XX	269H	SARC Path RALM Enable
026AH	0	XX	26AH	SARC Path RPAISINS Enable

REG #	A[12] RX/TX	A[11:10] QUAD	A[9:0]	Register Description
026BH	0	XX	26BH	SARC TU3 Path Configuration
026CH	0	XX	26CH	SARC TU3 Path RALM Enable
026DH	0	XX	26DH	SARC TU3 Path RPAISINS Enable
026EH	0	XX	26EH	SARC Unused
026FH	0	XX	26FH	SARC Unused
0270H	0	XX	270H	SARC LOP Pointer Status
0271H	0	XX	271H	SARC LOP Pointer Interrupt Enable
0272H	0	XX	272H	SARC LOP Pointer Interrupt Status
0273H	0	XX	273H	SARC AIS Pointer Status
0274H	0	XX	274H	SARC AIS Pointer Interrupt Enable
0275H	0	XX	275H	SARC AIS Pointer Interrupt Status
0276H	0	XX	276H	SARC Unused
0277H	0	XX	277H	SARC Unused
0278H	0	XX	278H	SARC TU3 LOP Pointer Status
0279H	0	XX	279H	SARC TU3 LOP Pointer Interrupt Enable
027AH	0	XX	27AH	SARC TU3 LOP Pointer Interrupt Status
027BH	0	XX	27BH	SARC TU3 AIS Pointer Status
027CH	0	XX	27CH	SARC TU3 AIS Pointer Interrupt Enable
027DH	0	XX	27DH	SARC TU3 AIS Pointer Interrupt Status
027EH	0	XX	27EH	SARC Unused
027FH	0	XX	27FH	SARC Unused
0280-029FH	0	XX	280-29FH	Reserved
02A0-02BFH	0	XX	2A0-2BFH	Reserved
02C0-02DFH	0	XX	2C0-2DFH	Reserved
02E0-02FFH	0	XX	2E0-2FFH	Reserved
0300-0301H	0	XX	300-301H	DDLL Reserved
0302H	0	XX	302H	DDLL Reset
0303-031FH	0	XX	303-31FH	DDLL Reserved
0320-033FH	0	XX	320-33FH	Reserved
0340-035FH	0	XX	340-35FH	Reserved
0360-037FH	0	XX	360-37FH	Reserved
0380-039FH	0	XX	380-39FH	Reserved

REG #	A[12] RX/TX	A[11:10] QUAD	A[9:0]	Register Description
03A0-03BFH	0	XX	3A0-3BFH	Reserved
03C0-03DFH	0	XX	3C0-3DFH	Reserved
03E0-03FFH	0	XX	3E0-3FFH	Reserved
1000-101FH	1	XX	000-01FH	SP2488 Reserved
1020-103FH	1	XX	020-03FH	SP2488 TX Slice Reserved
1040H	1	00	040H	STLI Clock Configuration
1041H	1	00	041H	STLI PGM Clock Configuration
1042-105FH	1	00	042-05FH	STLI Reserved
1060-107FH	1	XX	060-07FH	Reserved
1080H	1	XX	080H	TRMP Configuration
1081H	1	XX	081H	TRMP Register Insertion
1082H	1	XX	082H	TRMP Error Insertion
1083H	1	XX	083H	TRMP Transmit J0 and Z0
1084H	1	XX	084H	TRMP Transmit E1 and F1
1085H	1	XX	085H	TRMP Transmit D1D3 and D4D12
1086H	1	XX	086H	TRMP Transmit K1 and K2
1087H	1	XX	087H	TRMP Transmit S1 and Z1
1088H	1	XX	088H	TRMP Transmit Z2 and E2
1089H	1	XX	089H	TRMP H1 and H2 Mask
108AH	1	XX	08AH	TRMP B1 and B2 Mask
108B-109FH	1	XX	08B-09FH	TRMP Reserved
10A0H	1	XX	0A0H	TTTP SECTION Indirect Address
10A1H	1	XX	0A1H	TTTP SECTION Indirect Data
10A2-10BFH	1	XX	0A2-0BFH	TTTP SECTION Reserved
10C0H	1	XX	0C0H	TTTP PATH Indirect Address
10C1H	1	XX	0C1H	TTTP PATH Indirect Data
10C2-10DFH	1	XX	0C2-0DFH	TTTP PATH Reserved
10E0H	1	XX	0E0H	TTTP PATH TU3 Indirect Address
10E1H	1	XX	0E1H	TTTP PATH TU3 Indirect Data
10E2-10FFH	1	XX	0E2-0FFH	TTTP PATH TU3 Reserved
1100H	1	XX	100H	THPP Indirect Address
1101H	1	XX	101H	THPP Indirect Data

REG #	A[12] RX/TX	A[11:10] QUAD	A[9:0]	Register Description
1102H	1	XX	102H	THPP Payload Configuration
1103-117FH	1	XX	103-17FH	THPP Reserved
1180H	1	XX	180H	THPP TU3 Indirect Address
1181H	1	XX	181H	THPP TU3 Indirect Data
1182H	1	XX	182H	THPP TU3 Payload Configuration
1183 - 11FFH	1	XX	183-1FFH	THPP TU3 Reserved
1200H	1	XX	200H	TSVCA Indirect Address
1201H	1	XX	201H	TSVCA Indirect Data
1202H	1	XX	202H	TSVCA Payload Configuration
1203H	1	XX	203H	TSVCA Positive Justification Interrupt Status
1204H	1	XX	204H	TSVCA Negative Justification Interrupt Status
1205H	1	XX	205H	TSVCA FIFO Overflow Interrupt Status
1206H	1	XX	206H	TSVCA FIFO Underflow Interrupt Status
1207H	1	XX	207H	TSVCA Pointer Justification Interrupt Enable
1208H	1	XX	208H	TSVCA FIFO Interrupt Enable
1209H	1	XX	209H	TSVCA Reserved
120AH	1	XX	20AH	TSVCA Misc
120BH	1	XX	20BH	TSVCA Counter Update
120C-121FH	1	XX	20C-21FH	TSVCA Reserved
1220H	1	00	220H	ASTSI Indirect Address
1221H	1	00	221H	ASTSI Indirect Data
1222H	1	00	222H	ASTSI Configuration
1223H	1	00	223H	ASTSI Interrupt Status
1224-123FH	1	00	224-23FH	ASTSI Reserved
1240H	1	XX	240H	APRGM Indirect Address
1241H	1	XX	241H	APRGM Indirect Data
1242H	1	XX	242H	APRGM Generator Payload Configuration
1243H	1	XX	243H	APRGM Monitor Payload Configuration
1244H	1	XX	244H	APRGM Monitor Byte Error Interrupt Status
1245H	1	XX	245H	APRGM Monitor Byte Error Interrupt Enable
1246H	1	XX	246H	APRGM Monitor B1/E1 Bytes Interrupt Status
1247H	1	XX	247H	APRGM Monitor B1/E1 Bytes Interrupt Enable
1248H	1	XX	248H	APRGM Reserved
1249H	1	XX	249H	APRGM Monitor Synchronization Interrupt Status
124AH	1	XX	24AH	APRGM Monitor Synchronization Interrupt Enabble
124BH	1	XX	24BH	APRGM Monitor Synchronization Status

REG #	A[12] RX/TX	A[11:10] QUAD	A[9:0]	Register Description
124CH	1	XX	24CH	APRGM Counter Update
124D-125FH	1	XX	24D-35FH	APRGM Reserved
1260-127FH	1	XX	260-27FH	Reserved
1280H	1	XX	280H	TAPI Indirect Address
1281H	1	XX	281H	TAPI Indirect Data
1282H	1	XX	282H	TAPI Payload Configuration
1283H	1	XX	283H	TAPI Counter Update
1284H	1	XX	284H	TAPI Path Interrupt Status
1285H	1	XX	285H	TAPI Pointer Concatenation Processing Disable
1286H	1	XX	286H	TAPI Reserved
1287H	1	XX	287H	TAPI Reserved
1288H	1	XX	288H	TAPI Pointer Interpreter Status STS-1/STM-0 #1
1289H	1	XX	289H	TAPI Pointer Interpreter Interrupt Enable STS-1/STM-0 #1
128AH	1	XX	28AH	TAPI Pointer Interpreter Interrupt Status STS-1/STM-0 #1
128BH	1	XX	28BH	TAPI Error Monitor Status STS-1/STM-0 #1
128CH	1	XX	28CH	TAPI Error Monitor Interrupt Enable STS-1/STM-0 #1
128DH	1	XX	28DH	TAPI Error Monitor Interrupt Status STS-1/STM-0 #1
128EH	1	XX	28EH	TAPI Reserved STS-1/STM-0 #1
128FH	1	XX	28FH	TAPI Reserved STS-1/STM-0 #1
…	…	…	…	…
12E0H	1	XX	2E0H	TAPI Pointer Interpreter Status STS-1/STM-0 #12
12E1H	1	XX	2E1H	TAPI Pointer Interpreter Interrupt Enable STS-1/STM-0 #12
12E2H	1	XX	2E2H	TAPI Pointer Interpreter Interrupt Status STS-1/STM-0 #12
12E3H	1	XX	2E3H	TAPI Error Monitor Status STS-1/STM-0 #12
12E4H	1	XX	2E4H	TAPI Error Monitor Interrupt Enable STS-1/STM-0 #12
12E5H	1	XX	2E5H	TAPI Error Monitor Interrupt Status STS-1/STM-0 #12
12E6H	1	XX	2E6H	TAPI Reserved STS-1/STM-0 #12

REG #	A[12] RX/TX	A[11:10] QUAD	A[9:0]	Register Description
12E7H	1	XX	2E7H	TAPI Reserved STS-1/STM-0 #12
12E8-12FFH	1	XX	2E8-2FFH	TAPI Reserved
1300-1301H	1	XX	300-301H	ADLL Reserved
1302H	1	XX	302H	ADLL Reset
1303-131FH	1	XX	303-31FH	ADLL Reserved
1320-133FH	1	XX	320-33FH	Reserved
1340-135FH	1	XX	340-35FH	Reserved
1360-137FH	1	XX	360-37FH	Reserved
1380-139FH	1	XX	380-39FH	Reserved
13A0-13BFH	1	XX	3A0-3BFH	Reserved
13C0-13DFH	1	XX	3C0-3DFH	Reserved
13E0-13FFH	1	XX	3E0-3FFH	Reserved

Notes on Register Memory Map

1. For all register accesses, CSB must be low.
2. Addresses that are not shown must be treated as Reserved.
3. A[13] is the test resister select (TRS) and should be set to logic 0 for normal mode register access.

11 Normal Mode Register Description

Normal mode registers are used to configure and monitor the operation of the SPECTRA-2488. Normal mode registers (as opposed to test mode registers) are selected when TRS (A[13]) is low.

Notes on Normal Mode Register Bits:

1. Writing values into unused register bits has no effect. However, to ensure software compatibility with future, feature-enhanced versions of this product, unused register bits must be written with logic 0. Reading back unused bits can produce either a logic 1 or a logic 0; hence, unused register bits should be masked off by software when read.

2. All configuration bits that can be written into can also be read back. This allows the processor controlling the SPECTRA-2488 to determine the programming state of the device.

3. Writeable normal mode register bits are cleared to logic 0 upon reset unless otherwise noted.

4. Writing into read-only normal mode register bit locations does not affect SPECTRA-2488 operation unless otherwise noted.

5. Certain register bits are reserved. These bits are associated with megacell functions that are unused in this application. To ensure that the SPECTRA-2488 operates as intended, reserved register bits must only be written with the logic level as specified. Writing to reserved registers should be avoided.

Register 0000H: SP2488 Master Configuration

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12	R/W	Reserved	0
Bit 11	R/W	WCIMODE	0
Bit 10	R/W	RESETSL[4]	0
Bit 9	R/W	RESETSL[3]	0
Bit 8	R/W	RESETSL[2]	0
Bit 7	R/W	RESETSL[1]	0
Bit 6	R/W	RESET	0
Bit 5	R	TIP	X
Bit 4		Unused	
Bit 3		Unused	
Bit 2		Unused	
Bit 1		Unused	
Bit 0	R	QUAD622	X

The Master Configuration Register is provided at SP2488 r/w address 00H.

QUAD622

The quad 622 operating mode (QUAD622) signal is asserted high while the device operates in the quad OC-12 mode and is negated while the device operates in single OC-48 mode. The operating mode of the SPECTRA-2488 is selected by the QUAD622 pin.

TIP

The transfer in progress (TIP) signal is asserted high while the performance monitors are being transferred to the holding registers. The transfer is initiated by writing to the Master Configuration Register. TIP is negated when the transfer is completed.

RESET

The software reset (RESET) bit resets the whole device. When a logic 1 is written to RESET, the SP2488 is held in reset. When a logic 0 is written to RESET, the SP2488 operates normally.

RESETSL[1:4]

The slice software reset (RESETSL[1:4]) bits reset the corresponding STS-12/STM-4 slice. When a logic 1 is written to RESETSL[X], the STS-12/STM-4 slice is held in reset. When a logic 0 is written to RESETSL[X], the STS-12/STM-4 slice operates normally.

WCIMODE

The write on clear interrupt mode (WCIMODE) bit selects the clear interrupt mode. When a logic 1 is written to WCIMODE, the clear interrupt mode is clear on write. When a logic 0 is written to WCIMODE, the clear interrupt mode is clear on read.

Register 0001H: SP2488 Receive Configuration

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14	R/W	RDCC[1]	0
Bit 13	R/W	RDCC[0]	0
Bit 12	R/W	FORCEB3E	0
Bit 11	R/W	DSTSISW[1]	0
Bit 10	R/W	DSTSISW[0]	1
Bit 9	R/W	RDDS	0
Bit 8	R/W	RESDIS	0
Bit 7	R/W	RSTS12C[4]	0
Bit 6	R/W	RSTS12C[3]	0
Bit 5	R/W	RSTS12C[2]	0
Bit 4	R/W	RSTS12C[1]	0
Bit 3	R/W	RSTS12CSL[4]	0
Bit 2	R/W	RSTS12CSL[3]	0
Bit 1	R/W	RSTS12CSL[2]	0
Bit 0	R/W	RSTS12CSL[1]	0

The Receive Configuration Register is provided at SP2488 r/w address 01H.

RSTS12CSL[1:4]

The receive STS-12 slave concatenation mode (RSTS12CSL[1:4]) bits enable the slave processing of an STS-12c (VC-4-4c) payload for the corresponding STS-12/STM-4 slice. When a logic 1 is written to RSTS12CSL[X] and a logic 1 is written to RSTS12C[X], the receive STS-12/STM-4 slice process a slave STS-12c (VC-4-4c) payload. When a logic 0 is written to RSTS12CSL[X] and a logic 1 is written to RSTS12C[X], the receive STS-12/STM-4 slice process a master STS-12c (VC-4-4c) payload. When a logic 0 is written to RSTS12CSL[X] and a logic 0 is written to RSTS12C[X], the receive STS-12/STM-4 slice is not processing a STS-12c (VC-4-4c) payload.

RSTS12C[1:4]

The receive STS-12 concatenation mode (RSTS12C[1:4]) bits enable the processing of an STS-12c (VC-4-4c) payload for the corresponding STS-12/STM-4 slice. When a logic 1 is written to RSTS12CSL[X] and a logic 1 is written to RSTS12C[X], the receive STS-12/STM-4 slice process a slave STS-12c (VC-4-4c) payload. When a logic 0 is written to RSTS12CSL[X] and a logic 1 is written to RSTS12C[X], the receive STS-12/STM-4 slice process a master STS-12c (VC-4-4c) payload. When a logic 0 is written to RSTS12CSL[X] and a logic 0 is written to RSTS12C[X], the receive STS-12/STM-4 slice is not processing a STS-12c (VC-4-4c) payload.

RESDIS

The receive elastic store disable (RESDIS) bit disable the internal FIFO. When a logic 1 is written to RESDIS, the input data is not buffered inside the FIFO and is not re-aligned to a new transport frame. When a logic 0 is written to RESDIS, the input data is buffered inside the FIFO and re-aligned to a new transport frame.

RDDS

The receive disable de scrambling (RDDS) bit disables the de scrambling of the input data stream. When a logic 1 is written to RDDS, the input data stream is not de scrambled. When a logic 0 is written to RDDS, the input data stream is de scrambled.

DSTSISW[1:0]

The drop STSI switching mode (DSTSISW[1:0]) bits select the operational switching mode of the STSI.

DSTSISW[1:0]	Mode	Comment
00	dynamic mode	Switching is controlled by the Current active page.
01	bypass mode	Straight-through connection, no timeslot interchange.
10	12-48c mode	Straight-through connection, no timeslot interchange. The space switch function is used to map 4 OC-12 streams into a single OC-48c stream.
11	48c-12 mode	Straight-through connection, no timeslot interchange. The space switch function is used to map a single OC-48c stream into 4 OC-12 streams.

FORCEB3E

The force B3E (FORCEB3E) bit forces the B3E[X] errors to appear on the RALM_B3E[X] pins instead of the RALM[X] alarms in the quad OC-12 mode. When a logic 1 is written to FORCEB3E, B3E[X] errors appears onto SALM_B3E[X] pins. When a logic 0 is written to FORCEB3E, SALM[X] alarms appears onto SALM_B3E[X] pins.

RDCC[1:0]

The receive DCC (RDCC[1:0]) bits select from which STS-12/STM-4 slice the section and line DCC are extracted in the quad OC-12 mode.

RDCC[1:0]	STS-12/STM-4 Slice
00	Slice 1
01	Slice 2
10	Slice 3
11	Slice 4

Register 0002H: SP2488 Transmit Configuration

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14	R/W	TDCC[1]	0
Bit 13	R/W	TDCC[0]	0
Bit 12	R/W	TAPIDIS	1
Bit 11	R/W	ASTSISW[1]	0
Bit 10	R/W	ASTSISW[0]	1
Bit 9	R/W	TDS	0
Bit 8	R/W	TESDIS	0
Bit 7	R/W	TSTS12C[4]	0
Bit 6	R/W	TSTS12C[3]	0
Bit 5	R/W	TSTS12C[2]	0
Bit 4	R/W	TSTS12C[1]	0
Bit 3	R/W	TSTS12CSL[4]	0
Bit 2	R/W	TSTS12CSL[3]	0
Bit 1	R/W	TSTS12CSL[2]	0
Bit 0	R/W	TSTS12CSL[1]	0

The Transmit Configuration Register is provided at SP2488 r/w address 02H.

TSTS12CSL[1:4]

The transmit STS-12 slave concatenation mode (TSTS12CSL[1:4]) bits enable the slave processing of an STS-12c (VC-4-4c) payload for the corresponding STS-12/STM-4 slice. When a logic 1 is written to TSTS12CSL[X] and a logic 1 is written to TSTS12C[X], the receive STS-12/STM-4 slice process a slave STS-12c (VC-4-4c) payload. When a logic 0 is written to TSTS12CSL[X] and a logic 1 is written to TSTS12C[X], the receive STS-12/STM-4 slice process a master STS-12c (VC-4-4c) payload. When a logic 0 is written to TSTS12CSL[X] and a logic 0 is written to TSTS12C[X], the receive STS-12/STM-4 slice is not processing a STS-12c (VC-4-4c) payload.

TSTS12C[1:4]

The transmit STS-12 concatenation mode (TSTS12C[1:4]) bits enable the processing of an STS-12c (VC-4-4c) payload for the corresponding STS-12/STM-4 slice. When a logic 1 is written to TSTS12CSL[X] and a logic 1 is written to TSTS12C[X], the receive STS-12/STM-4 slice process a slave STS-12c (VC-4-4c) payload. When a logic 0 is written to TSTS12CSL[X] and a logic 1 is written to TSTS12C[X], the receive STS-12/STM-4 slice process a master STS-12c (VC-4-4c) payload. When a logic 0 is written to TSTS12CSL[X] and a logic 0 is written to TSTS12C[X], the receive STS-12/STM-4 slice is not processing a STS-12c (VC-4-4c) payload.

TESDIS

The transmit elastic store disable (TESDIS) bit disable the internal FIFO. When a logic 1 is written to TESDIS, the input data is not buffered inside the FIFO and is not re-aligned to a new transport frame. When a logic 0 is written to TESDIS, the input data is buffered inside the FIFO and re-aligned to a new transport frame.

TDS

The transmit disable scrambling (TDS) bit disables the scrambling of the output data stream. When a logic 1 is written to TDS, the output data stream is not scrambled. When a logic 0 is written to TDS, the output data stream is scrambled.

ASTSISW[1:0]

The add STSI switching mode (ASTSISW[1:0]) bits select the operational switching mode of the STSI.

ASTSISW[1:0]	Mode	Comment
00	dynamic mode	Switching is controlled by the Current active page.
01	bypass mode	Straight-through connection, no timeslot interchange.
10	12-48c mode	Straight-through connection, no timeslot interchange. The space switch function is used to map 4 OC-12 streams into a single OC-48c stream.
11	48c-12 mode	Straight-through connection, no timeslot interchange. The space switch function is used to map a single OC-48c stream into 4 OC-12 streams.

TAPIDIS

The transmit add bus pointer interpreter disable (TAPIDIS) bit disables the pointer interpreter. When a logic 1 is written to TAPIDIS, the add bus pointer interpreter is disable. When a logic 0 is written to TAPIDIS, the add bus pointer interpreter is enable.

TDCC[1:0]

The transmit DCC (TDCC[1:0]) bits select from which STS-12/STM-4 slice the section and line DCC are inserted.

TDCC[1:0]	STS-12/STM-4 Slice
00	Slice 1
01	Slice 2
10	Slice 3
11	Slice 4

Register 0003H: SP2488 Loop Timing Configuration

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9		Unused	
Bit 8		Unused	
Bit 7		Unused	
Bit 6	R/W	Reserved	0
Bit 5	R/W	PHASESYNC	0
Bit 4	R/W	LPTDCLK[4]	0
Bit 3	R/W	LPTDCLK[3]	0
Bit 2	R/W	LPTDCLK[2]	0
Bit 1	R/W	LPTDCLK[1]	0
Bit 0	R/W	LPTDCLK	0

The Loop Timing Configuration Register is provided at SP2488 r/w address 03H.

LPTDCLK

The TDCLK loop timing (LPTDCLK) bit enables RDCLK loop timing onto TDCLK. When a logic 1 is written to LPTDCLK, RDCLK is two stage muxed onto TDCLK. When a logic 0 is written to LPTDCLK, loop timing is disabled.

LPTDCLK[1:4]

The TDCLK[1:4] loop timing (LPTDCLK[1:4]) bit enables RDCLK1-4 loop timing onto TDCLK1-4. When a logic 1 is written to LPTDCLK[X], RDCLKX is two stage muxed onto TDCLKX. When a logic 0 is written to LPTDCLK[X], loop timing is disabled.

PHASESYNC

The phase synchronization (PHASESYNC) bit synchronizes the phase of the internal STS-12 slice clocks derived from RDCLK+/- and TDCLK+/- when the SPECTRA-2488 is configured in OC-48 mode. Phase synchronization is needed for proper data loop back in single OC-48 mode. When a logic 1 is written to PHASESYNC, TFPI is ignored and the phase of the internal transmit clocks are synchronized with the internal receive clocks. When a logic 0 is written to PHASESYNC, the phase of the internal transmit clocks is synchronized to TFPI. This bit is not valid quad OC-12 mode.

Register 0008H: SP2488 System Side Line Loop Back #1

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11	R/W	SLLBEN[1][12]	0
Bit 10	R/W	SLLBEN[1][11]	0
Bit 9	R/W	SLLBEN[1][10]	0
Bit 8	R/W	SLLBEN[1][9]	0
Bit 7	R/W	SLLBEN[1][8]	0
Bit 6	R/W	SLLBEN[1][7]	0
Bit 5	R/W	SLLBEN[1][6]	0
Bit 4	R/W	SLLBEN[1][5]	0
Bit 3	R/W	SLLBEN[1][4]	0
Bit 2	R/W	SLLBEN[1][3]	0
Bit 1	R/W	SLLBEN[1][2]	0
Bit 0	R/W	SLLBEN[1][1]	0

The Loop Back Register is provided at SP2488 r/w address 08H.

SLLBEN[1][1:12]

The system side/line loop back (SLLBEN[1][1:12]) bits enable the SLLBEN for the first STS-12/STM-4 slice. When a logic 1 is written to SLLBEN[1][X], the drop system data of STS-1/STM-0 path X is loop back into the add system data of STS-1/STM-0 path X. When a logic 0 is written to SLLBEN[1][X], the system side/line loop back is inactive.
Note: For proper operation when the AJ0J1_FP port contains no valid framing, the AFPEN mode (bit 14 of register 0016H) must be configure and the AFPMASK mask (bit 15 of register 001DH) must be enable.

Register 0009H: SP2488 System Side Line Loop Back #2

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11	R/W	SLLBEN[2][12]	0
Bit 10	R/W	SLLBEN[2][11]	0
Bit 9	R/W	SLLBEN[2][10]	0
Bit 8	R/W	SLLBEN[2][9]	0
Bit 7	R/W	SLLBEN[2][8]	0
Bit 6	R/W	SLLBEN[2][7]	0
Bit 5	R/W	SLLBEN[2][6]	0
Bit 4	R/W	SLLBEN[2][5]	0
Bit 3	R/W	SLLBEN[2][4]	0
Bit 2	R/W	SLLBEN[2][3]	0
Bit 1	R/W	SLLBEN[2][2]	0
Bit 0	R/W	SLLBEN[2][1]	0

The Loop Back Register is provided at SP2488 r/w address 09H.

SLLBEN[2][1:12]

The system side/line loop back (SLLBEN[2][1:12]) bits enable the SLLBEN for the second STS-12/STM-4 slice. When a logic 1 is written to SLLBEN[2][X], the drop system data of STS-1/STM-0 path X is loop back into the add system data of STS-1/STM-0 path X. When a logic 0 is written to SLLBEN[2][X], the system side/line loop back is inactive.
Note: For proper operation when the AJ0J1_FP port contains no valid framing, the AFPEN mode (bit 14 of register 0016H) must be configure and the AFPMASK mask (bit 15 of register 001DH) must be enable.

Register 000AH: SP2488 System Side Line Loop Back #3

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11	R/W	SLLBEN[3][12]	0
Bit 10	R/W	SLLBEN[3][11]	0
Bit 9	R/W	SLLBEN[3][10]	0
Bit 8	R/W	SLLBEN[3][9]	0
Bit 7	R/W	SLLBEN[3][8]	0
Bit 6	R/W	SLLBEN[3][7]	0
Bit 5	R/W	SLLBEN[3][6]	0
Bit 4	R/W	SLLBEN[3][5]	0
Bit 3	R/W	SLLBEN[3][4]	0
Bit 2	R/W	SLLBEN[3][3]	0
Bit 1	R/W	SLLBEN[3][2]	0
Bit 0	R/W	SLLBEN[3][1]	0

The Loop Back Register is provided at SP2488 r/w address 0AH.

SLLBEN[3][1:12]

The system side/line loop back (SLLBEN[3][1:12]) bits enable the SLLBEN for the third STS-12/STM-4 slice. When a logic 1 is written to SLLBEN[3][X], the drop system data of STS-1/STM-0 path X is loop back into the add system data of STS-1/STM-0 path X. When a logic 0 is written to SLLBEN[3][X], the system side/line loop back is inactive.

Note: For proper operation when the AJ0J1_FP port contains no valid framing, the AFPEN mode (bit 14 of register 0016H) must be configure and the AFPMASK mask (bit 15 of register 001DH) must be enable.

Register 000BH: SP2488 System Side Line Loop Back #4

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11	R/W	SLLBEN[4][12]	0
Bit 10	R/W	SLLBEN[4][11]	0
Bit 9	R/W	SLLBEN[4][10]	0
Bit 8	R/W	SLLBEN[4][9]	0
Bit 7	R/W	SLLBEN[4][8]	0
Bit 6	R/W	SLLBEN[4][7]	0
Bit 5	R/W	SLLBEN[4][6]	0
Bit 4	R/W	SLLBEN[4][5]	0
Bit 3	R/W	SLLBEN[4][4]	0
Bit 2	R/W	SLLBEN[4][3]	0
Bit 1	R/W	SLLBEN[4][2]	0
Bit 0	R/W	SLLBEN[4][1]	0

The Loop Back Register is provided at SP2488 r/w address 0BH.

SLLBEN[4][1:12]

The system side/line loop back (SLLBEN[4][1:12]) bits enable the SLLBEN for the fourth STS-12/STM-4 slice. When a logic 1 is written to SLLBEN[4][X], the drop system data of STS-1/STM-0 path X is loop back into the add system data of STS-1/STM-0 path X. When a logic 0 is written to SLLBEN[4][X], the system side/line loop back is inactive.

Note: For proper operation when the AJ0J1_FP port contains no valid framing, the AFPEN mode (bit 14 of register 0016H) must be configure and the AFPMASK mask (bit 15 of register 001DH) must be enable.

Register 000CH: SP2488 Line Side Loop Back

Bit	Type	Function	Default
Bit 15	R/W	LSLBEN[4]	0
Bit 14	R/W	LSLBEN [3]	0
Bit 13	R/W	LSLBEN [2]	0
Bit 12	R/W	LSLBEN [1]	0
Bit 11	R/W	LLLBEN [4]	0
Bit 10	R/W	LLLBEN [3]	0
Bit 9	R/W	LLLBEN [2]	0
Bit 8	R/W	LLLBEN [1]	0
Bit 7	R/W	Reserved	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	Reserved	0

The Loop Back Register is provided at SP2488 r/w address 0CH.

LLLBEN[1:4]

The line side/line loop back (LLLBEN[1:4]) bits enable the LLLBEN for the corresponding STS-12/STM-4 slice. When a logic 1 is written to LLLBEN[X], the line RX data of slice X is loop back into the line TX data of slice X. When a logic 0 is written to LLLBEN[X], the line side/line loop back is inactive.

Note: For proper operation, RDCLK must be muxed over TDCLK (bit 0 and 5 of register 0003H for single mode operation, bit 1 to 4 of register 0003H for quad mode operation).
Note: For proper operation after the loopback is enable, the transmit and receive datastreams must be manually frame aligned. This can be accomplish by forcing a new frame alignment using the FOOF bit in the RRMP block (Register 0080H for single mode operation and registers 0080H, 0480H, 0880H and 0C80H for quad mode operation)

LSLBEN[1:4]

The line side/system loop back (LSLBEN[1:4]) bits enable the LSLBEN for the corresponding STS-12/STM-4 slice. When a logic 1 is written to LSLBEN[X], the line TX data and line TX clock of slice X is loop back into the line RX data and line RX clock of slice X. When a logic 0 is written to LSLBEN[X], the line side/system loop back is inactive.

Note: Enabling the line side/system loop back of slice X will also muxed TDCLK over RDCLK for the corresponding slice.

Register 000EH: SP2488 Line Activity Monitor

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9		Unused	
Bit 8		Unused	
Bit 7	R	TCLKACT[4]	X
Bit 6	R	TCLKACT[3]	X
Bit 5	R	TCLKACT[2]	X
Bit 4	R	TCLKACT[1]	X
Bit 3	R	RCLKACT[4]	X
Bit 2	R	RCLKACT[3]	X
Bit 1	R	RCLKACT[2]	X
Bit 0	R	RCLKACT[1]	X

The Line Activity Monitor is provided at SP2488 r/w address 0EH.

RCLKACT[1:4]

The receive line activity monitor (RCLKACT[1:4]) signals are event detectors. RCLKACT[X] is asserted when a low to high transition occurs on the internal receive clock of slice X. RCLKACT[X] is cleared when the line activity monitor register is read.

TCLKACT[1:4]

The transmit line activity monitor (TCLKACT[1:4]) signals are event detectors. TCLKACT[X] is asserted when a low to high transition occurs on the internal transmit clock of slice X. TCLKACT[X] is cleared when the line activity monitor register is read.

Register 0010H: SP2488 Interrupt Status #1

Bit	Type	Function	Default
Bit 15	R/W	INTE[1]	0
Bit 14	R	ASTSII	X
Bit 13	R	TAPII[1]	X
Bit 12	R	APRGMI[1]	X
Bit 11	R	TSVCAI[1]	X
Bit 10	R	DSTSII	X
Bit 9	R	DPRGMI[1]	X
Bit 8	R	SARCI[1]	X
Bit 7	R	RSVCAI[1]	X
Bit 6	R	PATHTU3RTTPI[1]	X
Bit 5	R	TU3RHPPI[1]	X
Bit 4	R	PATHRTTPI[1]	X
Bit 3	R	RHPPI[1]	X
Bit 2	R	SBERI[1]	X
Bit 1	R	RTTPI[1]	X
Bit 0	R	RRMPI[1]	X

The Interrupt Status Register is provided at SP2488 r/w address 10H.

RRMPI[1] to ASTSI

The RRMPI[1] to ASTSI are interrupt status indicators for the corresponding block. The interrupt status is set to logic 1 to indicate a pending interrupt from the corresponding block. The interrupt status bits are independent of the interrupt enable bit.

INTE[1]

The interrupt enable (INTE[1]) bit controls the activation of the interrupt (INT) output. When a logic 1 is written to INTE[1], the RRMP[1] to ASTSI pending interrupt will assert the interrupt (INT) output. When a logic 0 is written to INTE[1], the RRMP[1] to ASTSI pending interrupt will not assert the interrupt (INT) output.

Register 0011H: SP2488 Interrupt Status #2

Bit	Type	Function	Default
Bit 15	R/W	INTE[2]	0
Bit 14		Unused	
Bit 13	R	TAPII[2]	X
Bit 12	R	APRGMI[2]	X
Bit 11	R	TSVCAI[2]	X
Bit 10		Unused	
Bit 9	R	DPRGMI[2]	X
Bit 8	R	SARCI[2]	X
Bit 7	R	RSVCAI[2]	X
Bit 6	R	PATHTU3RTTPI[2]	X
Bit 5	R	TU3RHPPI[2]	X
Bit 4	R	PATHRTTPI[2]	X
Bit 3	R	RHPPI[2]	X
Bit 2	R	SBERI[2]	X
Bit 1	R	RTTPI[2]	X
Bit 0	R	RRMPI[2]	X

The Interrupt Status Register is provided at SP2488 r/w address 11H.

RRMPI[2] to TAPII[2]

The RRMPI[2] to TAPII[2] are interrupt status indicators for the corresponding block. The interrupt status is set to logic 1 to indicate a pending interrupt from the corresponding block. The interrupt status bits are independent of the interrupt enable bit.

INTE[2]

The interrupt enable (INTE[2]) bit controls the activation of the interrupt (INT) output. When a logic 1 is written to INTE[2], the RRMP[2] to TAPII[2] pending interrupt will assert the interrupt (INT) output. When a logic 0 is written to INTE[2], the RRMP[2] to TAPII[2] pending interrupt will not assert the interrupt (INT) output.

Register 0012H: SP2488 Interrupt Status #3

Bit	Type	Function	Default
Bit 15	R/W	INTE[3]	0
Bit 14		Unused	
Bit 13	R	TAPII[3]	X
Bit 12	R	APRGMI[3]	X
Bit 11	R	TSVCAI[3]	X
Bit 10		Unused	
Bit 9	R	DPRGMI[3]	X
Bit 8	R	SARCI[3]	X
Bit 7	R	RSVCAI[3]	X
Bit 6	R	PATHTU3RTTPI[3]	X
Bit 5	R	TU3RHPPI[3]	X
Bit 4	R	PATHRTTPI[3]	X
Bit 3	R	RHPPI[3]	X
Bit 2	R	SBERI[3]	X
Bit 1	R	RTTPI[3]	X
Bit 0	R	RRMPI[3]	X

The Interrupt Status Register is provided at SP2488 r/w address 12H.

RRMPI[3] to TAPII[3]

The RRMPI[3] to TAPII[3] are interrupt status indicators for the corresponding block. The interrupt status is set to logic 1 to indicate a pending interrupt from the corresponding block. The interrupt status bits are independent of the interrupt enable bit.

INTE[3]

The interrupt enable (INTE[3]) bit controls the activation of the interrupt (INT) output. When a logic 1 is written to INTE[3], the RRMP[3] to TAPII[3] pending interrupt will assert the interrupt (INT) output. When a logic 0 is written to INTE[3], the RRMP[3] to TAPII[3] pending interrupt will not assert the interrupt (INT) output.

Register 0013H: SP2488 Interrupt Status #4

Bit	Type	Function	Default
Bit 15	R/W	INTE[4]	0
Bit 14	R	Reserved	X
Bit 13	R	TAPII[4]	X
Bit 12	R	APRGMI[4]	X
Bit 11	R	TSVCAI[4]	X
Bit 10	R	Reserved	X
Bit 9	R	DPRGMI[4]	X
Bit 8	R	SARCI[4]	X
Bit 7	R	RSVCAI[4]	X
Bit 6	R	PATHTU3RTTPI[4]	X
Bit 5	R	TU3RHPPI[4]	X
Bit 4	R	PATHRTTPI[4]	X
Bit 3	R	RHPPI[4]	X
Bit 2	R	SBERI[4]	X
Bit 1	R	RTTPI[4]	X
Bit 0	R	RRMPI[4]	X

The Interrupt Status Register is provided at SP2488 r/w address 13H.

RRMPI[4] to TAPII[4]

The RRMPI[4] to TAPII[4] are interrupt status indicators for the corresponding block. The interrupt status is set to logic 1 to indicate a pending interrupt from the corresponding block. The interrupt status bits are independent of the interrupt enable bit.

INTE[4]

The interrupt enable (INTE[4]) bit controls the activation of the interrupt (INT) output. When a logic 1 is written to INTE[4], the RRMP[4] to TAPII[4] pending interrupt will assert the interrupt (INT) output. When a logic 0 is written to INTE[4], the RRMP[4] to TAPII[4] pending interrupt will not assert the interrupt (INT) output.

Register 0014H: SP2488 Drop System Configuration

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14	R/W	DFPEN	0
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9		Unused	
Bit 8		Unused	
Bit 7		Unused	
Bit 6		Unused	
Bit 5		Unused	
Bit 4		Unused	
Bit 3	R/W	DJ0J1PAREN	0
Bit 2	R/W	DPLPAREN	0
Bit 1	R/W	D32PAREN	0
Bit 0	R/W	DODDPAREN	0

The Drop Side Configuration Register is provided at SP2488 r/w address 14H.

DODDPAREN

The drop bus odd parity enable (DODDPAREN) bit selects the parity of the drop bus. When a logic 1 is written to DODDPAREN, the parity of the drop bus is ODD. When a logic 0 is written to DODDPAREN, the parity of the drop bus is even.

D32PAREN

The drop bus 32 bits parity enable (D32PAREN) bit selects between an independent parity for each drop bus or a combine parity for the four drop bus. When a logic 1 is written to D32PAREN, DP1 contains a parity calculated over the four drop bus (DP2-4 are set to zero). When a logic 0 is written to D32PAREN, DP1-4 contain a parity calculated over the individual drop bus.

DPLPAREN

The drop bus payload indication parity enable (DPLPAREN) bit selects if the payload indication is included or not in the parity calculation. When a logic 1 is written to DPLPAREN, DPL is included in the parity calculation. When a logic 0 is written to DPLPAREN, DPL is not included in the parity calculation.

DJ0J1PAREN

The drop bus J0J1 indication parity enable (DJ0J1PAREN) bit selects if the J0J1 indication is included or not in the parity calculation. When a logic 1 is written to DJ0J1PAREN, DJ0J1 is included in the parity calculation. When a logic 0 is written to DJ0J1PAREN, DJ0J1 is not included in the parity calculation.

DFPEN

The drop bus frame pulse enable (DFPEN) bit selects if the DJ0REF input is asserted to force the J0 byte on the drop bus or to force the payload byte following the J0/Z0 bytes on the drop bus. When a logic 1 is written to DFPEN, DJ0REF is asserted to force the payload byte following the J0/Z0 byte on the drop bus. When a logic 0 is written to DFPEN, DJ0REF is asserted to force the J0 bytes on the drop bus.

Register 0016H: SP2488 Add System Configuration

Bit	Type	Function	Default
Bit 15	R/W	Reserved	0
Bit 14	R/W	AFPEN	0
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9		Unused	
Bit 8		Unused	
Bit 7	R/W	APARERRE[4]	0
Bit 6	R/W	APARERRE[3]	0
Bit 5	R/W	APARERRE[2]	0
Bit 4	R/W	APARERRE[1]	0
Bit 3	R/W	AJ0J1PAREN	0
Bit 2	R/W	APLPAREN	0
Bit 1	R/W	A32PAREN	0
Bit 0	R/W	AODDPAREN	0

The Add System Configuration Register is provided at SP2488 r/w address 16H.

AODDPAREN

The add bus odd parity enable (AODDPAREN) bit selects the parity of the add bus. When a logic 1 is written to AODDPAREN, the parity of the drop bus is ODD. When a logic 0 is written to AODDPAREN, the parity of the drop bus is even.

A32PAREN

The add bus 32 bits parity enable (A32PAREN) bit selects between an independent parity for each add bus or a combine parity for the four add bus. When a logic 1 is written to A32PAREN, AP1 contains a parity calculated over the four add bus (AP2-4 must be set to zero). When a logic 0 is written to A32PAREN, AP1-4 contain a parity calculated over the individual add bus.

APLPAREN

The add bus payload indication parity enable (APLPAREN) bit selects if the payload indication is included or not in the parity calculation. When a logic 1 is written to APLPAREN, APL is included in the parity calculation. When a logic 0 is written to APLPAREN, APL is not included in the parity calculation.

AJ0J1PAREN

The add bus J0J1 indication parity enable (AJ0J1PAREN) bit selects if the J0J1 indication is included or not in the parity calculation. When a logic 1 is written to AJ0J1PAREN, AJ0J1 is included in the parity calculation. When a logic 0 is written to AJ0J1PAREN, AJ0J1 is not included in the parity calculation.

APARERRE[1:4]

The add bus parity error interrupt enable (APARERRE[1:4]) bits control the activation of the interrupt (INT) output for the corresponding add bus. When a logic 1 is written to APARERRE[X], an add bus parity error will assert the interrupt (INT) output. When a logic 0 is written to APARERRE[X], an add bus parity error will not assert the interrupt (INT) output.

AFPEN

The add bus frame pulse enable (AFPEN) bit selects if the AJ0J1_FP input is asserted to indicate the J0 byte on the add bus or to indicate the payload byte following the J0/Z0 bytes on the add bus. When a logic 1 is written to AFPEN, AJ0J1_FP is asserted to indicate the payload byte following the J0/Z0 byte on the add bus. When a logic 0 is written to AFPEN, AJ0J1_FP is asserted to indicate the J0 byte on the add bus.

Register 0017H: SP2488 Add Parity Interrupt Status

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9		Unused	
Bit 8		Unused	
Bit 7		Unused	
Bit 6		Unused	
Bit 5		Unused	
Bit 4		Unused	
Bit 3	R	APARRERRI[4]	X
Bit 2	R	APARRERRI[3]	X
Bit 1	R	APARRERRI[2]	X
Bit 0	R	APARRERRI[1]	X

The Add Parity Interrupt Status Register is provided at SP2488 r/w address 17H.

APARERRI[1:4]

The add bus parity error interrupt status (APARERRI[1:4]) bits are event indicators. APARERRI[X] is set to logic 1 to indicate any add bus parity error in the corresponding add bus. The interrupt status bits are independent of the interrupt enable bits. APARERR[X] is cleared when the add parity interrupt status register is read.

Register 0018H: SP2488 System Activity Monitor

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13	R	DCKACT	X
Bit 12	R	ACKACT	X
Bit 11	R	AJ0J1ACT[4]	X
Bit 10	R	APLDACT [4]	X
Bit 9	R	ADATAACT [4]	X
Bit 8	R	AJ0J1ACT [3]	X
Bit 7	R	APLDACT [3]	X
Bit 6	R	ADATAACT [3]	X
Bit 5	R	AJ0J1ACT [2]	X
Bit 4	R	APLDACT [2]	X
Bit 3	R	ADATAACT [2]	X
Bit 2	R	AJ0J1ACT [1]	X
Bit 1	R	APLDACT [1]	X
Bit 0	R	ADATAACT [1]	X

The System Activity Monitor is provided at SP2488 r/w address 18H.

ADATAACT[1:4]

The add data activity monitor (ADATAACT[1:4]) signals are event detectors. ADATAACT[X] is asserted when a low to high transition occurs on the add data bus of slice X. ADATAACT[X] is cleared when the system activity monitor register is read.

APLDACT[1:4]

The add payload activity monitor (APLDACT[1:4]) signals are event detectors. APLDACT[X] is asserted when a low to high transition occurs on the add payload indication of slice X. APLDACT[X] is cleared when the system activity monitor register is read.

AJ0J1ACT[1:4]

The add J0J1 activity monitor (AJ0J1ACT[1:4]) signals are event detectors. AJ0J1ACT[X] is asserted when a low to high transition occurs on the add J0J1 indication of slice X. AJ0J1ACT[X] is cleared when the system activity monitor register is read.

ACKACT

The add system clock activity monitor (ACKACT) signal is an event detector. ACKACT is asserted when a low to high transition occurs on the add system clock. ACKACT is cleared when the system activity monitor register is read.

DCKACT

The drop system clock activity monitor (DCKACT) signal is an event detector. DCKACT is asserted when a low to high transition occurs on the drop system clock. DCKACT is cleared when the system activity monitor register is read.

Register 0019H: SP2488 TAPI Path AIS Configuration

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9		Unused	
Bit 8		Unused	
Bit 7		Unused	
Bit 6		Unused	
Bit 5		Unused	
Bit 4		Unused	
Bit 3	R/W	PAISPTRCFG[1]	0
Bit 2	R/W	PAISPTRCFG[0]	0
Bit 1	R/W	PLOPTRCFG[1]	0
Bit 0	R/W	PLOPTRCFG [0]	0

The TAPI Path AIS Configuration is provided at SP2488 r/w address 19H.

PLOPTRCFG[1:0]

The path loss of pointer configuration (PLOPTRCFG[1:0]) bits define the LOP-P defect. When PLOPTRCFG[1:0] is set to 00b, an LOP-P defect is declared when the pointer is in the LOP state and an LOP-P defect is removed when the pointer is not in the LOP state. When PLOPTRCFG[1:0] is set to 01b, an LOP-P defect is declared when the pointer or any of the concatenated pointers is in the LOP state and an LOP-P defect is removed when the pointer and all the concatenation pointers are not in the LOP state. When PLOPTRCFG[1:0] is set to 10b, an LOP-P defect is declared when the pointer or any of the concatenated pointers is in the LOP state or in the AIS state and an LOP-P defect is removed when the pointer and all the concatenation pointers are not in the LOP state or in the AIS state.

PAISPTRCFG[1:0]

The path AIS pointer configuration (PAISPTRCFG[1:0]) bits define the AIS-P defect. When PAISPTRCFG[1:0] is set to 00b, an AIS-P defect is declared when the pointer is in the AIS state and an AIS-P defect is removed when the pointer is not in the AIS state. When PAISPTRCFG[1:0] is set to 01b, an AIS-P defect is declared when the pointer or any of the concatenated pointers is in the AIS state and an AIS-P defect is removed when the pointer and all the concatenation pointers are not in the AIS state. When PAISPTRCFG[1:0] is set to 10b, an AIS-P defect is declared when the pointer and all the concatenated pointers are in the AIS state and an AIS-P defect is removed when the pointer or any of the concatenation pointers is not in the AIS state.

Register 001AH: SP2488 JTAG ID (MSB)

Bit	Type	Function	Default
Bit 15	R	JTAGID[31]	0
Bit 14	R	JTAGID[30]	0
Bit 13	R	JTAGID[29]	0
Bit 12	R	JTAGID[28]	1
Bit 11	R	JTAGID[27]	0
Bit 10	R	JTAGID[26]	1
Bit 9	R	JTAGID[25]	0
Bit 8	R	JTAGID[24]	1
Bit 7	R	JTAGID[23]	0
Bit 6	R	JTAGID[22]	0
Bit 5	R	JTAGID[21]	1
Bit 4	R	JTAGID[20]	1
Bit 3	R	JTAGID[19]	0
Bit 2	R	JTAGID[18]	0
Bit 1	R	JTAGID[17]	0
Bit 0	R	JTAGID[16]	1

The JTAG ID (MSB) is provided at SP2488 r/w address 1AH.

JTAGID[31:28] / VERSION[3:0]

The JTAGID[31:28] / VERSION[3:0] bits report the revision of the SPECTRA-2488 silicon.

JTAGID[27:16] / PART_NUMBER[15:4]

The JTAGID[27:16] / PART_NUMBER[15:4] bits represent the 12 most significant bits of the part number of the SPECTRA-2488 device.

Register 001BH: SP2488 JTAG ID (LSB)

Bit	Type	Function	Default
Bit 15	R	JTAGID[15]	0
Bit 14	R	JTAGID[14]	1
Bit 13	R	JTAGID[13]	0
Bit 12	R	JTAGID[12]	1
Bit 11	R	JTAGID[11]	0
Bit 10	R	JTAGID[10]	0
Bit 9	R	JTAGID[9]	0
Bit 8	R	JTAGID[8]	0
Bit 7	R	JTAGID[7]	1
Bit 6	R	JTAGID[6]	1
Bit 5	R	JTAGID[5]	0
Bit 4	R	JTAGID[4]	0
Bit 3	R	JTAGID[3]	1
Bit 2	R	JTAGID[2]	1
Bit 1	R	JTAGID[1]	0
Bit 0	R	JTAGID[0]	1

The JTAG ID (LSB) is provided at SP2488 r/w address 1BH.

JTAGID[15:12] / PART_NUMBER[3:0]

The JTAGID[15:12] / PART_NUMBER[3:0] bits represent the 3 least significant bits of the part number of the SPECTRA-2488 device.

JTAGID[11:1] / MANUFACTURER_ID[10:0]

The JTAGID[11:1] / MANUFACTURER_ID[10:0] bits represent the 11 bit manufacturer's code assigned to PMC-Sierra, Inc. for inclusion in the JTAG Boundary Scan Identification Code.

Register 001DH: SP2488 Misc Config

Bit	Type	Function	Default
Bit 15	R/W	AFPMASK	0
Bit 14	R/W	Reserved	0
Bit 13	R/W	Reserved	0
Bit 12	R/W	Reserved	0
Bit 11	R/W	Reserved	0
Bit 10	R/W	Reserved	0
Bit 9	R/W	Reserved	0
Bit 8	R/W	Reserved	0
Bit 7	R/W	Reserved	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	Reserved	0

The Misc Config Register is provided at SP2488 r/w address 1DH.

AFPMASK

The Add Frame Pulse Mask (AFPMASK) bit defines the behavior of the AJ0J1_FP[1:4] input pin. When a logic 1 is written to AFPMASK, AJ0J1_FP[1:4] input pin is not resetting the frame counter. When a logic 0 is written to AFPMASK, AJ0J1_FP[1:4] input pin resets the frame counter. AFPEN must be set to logic 1 for AFPMASK to mask AJ0J1_FP[1:4].

Bit	Type	Function	Default
Bit 15	R/W	TTLIENB	0
Bit 14	R/W	TTLOENB	0
Bit 13	R/W	QUAD622ENB	0
Bit 12	R/W	Unused	0
Bit 11	R/W	Unused	0
Bit 10	R/W	Unused	0
Bit 9	R/W	Unused	0
Bit 8	R/W	Unused	0
Bit 7	R/W	Unused	0
Bit 6	R/W	TCSRCEN	1
Bit 5	R/W	RXPECLMODE0	1
Bit 4	R/W	RXPECLIDDQ	0
Bit 3	R/W	RXPECLENB	0
Bit 2	R/W	TXPECLMODE0	1
Bit 1	R/W	TXPECLMODE1	0
Bit 0	R/W	TXPECLENB	0

Register 001FH: SP2488 FREE Registers

Bit	Type	Function	Default
Bit 15	R/W	FREE[15]	0
Bit 14	R/W	FREE[14]	0
Bit 13	R/W	FREE[13]	0
Bit 12	R/W	FREE[12]	0
Bit 11	R/W	FREE[11]	0
Bit 10	R/W	FREE[10]	0
Bit 9	R/W	FREE[9]	0
Bit 8	R/W	FREE[8]	0
Bit 7	R/W	FREE[7]	0
Bit 6	R/W	FREE[6]	0
Bit 5	R/W	FREE[5]	0
Bit 4	R/W	FREE[4]	0
Bit 3	R/W	FREE[3]	0
Bit 2	R/W	FREE[2]	0
Bit 1	R/W	FREE[1]	0
Bit 0	R/W	FREE[0]	0

The Free Register is provided at SP2488 r/w address 1FH.

FREE[15:0]

The free registers (FREE[15:0]) bits can be used as scratch registers by the external micro processor.

Register 0040H: SRLI Clock Configuration

Bit	Type	Function	Default
Bit 15	R/W	ROTATEEN	1
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9	R/W	DISFRM4	0
Bit 8	R/W	DISFRM3	0
Bit 7	R/W	DISFRM2	0
Bit 6	R/W	DISFRM1	0
Bit 5	R/W	DISFRM	0
Bit 4	R/W	RCLK4EN	0
Bit 3	R/W	RCLK3EN	0
Bit 2	R/W	RCLK2EN	0
Bit 1	R/W	RCLK1EN	0
Bit 0		Unused	

The Clock Configuration Register is provided at SRLI r/w address 00H.

RCLK1EN

The receive clock enable (RCLK1EN) bit controls the gating of the RCLK1 output clock. When RCLK1EN is set to logic 1, the RCLK1 output clock operates normally. When RCLK1EN is set to logic 0, the RCLK1 output clock is held low.

RCLK2EN

The receive clock enable (RCLK2EN) bit controls the gating of the RCLK2 output clock. When RCLK2EN is set to logic 1, the RCLK2 output clock operates normally. When RCLK2EN is set to logic 0, the RCLK2 output clock is held low.

RCLK3EN

The receive clock enable (RCLK3EN) bit controls the gating of the RCLK3 output clock. When RCLK3EN is set to logic 1, the RCLK3 output clock operates normally. When RCLK3EN is set to logic 0, the RCLK3 output clock is held low.

RCLK4EN

The receive clock enable (RCLK4EN) bit controls the gating of the RCLK4 output clock. When RCLK4EN is set to logic 1, the RCLK4 output clock operates normally. When RCLK4EN is set to logic 0, the RCLK4 output clock is held low.

DISFRM

The disable framing (DISFRM) bit disables the framing algorithm and resets the bit alignment on the RD[15:0] input bus to none. When DISFRM is set to logic 1, the framing algorithm is disable and the bit alignment is reset to none. When DISFRM is set to logic 0, the framing algorithm is enable and the bit alignment is done when out of frame is declared.

DISFRM1

The disable framing (DISFRM1) bit disables the framing algorithm and resets the bit alignment on the RD1[7:0] input bus to none. When DISFRM1 is set to logic 1, the framing algorithm is disable and the bit alignment is reset to none. When DISFRM1 is set to logic 0, the framing algorithm is enable and the bit alignment is done when out of frame is declared.

DISFRM2

The disable framing (DISFRM2) bit disables the framing algorithm and resets the bit alignment on the RD2[7:0] input bus to none. When DISFRM2 is set to logic 1, the framing algorithm is disable and the bit alignment is reset to none. When DISFRM2 is set to logic 0, the framing algorithm is enable and the bit alignment is done when out of frame is declared.

DISFRM3

The disable framing (DISFRM3) bit disables the framing algorithm and resets the bit alignment on the RD3[7:0] input bus to none. When DISFRM3 is set to logic 1, the framing algorithm is disable and the bit alignment is reset to none. When DISFRM3 is set to logic 0, the framing algorithm is enable and the bit alignment is done when out of frame is declared.

DISFRM4

The disable framing (DISFRM4) bit disables the framing algorithm and resets the bit alignment on the RD4[7:0] input bus to none. When DISFRM4 is set to logic 1, the framing algorithm is disable and the bit alignment is reset to none. When DISFRM4 is set to logic 0, the framing algorithm is enable and the bit alignment is done when out of frame is declared.

ROTATEEN

The rotate enable (ROTATEEN) bit controls the line rotation matrix when the SPECTRA-2488 is configured for OC-48 mode. When ROTATEEN is set to logic 1, the rotation matrix is active and the bytes on the RD[15:0] input bus are de-interleaved and distributed to the 4 STS-12 processing slices. When ROTATEEN is set to logic 0, the rotation matrix is inactive and the de-interleaving is expected to have been performed by the SERDES device. Most SERDES devices do not perform byte de-interleaving so ROTATEEN default to logic 1. Check with SERDES functionality to determine correct setting of this bit. This bit is not valid in quad OC-12 mode.

Register 0041H: SRLI PGM Clock Configuration

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9		Unused	
Bit 8		Unused	
Bit 7		Unused	
Bit 6		Unused	
Bit 5		Unused	
Bit 4		Unused	
Bit 3	R/W	PGMRCLKSRC[1]	0
Bit 2	R/W	PGMRCLKSRC[0]	0
Bit 1	R/W	PGMRCLKSEL	0
Bit 0	R/W	PGMRCLKEN	0

The PGM Clock Configuration Register is provided at SRLI r/w address 01H.

PGMRCLKEN

The programmable receive clock enable (PGMRCLKEN) bit controls the gating of the PGMRCLK output clock. When PGMRCLKEN is set to logic one, the PGMRCLK output clock operates normally. When PGMRCLKEN is set to logic zero, the PGMRCLK output clock is held low.

PGMRCLKSEL

The programmable receive clock frequency selection (PGMRCLKSEL) bit selects the frequency of the PGMRCLK output clock. When PGMRCLKSEL is set high, PGMRCLK is a nominal 8 KHz clock. When PGMRCLKSEL is set to logic zero, PGMRCLK is a nominal 19.44 MHz clock.

PGMRCLKSRC[1:0]

The programmable receive clock source (PGMRCLKSRC[1:0]) bits select the source of the PGMRCLK output clock when the SP2488 is in quad STS-12 (STM-4) mode. When the SP2488 is in STS-48 (STM-16) mode, RDCLK is the source of the PGMRCLK output clock.

PGMRCLKSRC[1:0]	Source
00	RDCLK1
01	RDCLK2
10	RDCLK3
11	RDCLK4

Register 0060H, 0460H, 0860H and 0C60H: SBER Configuration

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9		Unused	
Bit 8		Unused	
Bit 7		Unused	
Bit 6		Unused	
Bit 5	R/W	SFBERTEN	0
Bit 4	R/W	SFSMODE	0
Bit 3	R/W	SFCMODE	0
Bit 2	R/W	SDBERTEN	0
Bit 1	R/W	SDSMODE	0
Bit 0	R/W	SDCMODE	0

The Configuration Register is provided at SBER r/w address 00H.

SDCMODE

The SDCMODE alarm bit selects the Signal Degrade BERM window size to use for clearing alarms. When SDCMODE is a logic 0 the SD BERM will clear an alarm using the same window size used for declaration. When SDCMODE is a logic 1 the SD BERM will clear an alarm using a window size that is 8 times longer than alarm declaration window size. The declaration window size is defined by the SD BERM Accumulation Period register. SFCMODE at logic 1 should be used with extreme caution when using Evaluation Periods equal or near a Bellcore or ITU requirement. Working with 8 times the declaration window size would then cause to fail on the requirements, where clearing time requirements are equal to declare time requirements.

SDSMODE

The SDSMODE bit selects the Signal Degrade BERM saturation mode. When SDSMODE is a logic 0 the SD BERM will saturate the BIP count on a per frame basis using the SD Saturation Threshold register value. When SDSMODE is a logic 1 the SD BERM will saturate the BIP count on a per window subtotals accumulation period basis using the SD Saturation Threshold register value.

SDBERTEN

The SDBERTEN bit enables automatic monitoring of line bit error rate threshold events by the Signal Degrade BERM. When SDBERTEN is a logic one, the SD BERM continuously monitors line BIP errors over a period defined in the BERM configuration registers. When SDBERTEN is a logic zero, the SD BERM BIP accumulation logic is disabled, and the BERM logic is reset to restart in the declaration monitoring state. All SD BERM configuration registers should be set up before the monitoring is enabled.

SFCMODE

The SFCMODE alarm bit selects the Signal Failure BERM window size to use for clearing alarms. When SFCMODE is a logic 0 the SF BERM will clear an alarm using the same window size used for declaration. When SFCMODE is a logic 1 the SF BERM will clear an alarm using a window size that is 8 times longer than alarm declaration window size. The declaration window size is defined by the SF BERM Accumulation Period register. SFCMODE at logic 1 should be used with extreme caution when using Evaluation Periods equal or near a Bellcore or ITU requirement. Working with 8 times the declaration window size would then cause to fail on the requirements, where clearing time requirements are equal to declare time requirements.

SFSMODE

The SFSMODE bit selects the Signal Failure BERM saturation mode. When SFSMODE is a logic 0 the SF BERM will saturate the BIP count on a per frame basis using the SF Saturation Threshold register value. When SFSMODE is a logic 1 the SF BERM will saturate the BIP count on a per window subtotals accumulation period basis using the SF Saturation Threshold register value.

SFBERTEN

The SFBERTEN bit enables automatic monitoring of line bit error rate threshold events by the Signal Failure BERM. When SFBERTEN is a logic one, the SF BERM continuously monitors line BIP errors over a period defined in the BERM configuration registers. When SFBERTEN is a logic zero, the SF BERM BIP accumulation logic is disabled, and the BERM logic is reset to restart in the declaration monitoring state. All SF BERM configuration registers should be set up before the monitoring is enabled.

Register 0061H, 0461H, 0861H and 0C61H: SBER Status

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9		Unused	
Bit 8		Unused	
Bit 7		Unused	
Bit 6		Unused	
Bit 5		Unused	
Bit 4		Unused	
Bit 3		Unused	
Bit 2		Unused	
Bit 1	R	SFBERV	X
Bit 0	R	SDBERV	X

The Status Register is provided at SBER r/w address 01H.

SDBERV

The SDBERV bit indicates the Signal Degrade BERM alarm state. The alarm is declared (SDBERV is a logic one) when the declaring threshold has been exceeded. The alarm is removed (SDBERV is a logic zero) when the clearing threshold has been reached.

SFBERV

The SFBERV bit indicates the Signal Failure BERM alarm state. The alarm is declared (SFBERV is a logic one) when the declaring threshold has been exceeded. The alarm is removed (SFBERV is a logic zero) when the clearing threshold has been reached.

Register 0062H, 0462H, 0862H and 0C62H: SBER Interrupt Enable

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9		Unused	
Bit 8		Unused	
Bit 7		Unused	
Bit 6		Unused	
Bit 5		Unused	
Bit 4		Unused	
Bit 3		Unused	
Bit 2		Unused	
Bit 1	R/W	SFBERE	0
Bit 0	R/W	SDBERE	0

The Interrupt Enable Register is provided at SBER r/w address 02H.

SDBERE

The SDBERE bit is the interrupt enable for the SDBER alarm. When SDBERE is set to logic 1, the pending interrupt in the Interrupt Status Register, SDBERI, will assert the interrupt output. When SDBERE is set to logic 0, the pending interrupt will not assert the interrupt output.

SFBERE

The SFBERE bit is the interrupt enable for the SFBER alarm. When SFBERE is set to logic 1, the pending interrupt in the Interrupt Status Register, SFBERI, will assert the interrupt output. When SFBERE is set to logic 0, the pending interrupt will not assert the interrupt output.

Register 0063H, 0463H, 0863H and 0C63H: SBER Interrupt Status

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9		Unused	
Bit 8		Unused	
Bit 7		Unused	
Bit 6		Unused	
Bit 5		Unused	
Bit 4		Unused	
Bit 3		Unused	
Bit 2		Unused	
Bit 1	R	SFBERI	X
Bit 0	R	SDBERI	X

The Interrupt Status Register is provided at SBER r/w address 03H.

SDBERI

The SDBERI bit is an event indicator set to logic 1 to indicate any changes in the status of SDBERV. This interrupt status bit is independent of the SDBERE interrupt enable bit. When WCIMODE is low (read mode), SDBERI is cleared by reading the interrupt status register. When WCIMODE is high (write mode), SDBERI is cleared by writing a high value to bit 1 of the interrupt status register.

SFBERI

The SFBERI bit is an event indicator set to logic 1 to indicate any changes in the status of SFBERV. This interrupt status bit is independent of the SFBERE interrupt enable bit. When WCIMODE is low (read mode), SFBERI is cleared by reading the interrupt status register. When WCIMODE is high (write mode), SFBERI is cleared by writing a high value to bit 0 of the interrupt status register.

Register 0064H, 0464H, 0864H and 0C64H: SBER SF BERM Accumulation Period (LSB)

Bit	Type	Function	Default
Bit 15	R/W	SFSAP[15]	0
Bit 14	R/W	SFSAP[14]	0
Bit 13	R/W	SFSAP[13]	0
Bit 12	R/W	SFSAP[12]	0
Bit 11	R/W	SFSAP[11]	0
Bit 10	R/W	SFSAP[10]	0
Bit 9	R/W	SFSAP[9]	0
Bit 8	R/W	SFSAP[8]	0
Bit 7	R/W	SFSAP[7]	0
Bit 6	R/W	SFSAP[6]	0
Bit 5	R/W	SFSAP[5]	0
Bit 4	R/W	SFSAP[4]	0
Bit 3	R/W	SFSAP[3]	0
Bit 2	R/W	SFSAP[2]	0
Bit 1	R/W	SFSAP[1]	0
Bit 0	R/W	SFSAP[0]	0

This register is provided at SBER r/w address 04H.

Register 0065H, 0465H, 0865H and 0C65H: SBER SF BERM Accumulation Period (MSB)

Bit	Type	Function	Default
Bit 15	R/W	SFSAP[31]	0
Bit 14	R/W	SFSAP[30]	0
Bit 13	R/W	SFSAP[29]	0
Bit 12	R/W	SFSAP[28]	0
Bit 11	R/W	SFSAP[27]	0
Bit 10	R/W	SFSAP[26]	0
Bit 9	R/W	SFSAP[25]	0
Bit 8	R/W	SFSAP[24]	0
Bit 7	R/W	SFSAP[23]	0
Bit 6	R/W	SFSAP[22]	0
Bit 5	R/W	SFSAP[21]	0
Bit 4	R/W	SFSAP[20]	0
Bit 3	R/W	SFSAP[19]	0
Bit 2	R/W	SFSAP[18]	0
Bit 1	R/W	SFSAP[17]	0
Bit 0	R/W	SFSAP[16]	0

This register is provided at SBER r/w address 05H.

SFSAP[31:0]

The SFSAP[31:0] bits represent the number of STS-N frames to be used to accumulate a BIP error subtotal. The total evaluation window to declare an alarm is broken into 8 subtotals, so this register value represents 1/8 of the total sliding window size. **Refer to the Operations section for the recommended settings.**

Register 0066H, 0466H, 0866H and 0C66H: SBER SF BERM Saturation Threshold (LSB)

Bit	Type	Function	Default
Bit 15	R/W	SFSATH[15]	1
Bit 14	R/W	SFSATH[14]	1
Bit 13	R/W	SFSATH[13]	1
Bit 12	R/W	SFSATH[12]	1
Bit 11	R/W	SFSATH[11]	1
Bit 10	R/W	SFSATH[10]	1
Bit 9	R/W	SFSATH[9]	1
Bit 8	R/W	SFSATH[8]	1
Bit 7	R/W	SFSATH[7]	1
Bit 6	R/W	SFSATH[6]	1
Bit 5	R/W	SFSATH[5]	1
Bit 4	R/W	SFSATH[4]	1
Bit 3	R/W	SFSATH[3]	1
Bit 2	R/W	SFSATH[2]	1
Bit 1	R/W	SFSATH[1]	1
Bit 0	R/W	SFSATH[0]	1

This register is provided at SBER r/w address 06H.

Register 0067H, 0467H, 0867H and 0C67H: SBER SF BERM Saturation Threshold (MSB)

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9		Unused	
Bit 8		Unused	
Bit 7	R/W	SFSATH[23]	1
Bit 6	R/W	SFSATH[22]	1
Bit 5	R/W	SFSATH[21]	1
Bit 4	R/W	SFSATH[20]	1
Bit 3	R/W	SFSATH[19]	1
Bit 2	R/W	SFSATH[18]	1
Bit 1	R/W	SFSATH[17]	1
Bit 0	R/W	SFSATH[16]	1

This register is provided at SBER r/w address 07H.

SFSATH[23:0]

The SFSATH[23:0] bits represent the allowable number of BIP errors that can be accumulated either during a frame period or during a complete sub accumulation period (depending on SFSMODE) before the error count is saturated to this threshold value. Setting this threshold to 0xFFFFFF disables the saturation functionality.

Register 0068H, 0468H, 0868H and 0C68H: SBER SF BERM Declaration Threshold (LSB)

Bit	Type	Function	Default
Bit 15	R/W	SFDECTH[15]	0
Bit 14	R/W	SFDECTH[14]	0
Bit 13	R/W	SFDECTH[13]	0
Bit 12	R/W	SFDECTH[12]	0
Bit 11	R/W	SFDECTH[11]	0
Bit 10	R/W	SFDECTH[10]	0
Bit 9	R/W	SFDECTH[9]	0
Bit 8	R/W	SFDECTH[8]	0
Bit 7	R/W	SFDECTH[7]	0
Bit 6	R/W	SFDECTH[6]	0
Bit 5	R/W	SFDECTH[5]	0
Bit 4	R/W	SFDECTH[4]	0
Bit 3	R/W	SFDECTH[3]	0
Bit 2	R/W	SFDECTH[2]	0
Bit 1	R/W	SFDECTH[1]	0
Bit 0	R/W	SFDECTH[0]	0

This register is provided at SBER r/w address 08H.

Register 0069H, 0469H, 0869H and 0C69H: SBER SF BERM Declaration Threshold (MSB)

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9		Unused	
Bit 8		Unused	
Bit 7	R/W	SFDECTH[23]	0
Bit 6	R/W	SFDECTH[22]	0
Bit 5	R/W	SFDECTH[21]	0
Bit 4	R/W	SFDECTH[20]	0
Bit 3	R/W	SFDECTH[19]	0
Bit 2	R/W	SFDECTH[18]	0
Bit 1	R/W	SFDECTH[17]	0
Bit 0	R/W	SFDECTH[16]	0

This register is provided at SBER r/w address 09H.

SFDECTH[23:0]

The SFDECTH[23:0] register represent the number of BIP errors that must be accumulated during a full evaluation window in order to declare a BER alarm. **Refer to the Operations section for the recommended settings.**

Register 006AH, 046AH, 086AH and 0C6AH: SBER SF BERM Clearing Threshold (LSB)

Bit	Type	Function	Default
Bit 15	R/W	SFCLRTH[15]	0
Bit 14	R/W	SFCLRTH[14]	0
Bit 13	R/W	SFCLRTH[13]	0
Bit 12	R/W	SFCLRTH[12]	0
Bit 11	R/W	SFCLRTH[11]	0
Bit 10	R/W	SFCLRTH[10]	0
Bit 9	R/W	SFCLRTH[9]	0
Bit 8	R/W	SFCLRTH[8]	0
Bit 7	R/W	SFCLRTH[7]	0
Bit 6	R/W	SFCLRTH[6]	0
Bit 5	R/W	SFCLRTH[5]	0
Bit 4	R/W	SFCLRTH[4]	0
Bit 3	R/W	SFCLRTH[3]	0
Bit 2	R/W	SFCLRTH[2]	0
Bit 1	R/W	SFCLRTH[1]	0
Bit 0	R/W	SFCLRTH[0]	0

This register is provided at SBER r/w address 0AH.

Register 006BH, 046BH, 086BH and 0C6BH: SBER SF BERM Clearing Threshold (MSB)

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9		Unused	
Bit 8		Unused	
Bit 7	R/W	SFCLRTH[23]	0
Bit 6	R/W	SFCLRTH[22]	0
Bit 5	R/W	SFCLRTH[21]	0
Bit 4	R/W	SFCLRTH[20]	0
Bit 3	R/W	SFCLRTH[19]	0
Bit 2	R/W	SFCLRTH[18]	0
Bit 1	R/W	SFCLRTH[17]	0
Bit 0	R/W	SFCLRTH[16]	0

This register is provided at SBER r/w address 0BH.

SFCLRTH[23:0]

The SFCLRTH[23:0] register represent the number of BIP errors that can be accumulated but not exceeded during a full evaluation window in order to clear a BER alarm. **Refer to the Operations section for the recommended settings.**

Register 006CH, 046CH, 086CH and 0C6CH: SBER SD BERM Accumulation Period (LSB)

Bit	Type	Function	Default
Bit 15	R/W	SDSAP[15]	0
Bit 14	R/W	SDSAP[14]	0
Bit 13	R/W	SDSAP[13]	0
Bit 12	R/W	SDSAP[12]	0
Bit 11	R/W	SDSAP[11]	0
Bit 10	R/W	SDSAP[10]	0
Bit 9	R/W	SDSAP[9]	0
Bit 8	R/W	SDSAP[8]	0
Bit 7	R/W	SDSAP[7]	0
Bit 6	R/W	SDSAP[6]	0
Bit 5	R/W	SDSAP[5]	0
Bit 4	R/W	SDSAP[4]	0
Bit 3	R/W	SDSAP[3]	0
Bit 2	R/W	SDSAP[2]	0
Bit 1	R/W	SDSAP[1]	0
Bit 0	R/W	SDSAP[0]	0

This register is provided at SBER r/w address 0CH.

Register 006DH, 046DH, 086DH and 0C6DH: SBER SD BERM Accumulation Period (MSB)

Bit	Type	Function	Default
Bit 15	R/W	SDSAP[31]	0
Bit 14	R/W	SDSAP[30]	0
Bit 13	R/W	SDSAP[29]	0
Bit 12	R/W	SDSAP[28]	0
Bit 11	R/W	SDSAP[27]	0
Bit 10	R/W	SDSAP[26]	0
Bit 9	R/W	SDSAP[25]	0
Bit 8	R/W	SDSAP[24]	0
Bit 7	R/W	SDSAP[23]	0
Bit 6	R/W	SDSAP[22]	0
Bit 5	R/W	SDSAP[21]	0
Bit 4	R/W	SDSAP[20]	0
Bit 3	R/W	SDSAP[19]	0
Bit 2	R/W	SDSAP[18]	0
Bit 1	R/W	SDSAP[17]	0
Bit 0	R/W	SDSAP[16]	0

This register is provided at SBER r/w address 0DH.

SDSAP[31:0]

The SDSAP[31:0] bits represent the number of STS-N frames to be used to accumulate a BIP error subtotal. The total evaluation window to declare an alarm is broken into 8 subtotals, so this register value represents 1/8 of the total sliding window size. **Refer to the Operations section for the recommended settings.**

Register 006EH, 046EH, 086EH and 0C6EH: SBER SD BERM Saturation Threshold (LSB)

Bit	Type	Function	Default
Bit 15	R/W	SDSATH[15]	1
Bit 14	R/W	SDSATH[14]	1
Bit 13	R/W	SDSATH[13]	1
Bit 12	R/W	SDSATH[12]	1
Bit 11	R/W	SDSATH[11]	1
Bit 10	R/W	SDSATH[10]	1
Bit 9	R/W	SDSATH[9]	1
Bit 8	R/W	SDSATH[8]	1
Bit 7	R/W	SDSATH[7]	1
Bit 6	R/W	SDSATH[6]	1
Bit 5	R/W	SDSATH[5]	1
Bit 4	R/W	SDSATH[4]	1
Bit 3	R/W	SDSATH[3]	1
Bit 2	R/W	SDSATH[2]	1
Bit 1	R/W	SDSATH[1]	1
Bit 0	R/W	SDSATH[0]	1

This register is provided at SBER r/w address 0EH.

Register 006FH, 046FH, 086FH and 0C6FH: SBER SD BERM Saturation Threshold (MSB)

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9		Unused	
Bit 8		Unused	
Bit 7	R/W	SDSATH[23]	1
Bit 6	R/W	SDSATH[22]	1
Bit 5	R/W	SDSATH[21]	1
Bit 4	R/W	SDSATH[20]	1
Bit 3	R/W	SDSATH[19]	1
Bit 2	R/W	SDSATH[18]	1
Bit 1	R/W	SDSATH[17]	1
Bit 0	R/W	SDSATH[16]	1

This register is provided at SBER r/w address 0FH.

SDSATH[23:0]

The SDSATH[23:0] bits represent the allowable number of BIP errors that can be accumulated either during a frame period or during a complete sub accumulation period (depending on SDSMODE) before the error count is saturated to this threshold value. Setting this threshold to 0xFFFFFF disables the saturation functionality.

Register 0070H, 0470H, 0870H and 0C70H: SBER SD BERM Declaration Threshold (LSB)

Bit	Type	Function	Default
Bit 15	R/W	SDDECTH[15]	0
Bit 14	R/W	SDDECTH[14]	0
Bit 13	R/W	SDDECTH[13]	0
Bit 12	R/W	SDDECTH[12]	0
Bit 11	R/W	SDDECTH[11]	0
Bit 10	R/W	SDDECTH[10]	0
Bit 9	R/W	SDDECTH[9]	0
Bit 8	R/W	SDDECTH[8]	0
Bit 7	R/W	SDDECTH[7]	0
Bit 6	R/W	SDDECTH[6]	0
Bit 5	R/W	SDDECTH[5]	0
Bit 4	R/W	SDDECTH[4]	0
Bit 3	R/W	SDDECTH[3]	0
Bit 2	R/W	SDDECTH[2]	0
Bit 1	R/W	SDDECTH[1]	0
Bit 0	R/W	SDDECTH[0]	0

This register is provided at SBER r/w address 10H.

Register 0071H, 0471H, 0871H and 0C71H: SBER SD BERM Declaration Threshold (MSB)

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9		Unused	
Bit 8		Unused	
Bit 7	R/W	SDDECTH[23]	0
Bit 6	R/W	SDDECTH[22]	0
Bit 5	R/W	SDDECTH[21]	0
Bit 4	R/W	SDDECTH[20]	0
Bit 3	R/W	SDDECTH[19]	0
Bit 2	R/W	SDDECTH[18]	0
Bit 1	R/W	SDDECTH[17]	0
Bit 0	R/W	SDDECTH[16]	0

This register is provided at SBER r/w address 11H.

SDDECTH[23:0]

The SDDECTH[23:0] register represent the number of BIP errors that must be accumulated during a full evaluation window in order to declare a BER alarm. **Refer to the Operations section for the recommended settings.**

Register 0072H, 0472H, 0872H and 0C72H: SBER SD BERM Clearing Threshold (LSB)

Bit	Type	Function	Default
Bit 15	R/W	SDCLRTH[15]	0
Bit 14	R/W	SDCLRTH[14]	0
Bit 13	R/W	SDCLRTH[13]	0
Bit 12	R/W	SDCLRTH[12]	0
Bit 11	R/W	SDCLRTH[11]	0
Bit 10	R/W	SDCLRTH[10]	0
Bit 9	R/W	SDCLRTH[9]	0
Bit 8	R/W	SDCLRTH[8]	0
Bit 7	R/W	SDCLRTH[7]	0
Bit 6	R/W	SDCLRTH[6]	0
Bit 5	R/W	SDCLRTH[5]	0
Bit 4	R/W	SDCLRTH[4]	0
Bit 3	R/W	SDCLRTH[3]	0
Bit 2	R/W	SDCLRTH[2]	0
Bit 1	R/W	SDCLRTH[1]	0
Bit 0	R/W	SDCLRTH[0]	0

This register is provided at SBER r/w address 12H.

Register 0073H, 0473H, 0873H and 0C73H: SBER SD BERM Clearing Threshold (MSB)

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9		Unused	
Bit 8		Unused	
Bit 7	R/W	SDCLRTH[23]	0
Bit 6	R/W	SDCLRTH[22]	0
Bit 5	R/W	SDCLRTH[21]	0
Bit 4	R/W	SDCLRTH[20]	0
Bit 3	R/W	SDCLRTH[19]	0
Bit 2	R/W	SDCLRTH[18]	0
Bit 1	R/W	SDCLRTH[17]	0
Bit 0	R/W	SDCLRTH[16]	0

This register is provided at SBER r/w address 13H.

SDCLRTH[23:0]

The SDCLRTH[23:0] register represent the number of BIP errors that can be accumulated but not exceeded during a full evaluation window in order to clear a BER alarm. **Refer to the Operations section for the recommended settings.**

Register 0080H, 0480H, 0880H and 0C80H: RRMP Configuration

Bit	Type	Function	Default
Bit 15	R	Reserved	X
Bit 14		Unused	
Bit 13	R/W	Reserved	0
Bit 12	R/W	LREIACCBLK	0
Bit 11	R/W	LBIPEREIBLK	0
Bit 10	R/W	LBIPEBERBLK	0
Bit 9	R/W	LBIPEACCBLK	0
Bit 8	R/W	Reserved	0
Bit 7	R/W	SBIPEACCBLK	0
Bit 6	R/W	RLDTS	1
Bit 5	R/W	RSLDSEL	0
Bit 4	R/W	RSLDTS	1
Bit 3	R/W	LRDI3	0
Bit 2	R/W	LAIS3	0
Bit 1	R/W	ALGO2	0
Bit 0	W	FOOF	X

The Configuration Register is provided at RRMP r/w address 00H.

FOOF

The force out of frame (FOOF) bit forces out of frame condition. When a logic 1 is written to FOOF, the framer block is forced out of frame at the next frame boundary regardless of the framing pattern value. The OOF event initiates re framing in an upstream frame detector.

ALGO2

The ALGO2 bit selects the framing pattern used to determine and maintain the frame alignment. When ALGO2 is set to logic 1, the framing pattern consist of the 8 bits of the first A1 framing bytes and the first 4 bits of the last A2 framing bytes (12 bits total). When ALGO2 is set to logic 0, the framing patterns consist of all the A1 framing bytes and all the A2 framing bytes.

LAIS3

The line alarm indication signal detection (LAIS3) bit selects the Line AIS detection algorithm. When LAIS3 is set to logic 1, Line AIS is declared when a 111 pattern is detected in bits 6,7,8 of the K2 byte for three consecutive frames. When LAIS3 is set to logic 0, Line AIS is declared when a 111 pattern is detected in bits 6,7,8 of the K2 byte for five consecutive frames.

LRDI3

The line remote defect indication detection (LRDI3) bit selects the Line RDI detection algorithm. When LRDI3 is set to logic 1, Line RDI is declared when a 110 pattern is detected in bits 6,7,8 of the K2 byte for three consecutive frames. When LRDI3 is set to logic 0, Line RDI is declared when a 110 pattern is detected in bits 6,7,8 of the K2 byte for five consecutive frames.

RSLDTS

The RSLD tri-state control (RSLDTS) bit controls the RSLDCLK and RSLD output ports. When RSLDTS is set to logic 1, the RSLDCLK and RSLD output ports are tri-state. When RSLDTS is set to logic 0, the RSLDCLK and RSLD output ports are enable.

RSLDSEL

The receive section line data communication channel select (RSLDSEL) bit selects the contents of the RSLD serial output and the frequency of the RSLDCLK clock.

RSLDSEL	Contents	RSLDCLK
0	Section DCC (D1-D3)	Nominal 192 kHz
1	Line DCC (D4-D12)	Nominal 576 kHz

RLDTS

The RLD tri-state control (RLDTS) bit controls the RLDCLK and RLD output ports. When RLDTS is set to logic 1, the RLDCLK and RLD output ports are tri-state. When RLDTS is set to logic 0, the RLDCLK and RLD output ports are enable.

SBIPEACCBLK

The section BIP error accumulation block (SBIPEACCBLK) bit controls the accumulation of section BIP errors. When SBIPEACCBLK is set to logic 1, the section BIP accumulation represents BIP-8 block errors (a maximum of 1 error per frame). When SBIPEACCBLK is set to logic 0, the section BIP accumulation represents BIP-8 errors (a maximum of 8 errors per frame).

LBIPEACCBLK

The line BIP error accumulation block (LBIPEACCBLK) bit controls the accumulation of line BIP errors. When LBIPEACCBLK is set to logic 1, the line BIP accumulation represents BIP-24 block errors (a maximum of 1 error per STS-3/STM-1 per frame). When LBIPEACCBLK is set to logic 0, the line BIP accumulation represents BIP-8 errors (a maximum of 8 errors per STS-1/STM-0 per frame).

LBIPEBERBLK

The line BIP error BER block (LBIPEBERBLK) bit controls the indication of line BIP errors for the BER. When LBIPEBERBLK is set to logic 1, the line BIP represents BIP-24 block errors (a maximum of 1 error per STS-3/STM-1 per frame). When LBIPEBERBLK is set to logic 0, the line BIP represents BIP-8 errors (a maximum of 8 errors per STS-1/STM-0 per frame).

LBIPEREIBLK

The line BIP error REI block (LBIPEREIBLK) bit controls the indication of line BIP errors for the REI. When LBIPEREIBLK is set to logic 1, the line BIP represents BIP-24 block errors (a maximum of 1 error per STS-3/STM-1 per frame saturated to 255). When LBIPEREIBLK is set to logic 0, the line BIP represents BIP-8 errors (a maximum of 8 errors per STS-1/STM-0 per frame saturated to 255).

LREIACCBLK

The line REI accumulation block (LREIACCBLK) bit controls the extraction and accumulation of line REI errors from the M1 byte. When LREIACCBLK is set to logic 1, the extracted line REI are interpreted as block BIP-24 errors (a maximum of 1 error per STS-3/STM-1 per frame). When LREIACCBLK is set to logic 0, the extracted line REI are interpreted as BIP-8 errors (a maximum of 8 errors per STS-1/STM-0 per frame).

Register 0081H, 0481H, 0881H and 0C81H: RRMP Status

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9		Unused	
Bit 8		Unused	
Bit 7		Unused	
Bit 6		Unused	
Bit 5	R	APSBFV	X
Bit 4	R	LRDIV	X
Bit 3	R	LAISV	X
Bit 2	R	LOSV	X
Bit 1	R	LOFV	X
Bit 0	R	OOFV	X

The Status Register is provided at RRMP r/w address 01H.

OOFV

The OOFV bit reflects the current status of the out of frame defect. The OOF defect is declared when four consecutive frames have one or more bit error in their framing pattern. The OOF defect is cleared when two consecutive error free framing pattern are found.

LOFV

The LOFV bit reflects the current status of the loss of frame defect. The LOF defect is declared when an out of frame condition exists for a total period of 3ms during which there is no continuous in frame period of 3ms. The LOF defect is cleared when an in frame condition exists for a continuous period of 3 ms.

LOSV

The LOSV bit reflects the current status of the loss of signal defect. The LOS defect is declared when 20 µs of consecutive all zeros pattern is detected in the receive data stream. The LOS defect is cleared when two consecutive error free framing patterns are found and during the intervening time (one frame) there is no violating period of consecutive all zeros pattern.

LAISV

The LAISV bit reflects the current status of the line alarm indication signal defect. The AIS-L defect is declared when the 111 pattern is detected in bits 6,7 and 8 of the K2 byte for three or five consecutive frames. The AIS-L defect is cleared when any pattern other than 111 is detected in bits 6, 7, and 8 of the K2 byte for three or five consecutive frames.

LRDIV

The LRDIV bit reflects the current status of the line remote defect indication signal defect. The RDI-L defect is declared when the 110 pattern is detected in bits 6, 7, and 8 of the k2 byte for three or five consecutive frames. The RDI-L defect is cleared when any pattern other than 110 is detected in bits 6, 7, and 8 of the K2 byte for three or five consecutive frames.

APSBFV

The APSBF bit reflects the current status of the APS byte failure defect. The APS byte failure defect is declared when no three consecutive identical K1 bytes are received in the last twelve consecutive frames starting with the last frame containing a previously consistent byte. The APS byte failure defect is cleared when three consecutive identical K1 bytes are received.

Register 0082H, 0482H, 0882H and 0C82H: RRMP Interrupt Enable

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10	R/W	LREIEE	0
Bit 9	R/W	LBIPEE	0
Bit 8	R/W	SBIPEE	0
Bit 7	R/W	COSSME	0
Bit 6	R/W	COAPSE	0
Bit 5	R/W	APSBFE	0
Bit 4	R/W	LRDIE	0
Bit 3	R/W	LAISE	0
Bit 2	R/W	LOSE	0
Bit 1	R/W	LOFE	0
Bit 0	R/W	OOFE	0

The Interrupt Enable Register is provided at RRMP r/w address 02H.

OOFE

The out of frame interrupt enable (OOFE) bit controls the activation of the interrupt output. When OOFE is set to logic 1, the OOFI pending interrupt will assert the interrupt output. When OOFE is set to logic 0, the OOFI pending interrupt will not assert the interrupt output.

LOFE

The loss of frame interrupt enable (LOFE) bit controls the activation of the interrupt output. When LOFE is set to logic 1, the LOFI pending interrupt will assert the interrupt output. When LOFE is set to logic 0, the LOFI pending interrupt will not assert the interrupt output.

LOSE

The loss of signal interrupt enable (LOSE) bit controls the activation of the interrupt output. When LOSE is set to logic 1, the LOSI pending interrupt will assert the interrupt output. When LOSE is set to logic 0, the LOSI pending interrupt will not assert the interrupt output.

LAISE

The line alarm indication signal enable (LAISE) bit controls the activation of the interrupt output. When LAISE is set to logic 1, the LAISI pending interrupt will assert the interrupt output. When LAISE is set to logic 0, the LAISI pending interrupt will not assert the interrupt output.

LRDIE

The line remote defect indication interrupt enable (LRDIE) bit controls the activation of the interrupt output. When LRDIE is set to logic 1, the LRDII pending interrupt will assert the interrupt output. When LRDIE is set to logic 0, the LRDII pending interrupt will not assert the interrupt output.

APSBFE

The APS byte failure interrupt enable (APSBFE) bit controls the activation of the interrupt output. When APSBFE is set to logic 1, the APSBFI pending interrupt will assert the interrupt output. When APSBFE is set to logic 0, the APSBFI pending interrupt will not assert the interrupt output.

COAPSE

The change of APS bytes interrupt enable (COAPSE) bit controls the activation of the interrupt output. When COAPSE is set to logic 1, the COAPSI pending interrupt will assert the interrupt output. When COAPSE is set to logic 0, the COAPSI pending interrupt will not assert the interrupt output.

COSSME

The change of SSM message interrupt enable (COSSME) bit controls the activation of the interrupt output. When COSSME is set to logic 1, the COSSMI pending interrupt will assert the interrupt output. When COSSME is set to logic 0, the COSSMI pending interrupt will not assert the interrupt output.

SBIPEE

The section BIP errors interrupt enable (SBIPEE) bit controls the activation of the interrupt output. When SBIPEE is set to logic 1, the SBIPEI pending interrupt will assert the interrupt output. When SBIPEE is set to logic 0, the SBIPEI pending interrupt will not assert the interrupt output.

LBIPEE

The line BIP errors interrupt enable (LBIPEE) bit controls the activation of the interrupt output. When LBIPEE is set to logic 1, the LBIPEI pending interrupt will assert the interrupt output. When LBIPEE is set to logic 0, the LBIPEI pending interrupt will not assert the interrupt output.

LREIEE

The line REI errors interrupt enable (LREIEE) bit controls the activation of the interrupt output. When LREIEE is set to logic 1, the LREIEI pending interrupt will assert the interrupt output. When LREIEE is set to logic 0, the LREIEI pending interrupt will not assert the interrupt output.

Register 0083H, 0483H, 0883H and 0C83H: RRMP Interrupt Status

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10	R	LREIEI	X
Bit 9	R	LBIPEI	X
Bit 8	R	SBIPEI	X
Bit 7	R	COSSMI	X
Bit 6	R	COAPSI	X
Bit 5	R	APSBFI	X
Bit 4	R	LRDII	X
Bit 3	R	LAISI	X
Bit 2	R	LOSI	X
Bit 1	R	LOFI	X
Bit 0	R	OOFI	X

The Interrupt Status Register is provided at RRMP r/w address 03H.

Clear mode of interrupts depends on the WCIMODE mode. When WCIMODE input is logic 0, all the interrupts are cleared when the Interrupt Status Register is read. When WCIMODE input is logic 1, a given interrupt is cleared only if the corresponding bit is logic 1 when the Interrupt Status Register is written.

OOFI

The out of frame interrupt status (OOFI) bit is an event indicator. OOFI is set to logic 1 to indicate any change in the status of OOFV. The interrupt status bit is independent of the interrupt enable bit.

LOFI

The loss of frame interrupt status (LOFI) bit is an event indicator. LOFI is set to logic 1 to indicate any change in the status of LOFV. The interrupt status bit is independent of the interrupt enable bit.

LOSI

The loss of signal interrupt status (LOSI) bit is an event indicator. LOSI is set to logic 1 to indicate any change in the status of LOSV. The interrupt status bit is independent of the interrupt enable bit.

LAISI

The line alarm indication signal interrupt status (LAISI) bit is an event indicator. LAISI is set to logic 1 to indicate any change in the status of LAISV. The interrupt status bit is independent of the interrupt enable bit.

LRDII

The line remote defect indication interrupt status (LRDII) bit is an event indicator. LRDII is set to logic 1 to indicate any change in the status of LRDIV. The interrupt status bit is independent of the interrupt enable bit.

APSBFI

The APS byte failure interrupt status (APSBFI) bit is an event indicator. APSBFI is set to logic 1 to indicate any change in the status of APSBFV. The interrupt status bit is independent of the interrupt enable bit.

COAPSI

The change of APS bytes interrupt status (COAPSI) bit is an event indicator. COAPSI is set to logic 1 to indicate new APS bytes. The interrupt status bit is independent of the interrupt enable bit.

COSSMI

The change of SSM message interrupt status (COSSMI) bit is an event indicator. COSSMI is set to logic 1 to indicate a new SSM message. The interrupt status bit is independent of the interrupt enable bit.

SBIPEI

The section BIP error interrupt status (SBIPEI) bit is an event indicator. SBIPEI is set to logic 1 to indicate a section BIP error. The interrupt status bit is independent of the interrupt enable bit.

LBIPEI

The line BIP error interrupt status (LBIPEI) bit is an event indicator. LBIPEI is set to logic 1 to indicate a line BIP error. The interrupt status bit is independent of the interrupt enable bit.

LREIEI

The line REI error interrupt status (LREIEI) bit is an event indicator. LREIEI is set to logic 1 to indicate a line REI error. The interrupt status bit is independent of the interrupt enable bit.

Register 0084H, 0484H, 0884H and 0C84H: RRMP Receive APS

Bit	Type	Function	Default
Bit 15	R	K1V[7]	X
Bit 14	R	K1V[6]	X
Bit 13	R	K1V[5]	X
Bit 12	R	K1V[4]	X
Bit 11	R	K1V[3]	X
Bit 10	R	K1V[2]	X
Bit 9	R	K1V[1]	X
Bit 8	R	K1V[0]	X
Bit 7	R	K2V[7]	X
Bit 6	R	K2V[6]	X
Bit 5	R	K2V[5]	X
Bit 4	R	K2V[4]	X
Bit 3	R	K2V[3]	X
Bit 2	R	K2V[2]	X
Bit 1	R	K2V[1]	X
Bit 0	R	K2V[0]	X

The Receive APS Register is provided at RRMP r/w address 04H.

K1V[7:0]/K2V[7:0]

The APS K1/K2 bytes value (K1V[7:0]/K2V[7:0]) bits represent the extracted K1/K2 APS bytes. K1V/K2V is updated when the same K1 and K2 bytes (forming a single entity) are received for three consecutive frames.

Register 0085H, 0485H, 0885H and 0C85H: RRMP Receive SSM

Bit	Type	Function	Default
Bit 15	R/W	BYTESSM	0
Bit 14	R/W	FLTRSSM	0
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9		Unused	
Bit 8		Unused	
Bit 7	R	SSMV[7]	X
Bit 6	R	SSMV[6]	X
Bit 5	R	SSMV[5]	X
Bit 4	R	SSMV[4]	X
Bit 3	R	SSMV[3]	X
Bit 2	R	SSMV[2]	X
Bit 1	R	SSMV[1]	X
Bit 0	R	SSMV[0]	X

The Receive SSM Register is provided at RRMP r/w address 05H.

SSMV[7:0]

The synchronization status message value (SSMV[7:0]) bits represent the extracted S1 nibble (or byte). When filtering is enabled via the FLTRSSM register bit, SSMV is updated when the same S1 nibble (or byte) is received for eight consecutive frames. When filtering is disable, SSMV is updated every frame.

FLTRSSM

The filter synchronization status message (FLTRSSM) bit enables the filtering of the SSM nibble (or byte). When FLTRSSM is set to logic 1, the SSM value is updated when the same SSM is received for eight consecutive frames. When FLTRSSM is set to logic 0, the SSM value is updated every frame.

BYTESSM

The byte synchronization status message (BYTESSM) bit is extends the SSM from a nibble to a byte. When BYTESSM is set to logic 1, the SSM is a byte and bit 1 to 8 of the S1 byte are considered. When BYTESSM is set to logic 0, the SSM is a nibble and only bit 5 to 8 of the S1 byte are considered.

Register 0086H, 0486H, 0886H and 0C86H: RRMP AIS Enable

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9		Unused	
Bit 8		Unused	
Bit 7		Unused	
Bit 6		Unused	
Bit 5		Unused	
Bit 4	R/W	K2AIS	0
Bit 3	R/W	RLAISINS	0
Bit 2	R/W	RLAISEN	0
Bit 1	R/W	RLOHAISEN	0
Bit 0	R/W	RSOHAISEN	0

The AIS Enable Register is provided at RRMP read/write address 09H.

RSOHAISEN

The receive section overhead AIS enable (RSOHAISEN) bit enables AIS insertion on RTOH and RSLD when carrying section overhead bytes. When RSOHAISEN is set to logic 1, all ones are forced on the section overhead bytes when AIS-L is declared. When RSOHAISEN is set to logic 0, no AIS are forced on the section overhead bytes regardless of the AIS-L status.

RLOHAISEN

The receive line overhead AIS enable (RLOHAISEN) bit enables AIS insertion on RTOH, RLD and RSLD when carrying line overhead bytes. When RLOHAISEN is set to logic 1, all ones are forced on the line overhead bytes when AIS-L is declared. When RLOHAISEN is set to logic 0, no AIS are forced on the line overhead bytes regardless of the AIS-L status.

RLAISEN

The receive line AIS enable (RLAISEN) bit enables line AIS insertion in the outgoing data stream. When RLAISEN is set to logic 1, line AIS is inserted in the outgoing data stream when AIS-L is declared. When RLAISEN is set to logic 0, no line AIS is inserted regardless of the AIS-L status.

RLAISINS

The receive line AIS insertion (RLAISIN) bit forces line AIS insertion in the outgoing data stream. When RLAISINS is set to logic 1, all ones are inserted in the line overhead bytes and in the payload bytes (all the bytes of the frame except the section overhead bytes) to force a line AIS condition. When RLAISINS is set to logic 0, the line AIS condition is removed.

K2AIS

The K2 line AIS (K2AIS) bit restricts line AIS to the K2 byte. When K2AIS is set to logic 1, line AIS is only inserted in bits 6, 7 and 8 of the K2 byte. When K2AIS is set to logic 0, line AIS is inserted in the line overhead bytes and in the payload bytes (all the bytes of the frame except the section overhead bytes).

Register 0087H, 0487H, 0887H and 0C87H: RRMP Section BIP Error Counter

Bit	Type	Function	Default
Bit 15	R	SBIPE[15]	X
Bit 14	R	SBIPE[14]	X
Bit 13	R	SBIPE[13]	X
Bit 12	R	SBIPE[12]	X
Bit 11	R	SBIPE[11]	X
Bit 10	R	SBIPE[10]	X
Bit 9	R	SBIPE[9]	X
Bit 8	R	SBIPE[8]	X
Bit 7	R	SBIPE[7]	X
Bit 6	R	SBIPE[6]	X
Bit 5	R	SBIPE[5]	X
Bit 4	R	SBIPE[4]	X
Bit 3	R	SBIPE[3]	X
Bit 2	R	SBIPE[2]	X
Bit 1	R	SBIPE[1]	X
Bit 0	R	SBIPE[0]	X

The Section BIP Error Counter Register is provided at RRMP r/w address 07H.

SBIPE[15:0]

The section BIP error (SBIPE[15:0]) bits represent the number of section BIP errors that have been detected since the last accumulation interval. The error counter is transferred to the holding registers by a microprocessor write to any of the holding register addresses (0X87H to 0X8BH) or the Master Configuration Register (0000H).

Register 0088H, 0488H, 0888H and 0C88H: RRMP Line BIP Error Counter (LSB)

Bit	Type	Function	Default
Bit 15	R	LBIPE[15]	X
Bit 14	R	LBIPE[14]	X
Bit 13	R	LBIPE[13]	X
Bit 12	R	LBIPE[12]	X
Bit 11	R	LBIPE[11]	X
Bit 10	R	LBIPE[10]	X
Bit 9	R	LBIPE[9]	X
Bit 8	R	LBIPE[8]	X
Bit 7	R	LBIPE[7]	X
Bit 6	R	LBIPE[6]	X
Bit 5	R	LBIPE[5]	X
Bit 4	R	LBIPE[4]	X
Bit 3	R	LBIPE[3]	X
Bit 2	R	LBIPE[2]	X
Bit 1	R	LBIPE[1]	X
Bit 0	R	LBIPE[0]	X

The Line BIP Error Counter Register is provided at RRMP r/w address 08H.

Register 0089H, 0489H, 0889H and 0C89H: RRMP Line BIP Error Counter (MSB)

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9		Unused	
Bit 8		Unused	
Bit 7	R	LBIPE[23]	X
Bit 6	R	LBIPE[22]	X
Bit 5	R	LBIPE[21]	X
Bit 4	R	LBIPE[20]	X
Bit 3	R	LBIPE[19]	X
Bit 2	R	LBIPE[18]	X
Bit 1	R	LBIPE[17]	X
Bit 0	R	LBIPE[16]	X

The Line BIP Error Counter Register is provided at RRMP r/w address 09H.

LBIPE[23:0]

The line BIP error (LBIPE[23:0]) bits represent the number of line BIP errors that have been detected since the last accumulation interval. The error counter is transferred to the holding registers by a microprocessor write access to any of the holding register addresses (0X87H to 0X8BH) or the Master Configuration Register (0000H).

Register 008AH, 048AH, 088AH and 0C8AH: RRMP Line REI Error Counter (LSB)

Bit	Type	Function	Default
Bit 15	R	LREIE[15]	X
Bit 14	R	LREIE[14]	X
Bit 13	R	LREIE[13]	X
Bit 12	R	LREIE[12]	X
Bit 11	R	LREIE[11]	X
Bit 10	R	LREIE[10]	X
Bit 9	R	LREIE[9]	X
Bit 8	R	LREIE[8]	X
Bit 7	R	LREIE[7]	X
Bit 6	R	LREIE[6]	X
Bit 5	R	LREIE[5]	X
Bit 4	R	LREIE[4]	X
Bit 3	R	LREIE[3]	X
Bit 2	R	LREIE[2]	X
Bit 1	R	LREIE[1]	X
Bit 0	R	LREIE[0]	X

The Line REI Error Counter Register is provided at RRMP r/w address 0AH.

Register 008BH, 048BH, 088BH and 0C8BH: RRMP Line REI Error Counter (MSB)

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9		Unused	
Bit 8		Unused	
Bit 7	R	LREIE[23]	X
Bit 6	R	LREIE[22]	X
Bit 5	R	LREIE[21]	X
Bit 4	R	LREIE[20]	X
Bit 3	R	LREIE[19]	X
Bit 2	R	LREIE[18]	X
Bit 1	R	LREIE[17]	X
Bit 0	R	LREIE[16]	X

The Line REI Error Counter Register is provided at RRMP r/w address 0BH.

LREIE[23:0]

The line REI error (LREIE[23:0]) bits represent the number of line REI errors that have been detected since the last accumulation interval. The error counter is transferred to the holding registers by a microprocessor write access to any of the holding register addresses (0X87H to 0X8BH) or the Master Configuration Register (0000H).

Register 00A0H, 04A0H, 08A0H and 0CA0H: RTTP SECTION Indirect Address

Bit	Type	Function	Default
Bit 15	R	BUSY	X
Bit 14	R/W	RWB	0
Bit 13	R/W	IADDR[7]	0
Bit 12	R/W	IADDR[6]	0
Bit 11	R/W	IADDR[5]	0
Bit 10	R/W	IADDR[4]	0
Bit 9	R/W	IADDR[3]	0
Bit 8	R/W	IADDR[2]	0
Bit 7	R/W	IADDR[1]	0
Bit 6	R/W	IADDR[0]	0
Bit 5		Unused	
Bit 4		Unused	
Bit 3	R/W	PATH[3]	0
Bit 2	R/W	PATH[2]	0
Bit 1	R/W	PATH[1]	0
Bit 0	R/W	PATH[0]	0

The Indirect Address Register is provided at RTTP r/w address 00H.

PATH[3:0]

The STS-1/STM-0 path (PATH[3:0]) bits select which STS-1/STM-0 path is accessed by the current indirect transfer. When the RTTP monitors section trace message, path #1 is valid.

PATH[3:0]	STS-1/STM-0 path #
0000	Invalid path
0001	SECTION
0010-1111	Invalid path

IADDR[7:0]

The indirect address location (IADDR[7:0]) bits select which indirect address location is accessed by the current indirect transfer.

Indirect Address IADDR[7:0]	Indirect Data
0000 0000	Configuration
0000 0001 to 0011 1111	Invalid address
0100 0000	First byte of the 1/16/64 byte captured trace

Indirect Address IADDR[7:0]	Indirect Data
0100 0001 to 0111 1111	Other bytes of the 16/64 byte captured trace
1000 0000	First byte of the 1/16/64 byte accepted trace
1000 0001 to 1011 1111	Other bytes of the 16/64 byte accepted trace
1100 0000	First byte of the 16/64 byte expected trace
1100 0001 to 1111 1111	Other bytes of the 16/64 byte expected trace

RWB

The active high read and active low write (RWB) bit selects if the current access to the internal RAM is an indirect read or an indirect write. Writing to the Indirect Address Register initiates an access to the internal RAM. When RWB is set to logic 1, an indirect read access to the RAM is initiated. The data from the addressed location in the internal RAM will be transferred to the Indirect Data Register. When RWB is set to logic 0, an indirect write access to the RAM is initiated. The data from the Indirect Data Register will be transferred to the addressed location in the internal RAM.

BUSY

The active high RAM busy (BUSY) bit reports if a previously initiated indirect access to the internal RAM has been completed. BUSY is set to logic 1 upon writing to the Indirect Address Register. BUSY is set to logic 0, upon completion of the RAM access. This register should be polled to determine when new data is available in the Indirect Data Register.
Note: Maximum busy bit set time is 22 clock cycles.

Register 00A1H, 04A1H, 08A1H and 0CA1H: RTTP SECTION Indirect Data

Bit	Type	Function	Default
Bit 15	R/W	DATA[15]	0
Bit 14	R/W	DATA[14]	0
Bit 13	R/W	DATA[13]	0
Bit 12	R/W	DATA[12]	0
Bit 11	R/W	DATA[11]	0
Bit 10	R/W	DATA[10]	0
Bit 9	R/W	DATA[9]	0
Bit 8	R/W	DATA[8]	0
Bit 7	R/W	DATA[7]	0
Bit 6	R/W	DATA[6]	0
Bit 5	R/W	DATA[5]	0
Bit 4	R/W	DATA[4]	0
Bit 3	R/W	DATA[3]	0
Bit 2	R/W	DATA[2]	0
Bit 1	R/W	DATA[1]	0
Bit 0	R/W	DATA[0]	0

The Indirect Data Register is provided at RTTP r/w address 01H.

DATA[15:0]

The indirect access data (DATA[15:0]) bits hold the data transfer to or from the internal RAM during indirect access. When RWB is set to logic 1 (indirect read), the data from the addressed location in the internal RAM will be transfer to DATA[15:0]. BUSY should be polled to determine when the new data is available in DATA[15:0]. When RWB is set to logic 0 (indirect write), the data from DATA[15:0] will be transferred to the addressed location in the internal RAM. The indirect Data register must contain valid data before the indirect write is initiated by writing to the Indirect Address Register.

DATA[15:0] has a different meaning depending on which address of the internal RAM is being accessed.

Register 00A2H, 04A2H, 08A2H and 0CA2H: RTTP SECTION Trace Unstable Status

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9		Unused	
Bit 8		Unused	
Bit 7		Unused	
Bit 6		Unused	
Bit 5		Unused	
Bit 4		Unused	
Bit 3		Unused	
Bit 2		Unused	
Bit 1		Unused	
Bit 0	R	TIUV	X

The Trace Unstable Status Register is provided at RTTP r/w address 02H.

TIUV

The trace identifier unstable status (TIUV) bit indicates the current status of the TIU defects for the section trace.

Algorithm 1: TIUV is set to logic 0.

Algorithm 2: TIUV is set to logic 1 when one or more erroneous bytes are detected between the current message and the previous message in a total of 8 tail trace messages without any persistent message in between. TIUV is set to logic 0 when a persistent message is found. A persistent message is found when the same message is receive for 3 or 5 consecutive multi-frames.

Algorithm 3: TIUV is set to logic 1 when one or more erroneous bytes are detected in three consecutive sixteen byte windows. The first window starts on the first erroneous tail trace byte. TIUV is set to logic 0 when the same tail trace byte is received for 48 consecutive frames.

Register 00A3H, 04A3H, 08A3H and 0CA3H: RTTP SECTION Trace Unstable Interrupt Enable

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9		Unused	
Bit 8		Unused	
Bit 7		Unused	
Bit 6		Unused	
Bit 5		Unused	
Bit 4		Unused	
Bit 3		Unused	
Bit 2		Unused	
Bit 1		Unused	
Bit 0	R/W	TIUE	0

The Trace Unstable Interrupt Enable Register is provided at RTTP r/w address 03H.

TIUE

The trace identifier unstable interrupt enable (TIUE) bit controls the activation of the interrupt output for the section trace. When this bit is set to logic 1, the corresponding pending interrupt will assert the interrupt output. When this bit is set to logic 0, the corresponding pending interrupt will not assert the interrupt output.

Register 00A4H, 04A4H, 08A4H and 0CA4H: RTTP SECTION Trace Unstable Interrupt Status

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9		Unused	
Bit 8		Unused	
Bit 7		Unused	
Bit 6		Unused	
Bit 5		Unused	
Bit 4		Unused	
Bit 3		Unused	
Bit 2		Unused	
Bit 1		Unused	
Bit 0	R	TIU	X

The Trace Unstable Interrupt Status Register is provided at RTTP r/w address 04H.

TIUI

The trace identifier unstable interrupt status (TIUI) bit is an event indicators for the section trace. TIUI is set to logic 1 to indicate any changes in the status of TIUV (stable to unstable, unstable to stable). This interrupt status bit is independent of the interrupt enable bit. TIUI is cleared to logic 0 when this register is read.

Register 00A5H, 04A5H, 08A5H and 0CA5H: RTTP SECTION Trace Mismatch Status

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9		Unused	
Bit 8		Unused	
Bit 7		Unused	
Bit 6		Unused	
Bit 5		Unused	
Bit 4		Unused	
Bit 3		Unused	
Bit 2		Unused	
Bit 1		Unused	
Bit 0	R	TIMV	X

The Trace Mismatch Status Register is provided at RTTP r/w address 05H.

TIMV

The trace identifier mismatch status (TIMV) bit indicates the current status of the TIM defects for the section trace.

Algorithm 1: TIMV is set to logic 1 when none of the last 20 messages matches the expected message. TIMV is set to logic 0 when 16 of the last 20 messages match the expected message.

Algorithm 2: TIMV is set to logic 1 when the accepted message does not match the expected message. TIMV is set to logic 0 when the accepted message matches the expected message.

Algorithm 3: TIMV is set to logic 0.

Register 00A6H, 04A6H, 08A6H and 0CA6H: RTTP SECTION Trace Mismatch Interrupt Enable

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9		Unused	
Bit 8		Unused	
Bit 7		Unused	
Bit 6		Unused	
Bit 5		Unused	
Bit 4		Unused	
Bit 3		Unused	
Bit 2		Unused	
Bit 1		Unused	
Bit 0	R/W	TIME	0

The Trace Mismatch Interrupt Enable Register is provided at RTTP r/w address 06H.

TIME

The trace identifier mismatch interrupt enable (TIME) bit controls the activation of the interrupt output for the section trace. When this bit is set to logic 1, the corresponding pending interrupt will assert the interrupt output. When this bit is set to logic 0, the corresponding pending interrupt will not assert the interrupt output.

Register 00A7H, 04A7H, 08A7H and 0CA7H: RTTP SECTION Trace Mismatch Interrupt Status

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9		Unused	
Bit 8		Unused	
Bit 7		Unused	
Bit 6		Unused	
Bit 5		Unused	
Bit 4		Unused	
Bit 3		Unused	
Bit 2		Unused	
Bit 1		Unused	
Bit 0	R	TIMI	X

The Trace Mismatch Interrupt Status Register is provided at RTTP r/w address 07H.

TIMI

The trace identifier mismatch interrupt status (TIMI) bit is an event indicator for the section trace. TIMI is set to logic 1 to indicate any changes in the status of TIMV (match to mismatch, mismatch to match). This interrupt status bit is independent of the interrupt enable bit. TIMI is cleared to logic 0 when this register is read.

Indirect Register 00H: RTTP SECTION Trace Configuration

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9		Unused	
Bit 8		Unused	
Bit 7		Unused	
Bit 6	R/W	SYNCCRLF	0
Bit 5	R/W	ZEROEN	0
Bit 4	R/W	PER5	0
Bit 3	R/W	NOSYNC	0
Bit 2	R/W	LENGTH16	0
Bit 1	R/W	ALGO[1]	0
Bit 0	R/W	ALGO[0]	0

The Trace Configuration Indirect Register is provided at RTTP r/w indirect address 00H.

ALGO[1:0]

The tail trace algorithm select (ALGO[1:0]) bits select the algorithm used to process the tail trace message.

ALGO[1:0]	Tail trace algorithm
00	Algorithm disable
01	Algorithm 1
10	Algorithm 2
11	Algorithm 3

When ALGO[1:0] is set to logic 00b, the tail trace algorithms are disabled. The corresponding TIUV, TIMV register bits and the corresponding TIU, TIM output signal are set to logic 0.

LENGTH16

The message length (LENGTH16) bit selects the length of the tail trace message used by algorithm 1 and algorithm 2. When LENGTH16 is set to logic 1, the length of the tail trace message is 16 byte. When LENGTH16 is set to logic 0, the length of the tail trace message is 64 byte.

NOSYNC

The synchronization disable (NOSYNC) bit disables the synchronization of the tail trace message in algorithm 1 and algorithm 2. When NOSYNC is set to logic 1, no synchronization is done on the tail trace message. The bytes of the tail trace message are written in the captured page as in a circular buffer. When NOSYNC is set to logic 0, synchronization is done on the tail trace message. See SYNCCRLF to determine how synchronization is handled when NOSYNC = 0.

PER5

The message persistency (PER5) bit selects the number of multi-frames a tail trace message must receive in order to be declared persistent in algorithm 2. When PER5 is set to logic 1, the same tail trace message must be received for 5 consecutive multi-frames to be declared persistent. When PER5 is set to logic 0, the same tail trace message must be received for 3 consecutive multi-frames to be declared persistent.

ZEROEN

The all zero message enable (ZEROEN) bit selects if the all zero messages are validated or not against the expected message in algorithm 1 and algorithm 2. When ZEROEN is set to logic 1, an all zero captured message in algorithm 1 and an all zero accepted message in algorithm 2 are validated against the expected message. A match is declared when both the captured/accepted message and the expected message are all zero. When ZEROEN is set to logic 0, an all zero captured message in algorithm 1 and an all zero accepted message in algorithm 2 are not validated against the expected message but are considered match. A match is declared when the captured/accepted message is all zero regardless of the expected message.

SYNCCRLF

The synchronization on CR/LF characters (SYNCCRLF) bit selects if the current algorithm (except algo3) synchronizes on the CR/LF ASCII characters or on the byte with its MSB set high. When SYNCCRLF is set to logic 1, the current algorithm synchronizes when it receives the ASCII character “CR” (carriage return) followed by “LF” (line feed) and the current active byte becomes the last byte of the message. When SYNCCRLF is set to 0, the current algorithm synchronizes when receiving a byte with its MSB set to logic 1. The current active byte then becomes the first byte of the message.

Indirect Register 40H to 7FH: RTTP SECTION Captured Trace

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9		Unused	
Bit 8		Unused	
Bit 7	R	CTRACE[7]	X
Bit 6	R	CTRACE[6]	X
Bit 5	R	CTRACE[5]	X
Bit 4	R	CTRACE[4]	X
Bit 3	R	CTRACE[3]	X
Bit 2	R	CTRACE[2]	X
Bit 1	R	CTRACE[1]	X
Bit 0	R	CTRACE[0]	X

The Captured Trace Indirect Register is provided at RTTP r/w indirect address 40H to 7FH.

CTRACE[7:0]

The captured tail trace message (CTRACE[7:0]) bits contain the currently received tail trace message. When algorithm 1 or 2 is selected and LENGTH16 is set to logic 1, the captured message is stored between address 40h and 4Fh. When algorithm 1 or 2 is selected and LENGTH16 is set to logic 0, the captured message is stored between address 40h and 7Fh. When NOSYNC is set to logic 1, the captured message is not synchronized. When NOSYNC is set to logic 0, the captured message is synchronized and the first byte of the message is stored at address 40h. When algorithm 3 is selected, the captured byte is stored at address 40h.

Indirect Register 80H to BFH: RTTP SECTION Accepted Trace

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9		Unused	
Bit 8		Unused	
Bit 7	R	ATRACE[7]	X
Bit 6	R	ATRACE[6]	X
Bit 5	R	ATRACE[5]	X
Bit 4	R	ATRACE[4]	X
Bit 3	R	ATRACE[3]	X
Bit 2	R	ATRACE[2]	X
Bit 1	R	ATRACE[1]	X
Bit 0	R	ATRACE[0]	X

The Accepted Trace Indirect Register is provided at RTTP r/w indirect address 80H to BFH.

ATRACE[7:0]

The accepted tail trace message (ATRACE[7:0]) bits contain the persistent tail trace message. When algorithm 1 is selected, the accepted message will not be updated. When algorithm 2 is selected and PER5 is set to logic 1, the accepted message is the same tail trace message received for 5 consecutive multi-frames. When algorithm 2 is selected and PER5 is set to logic 0, the accepted message is the same tail trace message received for 3 consecutive multi-frames. When algorithm 2 is selected and LENGTH16 is set to logic 1, the accepted message is stored between address 80h and 8Fh. When algorithm 2 is selected and LENGTH16 is set to logic 0, the accepted message is stored between address 80h and BFh. When algorithm 3 is selected, the accepted byte is the same tail trace byte received for 48 frames. When algorithm 3 is selected, the accepted byte is stored at address 80h.

Indirect Register C0H to FFH: RTTP SECTION Expected Trace

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9		Unused	
Bit 8		Unused	
Bit 7	R/W	ETRACE[7]	X
Bit 6	R/W	ETRACE[6]	X
Bit 5	R/W	ETRACE[5]	X
Bit 4	R/W	ETRACE[4]	X
Bit 3	R/W	ETRACE[3]	X
Bit 2	R/W	ETRACE[2]	X
Bit 1	R/W	ETRACE[1]	X
Bit 0	R/W	ETRACE[0]	X

The Expected Trace Indirect Register is provided at RTTP r/w indirect address C0H to FFH.

ETRACE[7:0]

The expected tail trace message (ETRACE[7:0]) bits contain a static message written by an external microprocessor. In algorithm 1 the expected message is used to validated the captured message. In algorithm 2 the expected message is used to validate the accepted message. When LENGTH16 is set to logic 1, the expected message must be written between address C0h and CFh. When LENGTH16 is set to logic 0, the accepted message must be written between address C0h and FFh.

Register 00C0H, 04C0H, 08C0H and 0CC0H: RTTP PATH Indirect Address

Bit	Type	Function	Default
Bit 15	R	BUSY	X
Bit 14	R/W	RWB	0
Bit 13	R/W	IADDR[7]	0
Bit 12	R/W	IADDR[6]	0
Bit 11	R/W	IADDR[5]	0
Bit 10	R/W	IADDR[4]	0
Bit 9	R/W	IADDR[3]	0
Bit 8	R/W	IADDR[2]	0
Bit 7	R/W	IADDR[1]	0
Bit 6	R/W	IADDR[0]	0
Bit 5		Unused	
Bit 4		Unused	
Bit 3	R/W	PATH[3]	0
Bit 2	R/W	PATH[2]	0
Bit 1	R/W	PATH[1]	0
Bit 0	R/W	PATH[0]	0

The Indirect Address Register is provided at RTTP r/w address 00H.

PATH[3:0]

The STS-1/STM-0 path (PATH[3:0]) bits select which STS-1/STM-0 path is accessed by the current indirect transfer. When the RTTP monitors path trace messages, paths #1 to #12 are valid.

PATH[3:0]	STS-1/STM-0 path #
0000	Invalid path
0001-1100	Path #1 to Path #12
1101-1111	Invalid path

IADDR[7:0]

The indirect address location (IADDR[7:0]) bits select which indirect address location is accessed by the current indirect transfer.

Indirect Address IADDR[7:0]	Indirect Data
0000 0000	Configuration
0000 0001 to 0011 1111	Invalid address
0100 0000	First byte of the 1/16/64 byte captured trace

Indirect Address IADDR[7:0]	Indirect Data
0100 0001 to 0111 1111	Other bytes of the 16/64 byte captured trace
1000 0000	First byte of the 1/16/64 byte accepted trace
1000 0001 to 1011 1111	Other bytes of the 16/64 byte accepted trace
1100 0000	First byte of the 16/64 byte expected trace
1100 0001 to 1111 1111	Other bytes of the 16/64 byte expected trace

RWB

The active high read and active low write (RWB) bit selects if the current access to the internal RAM is an indirect read or an indirect write. Writing to the Indirect Address Register initiates an access to the internal RAM. When RWB is set to logic 1, an indirect read access to the RAM is initiated. The data from the addressed location in the internal RAM will be transferred to the Indirect Data Register. When RWB is set to logic 0, an indirect write access to the RAM is initiated. The data from the Indirect Data Register will be transferred to the addressed location in the internal RAM.

BUSY

The active high RAM busy (BUSY) bit reports if a previously initiated indirect access to the internal RAM has been completed. BUSY is set to logic 1 upon writing to the Indirect Address Register. BUSY is set to logic 0, upon completion of the RAM access. This register should be polled to determine when new data is available in the Indirect Data Register.
Note: Maximum busy bit set time is 22 clock cycles.

Register 00C1H, 04C1H, 08C1H and 0CC1H: RTTP PATH Indirect Data

Bit	Type	Function	Default
Bit 15	R/W	DATA[15]	0
Bit 14	R/W	DATA[14]	0
Bit 13	R/W	DATA[13]	0
Bit 12	R/W	DATA[12]	0
Bit 11	R/W	DATA[11]	0
Bit 10	R/W	DATA[10]	0
Bit 9	R/W	DATA[9]	0
Bit 8	R/W	DATA[8]	0
Bit 7	R/W	DATA[7]	0
Bit 6	R/W	DATA[6]	0
Bit 5	R/W	DATA[5]	0
Bit 4	R/W	DATA[4]	0
Bit 3	R/W	DATA[3]	0
Bit 2	R/W	DATA[2]	0
Bit 1	R/W	DATA[1]	0
Bit 0	R/W	DATA[0]	0

The Indirect Data Register is provided at RTTP r/w address 01H.

DATA[15:0]

The indirect access data (DATA[15:0]) bits hold the data transfer to or from the internal RAM during indirect access. When RWB is set to logic 1 (indirect read), the data from the addressed location in the internal RAM will be transfer to DATA[15:0]. BUSY should be polled to determine when the new data is available in DATA[15:0]. When RWB is set to logic 0 (indirect write), the data from DATA[15:0] will be transferred to the addressed location in the internal RAM. The indirect Data register must contain valid data before the indirect write is initiated by writing to the Indirect Address Register.

DATA[15:0] has a different meaning depending on which address of the internal RAM is being accessed.

Register 00C2H, 04C2H, 08C2H and 0CC2H: RTTP PATH Trace Unstable Status

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11	R	TIUV[12]	X
Bit 10	R	TIUV[11]	X
Bit 9	R	TIUV[10]	X
Bit 8	R	TIUV[9]	X
Bit 7	R	TIUV[8]	X
Bit 6	R	TIUV[7]	X
Bit 5	R	TIUV[6]	X
Bit 4	R	TIUV[5]	X
Bit 3	R	TIUV[4]	X
Bit 2	R	TIUV[3]	X
Bit 1	R	TIUV[2]	X
Bit 0	R	TIUV[1]	X

The Trace Unstable Status Register is provided at RTTP r/w address 02H.

TIUV[12:1]

The trace identifier unstable status (TIUV[12:1]) bits indicate the current status of the TIU defects for STS-1/STM-0 paths #1 to #12.

Algorithm 1: TIUV is set to logic 0.

Algorithm 2: TIUV is set to logic 1 when one or more erroneous bytes are detected between the current message and the previous message in a total of 8 tail trace messages without any persistent message in between. TIUV is set to logic 0 when a persistent message is found. A persistent message is found when the same message is receive for 3 or 5 consecutive multi-frames.

Algorithm 3: TIUV is set to logic 1 when one or more erroneous bytes are detected in three consecutive sixteen byte windows. The first window starts on the first erroneous tail trace byte. TIUV is set to logic 0 when the same tail trace byte is received for 48 consecutive frames.

Register 00C3H, 04C3H, 08C3H and 0CC3H: RTTP PATH Trace Unstable Interrupt Enable

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11	R/W	TIUE[12]	0
Bit 10	R/W	TIUE[11]	0
Bit 9	R/W	TIUE[10]	0
Bit 8	R/W	TIUE[9]	0
Bit 7	R/W	TIUE[8]	0
Bit 6	R/W	TIUE[7]	0
Bit 5	R/W	TIUE[6]	0
Bit 4	R/W	TIUE[5]	0
Bit 3	R/W	TIUE[4]	0
Bit 2	R/W	TIUE[3]	0
Bit 1	R/W	TIUE[2]	0
Bit 0	R/W	TIUE[1]	0

The Trace Unstable Interrupt Enable Register is provided at RTTP r/w address 03H.

TIUE[12:1]

The trace identifier unstable interrupt enable (TIUE[12:1]) bits control the activation of the interrupt output for STS-1/STM-0 paths #1 to #12. When any of these bit locations is set to logic 1, the corresponding pending interrupt will assert the interrupt output. When any of these bit locations is set to logic 0, the corresponding pending interrupt will not assert the interrupt output.

Register 00C4H, 04C4H, 08C4H and 0CC4H: RTTP PATH Trace Unstable Interrupt Status

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11	R	TIUI[12]	X
Bit 10	R	TIUI[11]	X
Bit 9	R	TIUI[10]	X
Bit 8	R	TIUI[9]	X
Bit 7	R	TIUI[8]	X
Bit 6	R	TIUI[7]	X
Bit 5	R	TIUI[6]	X
Bit 4	R	TIUI[5]	X
Bit 3	R	TIUI[4]	X
Bit 2	R	TIUI[3]	X
Bit 1	R	TIUI[2]	X
Bit 0	R	TIUI[1]	X

The Trace Unstable Interrupt Status Register is provided at RTTP r/w address 04H.

TIUI[12:1]

The trace identifier unstable interrupt status (TIUI[12:1]) bits are event indicators for STS-1/STM-0 paths #1 to #12. TIUI[12:1] are set to logic 1 to indicate any changes in the status of TIUV[12:1] (stable to unstable, unstable to stable). These interrupt status bits are independent of the interrupt enable bits. TIUI[12:1] are cleared to logic 0 when this register is read.

Register 00C5H, 04C5H, 08C5H and 0CC5H: RTTP PATH Trace Mismatch Status

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11	R	TIMV[12]	X
Bit 10	R	TIMV[11]	X
Bit 9	R	TIMV[10]	X
Bit 8	R	TIMV[9]	X
Bit 7	R	TIMV[8]	X
Bit 6	R	TIMV[7]	X
Bit 5	R	TIMV[6]	X
Bit 4	R	TIMV[5]	X
Bit 3	R	TIMV[4]	X
Bit 2	R	TIMV[3]	X
Bit 1	R	TIMV[2]	X
Bit 0	R	TIMV[1]	X

The Trace Mismatch Status Register is provided at RTTP r/w address 05H.

TIMV[12:1]

The trace identifier mismatch status (TIMV[12:1]) bit indicate the current status of the TIM defects for STS-1/STM-0 paths #1 to #12.

Algorithm 1: TIMV is set to logic 1 when none of the last 20 messages matches the expected message. TIMV is set to logic 0 when 16 of the last 20 messages match the expected message.

Algorithm 2: TIMV is set to logic 1 when the accepted message does not match the expected message. TIMV is set to logic 0 when the accepted message matches the expected message.

Algorithm 3: TIMV is set to logic 0.

Register 00C6H, 04C6H, 08C6H and 0CC6H: RTTP PATH Trace Mismatch Interrupt Enable

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11	R/W	TIME[12]	0
Bit 10	R/W	TIME[11]	0
Bit 9	R/W	TIME[10]	0
Bit 8	R/W	TIME[9]	0
Bit 7	R/W	TIME[8]	0
Bit 6	R/W	TIME[7]	0
Bit 5	R/W	TIME[6]	0
Bit 4	R/W	TIME[5]	0
Bit 3	R/W	TIME[4]	0
Bit 2	R/W	TIME[3]	0
Bit 1	R/W	TIME[2]	0
Bit 0	R/W	TIME[1]	0

The Trace Mismatch Interrupt Enable Register is provided at RTTP r/w address 06H.

TIME[12:1]

The trace identifier mismatch interrupt enable (TIME[12:1]) bits control the activation of the interrupt output for STS-1/STM-0 paths #1 to #12. When any of these bit locations is set to logic 1, the corresponding pending interrupt will assert the interrupt output. When any of these bit locations is set to logic 0, the corresponding pending interrupt will not assert the interrupt output.

Register 00C7H, 04C7H, 08C7H and 0CC7H: RTTP PATH Trace Mismatch Interrupt Status

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11	R	TIMI[12]	X
Bit 10	R	TIMI[11]	X
Bit 9	R	TIMI[10]	X
Bit 8	R	TIMI[9]	X
Bit 7	R	TIMI[8]	X
Bit 6	R	TIMI[7]	X
Bit 5	R	TIMI[6]	X
Bit 4	R	TIMI[5]	X
Bit 3	R	TIMI[4]	X
Bit 2	R	TIMI[3]	X
Bit 1	R	TIMI[2]	X
Bit 0	R	TIMI[1]	X

The Trace Mismatch Interrupt Status Register is provided at RTTP r/w address 07H.

TIMI[12:1]

The trace identifier mismatch interrupt status (TIMI[12:1]) bits are event indicators for STS-1/STM-0 paths #1 to #12. TIMI[12:1] are set to logic 1 to indicate any changes in the status of TIMV[12:1] (match to mismatch, mismatch to match). These interrupt status bits are independent of the interrupt enable bits. TIMI[12:1] are cleared to logic 0 when this register is read.

Indirect Register 00H: RTTP PATH Trace Configuration

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9		Unused	
Bit 8		Unused	
Bit 7		Unused	
Bit 6	R/W	SYNCCRLF	0
Bit 5	R/W	ZEROEN	0
Bit 4	R/W	PER5	0
Bit 3	R/W	NOSYNC	0
Bit 2	R/W	LENGTH16	0
Bit 1	R/W	ALGO[1]	0
Bit 0	R/W	ALGO[0]	0

The Trace Configuration Indirect Register is provided at RTTP r/w indirect address 00H.

ALGO[1:0]

The tail trace algorithm select (ALGO[1:0]) bits select the algorithm used to process the tail trace message.

ALGO[1:0]	Tail trace algorithm
00	Algorithm disabled
01	Algorithm 1
10	Algorithm 2
11	Algorithm 3

When ALGO[1:0] is set to logic 00b, the tail trace algorithms are disabled. The corresponding TIUV, TIMV register bits and the corresponding TIU, TIM output signal time slots are set to logic 0.

LENGTH16

The message length (LENGTH16) bit selects the length of the tail trace message used by algorithm 1 and algorithm 2. When LENGTH16 is set to logic 1, the length of the tail trace message is 16 byte. When LENGTH16 is set to logic 0, the length of the tail trace message is 64 byte.

NOSYNC

The synchronization disable (NOSYNC) bit disables the synchronization of the tail trace message in algorithm 1 and algorithm 2. When NOSYNC is set to logic 1, no synchronization is done on the tail trace message. The bytes of the tail trace message are written in the captured page as in a circular buffer. When NOSYNC is set to logic 0, synchronization is done on the tail trace message. See SYNCCRLF to determine how synchronization is handled when NOSYNC = 0.

PER5

The message persistency (PER5) bit selects the number of multi-frames a tail trace message must receive in order to be declared persistent in algorithm 2. When PER5 is set to logic 1, the same tail trace message must be received for 5 consecutive multi-frames to be declared persistent. When PER5 is set to logic 0, the same tail trace message must be received for 3 consecutive multi-frames to be declared persistent.

ZEROEN

The all zero message enable (ZEROEN) bit selects if the all zero messages are validated or not against the expected message in algorithm 1 and algorithm 2. When ZEROEN is set to logic 1, an all zero captured message in algorithm 1 and an all zero accepted message in algorithm 2 are validated against the expected message. A match is declared when both the captured/accepted message and the expected message are all zero. When ZEROEN is set to logic 0, an all zero captured message in algorithm 1 and an all zero accepted message in algorithm 2 are not validated against the expected message but are considered match. A match is declared when the captured/accepted message is all zero regardless of the expected message.

SYNCCRLF

The synchronization on CR/LF characters (SYNCCRLF) bit selects if the current algorithm (except algo3) synchronizes on the CR/LF ASCII characters or on the byte with its MSB set high. When SYNCCRLF is set to logic 1, the current algorithm synchronizes when it receives the ASCII character “CR” (carriage return) followed by “LF” (line feed) and the current active byte becomes the last byte of the message. When SYNCCRLF is set to 0, the current algorithm synchronizes when receiving a byte with its MSB set to logic 1. The current active byte then becomes the first byte of the message.

Indirect Register 40H to 7FH: RTTP PATH Captured Trace

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9		Unused	
Bit 8		Unused	
Bit 7	R	CTRACE[7]	X
Bit 6	R	CTRACE[6]	X
Bit 5	R	CTRACE[5]	X
Bit 4	R	CTRACE[4]	X
Bit 3	R	CTRACE[3]	X
Bit 2	R	CTRACE[2]	X
Bit 1	R	CTRACE[1]	X
Bit 0	R	CTRACE[0]	X

The Captured Trace Indirect Register is provided at RTTP r/w indirect address 40H to 7FH.

CTRACE[7:0]

The captured tail trace message (CTRACE[7:0]) bits contain the currently received tail trace message. When algorithm 1 or 2 is selected and LENGTH16 is set to logic 1, the captured message is stored between address 40h and 4Fh. When algorithm 1 or 2 is selected and LENGTH16 is set to logic 0, the captured message is stored between address 40h and 7Fh. When NOSYNC is set to logic 1, the captured message is not synchronized. When NOSYNC is set to logic 0, the captured message is synchronized and the first byte of the message is stored at address 40h. When algorithm 3 is selected, the captured byte is stored at address 40h.

Indirect Register 80H to BFH: RTTP PATH Accepted Trace

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9		Unused	
Bit 8		Unused	
Bit 7	R	ATRACE[7]	X
Bit 6	R	ATRACE[6]	X
Bit 5	R	ATRACE[5]	X
Bit 4	R	ATRACE[4]	X
Bit 3	R	ATRACE[3]	X
Bit 2	R	ATRACE[2]	X
Bit 1	R	ATRACE[1]	X
Bit 0	R	ATRACE[0]	X

The Accepted Trace Indirect Register is provided at RTTP r/w indirect address 80H to BFH.

ATRACE[7:0]

The accepted tail trace message (ATRACE[7:0]) bits contain the persistent tail trace message. When algorithm 1 is selected, the accepted message will not be updated. When algorithm 2 is selected and PER5 is set to logic 1, the accepted message is the same tail trace message received for 5 consecutive multi-frames. When algorithm 2 is selected and PER5 is set to logic 0, the accepted message is the same tail trace message received for 3 consecutive multi-frames. When algorithm 2 is selected and LENGTH16 is set to logic 1, the accepted message is stored between address 80h and 8Fh. When algorithm 2 is selected and LENGTH16 is set to logic 0, the accepted message is stored between address 80h and BFh. When algorithm 3 is selected, the accepted byte is the same tail trace byte received for 48 frames. When algorithm 3 is selected, the accepted byte is stored at address 80h.

Indirect Register C0H to FFH: RTTP PATH Expected Trace

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9		Unused	
Bit 8		Unused	
Bit 7	R/W	ETRACE[7]	X
Bit 6	R/W	ETRACE[6]	X
Bit 5	R/W	ETRACE[5]	X
Bit 4	R/W	ETRACE[4]	X
Bit 3	R/W	ETRACE[3]	X
Bit 2	R/W	ETRACE[2]	X
Bit 1	R/W	ETRACE[1]	X
Bit 0	R/W	ETRACE[0]	X

The Expected Trace Indirect Register is provided at RTTP r/w indirect address C0H to FFH.

ETRACE[7:0]

The expected tail trace message (ETRACE[7:0]) bits contain a static message written by an external microprocessor. In algorithm 1 the expected message is used to validated the captured message. In algorithm 2 the expected message is used to validate the accepted message. When LENGTH16 is set to logic 1, the expected message must be written between address C0h and CFh. When LENGTH16 is set to logic 0, the accepted message must be written between address C0h and FFh.

Register 00E0H, 04E0H, 08E0H and 0AE0H: RTTP PATH TU3 Indirect Address

Bit	Type	Function	Default
Bit 15	R	BUSY	X
Bit 14	R/W	RWB	0
Bit 13	R/W	IADDR[7]	0
Bit 12	R/W	IADDR[6]	0
Bit 11	R/W	IADDR[5]	0
Bit 10	R/W	IADDR[4]	0
Bit 9	R/W	IADDR[3]	0
Bit 8	R/W	IADDR[2]	0
Bit 7	R/W	IADDR[1]	0
Bit 6	R/W	IADDR[0]	0
Bit 5		Unused	
Bit 4		Unused	
Bit 3	R/W	PATH[3]	0
Bit 2	R/W	PATH[2]	0
Bit 1	R/W	PATH[1]	0
Bit 0	R/W	PATH[0]	0

The Indirect Address Register is provided at RTTP r/w address 00H.

PATH[3:0]

The STS-1/STM-0 path (PATH[3:0]) bits select which STS-1/STM-0 path is accessed by the current indirect transfer. When the RTTP monitors path trace messages, paths #1 to #12 are valid.

PATH[3:0]	STS-1/STM-0 path #
0000	Invalid path
0001-1100	Path #1 to Path #12
1101-1111	Invalid path

IADDR[7:0]

The indirect address location (IADDR[7:0]) bits select which indirect address location is accessed by the current indirect transfer.

Indirect Address IADDR[7:0]	Indirect Data
0000 0000	Configuration
0000 0001 to 0011 1111	Invalid address
0100 0000	First byte of the 1/16/64 byte captured trace

Indirect Address IADDR[7:0]	Indirect Data
0100 0001 to 0111 1111	Other bytes of the 16/64 byte captured trace
1000 0000	First byte of the 1/16/64 byte accepted trace
1000 0001 to 1011 1111	Other bytes of the 16/64 byte accepted trace
1100 0000	First byte of the 16/64 byte expected trace
1100 0001 to 1111 1111	Other bytes of the 16/64 byte expected trace

RWB

The active high read and active low write (RWB) bit selects if the current access to the internal RAM is an indirect read or an indirect write. Writing to the Indirect Address Register initiates an access to the internal RAM. When RWB is set to logic 1, an indirect read access to the RAM is initiated. The data from the addressed location in the internal RAM will be transferred to the Indirect Data Register. When RWB is set to logic 0, an indirect write access to the RAM is initiated. The data from the Indirect Data Register will be transferred to the addressed location in the internal RAM.

BUSY

The active high RAM busy (BUSY) bit reports if a previously initiated indirect access to the internal RAM has been completed. BUSY is set to logic 1 upon writing to the Indirect Address Register. BUSY is set to logic 0, upon completion of the RAM access. This register should be polled to determine when new data is available in the Indirect Data Register.
Note: Maximum busy bit set time is 22 clock cycles.

Register 00E1H, 04E1H, 08E1H and 0CE1H: RTTP PATH TU3 Indirect Data

Bit	Type	Function	Default
Bit 15	R/W	DATA[15]	0
Bit 14	R/W	DATA[14]	0
Bit 13	R/W	DATA[13]	0
Bit 12	R/W	DATA[12]	0
Bit 11	R/W	DATA[11]	0
Bit 10	R/W	DATA[10]	0
Bit 9	R/W	DATA[9]	0
Bit 8	R/W	DATA[8]	0
Bit 7	R/W	DATA[7]	0
Bit 6	R/W	DATA[6]	0
Bit 5	R/W	DATA[5]	0
Bit 4	R/W	DATA[4]	0
Bit 3	R/W	DATA[3]	0
Bit 2	R/W	DATA[2]	0
Bit 1	R/W	DATA[1]	0
Bit 0	R/W	DATA[0]	0

The Indirect Data Register is provided at RTTP r/w address 01H.

DATA[15:0]

The indirect access data (DATA[15:0]) bits hold the data transfer to or from the internal RAM during indirect access. When RWB is set to logic 1 (indirect read), the data from the addressed location in the internal RAM will be transfer to DATA[15:0]. BUSY should be polled to determine when the new data is available in DATA[15:0]. When RWB is set to logic 0 (indirect write), the data from DATA[15:0] will be transferred to the addressed location in the internal RAM. The indirect Data register must contain valid data before the indirect write is initiated by writing to the Indirect Address Register.

DATA[15:0] has a different meaning depending on which address of the internal RAM is being accessed.

Register 00E2H, 04E2H, 08E2H and 0CE2H: RTTP PATH TU3 Trace Unstable Status

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11	R	TIUV[12]	X
Bit 10	R	TIUV[11]	X
Bit 9	R	TIUV[10]	X
Bit 8	R	TIUV[9]	X
Bit 7	R	TIUV[8]	X
Bit 6	R	TIUV[7]	X
Bit 5	R	TIUV[6]	X
Bit 4	R	TIUV[5]	X
Bit 3	R	TIUV[4]	X
Bit 2	R	TIUV[3]	X
Bit 1	R	TIUV[2]	X
Bit 0	R	TIUV[1]	X

The Trace Unstable Status Register is provided at RTTP r/w address 02H.

TIUV[12:1]

The trace identifier unstable status (TIUV[12:1]) bits indicate the current status of the TIU defects for STS-1/STM-0 paths #1 to #12.

Algorithm 1: TIUV is set to logic 0.

Algorithm 2: TIUV is set to logic 1 when one or more erroneous bytes are detected between the current message and the previous message in a total of 8 tail trace messages without any persistent message in between. TIUV is set to logic 0 when a persistent message is found. A persistent message is found when the same message is receive for 3 or 5 consecutive multi-frames.

Algorithm 3: TIUV is set to logic 1 when one or more erroneous bytes are detected in three consecutive sixteen byte windows. The first window starts on the first erroneous tail trace byte. TIUV is set to logic 0 when the same tail trace byte is received for 48 consecutive frames.

Register 00E3H, 04E3H, 08E3H and 0CE3H: RTTP PATH TU3 Trace Unstable Interrupt Enable

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11	R/W	TIUE[12]	0
Bit 10	R/W	TIUE[11]	0
Bit 9	R/W	TIUE[10]	0
Bit 8	R/W	TIUE[9]	0
Bit 7	R/W	TIUE[8]	0
Bit 6	R/W	TIUE[7]	0
Bit 5	R/W	TIUE[6]	0
Bit 4	R/W	TIUE[5]	0
Bit 3	R/W	TIUE[4]	0
Bit 2	R/W	TIUE[3]	0
Bit 1	R/W	TIUE[2]	0
Bit 0	R/W	TIUE[1]	0

The Trace Unstable Interrupt Enable Register is provided at RTTP r/w address 03H.

TIUE[12:1]

The trace identifier unstable interrupt enable (TIUE[12:1]) bits control the activation of the interrupt output for STS-1/STM-0 paths #1 to #12. When any of these bit locations is set to logic 1, the corresponding pending interrupt will assert the interrupt output. When any of these bit locations is set to logic 0, the corresponding pending interrupt will not assert the interrupt output.

Register 00E4H, 04E4H, 08E4H and 0CE4H: RTTP PATH TU3 Trace Unstable Interrupt Status

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11	R	TIUI[12]	X
Bit 10	R	TIUI[11]	X
Bit 9	R	TIUI[10]	X
Bit 8	R	TIUI[9]	X
Bit 7	R	TIUI[8]	X
Bit 6	R	TIUI[7]	X
Bit 5	R	TIUI[6]	X
Bit 4	R	TIUI[5]	X
Bit 3	R	TIUI[4]	X
Bit 2	R	TIUI[3]	X
Bit 1	R	TIUI[2]	X
Bit 0	R	TIUI[1]	X

The Trace Unstable Interrupt Status Register is provided at RTTP r/w address 04H.

TIUI[12:1]

The trace identifier unstable interrupt status (TIUI[12:1]) bits are event indicators for STS-1/STM-0 paths #1 to #12. TIUI[12:1] are set to logic 1 to indicate any changes in the status of TIUV[12:1] (stable to unstable, unstable to stable). These interrupt status bits are independent of the interrupt enable bits. TIUI[12:1] are cleared to logic 0 when this register is read.

Register 00E5H, 04E5H, 08E5H and 0CE5H: RTTP PATH TU3 Trace Mismatch Status

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11	R	TIMV[12]	X
Bit 10	R	TIMV[11]	X
Bit 9	R	TIMV[10]	X
Bit 8	R	TIMV[9]	X
Bit 7	R	TIMV[8]	X
Bit 6	R	TIMV[7]	X
Bit 5	R	TIMV[6]	X
Bit 4	R	TIMV[5]	X
Bit 3	R	TIMV[4]	X
Bit 2	R	TIMV[3]	X
Bit 1	R	TIMV[2]	X
Bit 0	R	TIMV[1]	X

The Trace Mismatch Status Register is provided at RTTP r/w address 05H.

TIMV[12:1]

The trace identifier mismatch status (TIMV[12:1]) bit indicate the current status of the TIM defects for STS-1/STM-0 paths #1 to #12.

Algorithm 1: TIMV is set to logic 1 when none of the last 20 messages matches the expected message. TIMV is set to logic 0 when 16 of the last 20 messages match the expected message.

Algorithm 2: TIMV is set to logic 1 when the accepted message does not match the expected message. TIMV is set to logic 0 when the accepted message matches the expected message.

Algorithm 3: TIMV is set to logic 0.

Register 00E6H, 04E6H, 08E6H and 0CE6H: RTTP PATH TU3 Trace Mismatch Interrupt Enable

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11	R/W	TIME[12]	0
Bit 10	R/W	TIME[11]	0
Bit 9	R/W	TIME[10]	0
Bit 8	R/W	TIME[9]	0
Bit 7	R/W	TIME[8]	0
Bit 6	R/W	TIME[7]	0
Bit 5	R/W	TIME[6]	0
Bit 4	R/W	TIME[5]	0
Bit 3	R/W	TIME[4]	0
Bit 2	R/W	TIME[3]	0
Bit 1	R/W	TIME[2]	0
Bit 0	R/W	TIME[1]	0

The Trace Mismatch Interrupt Enable Register is provided at RTTP r/w address 06H.

TIME[12:1]

The trace identifier mismatch interrupt enable (TIME[12:1]) bits control the activation of the interrupt output for STS-1/STM-0 paths #1 to #12. When any of these bit locations is set to logic 1, the corresponding pending interrupt will assert the interrupt output. When any of these bit locations is set to logic 0, the corresponding pending interrupt will not assert the interrupt output.

Register 00E7H, 04E7H, 08E7H and 0CE7H: RTTP PATH TU3 Trace Mismatch Interrupt Status

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11	R	TIMI[12]	X
Bit 10	R	TIMI[11]	X
Bit 9	R	TIMI[10]	X
Bit 8	R	TIMI[9]	X
Bit 7	R	TIMI[8]	X
Bit 6	R	TIMI[7]	X
Bit 5	R	TIMI[6]	X
Bit 4	R	TIMI[5]	X
Bit 3	R	TIMI[4]	X
Bit 2	R	TIMI[3]	X
Bit 1	R	TIMI[2]	X
Bit 0	R	TIMI[1]	X

The Trace Mismatch Interrupt Status Register is provided at RTTP r/w address 07H.

TIMI[12:1]

The trace identifier mismatch interrupt status (TIMI[12:1]) bits are event indicators for STS-1/STM-0 paths #1 to #12. TIMI[12:1] are set to logic 1 to indicate any changes in the status of TIMV[12:1] (match to mismatch, mismatch to match). These interrupt status bits are independent of the interrupt enable bits. TIMI[12:1] are cleared to logic 0 when this register is read.

Indirect Register 00H: RTTP PATH TU3 Trace Configuration

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9		Unused	
Bit 8		Unused	
Bit 7		Unused	
Bit 6	R/W	SYNCCRLF	0
Bit 5	R/W	ZEROEN	0
Bit 4	R/W	PER5	0
Bit 3	R/W	NOSYNC	0
Bit 2	R/W	LENGTH16	0
Bit 1	R/W	ALGO[1]	0
Bit 0	R/W	ALGO[0]	0

The Trace Configuration Indirect Register is provided at RTTP r/w indirect address 00H.

ALGO[1:0]

The tail trace algorithm select (ALGO[1:0]) bits select the algorithm used to process the tail trace message.

ALGO[1:0]	Tail Trace Algorithm
00	Algorithm disable
01	Algorithm 1
10	Algorithm 2
11	Algorithm 3

When ALGO[1:0] is set to logic 00b, the tail trace algorithms are disabled. The corresponding TIUV, TIMV register bits and the corresponding TIU, TIM output signal time slots are set to logic 0.

LENGTH16

The message length (LENGTH16) bit selects the length of the tail trace message used by algorithm 1 and algorithm 2. When LENGTH16 is set to logic 1, the length of the tail trace message is 16 byte. When LENGTH16 is set to logic 0, the length of the tail trace message is 64 byte.

NOSYNC

The synchronization disable (NOSYNC) bit disables the synchronization of the tail trace message in algorithm 1 and algorithm 2. When NOSYNC is set to logic 1, no synchronization is done on the tail trace message. The bytes of the tail trace message are written in the captured page as in a circular buffer. When NOSYNC is set to logic 0, synchronization is done on the tail trace message. See SYNC_CRLF to determine how synchronization is handled when NOSYNC = 0.

PER5

The message persistency (PER5) bit selects the number of multi-frames a tail trace message must receive in order to be declared persistent in algorithm 2. When PER5 is set to logic 1, the same tail trace message must be received for 5 consecutive multi-frames to be declared persistent. When PER5 is set to logic 0, the same tail trace message must be received for 3 consecutive multi-frames to be declared persistent.

ZEROEN

The all zero message enable (ZEROEN) bit selects if the all zero messages are validated or not against the expected message in algorithm 1 and algorithm 2. When ZEROEN is set to logic 1, an all zero captured message in algorithm 1 and an all zero accepted message in algorithm 2 are validated against the expected message. A match is declared when both the captured/accepted message and the expected message are all zero. When ZEROEN is set to logic 0, an all zero captured message in algorithm 1 and an all zero accepted message in algorithm 2 are not validated against the expected message but are considered match. A match is declared when the captured/accepted message is all zero regardless of the expected message.

SYNCCRLF

The synchronization on CR/LF characters (SYNCCRLF) bit selects if the current algorithm (except algo3) synchronizes on the CR/LF ASCII characters or on the byte with its MSB set high. When SYNCCRLF is set to logic 1, the current algorithm synchronizes when it receives the ASCII character “CR” (carriage return) followed by “LF” (line feed) and the current active byte becomes the last byte of the message. When SYNCCRLF is set to 0, the current algorithm synchronizes when receiving a byte with its MSB set to logic 1. The current active byte then becomes the first byte of the message.

Indirect Register 40H to 7FH: RTTP PATH TU3 Captured Trace

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9		Unused	
Bit 8		Unused	
Bit 7	R	CTRACE[7]	X
Bit 6	R	CTRACE[6]	X
Bit 5	R	CTRACE[5]	X
Bit 4	R	CTRACE[4]	X
Bit 3	R	CTRACE[3]	X
Bit 2	R	CTRACE[2]	X
Bit 1	R	CTRACE[1]	X
Bit 0	R	CTRACE[0]	X

The Captured Trace Indirect Register is provided at RTTP r/w indirect address 40H to 7FH.

CTRACE[7:0]

The captured tail trace message (CTRACE[7:0]) bits contain the currently received tail trace message. When algorithm 1 or 2 is selected and LENGTH16 is set to logic 1, the captured message is stored between address 40h and 4Fh. When algorithm 1 or 2 is selected and LENGTH16 is set to logic 0, the captured message is stored between address 40h and 7Fh. When NOSYNC is set to logic 1, the captured message is not synchronized. When NOSYNC is set to logic 0, the captured message is synchronized and the first byte of the message is stored at address 40h. When algorithm 3 is selected, the captured byte is stored at address 40h.

Indirect Register 80H to BFH: RTTP PATH TU3 Accepted Trace

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9		Unused	
Bit 8		Unused	
Bit 7	R/W	ATRACE[7]	X
Bit 6	R/W	ATRACE[6]	X
Bit 5	R/W	ATRACE[5]	X
Bit 4	R/W	ATRACE[4]	X
Bit 3	R/W	ATRACE[3]	X
Bit 2	R/W	ATRACE[2]	X
Bit 1	R/W	ATRACE[1]	X
Bit 0	R/W	ATRACE[0]	X

The Accepted Trace Indirect Register is provided at RTTP r/w indirect address 80H to BFH.

ATRACE[7:0]

The accepted tail trace message (ATRACE[7:0]) bits contain the persistent tail trace message. When algorithm 1 is selected, the accepted message will not be updated. When algorithm 2 is selected and PER5 is set to logic 1, the accepted message is the same tail trace message received for 5 consecutive multi-frames. When algorithm 2 is selected and PER5 is set to logic 0, the accepted message is the same tail trace message received for 3 consecutive multi-frames. When algorithm 2 is selected and LENGTH16 is set to logic 1, the accepted message is stored between address 80h and 8Fh. When algorithm 2 is selected and LENGTH16 is set to logic 0, the accepted message is stored between address 80h and BFh. When algorithm 3 is selected, the accepted byte is the same tail trace byte received for 48 frames. When algorithm 3 is selected, the accepted byte is stored at address 80h.

Indirect Register C0H to FFH: RTTP PATH TU3 Expected Trace

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9		Unused	
Bit 8		Unused	
Bit 7	R/W	ETRACE[7]	X
Bit 6	R/W	ETRACE[6]	X
Bit 5	R/W	ETRACE[5]	X
Bit 4	R/W	ETRACE[4]	X
Bit 3	R/W	ETRACE[3]	X
Bit 2	R/W	ETRACE[2]	X
Bit 1	R/W	ETRACE[1]	X
Bit 0	R/W	ETRACE[0]	X

The Expected Trace Indirect Register is provided at RTTP r/w indirect address C0H to FFH.

ETRACE[7:0]

The expected tail trace message (ETRACE[7:0]) bits contain a static message written by an external microprocessor. In algorithm 1 the expected message is used to validated the captured message. In algorithm 2 the expected message is used to validate the accepted message. When LENGTH16 is set to logic 1, the expected message must be written between address C0h and CFh. When LENGTH16 is set to logic 0, the accepted message must be written between address C0h and FFh.

Register 0100H, 0500H, 0900H and 0D00H: RHPP Indirect Address

Bit	Type	Function	Default
Bit 15	R	BUSY	X
Bit 14	R/W	RWB	0
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9	R/W	IADDR[3]	0
Bit 8	R/W	IADDR[2]	0
Bit 7	R/W	IADDR[1]	0
Bit 6	R/W	IADDR[0]	0
Bit 5		Unused	
Bit 4		Unused	
Bit 3	R/W	PATH[3]	0
Bit 2	R/W	PATH[2]	0
Bit 1	R/W	PATH[1]	0
Bit 0	R/W	PATH[0]	0

The Indirect Address Register is provided at RHPP r/w address 00H.

PATH[3:0]

The STS-1/STM-0 path (PATH[3:0]) bits select which STS-1/STM-0 path is accessed by the current indirect transfer.

PATH[3:0]	STS-1/STM-0 path #
0000	Invalid path
0001-1100	Path #1 to Path #12
1101-1111	Invalid path

IADDR[3:0]

The indirect address location (IADDR[3:0]) bits select which address location is accessed by the current indirect transfer.

Indirect Address ADDR[3:0]	Indirect Data
0000	Pointer Interpreter Configuration
0001	Error Monitor Configuration
0010	Pointer Value and ERDI
0011	Captured and Accepted PSL
0100	Expected PSL and PDI

Indirect Address ADDR[3:0]	Indirect Data
0101	Pointer Interpreter status
0110	Path BIP Error Counter
0111	Path REI Error Counter
1000	Path Negative Justification Event Counter
1001	Path Positive Justification Event Counter
1010 to 1111	Unused

RWB

The active high read and active low write (RWB) bit selects if the current access to the internal RAM is an indirect read or an indirect write. Writing to the Indirect Address Register initiates an access to the internal RAM. When RWB is set to logic 1, an indirect read access to the RAM is initiated. The data from the addressed location in the internal RAM will be transferred to the Indirect Data Register. When RWB is set to logic 0, an indirect write access to the RAM is initiated. The data from the Indirect Data Register will be transferred to the addressed location in the internal RAM.

BUSY

The active high RAM busy (BUSY) bit reports if a previously initiated indirect access to the internal RAM has been completed. BUSY is set to logic 1 upon writing to the Indirect Address Register. BUSY is set to logic 0, upon completion of the RAM access. This register should be polled to determine when new data is available in the Indirect Data Register.
Note: Maximum busy bit set time is 22 clock cycles.

Register 0101H, 0501H, 0901H and 0D01H: RHPP Indirect Data

Bit	Type	Function	Default
Bit 15	R/W	DATA[15]	0
Bit 14	R/W	DATA[14]	0
Bit 13	R/W	DATA[13]	0
Bit 12	R/W	DATA[12]	0
Bit 11	R/W	DATA[11]	0
Bit 10	R/W	DATA[10]	0
Bit 9	R/W	DATA[9]	0
Bit 8	R/W	DATA[8]	0
Bit 7	R/W	DATA[7]	0
Bit 6	R/W	DATA[6]	0
Bit 5	R/W	DATA[5]	0
Bit 4	R/W	DATA[4]	0
Bit 3	R/W	DATA[3]	0
Bit 2	R/W	DATA[2]	0
Bit 1	R/W	DATA[1]	0
Bit 0	R/W	DATA[0]	0

The Indirect Data Register is provided at RHPP r/w address 01H.

DATA[15:0]

The indirect access data (DATA[15:0]) bits hold the data transfer to or from the internal RAM during indirect access. When RWB is set to logic 1 (indirect read), the data from the addressed location in the internal RAM will be transferred to DATA[15:0]. BUSY should be polled to determine when the new data is available in DATA[15:0]. When RWB is set to logic 0 (indirect write), the data from DATA[15:0] will be transferred to the addressed location in the internal RAM. The indirect Data register must contain valid data before the indirect write is initiated by writing to the Indirect Address Register.

DATA[15:0] has a different meaning depending on which address of the internal RAM is being accessed.

Register 0102H, 0502H, 0902H and 0D02H: RHPP Payload Configuration

Bit	Type	Function	Default
Bit 15	R/W	STS12CSL	0
Bit 14	R/W	STS12C	0
Bit 13	R/W	Reserved	0
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9		Unused	
Bit 8	R/W	Reserved	0
Bit 7	R/W	Reserved	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	STS3C[4]	0
Bit 2	R/W	STS3C[3]	0
Bit 1	R/W	STS3C[2]	0
Bit 0	R/W	STS3C[1]	0

The Payload Configuration Register is provided at RHPP r/w address 02H.

STS3C[1]

The STS-3c (VC-4) payload configuration (STS3C[1]) bit selects the payload configuration. When STS3C[1] is set to logic 1, the STS-1/STM-0 paths #1, #5 and #9 are part of a STS-3c (VC-4) payload. When STS3C[1] is set to logic 0, the paths are STS-1 (VC-3) payloads. When STS12C is set to logic 1, STS3C[1] must be set to logic 0.

STS3C[2]

The STS-3c (VC-4) payload configuration (STS3C[2]) bit selects the payload configuration. When STS3C[2] is set to logic 1, the STS-1/STM-0 paths #2, #6 and #10 are part of a STS-3c (VC-4) payload. When STS3C[2] is set to logic 0, the paths are STS-1 (VC-3) payloads. When STS12C is set to logic 1, STS3C[2] must be set to logic 0.

STS3C[3]

The STS-3c (VC-4) payload configuration (STS3C[3]) bit selects the payload configuration. When STS3C[3] is set to logic 1, the STS-1/STM-0 paths #3, #7 and #11 are part of a STS-3c (VC-4) payload. When STS3C[3] is set to logic 0, the paths are STS-1 (VC-3) payloads. When STS12C is set to logic 1, STS3C[3] must be set to logic 0.

STS3C[4]

The STS-3c (VC-4) payload configuration (STS3C[4]) bit selects the payload configuration. When STS3C[4] is set to logic 1, the STS-1/STM-0 paths #4, #8 and #12 are part of a STS-3c (VC-4) payload. When STS3C[4] is set to logic 0, the paths are STS-1 (VC-3) payloads. When STS12C is set to logic 1, STS3C[4] must be set to logic 0.

STS12C

The STS-12c (VC-4-4c) payload configuration (STS12C) bit selects the payload configuration. When STS12C is set to logic 1, the STS-1/STM-0 paths #1 to #12 are part of a STS-12c (VC-4-4c) payload. When STS12C is set to logic 0, the STS-1/STM-0 paths are defined with the STS3C[1:4] register bit.

STS12CSL

The slave STS-12c (VC-4-4c) payload configuration (STS12CSL) bit selects the slave payload configuration. When STS12CSL is set to logic 1, the STS-1/STM-0 paths #1 to #12 are part of a STS-12c (VC-4-4c) slave payload. When STS12CSL is set to logic 0, the STS-1/STM-0 paths #1 to # 12 are part of a STS-12c (VC-4-4c) master payload. When STS12C is set to logic 0, STS12CSL must be set to logic 0.

Register 0103H, 0503H, 0903H and 0D03H: RHPP Counter update

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9		Unused	
Bit 8		Unused	
Bit 7		Unused	
Bit 6		Unused	
Bit 5		Unused	
Bit 4		Unused	
Bit 3		Unused	
Bit 2		Unused	
Bit 1		Unused	
Bit 0		Unused	

Any write to the RHPP Counters Update Register (address 0X03H) or to the Master Configuration Register (0000H) will trigger the transfer of all counter values to their holding registers.

Register 0104H, 0504H, 0904H and 0D04H: RHPP Path Interrupt Status

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11	R	P_INT[12]	X
Bit 10	R	P_INT[11]	X
Bit 9	R	P_INT[10]	X
Bit 8	R	P_INT[9]	X
Bit 7	R	P_INT[8]	X
Bit 6	R	P_INT[7]	X
Bit 5	R	P_INT[6]	X
Bit 4	R	P_INT[5]	X
Bit 3	R	P_INT[4]	X
Bit 2	R	P_INT[3]	X
Bit 1	R	P_INT[2]	X
Bit 0	R	P_INT[1]	X

The Path Interrupt Status Register is provided at RHPP read address 04H.

P_INT[1:12]

The Path Interrupt Status bit (P_INT[1:12]) tells which path(s) have interrupts that are still active. Reading from this register will not clear any of the interrupts, it is simply added to reduce the average number of accesses required to service interrupts.

Register 0105H, 0505H, 0905H and 0D05H: RHPP Pointer Concatenation processing Disable

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11	R/W	PTRCDIS[12]	0
Bit 10	R/W	PTRCDIS[11]	0
Bit 9	R/W	PTRCDIS[10]	0
Bit 8	R/W	PTRCDIS[9]	0
Bit 7	R/W	PTRCDIS[8]	0
Bit 6	R/W	PTRCDIS[7]	0
Bit 5	R/W	PTRCDIS[6]	0
Bit 4	R/W	PTRCDIS[5]	0
Bit 3	R/W	PTRCDIS[4]	0
Bit 2	R/W	PTRCDIS[3]	0
Bit 1	R/W	PTRCDIS[2]	0
Bit 0	R/W	PTRCDIS[1]	0

The Pointer Concatenation processing Disable Register is provided at RHPP r/w address 05H.

PTRCDIS[1:12]

The concatenation pointer processing disable (PTRCDIS[1:12]) bits disable the path concatenation pointer interpreter state machine. When PTRCDIS[n] is set to logic 1, the path concatenation pointer interpreter state-machine (for the path n) is disabled and excluded from the LOPC-P, AISC-P and ALLAISC-P defect declaration. When PTRCDIS is set to logic 0, the path concatenation pointer interpreter state-machine is enabled and included in the LOPC-P, AISC-P and ALLAISC-P defect declaration.

Register 0108H, 0508H, 0908H and 0D08H: RHPP Pointer Interpreter Status(STS1/STM0 #1)
Register 0110H, 0510H, 0910H and 0D10H: RHPP Pointer Interpreter Status (STS1/STM0 #2)
Register 0118H, 0518H, 0918H and 0D18H: RHPP Pointer Interpreter Status (STS1/STM0 #3)
Register 0120H, 0520H, 0920H and 0D20H: RHPP Pointer Interpreter Status (STS1/STM0 #4)
Register 0128H, 0528H, 0928H and 0D28H: RHPP Pointer Interpreter Status (STS1/STM0 #5)
Register 0130H, 0530H, 0930H and 0D30H: RHPP Pointer Interpreter Status (STS1/STM0 #6)
Register 0138H, 0538H, 0938H and 0D38H: RHPP Pointer Interpreter Status (STS1/STM0 #7)
Register 0140H, 0540H, 0940H and 0D40H: RHPP Pointer Interpreter Status (STS1/STM0 #8)
Register 0148H, 0548H, 0948H and 0D48H: RHPP Pointer Interpreter Status (STS1/STM0 #9)
Register 0150H, 0550H, 0950H and 0D50H: RHPP Pointer Interpreter Status (STS1/STM0 #10)
Register 0158H, 0558H, 0958H and 0D58H: RHPP Pointer Interpreter Status (STS1/STM0 #11)
Register 0160H, 0560H, 0960H and 0D60H: RHPP Pointer Interpreter Status (STS1/STM0 #12)

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9		Unused	
Bit 8		Unused	
Bit 7		Unused	
Bit 6		Unused	
Bit 5	R	PAISCV	X
Bit 4	R	PLOPCV	X
Bit 3	R	PAISV	X
Bit 2	R	PLOPV	X
Bit 1		Unused	
Bit 0		Unused	

The Pointer Interpreter Status Register is provided at RHPP r/w address 08H 10H 18H 20H 28H 30H 38H 40H 48H 50H 58H and 60H.

PLOPV

The path lost of pointer state (PLOPV) bit indicates the current status of the pointer interpreter state machine. PLOPV is set to logic 1 when the state machine is in the LOP_state. PLOPV is set to logic 0 when the state machine is not in the LOP_state.

PAISV

The path alarm indication signal state (PAISV) bit indicates the current status of the pointer interpreter state machine. PAISV is set to logic 1 when the state machine is in the AIS_state. PAISV is set to logic 0 when the state machine is not in the AIS_state.

PLOPCV

The path lost of pointer concatenation state (PLOPCV) bit indicates the current status of the concatenation pointer interpreter state machine. PLOPCV is set to logic 1 when the state machine is in the LOPC_state. PLOPCV is set to logic 0 when the state machine is not in the LOPC_state.

PAISCV

The path concatenation alarm indication signal state (PAISCV) bit indicates the current status of the concatenation pointer interpreter state machine. PAISCV is set to logic 1 when the state machine is in the AISC_state. PAISCV is set to logic 0 when the state machine is not in the AISC_state.

Register 0109H, 0509H, 0909H and 0D09H: RHPP Pointer Interpreter Interrupt Enable (STS1/STM0 #1)
Register 0111H, 0511H, 0911H and 0D11H: RHPP Pointer Interpreter Interrupt Enable (STS1/STM0 #2)
Register 0119H, 0519H, 0919H and 0D19H: RHPP Pointer Interpreter Interrupt Enable (STS1/STM0 #3)
Register 0121H, 0521H, 0921H and 0D21H: RHPP Pointer Interpreter Interrupt Enable (STS1/STM0 #4)
Register 0129H, 0529H, 0929H and 0D29H: RHPP Pointer Interpreter Interrupt Enable (STS1/STM0 #5)
Register 0131H, 0531H, 0931H and 0D31H: RHPP Pointer Interpreter Interrupt Enable (STS1/STM0 #6)
Register 0139H, 0539H, 0939H and 0D39H: RHPP Pointer Interpreter Interrupt Enable (STS1/STM0 #7)
Register 0141H, 0541H, 0941H and 0D41H: RHPP Pointer Interpreter Interrupt Enable (STS1/STM0 #8)
Register 0149H, 0549H, 0949H and 0D49H: RHPP Pointer Interpreter Interrupt Enable (STS1/STM0 #9)
Register 0151H, 0551H, 0951H and 0D51H: RHPP Pointer Interpreter Interrupt Enable (STS1/STM0 #10)
Register 0159H, 0559H, 0959H and 0D59H: RHPP Pointer Interpreter Interrupt Enable (STS1/STM0 #11)
Register 0161H, 0561H, 0961H and 0D61H: RHPP Pointer Interpreter Interrupt Enable (STS1/STM0 #12)

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9		Unused	
Bit 8		Unused	
Bit 7		Unused	
Bit 6		Unused	
Bit 5	R/W	PAISCE	0
Bit 4	R/W	PLOPCE	0
Bit 3	R/W	PAISE	0
Bit 2	R/W	PLOPE	0
Bit 1		Unused	
Bit 0	R/W	PTRJEE	0

The Pointer Interpreter Interrupt Enable Register is provided at RHPP r/w address 09H 11H 19H 21H 29H 31H 39H 41H 49H 51H 59H and 61H.

PTRJEE

The pointer justification event interrupt enable (PTRJEE) bit control the activation of the interrupt output. When PTRJEE is set to logic 1, the NJEI and PJEI pending interrupt will assert the interrupt output. When PTRJEE is set to logic 0, the NJEI and PJEI pending interrupt will not assert the interrupt output.

PLOPE

The path loss of pointer interrupt enable (PLOPE) bit controls the activation of the interrupt output. When PLOPE is set to logic 1, the PLOPI pending interrupt will assert the interrupt output. When PLOPE is set to logic 0, the PLOPI pending interrupt will not assert the interrupt output.

PAISE

The path alarm indication signal interrupt enable (PAISE) bit controls the activation of the interrupt output. When PAISE is set to logic 1, the PAISI pending interrupt will assert the interrupt output. When PAISE is set to logic 0, the PAISI pending interrupt will not assert the interrupt output.

PLOPCE

The path loss of pointer concatenation interrupt enable (PLOPCE) bit controls the activation of the interrupt output. When PLOPCE is set to logic 1, the PLOPCI pending interrupt will assert the interrupt output. When PLOPCE is set to logic 0, the PLOPCI pending interrupt will not assert the interrupt output.

PAISCE

The path concatenation alarm indication signal interrupt enable (PAISCE) bit controls the activation of the interrupt output. When PAISCE is set to logic 1, the PAISCI pending interrupt will assert the interrupt output. When PAISCE is set to logic 0, the PAISCI pending interrupt will not assert the interrupt output.

Register 010AH, 050AH, 090AH and 0D0AH: RHPP Pointer Interpreter Interrupt Status (STS1/STM0 #1)
Register 0112H, 0512H, 0912H and 0D12H: RHPP Pointer Interpreter Interrupt Status (STS1/STM0 #2)
Register 011AH, 051AH, 091AH and 0D1AH: RHPP Pointer Interpreter Interrupt Status (STS1/STM0 #3)
Register 0122H, 0522H, 0922H and 0D22H: RHPP Pointer Interpreter Interrupt Status (STS1/STM0 #4)
Register 012AH, 052AH, 092AH and 0D2AH: RHPP Pointer Interpreter Interrupt Status (STS1/STM0 #5)
Register 0132H, 0532H, 0932H and 0D32H: RHPP Pointer Interpreter Interrupt Status (STS1/STM0 #6)
Register 013AH, 053AH, 093AH and 0D3AH: RHPP Pointer Interpreter Interrupt Status (STS1/STM0 #7)
Register 0142H, 0542H, 0942H and 0D42H: RHPP Pointer Interpreter Interrupt Status (STS1/STM0 #8)
Register 014AH, 054AH, 094AH and 0D4AH: RHPP Pointer Interpreter Interrupt Status (STS1/STM0 #9)
Register 0152H, 0552H, 0952H and 0D52H: RHPP Pointer Interpreter Interrupt Status (STS1/STM0 #10)
Register 015AH, 055AH, 095AH and 0D5AH: RHPP Pointer Interpreter Interrupt Status (STS1/STM0 #11)
Register 0162H, 0562H, 0962H and 0D62H: RHPP Pointer Interpreter Interrupt Status (STS1/STM0 #12)

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9		Unused	
Bit 8		Unused	
Bit 7		Unused	
Bit 6		Unused	
Bit 5	R	PAISCI	X
Bit 4	R	PLOPCI	X
Bit 3	R	PAISI	X
Bit 2	R	PLOPI	X
Bit 1	R	PJEI	X
Bit 0	R	NJEI	X

The Pointer Interpreter Interrupt Status Register is provided at RHPP r/w address 0AH 12H 1AH 22H 2AH 32H 3AH 42H 4AH 52H 5AH and 62H.

NJEI

The negative pointer justification event interrupt status (NJEI) bit is an event indicator. NJEI is set to logic 1 to indicate a negative pointer justification event. The interrupt status bit is independent of the interrupt enable bit. NJEI is cleared to logic 0 when this register is read.

PJEI

The positive pointer justification event interrupt status (PJEI) bit is an event indicator. PJEI is set to logic 1 to indicate a positive pointer justification event. The interrupt status bit is independent of the interrupt enable bit. PJEI is cleared to logic 0 when this register is read.

PLOPI

The path loss of pointer interrupt status (PLOPI) bit is an event indicator. PLOPI is set to logic 1 to indicate any change in the status of PLOPV (entry to the LOP_state or exit from the LOP_state). The interrupt status bit is independent of the interrupt enable bit. PLOPI is cleared to logic 0 when this register is read.

PAISI

The path alarm indication signal interrupt status (PAISI) bit is an event indicator. PAISI is set to logic 1 to indicate any change in the status of PAISV (entry to the AIS_state or exit from the AIS_state). The interrupt status bit is independent of the interrupt enable bit. PAISI is cleared to logic 0 when this register is read.

PLOPCI

The path loss of pointer concatenation interrupt status (PLOPCI) bit is an event indicator. PLOPCI is set to logic 1 to indicate any change in the status of PLOPCV (entry to the LOPC_state or exit from the LOPC_state). The interrupt status bit is independent of the interrupt enable bit. PLOPCI is cleared to logic 0 when this register is read.

PAISCI

The path concatenation alarm indication signal interrupt status (PAISCI) bit is an event indicator. PAISCI is set to logic 1 to indicate any change in the status of PAISCV (entry to the AISC_state or exit from the AISC_state). The interrupt status bit is independent of the interrupt enable bit. PAISCI is cleared to logic 0 when this register is read.

Register 010BH, 050BH, 090BH and 0D0BH: RHPP Error Monitor Status (STS1/STM0 #1)
Register 0113H, 0513H, 0913H and 0D13H: RHPP Error Monitor Status (STS1/STM0 #2)
Register 011BH, 051BH, 091BH and 0D1BH: RHPP Error Monitor Status (STS1/STM0 #3)
Register 0123H, 0523H, 0923H and 0D23H: RHPP Error Monitor Status (STS1/STM0 #4)
Register 012BH, 052BH, 092BH and 0D2BH: RHPP Error Monitor Status (STS1/STM0 #5)
Register 0133H, 0533H, 0933H and 0D33H: RHPP Error Monitor Status (STS1/STM0 #6)
Register 013BH, 053BH, 093BH and 0D3BH: RHPP Error Monitor Status (STS1/STM0 #7)
Register 0143H, 0543H, 0943H and 0D43H: RHPP Error Monitor Status (STS1/STM0 #8)
Register 014BH, 054BH, 094BH and 0D4BH: RHPP Error Monitor Status (STS1/STM0 #9)
Register 0153H, 0553H, 0953H and 0D53H: RHPP Error Monitor Status (STS1/STM0 #10)
Register 015BH, 055BH, 095BH and 0D5BH: RHPP Error Monitor Status (STS1/STM0 #11)
Register 0163H, 0563H, 0963H and 0D63H: RHPP Error Monitor Status (STS1/STM0 #12)

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9		Unused	
Bit 8		Unused	
Bit 7		Unused	
Bit 6	R	PERDIV	X
Bit 5	R	PRDIV	X
Bit 4	R	PPDIV	X
Bit 3	R	PUNEQV	X
Bit 2	R	PPLMV	X
Bit 1	R	PPLUV	X
Bit 0		Unused	

The Error Monitor Status Register is provided at RHPP r/w address 0BH 13H 1BH 23H 2BH 33H 3BH 43H 4BH 53H 5BH and 63H.

Note: The Error Monitor Status bits are don't care for slave time slots.

PPLUV

The path payload label unstable status (PPLUV) bit indicates the current status of the PLU-P defect.

Algorithm 1: PPLUV is set to logic 0.

Algorithm 2: PPLUV is set to logic 1 when a total of 5 received PSL differs from the previously accepted PSL without any persistent PSL in between. PPLUV is set to logic 0 when a persistent PSL is found. A persistent PSL is found when the same PSL is received for 3 or 5 consecutive frames.

PPLMV

The path payload label mismatch status (PPLMV) bit indicates the current status of the PLM-P defect.

Algorithm 1: PPLMV is set to logic 1 when the received PSL does not match, according to Table 3, the expected PSL for 3 or 5 consecutive frames (selectable with the PSL5 register bit). PPLMV is set to logic 0 when the received PSL matches, according to Table 3, the expected PSL for 3 or 5 consecutive frames.

Algorithm 2: PPLMV is set to logic 1 when the accepted PSL does not match, according to Table 3, the expected PSL. PPLMV is set to logic 0 when the accepted PSL matches, according to Table 3, the expected PSL.

PUNEQV

The path unequipped status (PUNEQV) bit indicates the current status of the UNEQ-P defect.

PUNEQV is set to logic 1 when the received PSL indicates unequipped, according to Table 3, for 3 or 5 consecutive frames (selectable with the PSL5 register bit). An PUNEQV is set to logic 0 when the received PSL indicates not unequipped, according to Table 3, for 3 or 5 consecutive frames.

PPDIV

The path payload defect indication status (PPDIV) bit indicates the current status of the PPDI-P defect.

Algorithm 1: PPDIV is set to logic one when the received PSL is a defect, according to Table 3, for 3 or 5 consecutive frames (selectable with the PSL5 register bit). PPDIV is set to logic 0 when the received PSL is not a defect, according to Table 3, for 3 or 5 consecutive frames.

Algorithm 2: PPDIV is set to logic 1 when the accepted PSL is a defect, according to Table 3. PPDI is set to logic 0 when the accepted PSL is not a defect, according to Table 3.

PRDIV

The path remote defect indication status (PRDIV) bit indicates the current status of the RDI-P defect. PRDIV is set to logic 1 when bit 5 of the G1 byte is set high for five or ten consecutive frames (selectable with the PRDI10 register bit). PRDIV is set to logic 0 when bit 5 of the G1 byte is set low for five or ten consecutive frames.

PERDIV

The path enhanced remote defect indication status (PERDIV) bit indicates the current status of the ERDI-P defect. PERDIV is set to logic 1 when the same 010, 100, 101, 110 or 111 pattern is detected in bits 5, 6 and 7 of the G1 byte for five or ten consecutive frames (selectable with the PRDI10 register bit). PERDIV is set to logic 0 when the same 000, 001 or 011 pattern is detected in bits 5, 6 and 7 of the G1 byte for five or ten consecutive frames.

Register 010CH, 050CH, 090CH and 0D0CH: RHPP Error Monitor Interrupt Enable (STS1/STM0 #1)
Register 0114H, 0514H, 0914H and 0D14H: RHPP Error Monitor Interrupt Enable (STS1/STM0 #2)
Register 011CH, 051CH, 091CH and 0D1CH: RHPP Error Monitor Interrupt Enable (STS1/STM0 #3)
Register 0124H, 0524H, 0924H and 0D24H: RHPP Error Monitor Interrupt Enable (STS1/STM0 #4)
Register 012CH, 052CH, 092CH and 0D2CH: RHPP Error Monitor Interrupt Enable (STS1/STM0 #5)
Register 0134H, 0534H, 0934H and 0D34H: RHPP Error Monitor Interrupt Enable (STS1/STM0 #6)
Register 013CH, 053CH, 093CH and 0D3CH: RHPP Error Monitor Interrupt Enable (STS1/STM0 #7)
Register 0144H, 0544H, 0944H and 0D44H: RHPP Error Monitor Interrupt Enable (STS1/STM0 #8)
Register 014CH, 054CH, 094CH and 0D4CH: RHPP Error Monitor Interrupt Enable (STS1/STM0 #9)
Register 0154H, 0554H, 0954H and 0D54H: RHPP Error Monitor Interrupt Enable (STS1/STM0 #10)
Register 015CH, 055CH, 095CH and 0D5CH: RHPP Error Monitor Interrupt Enable (STS1/STM0 #11)
Register 0164H, 0564H, 0964H and 0D64H: RHPP Error Monitor Interrupt Enable (STS1/STM0 #12)

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9	R/W	PREIEE	0
Bit 8	R/W	PBIPEE	0
Bit 7	R/W	COPERDIE	0
Bit 6	R/W	PERDIE	0
Bit 5	R/W	PRDIE	0
Bit 4	R/W	PPDIE	0
Bit 3	R/W	PUNEQE	0
Bit 2	R/W	PPLME	0
Bit 1	R/W	PPLUE	0
Bit 0	R/W	COPSLE	0

The Error Monitor Interrupt Enable Register is provided at RHPP r/w address 0CH 14H 1CH 24H 2CH 34H 3CH 44H 4CH 54H 5CH and 64H.

COPSLE

The change of path payload signal label interrupt enable (COPSLE) bit controls the activation of the interrupt output. When COPSLE is set to logic 1, the COPSLI pending interrupt will assert the interrupt output. When COPSLE is set to logic 0, the COPSLI pending interrupt will not assert the interrupt output.

PPLUE

The path payload label unstable interrupt enable (PPLUE) bit controls the activation of the interrupt output. When PPLUE is set to logic 1, the PPLUI pending interrupt will assert the interrupt output. When PPLUE is set to logic 0, the PPLUI pending interrupt will not assert the interrupt output.

PPLME

The path payload label mismatch interrupt enable (PPLME) bit controls the activation of the interrupt output. When PPLME is set to logic 1, the PPLMI pending interrupt will assert the interrupt output. When PPLME is set to logic 0, the PPLMI pending interrupt will not assert the interrupt output.

PUNEQE

The path payload unequipped interrupt enable (PUNEQE) bit controls the activation of the interrupt output. When PUNEQE is set to logic 1, the PUNEQI pending interrupt will assert the interrupt output. When PUNEQE is set to logic 0, the PUNEQI pending interrupt will not assert the interrupt output.

PPDIE

The path payload defect indication interrupt enable (PPDIE) bit controls the activation of the interrupt output. When PPDIE is set to logic 1, the PPDI pending interrupt will assert the interrupt output. When PPDIE is set to logic 0, the PPDI pending interrupt will not assert the interrupt output.

PRDIE

The path remote defect indication interrupt enable (PRDIE) bit controls the activation of the interrupt output. When PRDIE is set to logic 1, the PRDII pending interrupt will assert the interrupt output. When PRDIE is set to logic 0, the PRDII pending interrupt will not assert the interrupt output.

PERDIE

The path enhanced remote defect indication interrupt enable (PERDIE) bit controls the activation of the interrupt output. When PERDIE is set to logic 1, the PERDII pending interrupt will assert the interrupt output. When PERDIE is set to logic 0, the PERDII pending interrupt will not assert the interrupt output.

COPERDIE

The change of path enhanced remote defect indication interrupt enable (COPERDIE) bit controls the activation of the interrupt output. When COPERDIE is set to logic 1, the COPERDII pending interrupt will assert the interrupt output. When COPERDIE is set to logic 0, the COPERDII pending interrupt will not assert the interrupt output.

PBIPEE

The path BIP-8 error interrupt enable (PBIPEE) bit controls the activation of the interrupt output. When PBIPEE is set to logic 1, the PBIPEI pending interrupt will assert the interrupt output. When PBIPEE is set to logic 0, the PBIPEI pending interrupt will not assert the interrupt output.

PREIEE

The path REI error interrupt enable (PREIEE) bit controls the activation of the interrupt output. When PREIEE is set to logic 1, the PREIEI pending interrupt will assert the interrupt output. When PREIEE is set to logic 0, the PREIEI pending interrupt will not assert the interrupt output.

Register 010DH, 050DH, 090DH and 0D0DH: RHPP Error Monitor Interrupt Status (STS1/STM0 #1)
Register 0115H, 0515H, 0915H and 0D15H: RHPP Error Monitor Interrupt Status (STS1/STM0 #2)
Register 011DH, 051DH, 091DH and 0D1DH: RHPP Error Monitor Interrupt Status (STS1/STM0 #3)
Register 0125H, 0525H, 0925H and 0D25H: RHPP Error Monitor Interrupt Status (STS1/STM0 #4)
Register 012DH, 052DH, 092DH and 0D2DH: RHPP Error Monitor Interrupt Status (STS1/STM0 #5)
Register 0135H, 0535H, 0935H and 0D35H: RHPP Error Monitor Interrupt Status (STS1/STM0 #6)
Register 013DH, 053DH, 093DH and 0D3DH: RHPP Error Monitor Interrupt Status (STS1/STM0 #7)
Register 0145H, 0545H, 0945H and 0D45H: RHPP Error Monitor Interrupt Status (STS1/STM0 #8)
Register 014DH, 054DH, 094DH and 0D4DH: RHPP Error Monitor Interrupt Status (STS1/STM0 #9)
Register 0155H, 0555H, 0955H and 0D55H: RHPP Error Monitor Interrupt Status (STS1/STM0 #10)
Register 015DH, 055DH, 095DH and 0D5DH: RHPP Error Monitor Interrupt Status (STS1/STM0 #11)
Register 0165H, 0565H, 0965H and 0D65H: RHPP Error Monitor Interrupt Status (STS1/STM0 #12)

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9	R	PREIEI	X
Bit 8	R	PBIPEI	X
Bit 7	R	COPERDII	X
Bit 6	R	PERDII	X
Bit 5	R	PRDII	X
Bit 4	R	PPDII	X
Bit 3	R	PUNEQI	X
Bit 2	R	PPLMI	X
Bit 1	R	PPLUI	X
Bit 0	R	COPSLI	X

The Error Monitor Interrupt Status Register is provided at RHPP r/w address 0DH 15H 1DH 25H 2DH 35H 3DH 45H 4DH 55H 5DH and 65H.

COPSLI

The change of path payload signal label interrupt status (COPSLI) bit is an event indicator. COPSLI is set to logic 1 to indicate a new PSL-P value. The interrupt status bit is independent of the interrupt enable bit. COPSLI is cleared to logic 0 when this register is read. ALGO2 register bit has no effect on COPSLI.

PPLUI

The path payload label unstable interrupt status (PPLUI) bit is an event indicator. PPLUI is set to logic 1 to indicate any change in the status of PPLUV (stable to unstable or unstable to stable). The interrupt status bit is independent of the interrupt enable bit. PPLUI is cleared to logic 0 when this register is read.

PPLMI

The path payload label mismatch interrupt status (PPLMI) bit is an event indicator. PPLMI is set to logic 1 to indicate any change in the status of PPLMV (match to mismatch or mismatch to match). The interrupt status bit is independent of the interrupt enable bit. PPLMI is cleared to logic 0 when this register is read.

PUNEQI

The path payload unequipped interrupt status (PUNEQI) bit is an event indicator. PUNEQI is set to logic 1 to indicate any change in the status of PUNEQV (equipped to unequipped or unequipped to equipped). The interrupt status bit is independent of the interrupt enable bit. PUNEQI is cleared to logic 0 when this register is read.

PPDII

The path payload defect indication interrupt status (PPDII) bit is an event indicator. PPDII is set to logic 1 to indicate any change in the status of PPDIV (no defect to payload defect or payload defect to no defect). The interrupt status bit is independent of the interrupt enable bit. PPDII is cleared to logic 0 when this register is read.

PRDII

The path remote defect indication interrupt status (PRDII) bit is an event indicator. PRDII is set to logic 1 to indicate any change in the status of PRDIV (no defect to RDI defect or RDI defect to no defect). The interrupt status bit is independent of the interrupt enable bit. PRDII is cleared to logic 0 when this register is read.

PERDII

The path enhanced remote defect indication interrupt status (PERDII) bit is an event indicator. PERDII is set to logic 1 to indicate any change in the status of PERDIV (no defect to ERDI defect or ERDI defect to no defect). The interrupt status bit is independent of the interrupt enable bit. PERDII is cleared to logic 0 when this register is read.

COPERDII

The change of path enhanced remote defect indication interrupt status (COPERDII) bit is an event indicator. COPERDII is set to logic 1 to indicate a new ERDI-P value. The interrupt status bit is independent of the interrupt enable bit. COPERDII is cleared to logic 0 when this register is read.

PBIPEI

The path BIP-8 error interrupt status (PBIPEI) bit is an event indicator. PBIPEI is set to logic 1 to indicate a path BIP-8 error. The interrupt status bit is independent of the interrupt enable bit. PBIPEI is cleared to logic 0 when this register is read.

PREIEI

The path REI error interrupt status (PREIEI) bit is an event indicator. PREIEI is set to logic 1 to indicate a path REI error. The interrupt status bit is independent of the interrupt enable bit. PREIEI is cleared to logic 0 when this register is read.

Indirect Register 00H: RHPP Pointer Interpreter Configuration

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9		Unused	
Bit 8		Unused	
Bit 7	R/W	Reserved	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	NDFCNT	0
Bit 4	R/W	INVCNT	0
Bit 3	R/W	RELAYPAIS	0
Bit 2	R/W	JUST3DIS	0
Bit 1	R/W	SSEN	0
Bit 0		Unused	

The Pointer Interpreter Configuration Indirect Register is provided at RHPP r/w indirect address 00H.

SSEN

The SS bits enable (SSEN) bit selects whether or not the SS bits are taking into account in the pointer interpreter state machine. When SSEN is set to logic 1, the SS bits must be set to 10 for a valid NORM_POINT, NDF_ENABLE, INC_IND, DEC_IND or NEW_POINT indication. When SSEN is set to logic 0, the SS bits are ignored.

JUST3DIS

The “justification more than 3 frames ago disable” (JUST3DIS) bit selects whether or not the NDF_ENABLE, INC_IND or DEC_IND pointer justifications must be more than 3 frames apart to be considered valid. When JUST3DIS is set to logic 0, the previous NDF_ENABLE, INC_IND or DEC_IND indication must be more than 3 frames ago or the present NDF_ENABLE, INC_IND or DEC_IND indication is considered an INV_POINT indication. When JUST3DIS is set to logic 1, NDF_ENABLE, INC_IND or DEC_IND indication can be every frame.

RELAYPAIS

The relay path AIS (RELAYPAIS) bit selects the condition to enter the path AIS state in the pointer interpreter state machine. When RELAYPAIS is set to logic 1, the path AIS state is entered with 1 X AIS_ind indication. When RELAYPAIS is set to logic 0, the path AIS state is entered with 3 X AIS_ind indications. This configuration bit also affects the concatenation pointer interpreter state machine.

INVCNT

The invalid counter (INVCNT) bit selects the behavior of the consecutive INV_POINT event counter in the pointer interpreter state machine. When INVCNT is set to logic 1, the consecutive INV_POINT event counter is reset by 3 EQ_NEW_POINT indications. When INVCNT is set to logic 0, the counter is not reset by 3 EQ_NEW_POINT indications.

NDFCNT

The new data flag counter (NDFCNT) bit selects the behavior of the consecutive NDF_ENABLE event counter in the pointer interpreter state machine. When NDFCNT is set to logic 1, the NDF_ENABLE definition is enabled NDF + SS. When NDFCNT is set to logic 0, the NDF_ENABLE definition is enabled NDF + SS + offset value in the range 0 to 782 (764 in TU-3 mode). This configuration bit only changes the NDF_ENABLE definition for the consecutive NDF_ENABLE even counter to count towards LOP-P defect when the pointer is out of range, this configuration bit does not change the NDF_ENABLE definition for pointer justification.

Indirect Register 01H: RHPP Error Monitor Configuration

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11	R/W	B3EONRPOH	0
Bit 10	R/W	IPREIBLK	0
Bit 9	R/W	IBER	0
Bit 8	R/W	PREIBLKACC	0
Bit 7	R/W	B3EBLK	0
Bit 6	R/W	PBIPEBLKREI	0
Bit 5	R/W	PBIPEBLKACC	0
Bit 4	R/W	FSBIPDIS	0
Bit 3	R/W	PRDI10	0
Bit 2	R/W	PLMEND	0
Bit 1	R/W	PSL5	0
Bit 0	R/W	ALGO2	0

The Error Monitor Configuration Indirect Register is provided at RHPP r/w indirect address 01H.

ALGO2

The payload signal label algorithm 2 (ALGO2) bit selects the algorithm for the PSL monitoring. When ALGO2 is set to logic 1, the ITU compliant algorithm is (algorithm 2) is used to monitor the PSL. When ALGO2 is set to logic 0, the BELLCORE compliant algorithm (algorithm 1) is used to monitor the PSL. ALGO2 changes the PLU-P, PLM-P and PDI-P defect definitions but has no effect on UNEQ-P defect, accepted PSL and change of PSL definitions

PSL5

The payload signal label detection (PSL5) bit selects the path PSL persistence. When PSL5 is set to logic 1, a new PSL is accepted when the same PSL value is detected in the C2 byte for five consecutive frames. When PSL5 is set to logic 0, a new PSL is accepted when the same PSL value is detected in the C2 byte for three consecutive frames.

PLMEND

The payload label mismatch removal (PLMEND) bit controls the removal of a PLM-P defect when an UNEQ-P defect is declared. When PLMEND is set to logic 1, a PLM-P defect is terminated when an UNEQ-P defect is declared. When PLMEND is set to logic 0, a PLM-P defect is not terminated when an UNEQ-P defect is declared.

PRDI10

The path remote defect indication detection (PRDI10) bit selects the path RDI and path ERDI persistence. When PRDI10 is set to logic 1, path RDI and path ERDI are accepted when the same pattern is detected in bits 5,6,7 of the G1 byte for ten consecutive frames. When PRDI10 is set to logic 0, path RDI and path ERDI are accepted when the same pattern is detected in bits 5,6,7 of the G1 byte for five consecutive frames.

FSBIPDIS

The disable fixed stuff columns during BIP-8 calculation (FSBIPDIS) bit controls the path BIP-8 calculation for an STS-1 (VC-3) payload. When FSBIPDIS is set to logic 1, the fixed stuff columns are not part of the BIP-8 calculation when processing an STS-1 (VC-3) payload. When FSBIPDIS is set to logic 0, the fixed stuff columns are part of the BIP-8 calculation when processing an STS-1 (VC-3) payload.

PBIPEBLKACC

The path block BIP-8 errors accumulation (PBIPEBLKACC) bit controls the accumulation of path BIP-8 errors. When PBIPEBLKACC is set to logic 1, the path BIP-8 error accumulation represents block BIP-8 errors (a maximum of 1 error per frame). When PBIPEBLKACC is set to logic 0, the path BIP-8 error accumulation represents BIP-8 errors (a maximum of 8 errors per frame).

PBIPEBLKREI

The path block BIP-8 errors (PBIPEBLKREI) bit controls the path REI errors returned to the THPP. When PBIPEBLKREI is set to logic 1, the path REI is updated with block BIP-8 errors (a maximum of 1 error per frame). When PBIPEBLKREI is set to logic 0, the path REI is updated with BIP-8 errors (a maximum of 8 errors per frame).

B3EBLK

The serial path block BIP-8 errors (B3EBLK) bit controls the indication of path BIP-8 errors on the B3E serial output. When B3EBLK is set to logic 1, B3E outputs block BIP-8 errors (a maximum of 1 error per frame). When B3EBLK is set to logic 0, B3E outputs BIP-8 errors (a maximum of 8 errors per frame).

PREIBLKACC

The path block REI errors accumulation (PREIBLKACC) bit controls the accumulation of path REI errors from the path status (G1) byte. When PREIBLK is set to logic 1, the extracted path REI errors are interpreted as block BIP-8 errors (a maximum of 1 error per frame). When PREIBLK is set to logic 0, the extracted path REI errors are interpret as BIP-8 errors (a maximum of 8 errors per frame).

IBER

The inband error reporting (IBER) bit controls the inband regeneration of the path status (G1) byte. When IBER is set to logic 1, the path status byte is updated with the REI-P and the ERDI-P defects that must be returned to the far end. When IBER is set to logic 0, the path status byte is not altered.

IPREIBLK

The inband path REI block errors (IPREIBLK) bit controls the regeneration of the path REI errors in the path status (G1) byte. When IPREIBLK is set to logic 1, the path REI is updated with block BIP-8 errors (a maximum of 1 error per frame). When IPREIBLK is set to logic 0, the path REI is updated with BIP-8 errors (a maximum of 8 errors per frame).

B3EONRPOH

The B3EONRPOH bit controls the data presented on RPOH ports. When set to logic 0, the received B3 byte is place on RPOH port. When set to logic 1, the B3 error count is placed on the RPOH port as placed on the B3E port.

Indirect Register 02H: RHPP Pointer value and ERDI

Bit	Type	Function	Default
Bit 15	R	PERDIV[2]	X
Bit 14	R	PERDIV[1]	X
Bit 13	R	PERDIV[0]	X
Bit 12		Unused	
Bit 11	R	SSV[1]	X
Bit 10	R	SSV[0]	X
Bit 9	R	PTRV[9]	X
Bit 8	R	PTRV[8]	X
Bit 7	R	PTRV[7]	X
Bit 6	R	PTRV[6]	X
Bit 5	R	PTRV[5]	X
Bit 4	R	PTRV[4]	X
Bit 3	R	PTRV[3]	X
Bit 2	R	PTRV[2]	X
Bit 1	R	PTRV[1]	X
Bit 0	R	PTRV[0]	X

The Pointer Value Indirect Register is provided at RHPP r/w address 02H.

PTRV[9:0]

The path pointer value (PTRV[9:0]) bits represent the current STS (AU or TU3) pointer being process by the pointer interpreter state machine or by the concatenation pointer interpreter state machine.

SSV[1:0]

The SS value (SSV[1:0]) bits represent the current SS (DD) bits being processed by the pointer interpreter state machine or by the concatenation pointer interpreter state machine.

PERDIV[2:0]

The path enhanced remote defect indication value (PERDIV[2:0]) bits represent the filtered path enhanced remote defect indication value. PERDIV[2:0] is updated when the same ERDI pattern is detected in bits 5,6,7 of the G1 byte for five or ten consecutive frames (selectable with the PRDI10 register bit).

Indirect Register 03H: RHPP captured and accepted PSL

Bit	Type	Function	Default
Bit 15	R	CPSLV[7]	X
Bit 14	R	CPSLV[6]	X
Bit 13	R	CPSLV[5]	X
Bit 12	R	CPSLV[4]	X
Bit 11	R	CPSLV[3]	X
Bit 10	R	CPSLV[2]	X
Bit 9	R	CPSLV[1]	X
Bit 8	R	CPSLV[0]	X
Bit 7	R	APSLV[7]	X
Bit 6	R	APSLV[6]	X
Bit 5	R	APSLV[5]	X
Bit 4	R	APSLV[4]	X
Bit 3	R	APSLV[3]	X
Bit 2	R	APSLV[2]	X
Bit 1	R	APSLV[1]	X
Bit 0	R	APSLV[0]	X

The Accepted PSL and ERDI Indirect Register is provided at RHPP r/w address 03H.

APSLV[7:0]

The accepted path signal label value (APSLV[7:0]) bits represent the last accepted path signal label value. A new PSL is accepted when the same PSL value is detected in the C2 byte for three or five consecutive frames. (selectable with the PSL5 register bit).

CPSLV[7:0]

The captured path signal label value (CPSLV[7:0]) bits represent the last captured path signal label value. A new PSL is captured every frame from the C2 byte.

Indirect Register 04H: RHPP Expected PSL and PDI

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13	R/W	PDIRANGE	0
Bit 12	R/W	PDI[4]	0
Bit 11	R/W	PDI[3]	0
Bit 10	R/W	PDI[2]	0
Bit 9	R/W	PDI[1]	0
Bit 8	R/W	PDI[0]	0
Bit 7	R/W	EPSL[7]	0
Bit 6	R/W	EPSL[6]	0
Bit 5	R/W	EPSL[5]	0
Bit 4	R/W	EPSL[4]	0
Bit 3	R/W	EPSL[3]	0
Bit 2	R/W	EPSL[2]	0
Bit 1	R/W	EPSL[1]	0
Bit 0	R/W	EPSL[0]	0

The Expected PSL and PDI Indirect Register is provided at RHPP r/w indirect address 04H.

EPSL[7:0]

The expected path signal label (EPSL[7:0]) bits represent the expected path signal label. The expected PSL and the expected PDI validate the received or the accepted PSL to declare PLM-P, UNEQ-P and PDI-P defects according Table 3.

PDI[4:0], PDIRANGE

The payload defect indication (PDI[4:0]) bits and the payload defect indication range (PDIRANGE) bit determine the expected payload defect indication according to Table 4. When PDIRANGE is set to logic 1, the PDI range is enabled and the expected PDI range is from E1H to E0H+PDI[4:0]. When PDIRANGE is set to logic 0, the PDI range is disable and the expected PDI value is E0H+PDI[4:0]. The expected PSL and the expected PDI validate the received or the accepted PSL to declare PLM-P, UNEQ-P and PDI-P defects according Table 3.

Indirect Register 05H: RHPP Pointer Interpreter status

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9		Unused	
Bit 8		Unused	
Bit 7		Unused	
Bit 6	R	NDF	X
Bit 5	R	ILLPTR	X
Bit 4	R	INVNDF	X
Bit 3	R	DISCOPA	X
Bit 2	R	CONCAT	X
Bit 1	R	ILLJREQ	X
Bit 0		Unused	

The Pointer Interpreter Status Indirect Register is provided at RHPP r/w indirect address 05H.

Note: The Pointer Interpreter Status bits are don’t care for slave time slots.

ILLJREQ

The illegal pointer justification request (ILLJREQ) signal is set high when a positive and/or negative pointer adjustment is received within three frames of a pointer justification event (inc_ind, dec_ind) or an NDF triggered active offset adjustment (NDF_enable).

CONCAT

The CONCAT bit is set high if the H1 and H2 pointer bytes received matche the concatenation indication (one of the five NDF_enable patterns in the NDF field, don't care in the size field, and all-ones in the pointer offset field).

DISCOPA

The discontinuous change of pointer alignment (DISCOPA) signal is set high when there is a pointer adjustment due to receiving a pointer repeated three times.

INVNDF

The invalid new data flag (INVNDF) signal is set high when an invalid NDF code is received.

ILLPTR

The illegal pointer offset (ILLPTR) signal is set high when the pointer received is out of the range. Legal values are from 0 to 782 (764 in TU3 mode). Pointer justification requests (inc_req, dec_req) and AIS indications (AIS_ind) are not considered illegal.

NDF

The new data flag (NDF) signal is set high when an enabled New Data Flag is received indicating a pointer adjustment (NDF_enabled indication).

Indirect Register 06H: RHPP Path BIP Error Counter

Bit	Type	Function	Default
Bit 15	R	PBIPE[15]	X
Bit 14	R	PBIPE[14]	X
Bit 13	R	PBIPE[13]	X
Bit 12	R	PBIPE[12]	X
Bit 11	R	PBIPE[11]	X
Bit 10	R	PBIPE[10]	X
Bit 9	R	PBIPE[9]	X
Bit 8	R	PBIPE[8]	X
Bit 7	R	PBIPE[7]	X
Bit 6	R	PBIPE[6]	X
Bit 5	R	PBIPE[5]	X
Bit 4	R	PBIPE[4]	X
Bit 3	R	PBIPE[3]	X
Bit 2	R	PBIPE[2]	X
Bit 1	R	PBIPE[1]	X
Bit 0	R	PBIPE[0]	X

The Path BIP Error Counter register is provided at RHPP r/w indirect address 06H.

PBIPE[15:0]

The path BIP error (PBIPE[15:0]) bits represent the number of path BIP errors that have been detected in the B3 byte since the last accumulation interval. The error counters are transferred to the holding registers by a microprocessor write to the RHPP Counters Update register.

Indirect Register 07H: RHPP Path REI Error Counter

Bit	Type	Function	Default
Bit 15	R	PREIE[15]	X
Bit 14	R	PREIE[14]	X
Bit 13	R	PREIE[13]	X
Bit 12	R	PREIE[12]	X
Bit 11	R	PREIE[11]	X
Bit 10	R	PREIE[10]	X
Bit 9	R	PREIE[9]	X
Bit 8	R	PREIE[8]	X
Bit 7	R	PREIE[7]	X
Bit 6	R	PREIE[6]	X
Bit 5	R	PREIE[5]	X
Bit 4	R	PREIE[4]	X
Bit 3	R	PREIE[3]	X
Bit 2	R	PREIE[2]	X
Bit 1	R	PREIE[1]	X
Bit 0	R	PREIE[0]	X

The Path BIP Error Counter register is provided at RHPP r/w indirect address 07H.

PREIE[15:0]

The path REI error (PREIE[15:0]) bits represent the number of path REI errors that have been extracted from the G1 byte since the last accumulation interval. The error counters are transferred to the holding registers by a microprocessor write to the RHPP Counters Update register.

Indirect Register 08H: RHPP Path Negative Justification Event Counter

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12	R	PNJE[12]	X
Bit 11	R	PNJE[11]	X
Bit 10	R	PNJE[10]	X
Bit 9	R	PNJE[9]	X
Bit 8	R	PNJE[8]	X
Bit 7	R	PNJE[7]	X
Bit 6	R	PNJE[6]	X
Bit 5	R	PNJE[5]	X
Bit 4	R	PNJE[4]	X
Bit 3	R	PNJE[3]	X
Bit 2	R	PNJE[2]	X
Bit 1	R	PNJE[1]	X
Bit 0	R	PNJE[0]	X

The Path Negative Justification Event Counter register is provided at RHPP r/w indirect address 08H.

PNJE[12:0]

The Path Negative Justification Event (PNJE[12:0]) bits represent the number of Path Negative Justification Events that have occurred since the last accumulation interval. The event counters are transferred to the holding registers by a microprocessor write to RHPP Counters Update register.

Indirect Register 09H: RHPP Path Positive Justification Event Counter

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12	R	PPJE[12]	X
Bit 11	R	PPJE[11]	X
Bit 10	R	PPJE[10]	X
Bit 9	R	PPJE[9]	X
Bit 8	R	PPJE[8]	X
Bit 7	R	PPJE[7]	X
Bit 6	R	PPJE[6]	X
Bit 5	R	PPJE[5]	X
Bit 4	R	PPJE[4]	X
Bit 3	R	PPJE[3]	X
Bit 2	R	PPJE[2]	X
Bit 1	R	PPJE[1]	X
Bit 0	R	PPJE[0]	X

The Path Positive Justification Event Counter register is provided at RHPP r/w indirect address 09H.

PPJE[12:0]

The Path Positive Justification Event (PPJE[12:0]) bits represent the number of Path Positive Justification Events that have occurred since the last accumulation interval. The event counters are transferred to the holding registers by a microprocessor write to RHPP Counters Update register.

Register 0180H, 0580H, 0980H and 0D80H: RHPP TU3 Indirect Address

Bit	Type	Function	Default
Bit 15	R	BUSY	X
Bit 14	R/W	RWB	0
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9	R/W	IADDR[3]	0
Bit 8	R/W	IADDR[2]	0
Bit 7	R/W	IADDR[1]	0
Bit 6	R/W	IADDR[0]	0
Bit 5		Unused	
Bit 4		Unused	
Bit 3	R/W	PATH[3]	0
Bit 2	R/W	PATH[2]	0
Bit 1	R/W	PATH[1]	0
Bit 0	R/W	PATH[0]	0

The Indirect Address Register is provided at RHPP r/w address 00H.

PATH[3:0]

The STS-1/STM-0 path (PATH[3:0]) bits select which STS-1/STM-0 path is accessed by the current indirect transfer.

PATH[3:0]	STS-1/STM-0 path #
0000	Invalid path
0001-1100	Path #1 to Path #12
1101-1111	Invalid path

IADDR[3:0]

The indirect address location (IADDR[2:0]) bits select which address location is accessed by the current indirect transfer.

Indirect Address ADDR[3:0]	Indirect Data
0000	Pointer Interpreter Configuration
0001	Error Monitor Configuration
0010	Pointer Value and ERDI
0011	Captured and Accepted PSL

Indirect Address ADDR[3:0]	Indirect Data
0100	Expected PSL and PDI
0101	Pointer Interpreter status
0110	Path BIP Error Counter
0111	Path REI Error Counter
1000	Path Negative Justification Event Counter
1001	Path Positive Justification Event Counter
1010 to 1111	Unused

RWB

The active high read and active low write (RWB) bit selects if the current access to the internal RAM is an indirect read or an indirect write. Writing to the Indirect Address Register initiates an access to the internal RAM. When RWB is set to logic 1, an indirect read access to the RAM is initiated. The data from the addressed location in the internal RAM will be transferred to the Indirect Data Register. When RWB is set to logic 0, an indirect write access to the RAM is initiated. The data from the Indirect Data Register will be transferred to the addressed location in the internal RAM.

BUSY

The active high RAM busy (BUSY) bit reports if a previously initiated indirect access to the internal RAM has been completed. BUSY is set to logic 1 upon writing to the Indirect Address Register. BUSY is set to logic 0, upon completion of the RAM access. This register should be polled to determine when new data is available in the Indirect Data Register.
Note: Maximum busy bit set time is 22 clock cycles.

Register 0181H, 0581H, 0981H and 0D81H: RHPP TU3 Indirect Data

Bit	Type	Function	Default
Bit 15	R/W	DATA[15]	0
Bit 14	R/W	DATA[14]	0
Bit 13	R/W	DATA[13]	0
Bit 12	R/W	DATA[12]	0
Bit 11	R/W	DATA[11]	0
Bit 10	R/W	DATA[10]	0
Bit 9	R/W	DATA[9]	0
Bit 8	R/W	DATA[8]	0
Bit 7	R/W	DATA[7]	0
Bit 6	R/W	DATA[6]	0
Bit 5	R/W	DATA[5]	0
Bit 4	R/W	DATA[4]	0
Bit 3	R/W	DATA[3]	0
Bit 2	R/W	DATA[2]	0
Bit 1	R/W	DATA[1]	0
Bit 0	R/W	DATA[0]	0

The Indirect Data Register is provided at RHPP r/w address 01H.

DATA[15:0]

The indirect access data (DATA[15:0]) bits hold the data transfer to or from the internal RAM during indirect access. When RWB is set to logic 1 (indirect read), the data from the addressed location in the internal RAM will be transferred to DATA[15:0]. BUSY should be polled to determine when the new data is available in DATA[15:0]. When RWB is set to logic 0 (indirect write), the data from DATA[15:0] will be transferred to the addressed location in the internal RAM. The indirect Data register must contain valid data before the indirect write is initiated by writing to the Indirect Address Register.

DATA[15:0] has a different meaning depending on which address of the internal RAM is being accessed.

Register 0182H, 0582H, 0982H and 0D82H: RHPP TU3 Payload Configuration

Bit	Type	Function	Default
Bit 15	R/W	Reserved	0
Bit 14	R/W	Reserved	0
Bit 13	R/W	Reserved	0
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9		Unused	
Bit 8	R/W	Reserved	0
Bit 7	R/W	TUG3[4]	0
Bit 6	R/W	TUG3[3]	0
Bit 5	R/W	TUG3[2]	0
Bit 4	R/W	TUG3[1]	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	Reserved	0

The Payload Configuration Register is provided at RHPP r/w address 02H.

TUG3[1]

The TUG3 payload configuration (TUG3[1]) bit selects the payload configuration. When TUG3[1] is set to logic 1, the STS-1/STM-0 paths #1, #5 and #9 are part of a TUG3 payload. When TUG3[1] is set to logic 0, the paths are not part of a TUG3 payloads.

TUG3[2]

The TUG3 payload configuration (TUG3[2]) bit selects the payload configuration. When TUG3[2] is set to logic 1, the STS-1/STM-0 paths #2, #6 and #10 are part of a TUG3 payload. When TUG3[2] is set to logic 0, the paths are not part of a TUG3 payloads.

TUG3[3]

The TUG3 payload configuration (TUG3[3]) bit selects the payload configuration. When TUG3[3] is set to logic 1, the STS-1/STM-0 paths #3, #7 and #11 are part of a TUG3 payload. When TUG3[3] is set to logic 0, the paths are not part of a TUG3 payloads.

TUG3[4]

The TUG3 payload configuration (TUG3[4]) bit selects the payload configuration. When TUG3[4] is set to logic 1, the STS-1/STM-0 paths #4, #8 and #12 are part of a TUG3 payload. When TUG3[4] is set to logic 0, the paths are not part of a TUG3 payloads.

Register 0183H, 0583H, 0983H and 0D83H: RHPP TU3 Counters update

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9		Unused	
Bit 8		Unused	
Bit 7		Unused	
Bit 6		Unused	
Bit 5		Unused	
Bit 4		Unused	
Bit 3		Unused	
Bit 2		Unused	
Bit 1		Unused	
Bit 0		Unused	

Any write to the RHPP Counters Update Register (address 0X83H) or to the Master Configuration Register (0000H) will trigger the transfer of all counter values to their holding registers.

Register 0184H, 0584H, 0984H and 0D84H: RHPP TU3 Path Interrupt Status

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11	R	P_INT[12]	X
Bit 10	R	P_INT[11]	X
Bit 9	R	P_INT[10]	X
Bit 8	R	P_INT[9]	X
Bit 7	R	P_INT[8]	X
Bit 6	R	P_INT[7]	X
Bit 5	R	P_INT[6]	X
Bit 4	R	P_INT[5]	X
Bit 3	R	P_INT[4]	X
Bit 2	R	P_INT[3]	X
Bit 1	R	P_INT[2]	X
Bit 0	R	P_INT[1]	X

The Path Interrupt Status Register is provided at RHPP read address 04H.

P_INT[1:12]

The Path Interrupt Status bit (P_INT[1:12]) tells which path(s) have interrupts that are still active. Reading from this register will not clear any of the interrupts, it is simply added to reduce the average number of accesses required to service interrupts.

Register 0188H, 0588H, 0988H and 0D88H: RHPP TU3 Pointer Interpreter Status(STS1/STM0 #1)
Register 0190H, 0590H, 0990H and 0D90H: RHPP TU3 Pointer Interpreter Status (STS1/STM0 #2)
Register 0198H, 0598H, 0998H and 0D98H: RHPP TU3 Pointer Interpreter Status (STS1/STM0 #3)
Register 01A0H, 05A0H, 09A0H and 0DA0H: RHPP TU3 Pointer Interpreter Status (STS1/STM0 #4)
Register 01A8H, 05A8H, 09A8H and 0DA8H: RHPP TU3 Pointer Interpreter Status (STS1/STM0 #5)
Register 01B0H, 05B0H, 09B0H and 0DB0H: RHPP TU3 Pointer Interpreter Status (STS1/STM0 #6)
Register 01B8H, 05B8H, 09B8H and 0DB8H: RHPP TU3 Pointer Interpreter Status (STS1/STM0 #7)
Register 01C0H, 05C0H, 09C0H and 0DC0H: RHPP TU3 Pointer Interpreter Status (STS1/STM0 #8)
Register 01C8H, 05C8H, 09C8H and 0DC8H: RHPP TU3 Pointer Interpreter Status (STS1/STM0 #9)
Register 01D0H, 05D0H, 09D0H and 0DD0H: RHPP TU3 Pointer Interpreter Status (STS1/STM0 #10)
Register 01D8H, 05D8H, 09D8H and 0DD8H: RHPP TU3 Pointer Interpreter Status (STS1/STM0 #11)
Register 01E0H, 05E0H, 09E0H and 0DE0H: RHPP TU3 Pointer Interpreter Status (STS1/STM0 #12)

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9		Unused	
Bit 8		Unused	
Bit 7		Unused	
Bit 6		Unused	
Bit 5	R	Reserved	X
Bit 4	R	Reserved	X
Bit 3	R	PAISV	X
Bit 2	R	PLOPV	X
Bit 1		Unused	
Bit 0		Unused	

The Pointer Interpreter Status Register is provided at RHPP r/w address 08H 10H 18H 20H 28H 30H 38H 40H 48H 50H 58H and 60H.

PLOPV

The path lost of pointer state (PLOPV) bit indicates the current status of the pointer interpreter state machine. PLOPV is set to logic 1 when the state machine is in the LOP_state. PLOPV is set to logic 0 when the state machine is not in the LOP_state.

PAISV

The path alarm indication signal state (PAISV) bit indicates the current status of the pointer interpreter state machine. PAISV is set to logic 1 when the state machine is in the AIS_state. PAISV is set to logic 0 when the state machine is not in the AIS_state.

Register 0189H, 0589H, 0989H and 0D89H: RHPP TU3 Pointer Interpreter Interrupt Enable (STS1/STM0 #1)
Register 0191H, 0591H, 0991H and 0D91H: RHPP TU3 Pointer Interpreter Interrupt Enable (STS1/STM0 #2)
Register 0199H, 0599H, 0999H and 0D99H: RHPP TU3 Pointer Interpreter Interrupt Enable (STS1/STM0 #3)
Register 01A1H, 05A1H, 09A1H and 0DA1H: RHPP TU3 Pointer Interpreter Interrupt Enable (STS1/STM0 #4)
Register 01A9H, 05A9H, 09A9H and 0DA9H: RHPP TU3 Pointer Interpreter Interrupt Enable (STS1/STM0 #5)
Register 01B1H, 05B1H, 09B1H and 0DB1H: RHPP TU3 Pointer Interpreter Interrupt Enable (STS1/STM0 #6)
Register 01B9H, 05B9H, 09B9H and 0DB9H: RHPP TU3 Pointer Interpreter Interrupt Enable (STS1/STM0 #7)
Register 01C1H, 05C1H, 09C1H and 0DC1H: RHPP TU3 Pointer Interpreter Interrupt Enable (STS1/STM0 #8)
Register 01C9H, 05C9H, 09C9H and 0DC9H: RHPP TU3 Pointer Interpreter Interrupt Enable (STS1/STM0 #9)
Register 01D1H, 05D1H, 09D1H and 0DD1H: RHPP TU3 Pointer Interpreter Interrupt Enable (STS1/STM0 #10)
Register 01D9H, 05D9H, 09D9H and 0DD9H: RHPP TU3 Pointer Interpreter Interrupt Enable (STS1/STM0 #11)
Register 01E1H, 05E1H, 09E1H and 0DE1H: RHPP TU3 Pointer Interpreter Interrupt Enable (STS1/STM0 #12)

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9		Unused	
Bit 8		Unused	
Bit 7		Unused	
Bit 6		Unused	
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	PAISE	0
Bit 2	R/W	PLOPE	0
Bit 1		Unused	
Bit 0	R/W	PTRJEE	0

The Pointer Interpreter Interrupt Enable Register is provided at RHPP r/w address 09H 11H 19H 21H 29H 31H 39H 41H 49H 51H 59H and 61H.

PTRJEE

The pointer justification event interrupt enable (PTRJEE) bit control the activation of the interrupt output. When PTRJEE is set to logic 1, the NJEI and PJEI pending interrupt will assert the interrupt output. When PTRJEE is set to logic 0, the NJEI and PJEI pending interrupt will not assert the interrupt output.

PLOPE

The path loss of pointer interrupt enable (PLOPE) bit controls the activation of the interrupt output. When PLOPE is set to logic 1, the PLOPI pending interrupt will assert the interrupt output. When PLOPE is set to logic 0, the PLOPI pending interrupt will not assert the interrupt output.

PAISE

The path alarm indication signal interrupt enable (PAISE) bit controls the activation of the interrupt output. When PAISE is set to logic 1, the PAISI pending interrupt will assert the interrupt output. When PAISE is set to logic 0, the PAISI pending interrupt will not assert the interrupt output.

Register 018AH, 058AH, 098AH and 0D8AH: RHPP TU3 Pointer Interpreter Interrupt Status (STS1/STM0 #1)
Register 0192H, 0592H, 0992H and 0D92H: RHPP TU3 Pointer Interpreter Interrupt Status (STS1/STM0 #2)
Register 019AH, 059AH, 099AH and 0D9AH: RHPP TU3 Pointer Interpreter Interrupt Status (STS1/STM0 #3)
Register 01A2H, 05A2H, 09A2H and 0DA2H: RHPP TU3 Pointer Interpreter Interrupt Status (STS1/STM0 #4)
Register 01AAH, 05AAH, 09AAH and 0DAAH: RHPP TU3 Pointer Interpreter Interrupt Status (STS1/STM0 #5)
Register 01B2H, 05B2H, 09B2H and 0DB2H: RHPP TU3 Pointer Interpreter Interrupt Status (STS1/STM0 #6)
Register 01BAH, 05BAH, 09BAH and 0DBAH: RHPP TU3 Pointer Interpreter Interrupt Status (STS1/STM0 #7)
Register 01C2H, 05C2H, 09C2H and 0DC2H: RHPP TU3 Pointer Interpreter Interrupt Status (STS1/STM0 #8)
Register 01CAH, 05CAH, 09CAH and 0DCAH: RHPP TU3 Pointer Interpreter Interrupt Status (STS1/STM0 #9)
Register 01D2H, 05D2H, 09D2H and 0DD2H: RHPP TU3 Pointer Interpreter Interrupt Status (STS1/STM0 #10)
Register 01DAH, 05DAH, 09DAH and 0DDAH: RHPP TU3 Pointer Interpreter Interrupt Status (STS1/STM0 #11)
Register 01E2H, 05E2H, 09E2H and 0DE2H: RHPP TU3 Pointer Interpreter Interrupt Status (STS1/STM0 #12)

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9		Unused	
Bit 8		Unused	
Bit 7		Unused	
Bit 6		Unused	
Bit 5	R	Reserved	X
Bit 4	R	Reserved	X
Bit 3	R	PAISI	X
Bit 2	R	PLOPI	X
Bit 1	R	PJEI	X
Bit 0	R	NJEI	X

The Pointer Interpreter Interrupt Status Register is provided at RHPP r/w address 0AH 12H 1AH 22H 2AH 32H 3AH 42H 4AH 52H 5AH and 62H.

NJEI

The negative pointer justification event interrupt status (NJEI) bit is an event indicator. NJEI is set to logic 1 to indicate a negative pointer justification event. The interrupt status bit is independent of the interrupt enable bit. NJEI is cleared to logic 0 when this register is read.

PJEI

The positive pointer justification event interrupt status (PJEI) bit is an event indicator. PJEI is set to logic 1 to indicate a positive pointer justification event. The interrupt status bit is independent of the interrupt enable bit. PJEI is cleared to logic 0 when this register is read.

PLOPI

The path loss of pointer interrupt status (PLOPI) bit is an event indicator. PLOPI is set to logic 1 to indicate any change in the status of PLOPV (entry to the LOP_state or exit from the LOP_state). The interrupt status bit is independent of the interrupt enable bit. PLOPI is cleared to logic 0 when this register is read.

PAISI

The path alarm indication signal interrupt status (PAISI) bit is an event indicator. PAISI is set to logic 1 to indicate any change in the status of PAISV (entry to the AIS_state or exit from the AIS_state). The interrupt status bit is independent of the interrupt enable bit. PAISI is cleared to logic 0 when this register is read.

Register 018BH, 058BH, 098BH and 0D8BH: RHPP TU3 Error Monitor Status (STS1/STM0 #1)
Register 0193H, 0593H, 0993H and 0D93H: RHPP TU3 Error Monitor Status (STS1/STM0 #2)
Register 019BH, 059BH, 099BH and 0D9BH: RHPP TU3 Error Monitor Status (STS1/STM0 #3)
Register 01A3H, 05A3H, 09A3H and 0DA3H: RHPP TU3 Error Monitor Status (STS1/STM0 #4)
Register 01ABH, 05ABH, 09ABH and 0DABH: RHPP TU3 Error Monitor Status (STS1/STM0 #5)
Register 01B3H, 05B3H, 09B3H and 0DB3H: RHPP TU3 Error Monitor Status (STS1/STM0 #6)
Register 01BBH, 05BBH, 09BBH and 0DBBH: RHPP TU3 Error Monitor Status (STS1/STM0 #7)
Register 01C3H, 05C3H, 09C3H and 0DC3H: RHPP TU3 Error Monitor Status (STS1/STM0 #8)
Register 01CBH, 05CBH, 09CBH and 0DCBH: RHPP TU3 Error Monitor Status (STS1/STM0 #9)
Register 01D3H, 05D3H, 09D3H and 0DD3H: RHPP TU3 Error Monitor Status (STS1/STM0 #10)
Register 01DBH, 05DBH, 09DBH and 0DDBH: RHPP TU3 Error Monitor Status (STS1/STM0 #11)
Register 01E3H, 05E3H, 09E3H and 0DE3H: RHPP TU3 Error Monitor Status (STS1/STM0 #12)

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9		Unused	
Bit 8		Unused	
Bit 7		Unused	
Bit 6	R	PERDIV	X
Bit 5	R	PRDIV	X
Bit 4	R	PPDIV	X
Bit 3	R	PUNEQV	X
Bit 2	R	PPLMV	X
Bit 1	R	PPLUV	X
Bit 0		Unused	

The Error Monitor Status Register is provided at RHPP r/w address 0BH 13H 1BH 23H 2BH 33H 3BH 43H 4BH 53H 5BH and 63H.

Note: The Error Monitor Status bits are don't care for slave time slots.

PPLUV

The path payload label unstable status (PPLUV) bit indicates the current status of the PLU-P defect.

Algorithm 1: PPLUV is set to logic 0.

Algorithm 2: PPLUV is set to logic 1 when a total of 5 received PSL differs from the previously accepted PSL without any persistent PSL in between. PPLUV is set to logic 0 when a persistent PSL is found. A persistent PSL is found when the same PSL is received for 3 or 5 consecutive frames.

PPLMV

The path payload label mismatch status (PPLMV) bit indicates the current status of the PLM-P defect.

Algorithm 1: PPLMV is set to logic 1 when the received PSL does not match, according to Table 3, the expected PSL for 3 or 5 consecutive frames (selectable with the PSL5 register bit). PPLMV is set to logic 0 when the received PSL matches, according to Table 3, the expected PSL for 3 or 5 consecutive frames.

Algorithm 2: PPLMV is set to logic 1 when the accepted PSL does not match, according to Table 3, the expected PSL. PPLMV is set to logic 0 when the accepted PSL matches, according to Table 3, the expected PSL.

PUNEQV

The path unequipped status (PUNEQV) bit indicates the current status of the UNEQ-P defect.

PUNEQV is set to logic 1 when the received PSL indicates unequipped, according to Table 3, for 3 or 5 consecutive frames (selectable with the PSL5 register bit). An PUNEQV is set to logic 0 when the received PSL indicates not unequipped, according to Table 3, for 3 or 5 consecutive frames.

PPDIV

The path payload defect indication status (PPDIV) bit indicates the current status of the PPDI-P defect.

Algorithm 1: PPDIV is set to logic one when the received PSL is a defect, according to Table 3, for 3 or 5 consecutive frames (selectable with the PSL5 register bit). PPDIV is set to logic 0 when the received PSL is not a defect, according to Table 3, for 3 or 5 consecutive frames.

Algorithm 2: PPDIV is set to logic 1 when the accepted PSL is a defect, according to Table 3. PPDI is set to logic 0 when the accepted PSL is not a defect, according to Table 3.

PRDIV

The path remote defect indication status (PRDIV) bit indicates the current status of the RDI-P defect. PRDIV is set to logic 1 when bit 5 of the G1 byte is set high for five or ten consecutive frames (selectable with the PRDI10 register bit). PRDIV is set to logic 0 when bit 5 of the G1 byte is set low for five or ten consecutive frames.

PERDIV

The path enhanced remote defect indication status (PERDIV) bit indicates the current status of the ERDI-P defect. PERDIV is set to logic 1 when the same 010, 100, 101, 110 or 111 pattern is detected in bits 5, 6 and 7 of the G1 byte for five or ten consecutive frames (selectable with the PRDI10 register bit). PERDIV is set to logic 0 when the same 000, 001 or 011 pattern is detected in bits 5, 6 and 7 of the G1 byte for five or ten consecutive frames.

Register 018CH, 058CH, 098CH and 0D8CH: RHPP TU3 Error Monitor Interrupt Enable (STS1/STM0 #1)
Register 0194H, 0594H, 0994H and 0D94H: RHPP TU3 Error Monitor Interrupt Enable (STS1/STM0 #2)
Register 019CH, 059CH, 099CH and 0D9CH: RHPP TU3 Error Monitor Interrupt Enable (STS1/STM0 #3)
Register 01A4H, 05A4H, 09A4H and 0DA4H: RHPP TU3 Error Monitor Interrupt Enable (STS1/STM0 #4)
Register 01ACH, 05ACH, 09ACH and 0DACH: RHPP TU3 Error Monitor Interrupt Enable (STS1/STM0 #5)
Register 01B4H, 05B4H, 09B4H and 0DB4H: RHPP TU3 Error Monitor Interrupt Enable (STS1/STM0 #6)
Register 01BCH, 05BCH, 09BCH and 0DBCH: RHPP TU3 Error Monitor Interrupt Enable (STS1/STM0 #7)
Register 01C4H, 05C4H, 09C4H and 0DC4H: RHPP TU3 Error Monitor Interrupt Enable (STS1/STM0 #8)
Register 01CCH, 05CCH, 09CCH and 0DCCH: RHPP TU3 Error Monitor Interrupt Enable (STS1/STM0 #9)
Register 01D4H, 05D4H, 09D4H and 0DD4H: RHPP TU3 Error Monitor Interrupt Enable (STS1/STM0 #10)
Register 01DCH, 05DCH, 09DCH and 0DDCH: RHPP TU3 Error Monitor Interrupt Enable (STS1/STM0 #11)
Register 01E4H, 05E4H, 09E4H and 0DE4H: RHPP TU3 Error Monitor Interrupt Enable (STS1/STM0 #12)

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9	R/W	PREIEE	0
Bit 8	R/W	PBIPEE	0
Bit 7	R/W	COPERDIE	0
Bit 6	R/W	PERDIE	0
Bit 5	R/W	PRDIE	0
Bit 4	R/W	PPDIE	0
Bit 3	R/W	PUNEQE	0
Bit 2	R/W	PPLME	0
Bit 1	R/W	PPLUE	0
Bit 0	R/W	COPSLE	0

The Error Monitor Interrupt Enable Register is provided at RHPP r/w address 0CH 14H 1CH 24H 2CH 34H 3CH 44H 4CH 54H 5CH and 64H.

COPSLE

The change of path payload signal label interrupt enable (COPSLE) bit controls the activation of the interrupt output. When COPSLE is set to logic 1, the COPSLI pending interrupt will assert the interrupt output. When COPSLE is set to logic 0, the COPSLI pending interrupt will not assert the interrupt output.

PPLUE

The path payload label unstable interrupt enable (PPLUE) bit controls the activation of the interrupt output. When PPLUE is set to logic 1, the PPLUI pending interrupt will assert the interrupt output. When PPLUE is set to logic 0, the PPLUI pending interrupt will not assert the interrupt output.

PPLME

The path payload label mismatch interrupt enable (PPLME) bit controls the activation of the interrupt output. When PPLME is set to logic 1, the PPLMI pending interrupt will assert the interrupt output. When PPLME is set to logic 0, the PPLMI pending interrupt will not assert the interrupt output.

PUNEQE

The path payload unequipped interrupt enable (PUNEQE) bit controls the activation of the interrupt output. When PUNEQE is set to logic 1, the PUNEQI pending interrupt will assert the interrupt output. When PUNEQE is set to logic 0, the PUNEQI pending interrupt will not assert the interrupt output.

PPDIE

The path payload defect indication interrupt enable (PPDIE) bit controls the activation of the interrupt output. When PPDIE is set to logic 1, the PPDI pending interrupt will assert the interrupt output. When PPDIE is set to logic 0, the PPDI pending interrupt will not assert the interrupt output.

PRDIE

The path remote defect indication interrupt enable (PRDIE) bit controls the activation of the interrupt output. When PRDIE is set to logic 1, the PRDII pending interrupt will assert the interrupt output. When PRDIE is set to logic 0, the PRDII pending interrupt will not assert the interrupt output.

PERDIE

The path enhanced remote defect indication interrupt enable (PERDIE) bit controls the activation of the interrupt output. When PERDIE is set to logic 1, the PERDII pending interrupt will assert the interrupt output. When PERDIE is set to logic 0, the PERDII pending interrupt will not assert the interrupt output.

COPERDIE

The change of path enhanced remote defect indication interrupt enable (COPERDIE) bit controls the activation of the interrupt output. When COPERDIE is set to logic 1, the COPERDII pending interrupt will assert the interrupt output. When COPERDIE is set to logic 0, the COPERDII pending interrupt will not assert the interrupt output.

PBIPEE

The path BIP-8 error interrupt enable (PBIPEE) bit controls the activation of the interrupt output. When PBIPEE is set to logic 1, the PBIPEI pending interrupt will assert the interrupt output. When PBIPEE is set to logic 0, the PBIPEI pending interrupt will not assert the interrupt output.

PREIEE

The path REI error interrupt enable (PREIEE) bit controls the activation of the interrupt output. When PREIEE is set to logic 1, the PREIEI pending interrupt will assert the interrupt output. When PREIEE is set to logic 0, the PREIEI pending interrupt will not assert the interrupt output.

Register 018DH, 058DH, 098DH and 0D8DH: RHPP TU3 Error Monitor Interrupt Status (STS1/STM0 #1)
Register 0195H, 0595H, 0995H and 0D95H: RHPP TU3 Error Monitor Interrupt Status (STS1/STM0 #2)
Register 019DH, 059DH, 099DH and 0D9DH: RHPP TU3 Error Monitor Interrupt Status (STS1/STM0 #3)
Register 01A5H, 05A5H, 09A5H and 0DA5H: RHPP TU3 Error Monitor Interrupt Status (STS1/STM0 #4)
Register 01ADH, 05ADH, 09ADH and 0DADH: RHPP TU3 Error Monitor Interrupt Status (STS1/STM0 #5)
Register 01B5H, 05B5H, 09B5H and 0DB5H: RHPP TU3 Error Monitor Interrupt Status (STS1/STM0 #6)
Register 01BDH, 05BDH, 09BDH and 0DBDH: RHPP TU3 Error Monitor Interrupt Status (STS1/STM0 #7)
Register 01C5H, 05C5H, 09C5H and 0DC5H: RHPP TU3 Error Monitor Interrupt Status (STS1/STM0 #8)
Register 01CDH, 05CDH, 09CDH and 0DCDH: RHPP TU3 Error Monitor Interrupt Status (STS1/STM0 #9)
Register 01D5H, 05D5H, 09D5H and 0DD5H: RHPP TU3 Error Monitor Interrupt Status (STS1/STM0 #10)
Register 01DDH, 0D5DH, 09DDH and 0DDDH: RHPP TU3 Error Monitor Interrupt Status (STS1/STM0 #11)
Register 01E5H, 05E5H, 09E5H and 0DE5H: RHPP TU3 Error Monitor Interrupt Status (STS1/STM0 #12)

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9	R	PREIEI	X
Bit 8	R	PBIPEI	X
Bit 7	R	COPERDII	X
Bit 6	R	PERDII	X
Bit 5	R	PRDII	X
Bit 4	R	PPDII	X
Bit 3	R	PUNEQI	X
Bit 2	R	PPLMI	X
Bit 1	R	PPLUI	X
Bit 0	R	COPSLI	X

The Error Monitor Interrupt Status Register is provided at RHPP r/w address 0DH 15H 1DH 25H 2DH 35H 3DH 45H 4DH 55H 5DH and 65H.

COPSLI

The change of path payload signal label interrupt status (COPSLI) bit is an event indicator. COPSLI is set to logic 1 to indicate a new PSL-P value. The interrupt status bit is independent of the interrupt enable bit. COPSLI is cleared to logic 0 when this register is read. ALGO2 register bit has no effect on COPSLI.

PPLUI

The path payload label unstable interrupt status (PPLUI) bit is an event indicator. PPLUI is set to logic 1 to indicate any change in the status of PPLUV (stable to unstable or unstable to stable). The interrupt status bit is independent of the interrupt enable bit. PPLUI is cleared to logic 0 when this register is read.

PPLMI

The path payload label mismatch interrupt status (PPLMI) bit is an event indicator. PPLMI is set to logic 1 to indicate any change in the status of PPLMV (match to mismatch or mismatch to match). The interrupt status bit is independent of the interrupt enable bit. PPLMI is cleared to logic 0 when this register is read.

PUNEQI

The path payload unequipped interrupt status (PUNEQI) bit is an event indicator. PUNEQI is set to logic 1 to indicate any change in the status of PUNEQV (equipped to unequipped or unequipped to equipped). The interrupt status bit is independent of the interrupt enable bit. PUNEQI is cleared to logic 0 when this register is read.

PPDII

The path payload defect indication interrupt status (PPDII) bit is an event indicator. PPDII is set to logic 1 to indicate any change in the status of PPDIV (no defect to payload defect or payload defect to no defect). The interrupt status bit is independent of the interrupt enable bit. PPDII is cleared to logic 0 when this register is read.

PRDII

The path remote defect indication interrupt status (PRDII) bit is an event indicator. PRDII is set to logic 1 to indicate any change in the status of PRDIV (no defect to RDI defect or RDI defect to no defect). The interrupt status bit is independent of the interrupt enable bit. PRDII is cleared to logic 0 when this register is read.

PERDII

The path enhanced remote defect indication interrupt status (PERDII) bit is an event indicator. PERDII is set to logic 1 to indicate any change in the status of PERDIV (no defect to ERDI defect or ERDI defect to no defect). The interrupt status bit is independent of the interrupt enable bit. PERDII is cleared to logic 0 when this register is read.

COPERDII

The change of path enhanced remote defect indication interrupt status (COPERDII) bit is an event indicator. COPERDII is set to logic 1 to indicate a new ERDI-P value. The interrupt status bit is independent of the interrupt enable bit. COPERDII is cleared to logic 0 when this register is read.

PBIPEI

The path BIP-8 error interrupt status (PBIPEI) bit is an event indicator. PBIPEI is set to logic 1 to indicate a path BIP-8 error. The interrupt status bit is independent of the interrupt enable bit. PBIPEI is cleared to logic 0 when this register is read.

PREIEI

The path REI error interrupt status (PREIEI) bit is an event indicator. PREIEI is set to logic 1 to indicate a path REI error. The interrupt status bit is independent of the interrupt enable bit. PREIEI is cleared to logic 0 when this register is read.

Indirect Register 00H: RHPP TU3 Pointer Interpreter Configuration

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9		Unused	
Bit 8		Unused	
Bit 7	R/W	Reserved	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	NDFCNT	0
Bit 4	R/W	INVCNT	0
Bit 3	R/W	RELAYPAIS	0
Bit 2	R/W	JUST3DIS	0
Bit 1	R/W	SSEN	0
Bit 0		Unused	

The Pointer Interpreter Configuration Indirect Register is provided at RHPP r/w indirect address 00H.

SSEN

The SS bits enable (SSEN) bit selects whether or not the SS bits are taking into account in the pointer interpreter state machine. When SSEN is set to logic 1, the SS bits must be set to 10 for a valid NORM_POINT, NDF_ENABLE, INC_IND, DEC_IND or NEW_POINT indication. When SSEN is set to logic 0, the SS bits are ignored.

JUST3DIS

The “justification more than 3 frames ago disable” (JUST3DIS) bit selects whether or not the NDF_ENABLE, INC_IND or DEC_IND pointer justifications must be more than 3 frames apart to be considered valid. When JUST3DIS is set to logic 0, the previous NDF_ENABLE, INC_IND or DEC_IND indication must be more than 3 frames ago or the present NDF_ENABLE, INC_IND or DEC_IND indication is considered an INV_POINT indication. When JUST3DIS is set to logic 1, NDF_ENABLE, INC_IND or DEC_IND indication can be every frame.

RELAYPAIS

The relay path AIS (RELAYPAIS) bit selects the condition to enter the path AIS state in the pointer interpreter state machine. When RELAYPAIS is set to logic 1, the path AIS state is entered with 1 X AIS_ind indication. When RELAYPAIS is set to logic 0, the path AIS state is entered with 3 X AIS_ind indications. This configuration bit also affects the concatenation pointer interpreter state machine.

INVCNT

The invalid counter (INVCNT) bit selects the behavior of the consecutive INV_POINT event counter in the pointer interpreter state machine. When INVCNT is set to logic 1, the consecutive INV_POINT event counter is reset by 3 EQ_NEW_POINT indications. When INVCNT is set to logic 0, the counter is not reset by 3 EQ_NEW_POINT indications.

NDFCNT

The new data flag counter (NDFCNT) bit selects the behavior of the consecutive NDF_ENABLE event counter in the pointer interpreter state machine. When NDFCNT is set to logic 1, the NDF_ENABLE definition is enabled NDF + SS. When NDFCNT is set to logic 0, the NDF_ENABLE definition is enabled NDF + SS + offset value in the range 0 to 782 (764 in TU-3 mode). This configuration bit only changes the NDF_ENABLE definition for the consecutive NDF_ENABLE even counter to count towards LOP-P defect when the pointer is out of range, this configuration bit does not change the NDF_ENABLE definition for pointer justification.

Indirect Register 01H: RHPP TU3 Error Monitor Configuration

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11	R/W	B3EONRPOH	0
Bit 10	R/W	IPREIBLK	0
Bit 9	R/W	IBER	0
Bit 8	R/W	PREIBLKACC	0
Bit 7	R/W	B3EBLK	0
Bit 6	R/W	PBIPEBLKREI	0
Bit 5	R/W	PBIPEBLKACC	0
Bit 4	R/W	FSBIPDIS	0
Bit 3	R/W	PRDI10	0
Bit 2	R/W	PLMEND	0
Bit 1	R/W	PSL5	0
Bit 0	R/W	ALGO2	0

The Error Monitor Configuration Indirect Register is provided at RHPP r/w indirect address 01H.

ALGO2

The payload signal label algorithm 2 (ALGO2) bit selects the algorithm for the PSL monitoring. When ALGO2 is set to logic 1, the ITU compliant algorithm is (algorithm 2) is used to monitor the PSL. When ALGO2 is set to logic 0, the BELLCORE compliant algorithm (algorithm 1) is used to monitor the PSL. ALGO2 changes the PLU-P, PLM-P and PDI-P defect definitions but has no effect on UNEQ-P defect, accepted PSL and change of PSL definitions

PSL5

The payload signal label detection (PSL5) bit selects the path PSL persistence. When PSL5 is set to logic 1, a new PSL is accepted when the same PSL value is detected in the C2 byte for five consecutive frames. When PSL5 is set to logic 0, a new PSL is accepted when the same PSL value is detected in the C2 byte for three consecutive frames.

PLMEND

The payload label mismatch removal (PLMEND) bit controls the removal of a PLM-P defect when an UNEQ-P defect is declared. When PLMEND is set to logic 1, a PLM-P defect is terminated when an UNEQ-P defect is declared. When PLMEND is set to logic 0, a PLM-P defect is not terminated when an UNEQ-P defect is declared.

PRDI10

The path remote defect indication detection (PRDI10) bit selects the path RDI and path ERDI persistence. When PRDI10 is set to logic 1, path RDI and path ERDI are accepted when the same pattern is detected in bits 5,6,7 of the G1 byte for ten consecutive frames. When PRDI10 is set to logic 0, path RDI and path ERDI are accepted when the same pattern is detected in bits 5,6,7 of the G1 byte for five consecutive frames.

FSBIPDIS

The disable fixed stuff columns during BIP-8 calculation (FSBIPDIS) bit controls the path BIP-8 calculation for an STS-1 (VC-3) payload. When FSBIPDIS is set to logic 1, the fixed stuff columns are not part of the BIP-8 calculation when processing an STS-1 (VC-3) payload. When FSBIPDIS is set to logic 0, the fixed stuff columns are part of the BIP-8 calculation when processing an STS-1 (VC-3) payload.

PBIPEBLKACC

The path block BIP-8 errors accumulation (PBIPEBLKACC) bit controls the accumulation of path BIP-8 errors. When PBIPEBLKACC is set to logic 1, the path BIP-8 error accumulation represents block BIP-8 errors (a maximum of 1 error per frame). When PBIPEBLKACC is set to logic 0, the path BIP-8 error accumulation represents BIP-8 errors (a maximum of 8 errors per frame).

PBIPEBLKREI

The path block BIP-8 errors (PBIPEBLKREI) bit controls the path REI errors returned to the TU3 THPP. When PBIPEBLKREI is set to logic 1, the path REI is updated with block BIP-8 errors (a maximum of 1 error per frame). When PBIPEBLKREI is set to logic 0, the path REI is updated with BIP-8 errors (a maximum of 8 errors per frame).

B3EBLK

The serial path block BIP-8 errors (B3EBLK) bit controls the indication of path BIP-8 errors on the B3E serial output. When B3EBLK is set to logic 1, B3E outputs block BIP-8 errors (a maximum of 1 error per frame). When B3EBLK is set to logic 0, B3E outputs BIP-8 errors (a maximum of 8 errors per frame).

PREIBLKACC

The path block REI errors accumulation (PREIBLKACC) bit controls the accumulation of path REI errors from the path status (G1) byte. When PREIBLK is set to logic 1, the extracted path REI errors are interpreted as block BIP-8 errors (a maximum of 1 error per frame). When PREIBLK is set to logic 0, the extracted path REI errors are interpret as BIP-8 errors (a maximum of 8 errors per frame).

IBER

The inband error reporting (IBER) bit controls the inband regeneration of the path status (G1) byte. When IBER is set to logic 1, the path status byte is updated with the REI-P and the ERDI-P defects that must be returned to the far end. When IBER is set to logic 0, the path status byte is not altered.

IPREIBLK

The inband path REI block errors (IPREIBLK) bit controls the regeneration of the path REI errors in the path status (G1) byte. When IPREIBLK is set to logic 1, the path REI is updated with block BIP-8 errors (a maximum of 1 error per frame). When IPREIBLK is set to logic 0, the path REI is updated with BIP-8 errors (a maximum of 8 errors per frame).

B3EONRPOH

The B3EONRPOH bit controls the data presented on RPOH ports. When set to logic 0, the received B3 byte is place on RPOH port. When set to logic 1, the B3 error count is placed on RPOH port as placed on B3E port.

Indirect Register 02H: RHPP TU3 Pointer value and ERDI

Bit	Type	Function	Default
Bit 15	R	PERDIV[2]	X
Bit 14	R	PERDIV[1]	X
Bit 13	R	PERDIV[0]	X
Bit 12		Unused	
Bit 11	R	SSV[1]	X
Bit 10	R	SSV[0]	X
Bit 9	R	PTRV[9]	X
Bit 8	R	PTRV[8]	X
Bit 7	R	PTRV[7]	X
Bit 6	R	PTRV[6]	X
Bit 5	R	PTRV[5]	X
Bit 4	R	PTRV[4]	X
Bit 3	R	PTRV[3]	X
Bit 2	R	PTRV[2]	X
Bit 1	R	PTRV[1]	X
Bit 0	R	PTRV[0]	X

The Pointer Value Indirect Register is provided at RHPP r/w address 02H.

PTRV[9:0]

The path pointer value (PTRV[9:0]) bits represent the current STS (AU or TU3) pointer being process by the pointer interpreter state machine or by the concatenation pointer interpreter state machine.

SSV[1:0]

The SS value (SSV[1:0]) bits represent the current SS (DD) bits being processed by the pointer interpreter state machine or by the concatenation pointer interpreter state machine.

PERDIV[2:0]

The path enhanced remote defect indication value (PERDIV[2:0]) bits represent the filtered path enhanced remote defect indication value. PERDIV[2:0] is updated when the same ERDI pattern is detected in bits 5,6,7 of the G1 byte for five or ten consecutive frames (selectable with the PRDI10 register bit).

Indirect Register 03H: RHPP TU3 captured and accepted PSL

Bit	Type	Function	Default
Bit 15	R	CPSLV[7]	X
Bit 14	R	CPSLV[6]	X
Bit 13	R	CPSLV[5]	X
Bit 12	R	CPSLV[4]	X
Bit 11	R	CPSLV[3]	X
Bit 10	R	CPSLV[2]	X
Bit 9	R	CPSLV[1]	X
Bit 8	R	CPSLV[0]	X
Bit 7	R	APSLV[7]	X
Bit 6	R	APSLV[6]	X
Bit 5	R	APSLV[5]	X
Bit 4	R	APSLV[4]	X
Bit 3	R	APSLV[3]	X
Bit 2	R	APSLV[2]	X
Bit 1	R	APSLV[1]	X
Bit 0	R	APSLV[0]	X

The Accepted PSL and ERDI Indirect Register is provided at RHPP r/w address 03H.

APSLV[7:0]

The accepted path signal label value (APSLV[7:0]) bits represent the last accepted path signal label value. A new PSL is accepted when the same PSL value is detected in the C2 byte for three or five consecutive frames. (selectable with the PSL5 register bit).

CPSLV[7:0]

The captured path signal label value (CPSLV[7:0]) bits represent the last captured path signal label value. A new PSL is captured every frame from the C2 byte.

Indirect Register 04H: RHPP TU3 Expected PSL and PDI

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13	R/W	PDIRANGE	0
Bit 12	R/W	PDI[4]	0
Bit 11	R/W	PDI[3]	0
Bit 10	R/W	PDI[2]	0
Bit 9	R/W	PDI[1]	0
Bit 8	R/W	PDI[0]	0
Bit 7	R/W	EPSL[7]	0
Bit 6	R/W	EPSL[6]	0
Bit 5	R/W	EPSL[5]	0
Bit 4	R/W	EPSL[4]	0
Bit 3	R/W	EPSL[3]	0
Bit 2	R/W	EPSL[2]	0
Bit 1	R/W	EPSL[1]	0
Bit 0	R/W	EPSL[0]	0

The Expected PSL and PDI Indirect Register is provided at RHPP r/w indirect address 04H.

EPSL[7:0]

The expected path signal label (EPSL[7:0]) bits represent the expected path signal label. The expected PSL and the expected PDI validate the received or the accepted PSL to declare PLM-P, UNEQ-P and PDI-P defects according Table 3.

PDI[4:0], PDIRANGE

The payload defect indication (PDI[4:0]) bits and the payload defect indication range (PDIRANGE) bit determine the expected payload defect indication according to Table 4. When PDIRANGE is set to logic 1, the PDI range is enabled and the expected PDI range is from E1H to E0H+PDI[4:0]. When PDIRANGE is set to logic 0, the PDI range is disable and the expected PDI value is E0H+PDI[4:0]. The expected PSL and the expected PDI validate the received or the accepted PSL to declare PLM-P, UNEQ-P and PDI-P defects according Table 3.

Indirect Register 05H: RHPP TU3 Pointer Interpreter status

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9		Unused	
Bit 8		Unused	
Bit 7		Unused	
Bit 6	R	NDF	X
Bit 5	R	ILLPTR	X
Bit 4	R	INVNDF	X
Bit 3	R	DISCOPA	X
Bit 2	R	CONCAT	X
Bit 1	R	ILLJREQ	X
Bit 0		Unused	

The Pointer Interpreter Status Indirect Register is provided at RHPP r/w indirect address 05H.

Note: The Pointer Interpreter Status bits are don’t care for slave time slots.

ILLJREQ

The illegal pointer justification request (ILLJREQ) signal is set high when a positive and/or negative pointer adjustment is received within three frames of a pointer justification event (inc_ind, dec_ind) or an NDF triggered active offset adjustment (NDF_enable).

CONCAT

The CONCAT bit is set high if the H1 and H2 pointer bytes received matche the concatenation indication (one of the five NDF_enable patterns in the NDF field, don't care in the size field, and all-ones in the pointer offset field).

DISCOPA

The discontinuous change of pointer alignment (DISCOPA) signal is set high when there is a pointer adjustment due to receiving a pointer repeated three times.

INVNDF

The invalid new data flag (INVNDF) signal is set high when an invalid NDF code is received.

ILLPTR

The illegal pointer offset (ILLPTR) signal is set high when the pointer received is out of the range. Legal values are from 0 to 782 (764 in TU3 mode). Pointer justification requests (inc_req, dec_req) and AIS indications (AIS_ind) are not considered illegal.

NDF

The new data flag (NDF) signal is set high when an enabled New Data Flag is received indicating a pointer adjustment (NDF_enabled indication).

Indirect Register 06H: RHPP TU3 Path BIP Error Counter

Bit	Type	Function	Default
Bit 15	R	PBIPE[15]	X
Bit 14	R	PBIPE[14]	X
Bit 13	R	PBIPE[13]	X
Bit 12	R	PBIPE[12]	X
Bit 11	R	PBIPE[11]	X
Bit 10	R	PBIPE[10]	X
Bit 9	R	PBIPE[9]	X
Bit 8	R	PBIPE[8]	X
Bit 7	R	PBIPE[7]	X
Bit 6	R	PBIPE[6]	X
Bit 5	R	PBIPE[5]	X
Bit 4	R	PBIPE[4]	X
Bit 3	R	PBIPE[3]	X
Bit 2	R	PBIPE[2]	X
Bit 1	R	PBIPE[1]	X
Bit 0	R	PBIPE[0]	X

The Path BIP Error Counter register is provided at RHPP r/w indirect address 06H.

PBIPE[15:0]

The path BIP error (PBIPE[15:0]) bits represent the number of path BIP errors that have been detected in the B3 byte since the last accumulation interval. The error counters are transferred to the holding registers by a microprocessor write to the RHPP Counters Update register.

Indirect Register 07H: RHPP TU3 Path REI Error Counter

Bit	Type	Function	Default
Bit 15	R	PREIE[15]	X
Bit 14	R	PREIE[14]	X
Bit 13	R	PREIE[13]	X
Bit 12	R	PREIE[12]	X
Bit 11	R	PREIE[11]	X
Bit 10	R	PREIE[10]	X
Bit 9	R	PREIE[9]	X
Bit 8	R	PREIE[8]	X
Bit 7	R	PREIE[7]	X
Bit 6	R	PREIE[6]	X
Bit 5	R	PREIE[5]	X
Bit 4	R	PREIE[4]	X
Bit 3	R	PREIE[3]	X
Bit 2	R	PREIE[2]	X
Bit 1	R	PREIE[1]	X
Bit 0	R	PREIE[0]	X

The Path BIP Error Counter register is provided at RHPP r/w indirect address 07H.

PREIE[15:0]

The path REI error (PREIE[15:0]) bits represent the number of path REI errors that have been extracted from the G1 byte since the last accumulation interval. The error counters are transferred to the holding registers by a microprocessor write to the RHPP Counters Update register.

Indirect Register 08H: RHPP TU3 Path Negative Justification Event Counter

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12	R	PNJE[12]	X
Bit 11	R	PNJE[11]	X
Bit 10	R	PNJE[10]	X
Bit 9	R	PNJE[9]	X
Bit 8	R	PNJE[8]	X
Bit 7	R	PNJE[7]	X
Bit 6	R	PNJE[6]	X
Bit 5	R	PNJE[5]	X
Bit 4	R	PNJE[4]	X
Bit 3	R	PNJE[3]	X
Bit 2	R	PNJE[2]	X
Bit 1	R	PNJE[1]	X
Bit 0	R	PNJE[0]	X

The Path Negative Justification Event Counter register is provided at RHPP r/w indirect address 08H.

PNJE[12:0]

The Path Negative Justification Event (PNJE[12:0]) bits represent the number of Path Negative Justification Events that have occurred since the last accumulation interval. The event counters are transferred to the holding registers by a microprocessor write to RHPP Counters Update register.

Indirect Register 09H: RHPP TU3 Path Positive Justification Event Counter

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12	R	PPJE[12]	X
Bit 11	R	PPJE[11]	X
Bit 10	R	PPJE[10]	X
Bit 9	R	PPJE[9]	X
Bit 8	R	PPJE[8]	X
Bit 7	R	PPJE[7]	X
Bit 6	R	PPJE[6]	X
Bit 5	R	PPJE[5]	X
Bit 4	R	PPJE[4]	X
Bit 3	R	PPJE[3]	X
Bit 2	R	PPJE[2]	X
Bit 1	R	PPJE[1]	X
Bit 0	R	PPJE[0]	X

The Path Positive Justification Event Counter register is provided at RHPP r/w indirect address 09H.

PPJE[12:0]

The Path Positive Justification Event (PPJE[12:0]) bits represent the number of Path Positive Justification Events that have occurred since the last accumulation interval. The event counters are transferred to the holding registers by a microprocessor write to RHPP Counters Update register.

Register 0200H, 0600H, 0A00H and 0E00H: RSVCA Indirect Address

Bit	Type	Function	Default
Bit 15	R	BUSY	X
Bit 14	R/W	RWB	0
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9		Unused	
Bit 8		Unused	
Bit 7	R/W	IADDR[1]	0
Bit 6	R/W	IADDR[0]	0
Bit 5		Unused	
Bit 4		Unused	
Bit 3	R/W	PATH[3]	0
Bit 2	R/W	PATH[2]	0
Bit 1	R/W	PATH[1]	0
Bit 0	R/W	PATH[0]	0

The Indirect Address Register is provided at SVCA r/w address 00H.

RWB

The active high read and active low write (RWB) bit selects if the current access to the internal RAM is an indirect read or an indirect write. Writing to the Indirect Address Register initiates an access to the internal RAM. When RWB is set to logic 1, an indirect read access to the RAM is initiated. The data from the addressed location in the internal RAM will be transferred to the Indirect Data Register. When RWB is set to logic 0, an indirect write access to the RAM is initiated. The data from the Indirect Data Register will be transferred to the addressed location in the internal RAM.

BUSY

The active high RAM busy (BUSY) bit reports if a previously initiated indirect access to the internal RAM has been completed. BUSY is set to logic 1 upon writing to the Indirect Address Register. BUSY is set to logic 0, upon completion of the RAM access. This register should be polled to determine when new data is available in the Indirect Data Register.
Note: Maximum busy bit set time is 22 clock cycles.

PATH[3:0]

The STS-1/STM-0 path (PATH[3:0]) bits select which STS-1/STM-0 path is accessed by the current indirect transfer. Some indirect registers are valid only when the PATH[3:0] have certain values.

PATH[3:0]	STS-1/STM-0 path #
0000	Invalid path
0001-1100	Path #1 to Path #12
1101-1111	Invalid path

IADDR[1:0]

The indirect address location (ADDR[1:0]) bits select which address location is accessed by the current indirect transfer.

IADDR[1:0]	Indirect Register
00	SVCA Outgoing Positive Justification Performance Monitor
01	SVCA Outgoing Negative Justification Performance Monitor
10	SVCA Diagnostic/Configuration Register
11	Reserved

Register 0201H, 0601H, 0A01H and 0E01H: RSVCA Indirect Data

Bit	Type	Function	Default
Bit 15	R/W	DATA[15]	0
Bit 14	R/W	DATA[14]	0
Bit 13	R/W	DATA[13]	0
Bit 12	R/W	DATA[12]	0
Bit 11	R/W	DATA[11]	0
Bit 10	R/W	DATA[10]	0
Bit 9	R/W	DATA[9]	0
Bit 8	R/W	DATA[8]	0
Bit 7	R/W	DATA[7]	0
Bit 6	R/W	DATA[6]	0
Bit 5	R/W	DATA[5]	0
Bit 4	R/W	DATA[4]	0
Bit 3	R/W	DATA[3]	0
Bit 2	R/W	DATA[2]	0
Bit 1	R/W	DATA[1]	0
Bit 0	R/W	DATA[0]	0

The Indirect Data Register is provided at SVCA r/w address 01H.

DATA[15:0]

The indirect access data (DATA[15:0]) bits hold the data transfer to or from the internal RAM during indirect access. When RWB is set to logic 1 (indirect read), the data from the addressed location in the internal RAM will be transferred to DATA[15:0]. BUSY should be polled to determine when the new data is available in DATA[15:0]. When RWB is set to logic 0 (indirect write), the data from DATA[15:0] will be transferred to the addressed location in the internal RAM. The indirect Data register must contain valid data before the indirect write is initiated by writing to the Indirect Address Register.

DATA[15:0] has a different meaning depending on which address of the internal RAM is being accessed.

Register 0202H, 0602H, 0A02H and 0E02H: RSVCA Payload Configuration

Bit	Type	Function	Default
Bit 15	R/W	STS12CSL	0
Bit 14	R/W	STS12C	0
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9		Unused	
Bit 8		Unused	
Bit 7	R/W	TUG3[4]	0
Bit 6	R/W	TUG3[3]	0
Bit 5	R/W	TUG3[2]	0
Bit 4	R/W	TUG3[1]	0
Bit 3	R/W	STS3C[4]	0
Bit 2	R/W	STS3C[3]	0
Bit 1	R/W	STS3C[2]	0
Bit 0	R/W	STS3C[1]	0

The Payload Configuration Register is provided at SVCA r/w address 02H.

STS3C[1]

The STS-3c (VC-4) payload configuration (STS3C[1]) bit selects the payload configuration. When STS3C[1] is set to logic 1, the STS-1/STM-0 paths #1, #5 and #9 are part of an STS-3c (VC-4) payload. When STS3C[1] is set to logic 0, the paths are STS-1 (VC-3) payloads. When STS12C is set to logic 1, STS3C[1] must be set to logic 0.

STS3C[2]

The STS-3c (VC-4) payload configuration (STS3C[2]) bit selects the payload configuration. When STS3C[2] is set to logic 1, the STS-1/STM-0 paths #2, #6 and #10 are part of an STS-3c (VC-4) payload. When STS3C[2] is set to logic 0, the paths are STS-1 (VC-3) payloads. When STS12C is set to logic 1, STS3C[2] must be set to logic 0.

STS3C[3]

The STS-3c (VC-4) payload configuration (STS3C[3]) bit selects the payload configuration. When STS3C[3] is set to logic 1, the STS-1/STM-0 paths #3, #7 and #11 are part of an STS-3c (VC-4) payload. When STS3C[3] is set to logic 0, the paths are STS-1 (VC-3) payloads. When STS12C is set to logic 1, STS3C[3] must be set to logic 0.

STS3C[4]

The STS-3c (VC-4) payload configuration (STS3C[4]) bit selects the payload configuration. When STS3C[4] is set to logic 1, the STS-1/STM-0 paths #4, #8 and #12 are part of an STS-3c (VC-4) payload. When STS3C[4] is set to logic 0, the paths are STS-1 (VC-3) payloads. When STS12C is set to logic 1, STS3C[4] must be set to logic 0.

TUG3[1]

The TUG3 payload configuration (TUG3[1]) bit selects the payload configuration. When TUG3[1] is set to logic 1, the STS-1/STM-0 paths #1, #5 and #9 are part of a TUG3 payload. When TUG3[1] is set to logic 0, the paths are not part of a TUG3 payload. When STS12C is set to logic 1, TUG3[1] must be set to logic 0.

TUG3[2]

The TUG3 payload configuration (TUG3[2]) bit selects the payload configuration. When TUG3[2] is set to logic 1, the STS-1/STM-0 paths #2, #6 and #10 are part of a TUG3 payload. When TUG3[2] is set to logic 0, the paths are not part of a TUG3 payload. When STS12C is set to logic 1, TUG3[2] must be set to logic 0.

TUG3[3]

The TUG3 payload configuration (TUG3[3]) bit selects the payload configuration. When TUG3[3] is set to logic 1, the STS-1/STM-0 paths #3, #7 and #11 are part of a TUG3 payload. When TUG3[3] is set to logic 0, the paths are not part of a TUG3 payload. When STS12C is set to logic 1, TUG3[3] must be set to logic 0.

TUG3[4]

The TUG3 payload configuration (TUG3[4]) bit selects the payload configuration. When TUG3[4] is set to logic 1, the STS-1/STM-0 paths #4, #8 and #12 are part of a TUG3 payload. When TUG3[4] is set to logic 0, the paths are not part of a TUG3 payload. When STS12C is set to logic 1, TUG3[4] must be set to logic 0.

STS12C

The STS-12c (VC-4-4c) payload configuration (STS12C) bit selects the payload configuration. When STS12C is set to logic 1, the STS-1/STM-0 paths #1 to #12 are part of an STS-12c (VC-4-4c) payload. When STS12C is set to logic 0, the STS-1/STM-0 paths are defined with the STS3C[1:4] register bit.

STS12CSL

The slave STS-12c (VC-4-4c) payload configuration (STS12CSL) bit selects the slave payload configuration. When STS12CSL is set to logic 1, the STS-1/STM-0 paths #1 to #12 are part of a STS-12c (VC-4-4c) slave payload. When STS12CSL is set to logic 0, the STS-1/STM-0 paths #1 to #12 are part of a STS-12c (VC-4-4c) master payload. When STS12C is set to logic 0, STS12CSL must be set to logic 0.

Register 0203H, 0603H, 0A03H and 0E03H: RSVCA Positive Pointer Justification Interrupt Status

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11	R	PPJI[12]	0
Bit 10	R	PPJI[11]	0
Bit 9	R	PPJI[10]	0
Bit 8	R	PPJI[9]	0
Bit 7	R	PPJI[8]	0
Bit 6	R	PPJI[7]	0
Bit 5	R	PPJI[6]	0
Bit 4	R	PPJI[5]	0
Bit 3	R	PPJI[4]	0
Bit 2	R	PPJI[3]	0
Bit 1	R	PPJI[2]	0
Bit 0	R	PPJI[1]	0

The Positive Pointer Justification Interrupt Status Register is provided at SVCA r/w address 03H.

PPJI[12:1]

The positive pointer justification interrupt status (PPJI[12:1]) bits are event indicators for STS-1/STM-0 paths #1 to #12. PPJI[12:1] are set to logic 1 to indicate a positive pointer justification event in the outgoing data stream. These interrupt status bits are independent of the interrupt enable bits. PPJI[12:1] are cleared to logic 0 when this register is read.

Register 0204H, 0604H, 0A04H and 0E04H: RSVCA Negative Pointer Justification Interrupt Status

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11	R	NPJI[12]	0
Bit 10	R	NPJI[11]	0
Bit 9	R	NPJI[10]	0
Bit 8	R	NPJI[9]	0
Bit 7	R	NPJI[8]	0
Bit 6	R	NPJI[7]	0
Bit 5	R	NPJI[6]	0
Bit 4	R	NPJI[5]	0
Bit 3	R	NPJI[4]	0
Bit 2	R	NPJI[3]	0
Bit 1	R	NPJI[2]	0
Bit 0	R	NPJI[1]	0

The Negative Pointer Justification Interrupt Status Register is provided at SVCA r/w address 04H.

NPJI[12:1]

The negative pointer justification interrupt status (NPJI[12:1]) bits are event indicators for STS-1/STM-0 paths #1 to #12. NPJI[12:1] are set to logic 1 to indicate a negative pointer justification event in the outgoing data stream. These interrupt status bits are independent of the interrupt enable bits. NPJI[12:1] are cleared to logic 0 when this register is read.

Register 0205H, 0605H, 0A05H and 0E05H: RSVCA FIFO Overflow Interrupt Status

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11	R	FOVRI[12]	0
Bit 10	R	FOVRI[11]	0
Bit 9	R	FOVRI[10]	0
Bit 8	R	FOVRI[9]	0
Bit 7	R	FOVRI[8]	0
Bit 6	R	FOVRI[7]	0
Bit 5	R	FOVRI[6]	0
Bit 4	R	FOVRI[5]	0
Bit 3	R	FOVRI[4]	0
Bit 2	R	FOVRI[3]	0
Bit 1	R	FOVRI[2]	0
Bit 0	R	FOVRI[1]	0

The FIFO overflow Event Interrupt Status Register is provided at SVCA r/w address 05H.

FOVRI[12:1]

The FIFO overflow event interrupt status (FOVRI[12:1]) bits are event indicators for STS-1/STM-0 paths #1 to #12. FOVRI[12:1] are set to logic 1 to indicate a FIFO overflow event. These interrupt status bits are independent of the interrupt enable bits. FOVRI[12:1] are cleared to logic 0 when this register is read.

Register 0206H, 0606H, 0A06H and 0E06H: RSVCA FIFO Underflow Interrupt Status

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11	R	FUDRI[12]	0
Bit 10	R	FUDRI[11]	0
Bit 9	R	FUDRI[10]	0
Bit 8	R	FUDRI[9]	0
Bit 7	R	FUDRI[8]	0
Bit 6	R	FUDRI[7]	0
Bit 5	R	FUDRI[6]	0
Bit 4	R	FUDRI[5]	0
Bit 3	R	FUDRI[4]	0
Bit 2	R	FUDRI[3]	0
Bit 1	R	FUDRI[2]	0
Bit 0	R	FUDRI[1]	0

The FIFO underflow Event Interrupt Status Register is provided at SVCA r/w address 06H.

FUDRI[12:1]

The FIFO underflow event interrupt status (FUDR[12:1]) bits are event indicators for STS-1/STM-0 paths #1 to #12. FUDRI[12:1] are set to logic 1 to indicate a FIFO underflow event. These interrupt status bits are independent of the interrupt enable bits. FUDRI[12:1] are cleared to logic 0 when this register is read.

Register 0207H, 0607H, 0A07H and 0E07H: RSVCA Pointer Justification Interrupt Enable

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11	R/W	PJIE[12]	0
Bit 10	R/W	PJIE[11]	0
Bit 9	R/W	PJIE[10]	0
Bit 8	R/W	PJIE[9]	0
Bit 7	R/W	PJIE[8]	0
Bit 6	R/W	PJIE[7]	0
Bit 5	R/W	PJIE[6]	0
Bit 4	R/W	PJIE[5]	0
Bit 3	R/W	PJIE[4]	0
Bit 2	R/W	PJIE[3]	0
Bit 1	R/W	PJIE[2]	0
Bit 0	R/W	PJIE[1]	0

The Pointer Justification Interrupt Enable Register is provided at SVCA direct r/w address 07H.

PJIEN[12:1]

The pointer justification event interrupt enable (PJIE[12:1]) bits controls the activation of the interrupt output for STS-1/STM-0 paths #1 to #12. When any of these bit locations is set to logic 1, the corresponding pending interrupt will assert the interrupt output. When any of these bit locations is set to logic 0, the corresponding pending interrupt will not assert the interrupt output.

Register 0208H, 0608H, 0A08H and 0E08H: RSVCA FIFO Interrupt Enable

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11	R/W	FIE[12]	0
Bit 10	R/W	FIE[11]	0
Bit 9	R/W	FIE[10]	0
Bit 8	R/W	FIE[9]	0
Bit 7	R/W	FIE[8]	0
Bit 6	R/W	FIE[7]	0
Bit 5	R/W	FIE[6]	0
Bit 4	R/W	FIE[5]	0
Bit 3	R/W	FIE[4]	0
Bit 2	R/W	FIE[3]	0
Bit 1	R/W	FIE[2]	0
Bit 0	R/W	FIE[1]	0

The FIFO Event Interrupt Enable Register is provided at SVCA r/w address 08H.

FIEN[12:1]

The FIFO event interrupt enable (FIE[12:1]) bits controls the activation of the interrupt output for STS-1/STM-0 paths #1 to #12 caused by a FIFO overflow of a FIFO underflow. When any of these bit locations is set to logic 1, the corresponding pending interrupt will assert the interrupt output. When any of these bit locations is set to logic 0, the corresponding pending interrupt will not assert the interrupt output.

Register 020AH, 060AH, 0A0AH and 0E0AH: RSVCA Clear Fixed Stuff

Bit	Type	Function	Default
Bit 15	R/W	ESDIS	0
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11	R/W	CLRFS[12]	0
Bit 10	R/W	CLRFS[11]	0
Bit 9	R/W	CLRFS[10]	0
Bit 8	R/W	CLRFS[9]	0
Bit 7	R/W	CLRFS[8]	0
Bit 6	R/W	CLRFS[7]	0
Bit 5	R/W	CLRFS[6]	0
Bit 4	R/W	CLRFS[5]	0
Bit 3	R/W	CLRFS[4]	0
Bit 2	R/W	CLRFS[3]	0
Bit 1	R/W	CLRFS[2]	0
Bit 0	R/W	CLRFS[1]	0

The FIFO Fixed Stuff register provides miscellaneous control bits. It is provided at r/w address 10H.

ESDIS

When set high, forces the SVCA to bypass the internal FIFO. The input data is not buffered inside the FIFO and is not re-aligned to a new transport frame but simply clocked out on the next rising edge.

CLRFS

The Clear Fixed Stuff (CLRFS) enables the regeneration of fixed stuff columns (#30, #59) of an STS-1/VC-3. When set to logic one, STS-1/VC-3 incoming fixed stuff columns (#30, #59) are discarded and regenerated (set to 00h) on the outgoing stream. When set to logic 0, these fixed stuff columns are relayed through the SVCA.

Register 020BH, 060BH, 0A0BH and 0E0BH: RSVCA Counter Update

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9		Unused	
Bit 8		Unused	
Bit 7		Unused	
Bit 6		Unused	
Bit 5		Unused	
Bit 4		Unused	
Bit 3		Unused	
Bit 2		Unused	
Bit 1		Unused	
Bit 0		Unused	

The Performance monitor transfer register is provided at r/w address 0X0BH. Any write to this register or to the Master Configuration Register (0000H) triggers a transfer of all performance monitor counters to holding registers that can be read by the ecbi interface.

Indirect Register 00H: RSVCA Positive Justifications Performance Monitor

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12	R	PJPMON[12]	0
Bit 11	R	PJPMON[11]	0
Bit 10	R	PJPMON[10]	0
Bit 9	R	PJPMON[9]	0
Bit 8	R	PJPMON[8]	0
Bit 7	R	PJPMON[7]	0
Bit 6	R	PJPMON[6]	0
Bit 5	R	PJPMON[5]	0
Bit 4	R	PJPMON[4]	0
Bit 3	R	PJPMON[3]	0
Bit 2	R	PJPMON[2]	0
Bit 1	R	PJPMON[1]	0
Bit 0	R	PJPMON[0]	0

The Outgoing Positive justifications performance monitor is provided at SVCA indirect r/w address 00H.

PJPMON[12:0]

This register reports the number of positive pointer justification events that occurred on the outgoing side in the previous accumulation interval.

Indirect Register 01H: RSVCA Negative Justifications Performance Monitor

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12	R	NJPMON[12]	0
Bit 11	R	NJPMON[11]	0
Bit 10	R	NJPMON[10]	0
Bit 9	R	NJPMON[9]	0
Bit 8	R	NJPMON[8]	0
Bit 7	R	NJPMON[7]	0
Bit 6	R	NJPMON[6]	0
Bit 5	R	NJPMON[5]	0
Bit 4	R	NJPMON[4]	0
Bit 3	R	NJPMON[3]	0
Bit 2	R	NJPMON[2]	0
Bit 1	R	NJPMON[1]	0
Bit 0	R	NJPMON[0]	0

The outgoing Negative justifications performance monitor is provided at SVCA indirect r/w address 01H.

NJPMON[12:0]

This register reports the number of negative pointer justification events that occurred on the outgoing side in the previous accumulation interval.

Indirect Register 02H: RSVCA Diagnostic/Configuration

Bit	Type	Function	Default
Bit 15	R/W	PTRRST	0
Bit 14	R/W	PTRSS[1]	0
Bit 13	R/W	PTRSS[0]	0
Bit 12	R/W	JUS3DIS	0
Bit 11	R/W	PTRDD[1]	0
Bit 10	R/W	PTRDD[2]	0
Bit 9		Unused	
Bit 8		Unused	
Bit 7		Unused	
Bit 6		Unused	
Bit 5	R/W	Diag_NDFREQ	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	Diag_PAIS	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	Reserved	0

The SVCA Diagnostic Register is provided at SVCA r/w address 02H. These bits should be set to their default values during normal operation of the SVCA.

Diag_PAIS

When set high, the Diag_PAIS bit forces the SVCA to insert path AIS in the selected outgoing stream for at least three consecutive frames. AIS is inserted by writing an all ones pattern in the transport overhead bytes H1, H2, and H3, as well as in the entire STS synchronous payload envelope. The first frame after PAIS negates will contain a new data flag in the transport overhead H1 byte.

Diag_NDFREQ

When set high, Diag_NDFREQ bit forces the SVCA to insert a NEW DATA FLAG indication in the frame regardless of the state of the pointer generation state machine.

PTRDD[1:0]

The PTRDD[1:0] defines the STS-N/AU-N concatenation pointer bits DD. ITU requires that DD be set to 10 when processing AU-4, AU-3 or TU-3. On the other side, BELLCORE does not specify these two bits.

JUST3DIS

When set high, JUST3DIS allows the SVCA to perform 1 justification per frame when necessary. When set to zero, pointer justifications are allowed only every 4 frames.

PTRSS[1:0]

The PTRSS[1:0] defines the STS-N/AU-N pointer bits SS. ITU requires that SS be set to 10 when processing AU-4, AU-3 or TU-3. On the other side, BELLCORE does not specify these two bits. The SS bits are set to 00 when processing a slave sts-1.

PTR_RST

When set high, Incoming and outgoing pointers are reset to their default values. This bit is level sensitive

Register 0220H: DSTSI Indirect Address

Bit	Type	Function	Default
Bit 15	R	BUSY	X
Bit 14	R/W	RWB	0
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10	R/W	PAGE	0
Bit 9		Unused	
Bit 8		Unused	
Bit 7	R/W	TSOUT[3]	0
Bit 6	R/W	TSOUT[2]	0
Bit 5	R/W	TSOUT[1]	0
Bit 4	R/W	TSOUT[0]	0
Bit 3		Unused	
Bit 2		Unused	
Bit 1	R/W	DOUTSEL[1]	0
Bit 0	R/W	DOUTSEL[0]	0

This register provides the slice number; the time-slot number and the control page select used to access the control pages. Writing to this register triggers an indirect register access. This register cannot be written to when an indirect register access is in progress.

DOUTSEL[1:0]

The Slice Output Select (DOUTSEL[1:0]) bits select the slice accessed by the current indirect transfer.

DOUTSEL[1:0]	DOUT
00	Slice #1
01	Slice #2
10	Slice #3
11	Slice #4

TSOUT[3:0]

The indirect STS-1/STM-0 output time slot (TSOUT[3:0]) bits indicate the STS-1/STM-0 output time slot accessed in the current indirect access. Time slots #1 to #12 are valid.

TSOUT[3:0]	STS-1/STM-0 time slot #
0000	Invalid time slot
0001-1100	Time slot #1 to time slot #12
1101-1111	Invalid time slot

PAGE

The page (PAGE) bit selects which control page is accessed in the current indirect transfer. Two pages are defined: page 0 and page 1.

PAGE	Control Page
0	Page 0
1	Page 1

RWB

The indirect access control bit (RWB) selects between a configure (write) or interrogate (read) access to the control pages. Writing logic 0 to RWB triggers an indirect write operation. Data to be written is taken for the STSI Indirect Data register. Writing logic 1 to RWB triggers an indirect read operation. The data read from the control pages is stored in the STSI Indirect Data register after the BUSY bit has cleared.

BUSY

The indirect access status bit (BUSY) reports the progress of an indirect access. BUSY is set to logic 1 when this register is written, triggering an access. It remains logic 1 until the access is complete at which time it is set to logic 0. This register should be polled to determine when new data is available in the Indirect Data Register or when another write access can be initiated.
Note: Maximum busy bit set time is 10 clock cycles.

Register 0221H: DSTSI Indirect Data

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13	R/W	Reserved	0
Bit 12	R/W	Reserved	0
Bit 11	R/W	Reserved	0
Bit 10	R/W	Reserved	0
Bit 9	R/W	Reserved	0
Bit 8	R/W	Reserved	0
Bit 7	R/W	TSIN[3]	0
Bit 6	R/W	TSIN[2]	0
Bit 5	R/W	TSIN[1]	0
Bit 4	R/W	TSIN[0]	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	DINSEL[1]	0
Bit 0	R/W	DINSEL[0]	0

This register contains the data read from the control pages after an indirect read operation or the data to be written to the control pages in an indirect write operation. The data to be written to the control pages must be set up in this register before triggering a write. The STSI Indirect Data register reflects the last value read or written until the completion of a subsequent indirect read operation. This register cannot be written to while an indirect register access is in progress.

DINSEL[1:0]

The Slice Input Select (DINSEL[1:0]) field reports the slice number read from or written to an indirect register location.

DINSEL[1:0]	Data Stream
00	Slice #1
01	Slice #2
10	Slice #3
11	Slice #4

TSIN[3:0]

The STS-1/STM-0 Input Time Slot (TSIN[3:0]) field reports the time-slot number read from or written to an indirect register location.

TSIN[3:0]	STS-1/STM-0 time slot #
0000	Invalid time slot
0001-1100	Time slot #1 to time slot #12
1101-1111	Invalid time slot

Register 0222H: DSTSI Configuration

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9		Unused	
Bit 8		Unused	
Bit 7		Unused	
Bit 6		Unused	
Bit 5		Unused	
Bit 4		Unused	
Bit 3	R	ACTIVE	X
Bit 2	R/W	PSEL	0
Bit 1	R/W	J0RORDR	0
Bit 0	R/W	COAPE	0

COAPE

The change of active page interrupt enable (COAPE) bit enables/disables the change of active page interrupt output. When the COAPE bit is set to logic 1, an interrupt is generated when the active page changes from page 0 to page 1 or from page 1 to page 0. These interrupts are masked when COAPE is set to logic 0.

J0RORDR

The J0 Reorder (J0RORDR) bit enables/disables the reordering of the J0/Z0 bytes. This configuration bit only has an effect when the STSI is in the dynamic switching mode – if the STSI is in any of the static switching modes then the value of this bit is ignored. When this bit is set to logic 0 the J0/Z0 bytes are not reordered by the STSI. When this bit is set to logic 1, normal reordering of the J0/Z0 bytes is enabled.

PSEL

The page select (PSEL) bit is used in the selection of the current active page. This bit is logically XORed with the value of the external CMP port to determine which control page is currently active.

ACTIVE

The active page indication (ACTIVE) bit indicates which control page is currently active. When this bit is logic 0 then page 0 is controlling the dynamic mux. When this bit is logic 1 then page 1 is controlling the dynamic mux.

Register 0223H: DSTSI Interrupt Status

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9		Unused	
Bit 8		Unused	
Bit 7		Unused	
Bit 6		Unused	
Bit 5		Unused	
Bit 4		Unused	
Bit 3		Unused	
Bit 2		Unused	
Bit 1		Unused	
Bit 0	R	COAPI	X

COAPI

The change of active page interrupt statue bit (COAPI) reports the status of the change of active page interrupt. COAPI is set to logic 1 when the active control page changes from page 0 to page 1 or from page 1 to page 0. COAPI is cleared immediately following a read to this register when WCIMODE is logic 0. When WCIMODE is logic 1, COAPI is cleared immediately following a **write** (regardless of value) to this register. COAPI remains valid when the interrupt is not enabled (COAPE set to logic 0) and may be polled to detect change of active control page events.

Register 0240H, 0640H, 0A40H and 0E40H: DPRGM Indirect Address

Bit	Type	Function	Default
Bit 15	R	BUSY	X
Bit 14	R/W	RDWRB	0
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9	R/W	IADDR[3]	0
Bit 8	R/W	IADDR[2]	0
Bit 7	R/W	IADDR[1]	0
Bit 6	R/W	IADDR[0]	0
Bit 5		Unused	
Bit 4		Unused	
Bit 3	R/W	PATH[3]	0
Bit 2	R/W	PATH[2]	0
Bit 1	R/W	PATH[1]	0
Bit 0	R/W	PATH[0]	0

The PRGM Indirect Address Register is provided at PRGM r/w address 00h when TRSB is high and BSB is low.

PATH[3:0]

The PATH[3:0] bits select which time-multiplexed division is accessed by the current indirect transfer.

PATH[3:0]	time division #
0000	Invalid path
0001-1100	path #1 to path #12
1101-1111	Invalid path

IADDR[3:0]

The indirect address select which indirect register is access by the current indirect transfer. Six indirect registers are defined for the monitor (IADDR[3] = ‘0’) : the configuration, the PRBS[22:7], the PRBS[6:0], the B1/E1 value, the Monitor error count and the received B1/E1 byte.

IADDR[3:0]	RAM page
0000	STS-1 path Configuration
0001	PRBS[22:7]
0010	PRBS[6:0]

IADDR[3:0]	RAM page
0011	B1/E1 value
0100	Monitor error count
0101	Received B1 and E1

Four indirect registers are defined for the generator (IADDR [3] = '1') : the configuration, the PRBS[22:7], the PRBS[6:0] and the B1/E1 value.

IADDR[3:0]	RAM page
1000	STS-1 path Configuration
1001	PRBS[22:7]
1010	PRBS[6:0]
1011	B1/E1 value

RDWRB

The active high read and active low write (RDWRB) bit selects if the current access to the indirect register is an indirect read or an indirect write. Writing to the Indirect Address Register initiates an access to the indirect register. When RDWRB is set to logic 1, an indirect read access to the indirect register is initiated. The data from the addressed location will be transfer to the Indirect Data Register. When RDWRB is set to logic 0, an indirect write access to the indirect register is initiated. The data from the Indirect Data Register will be transfer to the addressed location.

BUSY

The active high busy (BUSY) bit reports if a previously initiated indirect access has been completed. BUSY is set to logic 1 upon writing to the Indirect Address Register. BUSY is set to logic 0, upon completion of the access. This register should be polled to determine when new data is available in the Indirect Data Register.
Note: Maximum busy bit set time is 22 clock cycles.

Register 0241H, 0641H, 0A41H and 0E41H: DPRGM Indirect Data

Bit	Type	Function	Default
Bit 15	R/W	DATA[15]	0
Bit 14	R/W	DATA[14]	0
Bit 13	R/W	DATA[13]	0
Bit 12	R/W	DATA[12]	0
Bit 11	R/W	DATA[11]	0
Bit 10	R/W	DATA[10]	0
Bit 9	R/W	DATA[9]	0
Bit 8	R/W	DATA[8]	0
Bit 7	R/W	DATA[7]	0
Bit 6	R/W	DATA[6]	0
Bit 5	R/W	DATA[5]	0
Bit 4	R/W	DATA[4]	0
Bit 3	R/W	DATA[3]	0
Bit 2	R/W	DATA[2]	0
Bit 1	R/W	DATA[1]	0
Bit 0	R/W	DATA[0]	0

The PRGM Indirect Data Register is provided at PRGM r/w address 01h when TRSB is high and BSB is low.

DATA[15:0]

The indirect access data (DATA[15:0]) bits hold the data transfer to or from during indirect access. When RDWRB is set to logic 1 (indirect read), the data from the addressed location will be transfer to DATA[15:0]. BUSY should be polled to determine when the new data is available in DATA[15:0]. When RDWRB is set to logic 0 (indirect write), the data from DATA[15:0] will be transfer to the addressed location. The indirect Data register must contain valid data before the indirect write is initiated by writing to the Indirect Address Register.

DATA[15:0] has a different meaning depending on which indirect register is being accessed.

Register 0242H, 0642H, 0A42H and 0E42H: DPRGM Generator Payload Configuration

Bit	Type	Function	Default
Bit 15	R/W	GEN_STS12CSL	0
Bit 14	R/W	GEN_STS12C	0
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10	R/W	GEN_MSSLEN[2]	0
Bit 9	R/W	GEN_MSSLEN[1]	0
Bit 8	R/W	GEN_MSSLEN[0]	0
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R/W	GEN_STS3C[4]	0
Bit 2	R/W	GEN_STS3C[3]	0
Bit 1	R/W	GEN_STS3C[2]	0
Bit 0	R/W	GEN_STS3C[1]	0

The Generator Payload Configuration register is provided at PRGM read address 02h when TRSB is high and BSB is low.

GEN_STS3C[1]

The STS-3c (VC-4) payload configuration (GEN_STS3C[1]) bit selects the payload configuration. When GEN_STS3C[1] is set to logic 1, the STS-1/STM-0 paths #1, #5 and #9 are part of a STS-3c (VC-4) payload. When GEN_STS3C[1] is set to logic 0, the paths are STS-1 (VC-3) payloads. When GEN_STS12C is set to logic 1, GEN_STS3C[1] must be set to logic 0.

GEN_STS3C[2]

The STS-3c (VC-4) payload configuration (GEN_STS3C[2]) bit selects the payload configuration. When GEN_STS3C[2] is set to logic 1, the STS-1/STM-0 paths #2, #6 and #10 are part of a STS-3c (VC-4) payload. When GEN_STS3C[2] is set to logic 0, the paths are STS-1 (VC-3) payloads. When GEN_STS12C is set to logic 1, GEN_STS3C[2] must be set to logic 0.

GEN_STS3C[3]

The STS-3c (VC-4) payload configuration (GEN_STS3C[3]) bit selects the payload configuration. When GEN_STS3C[3] is set to logic 1, the STS-1/STM-0 paths #3, #7 and #11 are part of a STS-3c (VC-4) payload. When GEN_STS3C[3] is set to logic 0, the paths are STS-1 (VC-3) payloads. When GEN_STS12C is set to logic 1, GEN_STS3C[3] must be set to logic 0.

GEN_STS3C[4]

The STS-3c (VC-4) payload configuration (GEN_STS3C[4]) bit selects the payload configuration. When GEN_STS3C[4] is set to logic 1, the STS-1/STM-0 paths #4, #8 and #12 are part of a STS-3c (VC-4) payload. When GEN_STS3C[4] is set to logic 0, the paths are STS-1 (VC-3) payloads. When GEN_STS12C is set to logic 1, GEN_STS3C[4] must be set to logic 0.

GEN_MSSLEN[2:0]

The Master/Slave Configuration Enable enables the master/slave configuration of the PRGM's generator.

GEN_MSSLEN[2:0]	Configuration
000	ms/sl configuration disable (STS-12/STM-4)
001	ms/sl configuration enable 2 PRGMs (STS-24/STM-8)
010	ms/sl configuration enable 3 PRGMs (STS-36/STM-12)
011	ms/sl configuration enable 4 PRGMs (STS-48/STM-16)
100 - 111	Invalid configuration

GEN_MSSLEN[2:0] must be set to "000" for rates STS-12c and below.

GEN_STS12C

The STS-12c (VC-4-4c) payload configuration (GEN_STS12C) bit selects the payload configuration. When GEN_STS12C is set to logic 1, the STS-1/STM-0 paths #1 to #12 are part of the same concatenated payload defined by GEN_MSSLEN. When GEN_STS12C is set to logic 0, the STS-1/STM-0 paths are defined with the GEN_STS3C[1:4] register bit.

GEN_STS12CSL

The slave STS-12c (VC-4-4c) payload configuration (GEN_STS12CSL) bit selects the slave payload configuration. When GEN_STS12CSL is set to logic 1, the STS-1/STM-0 paths #1 to #12 are part of a slave payload. When GEN_STS12CSL is set to logic 0, the STS-1/STM-0 paths are part of a master payload. When GEN_STS12C is set to logic 0, GEN_STS12CSL must be set to logic 0.

Register 0243H, 0643H, 0A43H and 0E43H: DPRGM Monitor Payload Configuration

Bit	Type	Function	Default
Bit 15	R/W	MON_STS12CSL	0
Bit 14	R/W	MON_STS12C	0
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10	R/W	MON_MSSLEN[2]	0
Bit 9	R/W	MON_MSSLEN[1]	0
Bit 8	R/W	MON_MSSLEN[0]	0
Bit 7		Unused	X
Bit 6	R/W	Reserved	0
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R/W	MON_STS3C[4]	0
Bit 2	R/W	MON_STS3C[3]	0
Bit 1	R/W	MON_STS3C[2]	0
Bit 0	R/W	MON_STS3C[1]	0

The Monitor Payload Configuration register is provided at PRGM read address 03h when TRSB is high and BSB is low.

MON_STS3C[1]

The STS-3c (VC-4) payload configuration (MON_STS3C[1]) bit selects the payload configuration. When MON_STS3C[1] is set to logic 1, the STS-1/STM-0 paths #1, #5 and #9 are part of a STS-3c/VC-4 payload. When MON_STS3C[1] is set to logic 0, the paths are STS-1/VC-3 payloads. When MON_STS12C is set to logic 1, MON_STS3C[1] must be set to logic 0.

MON_STS3C[2]

The STS-3c (VC-4) payload configuration (MON_STS3C[2]) bit selects the payload configuration. When MON_STS3C[2] is set to logic 1, the STS-1/STM-0 paths #2, #6 and #10 are part of a STS-3c/VC-4 payload. When MON_STS3C[2] is set to logic 0, the paths are STS-1/VC-3 payloads. When MON_STS12C is set to logic 1, MON_STS3C[2] must be set to logic 0.

MON_STS3C[3]

The STS-3c (VC-4) payload configuration (MON_STS3C[3]) bit selects the payload configuration. When MON_STS3C[3] is set to logic 1, the STS-1/STM-0 paths #3, #7 and #11 are part of a MON_STS-3c/VC-4 payload. When MON_STS3C[3] is set to logic 0, the paths are STS-1 (VC-3) payloads. When MON_STS12C is set to logic 1, MON_STS3C[3] must be set to logic 0.

MON_STS3C[4]

The STS-3c (VC-4) payload configuration (MON_STS3C[4]) bit selects the payload configuration. When MON_STS3C[4] is set to logic 1, the STS-1/STM-0 paths #4, #8 and #12 are part of a STS-3c/VC-4 payload. When MON_STS3C[4] is set to logic 0, the paths are STS-1/VC-3 payloads. When MON_STS12C is set to logic 1, MON_STS3C[4] must be set to logic 0.

To initialize the performance to counter to FFFAh, the ERR_CNT_TEST bit must be set high, and a LCLK pulse must be generated.

MON_MSSLEN[2:0]

The Master/Slave Configuration Enable enables the master/slave configuration of the PRGM's monitor.

GEN_MSSLEN[2:0]	Configuration
000	ms/sl configuration disable (STS-12/STM-4)
001	ms/sl configuration enable 2 PRGMs (STS-24/STM-8)
010	ms/sl configuration enable 3 PRGMs (STS-36/STM-12)
011	ms/sl configuration enable 4 PRGMs (STS-48/STM-16)
100 – 111	Invalid configuration

MON_MSSLEN[2:0] must be set to "000" for rates STS-12c and below.

MON_STS12C

The STS-12c (VC-4-4c) payload configuration (MON_STS12C) bit selects the payload configuration. When MON_STS12C is set to logic 1, the STS-1/STM-0 paths #1 to #12 are part of the same concatenated payload defined by MON_MSSLEN. When MON_STS12C is set to logic 0, the STS-1/STM-0 paths are defined with the MON_STS3C[3:0] register bit.

MON_STS12CSL

The slave STS-12c (VC-4-4c) payload configuration (MON_STS12CSL) bit selects the slave payload configuration. When MON_STS12CSL is set to logic 1, the STS-1/STM-0 paths #1 to #12 are part of a slave payload. When MON_STS12CSL is set to logic 0, the STS-1/STM-0 paths are part of a master payload. When MON_STS12C is set to logic 0, MON_STS12CSL must be set to logic 0.

Register 0244H, 0644H, 0A44H and 0E44H: DPRGM Monitor Byte Error Interrupt Status

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11	R	MON12_ERRI	X
Bit 10	R	MON11_ERRI	X
Bit 9	R	MON10_ERRI	X
Bit 8	R	MON9_ERRI	X
Bit 7	R	MON8_ERRI	X
Bit 6	R	MON7_ERRI	X
Bit 5	R	MON6_ERRI	X
Bit 4	R	MON5_ERRI	X
Bit 3	R	MON4_ERRI	X
Bit 2	R	MON3_ERRI	X
Bit 1	R	MON2_ERRI	X
Bit 0	R	MON1_ERRI	X

The Monitor Byte Error Interrupt Status register is provided at PRGM read address 04h when TRSB is high and BSB is low.

MON**x**_ERRI

The Monitor Byte Error Interrupt Status register, is the status of the interrupt generated by each of the 12 STS-1 paths when an error has been detected. The MON**x**_ERRI is set high when the monitor is in the synchronized state and when an error in a PRBS byte is detected in the STS-1 path **x**. This bit is independent of MON**x**_ERRE, and is cleared after it's been read.

Register 0245H, 0645H, 0A45H and 0E45H: DPRGM Monitor Byte Error Interrupt Enable

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11	R/W	MON12_ERRE	0
Bit 10	R/W	MON11_ERRE	0
Bit 9	R/W	MON10_ERRE	0
Bit 8	R/W	MON9_ERRE	0
Bit 7	R/W	MON8_ERRE	0
Bit 6	R/W	MON7_ERRE	0
Bit 5	R/W	MON6_ERRE	0
Bit 4	R/W	MON5_ERRE	0
Bit 3	R/W	MON4_ERRE	0
Bit 2	R/W	MON3_ERRE	0
Bit 1	R/W	MON2_ERRE	0
Bit 0	R/W	MON1_ERRE	0

The Monitor Byte Error Interrupt Enable register is provided at PRGM r/w address 05h when TRSB is high and BSB is low.

MON**x**_ERRE

The Monitor Byte Error Interrupt Enable register, enables the interrupt for each of the 12 STS-1 paths. When MON**x**_ERRE is set high, allows the Byte Error Interrupt to generate an external interrupt.

Register 0246H, 0646H, 0A46H and 0E46H: DPRGM Monitor B1/E1 Bytes Interrupt Status

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11	R	MON12_B1E1I	X
Bit 10	R	MON11_B1E1I	X
Bit 9	R	MON10_B1E1I	X
Bit 8	R	MON9_B1E1I	X
Bit 7	R	MON8_B1E1I	X
Bit 6	R	MON7_B1E1I	X
Bit 5	R	MON6_B1E1I	X
Bit 4	R	MON5_B1E1I	X
Bit 3	R	MON4_B1E1I	X
Bit 2	R	MON3_B1E1I	X
Bit 1	R	MON2_B1E1I	X
Bit 0	R	MON1_B1E1I	X

The Monitor B1/E1Bytes Interrupt Status register is provided at PRGM read address 06h when TRSB is high and BSB is low.

MON**x**_B1E1I

The Monitor B1/E1Bytes Interrupt Status register, is the status of the interrupt generated by each of the 12 STS-1 paths when a change in the status of the comparison has been detected on the B1/E1 bytes. The MON**x**_B1E1I is set high when the monitor is in the synchronized state and when the status change is detected on either the B1 or E1 bytes in the STS-1 path **x**. For example, if a mismatch is detected and the previous comparison was a match, the MON**x**_B1E1I will be set high. But if a mismatch is detected and the previous comparison was a mismatch, the MON**x**_B1E1I will keep its previous value. This bit is independent of MON**x**_B1E1E, and is cleared after it's been read.

Register 0247H, 0647H, 0A47H and 0E47H: DPRGM Monitor B1/E1 Bytes Interrupt Enable

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11	R/W	MON12_B1E1E	0
Bit 10	R/W	MON11_ B1E1E	0
Bit 9	R/W	MON10_ B1E1E	0
Bit 8	R/W	MON9_ B1E1E	0
Bit 7	R/W	MON8_ B1E1E	0
Bit 6	R/W	MON7_ B1E1E	0
Bit 5	R/W	MON6_ B1E1E	0
Bit 4	R/W	MON5_ B1E1E	0
Bit 3	R/W	MON4_ B1E1E	0
Bit 2	R/W	MON3_ B1E1E	0
Bit 1	R/W	MON2_ B1E1E	0
Bit 0	R/W	MON1_ B1E1E	0

The Monitor B1/E1Bytes Interrupt Enable register is provided at PRGM r/w address 07h when TRSB is high and BSB is low.

MON**x**_B1E1E

The Monitor B1/E1 Bytes Interrupt Enable register, enables the interrupt for each of the 12 STS-1 paths. When MON**x**_B1E1E is set high, allows the B1/E1Bytes Interrupt to generate an external interrupt.

Register 0249H, 0649H, 0A49H and 0E49H: DPRGM Monitor Synchronization Interrupt Status

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11	R	MON12_SYNCI	X
Bit 10	R	MON11_SYNCI	X
Bit 9	R	MON10_SYNCI	X
Bit 8	R	MON9_SYNCI	X
Bit 7	R	MON8_SYNCI	X
Bit 6	R	MON7_SYNCI	X
Bit 5	R	MON6_SYNCI	X
Bit 4	R	MON5_SYNCI	X
Bit 3	R	MON4_SYNCI	X
Bit 2	R	MON3_SYNCI	X
Bit 1	R	MON2_SYNCI	X
Bit 0	R	MON1_SYNCI	X

The Monitor Synchronization Interrupt Status register is provided at PRGM read address 09h when TRSB is high and BSB is low.1

MON**x**_SYNCI

The Monitor Synchronization Interrupt Status register, is set high when a change occurs in the monitor's synchronization status. Whenever a state machine of the **x** STS-1 path goes from Synchronized to Out Of Synchronization state or vice-versa, the MON**x**_SYNCI is set high. This bit is independent of MONx_SYNCE, and is cleared after it's been read.

Register 024AH, 064AH, 0A4AH and 0E4AH: DPRGM Monitor Synchronization Interrupt Enable

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11	R/W	MON12_SYNCE	0
Bit 10	R/W	MON11_SYNCE	0
Bit 9	R/W	MON10_SYNCE	0
Bit 8	R/W	MON9_SYNCE	0
Bit 7	R/W	MON8_SYNCE	0
Bit 6	R/W	MON7_SYNCE	0
Bit 5	R/W	MON6_SYNCE	0
Bit 4	R/W	MON5_SYNCE	0
Bit 3	R/W	MON4_SYNCE	0
Bit 2	R/W	MON3_SYNCE	0
Bit 1	R/W	MON2_SYNCE	0
Bit 0	R/W	MON1_SYNCE	0

The Monitor Synchronization Interrupt Enable register is provided at PRGM r/w address 0Ah when TRSB is high and BSB is low.

MON**x**_SYNCE

The Monitor Synchronization Interrupt Enable register, allows each individual STS-1 path to generate an external interrupt on INT. When MON**x**_SYNCE is set high, whenever a change occures in the synchronization state of the monitor in STS-1 path **x**, generates an interrupt.

Register 024BH, 064BH, 0A4BH and 0E4BH: DPRGM Monitor Synchronization Status

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11	R	MON12_SYNCV	X
Bit 10	R	MON11_SYNCV	X
Bit 9	R	MON10_SYNCV	X
Bit 8	R	MON9_SYNCV	X
Bit 7	R	MON8_SYNCV	X
Bit 6	R	MON7_SYNCV	X
Bit 5	R	MON6_SYNCV	X
Bit 4	R	MON5_SYNCV	X
Bit 3	R	MON4_SYNCV	X
Bit 2	R	MON3_SYNCV	X
Bit 1	R	MON2_SYNCV	X
Bit 0	R	MON1_SYNCV	X

The Monitor Synchronization Status register is provided at PRGM read address 0Bh when TRSB is high and BSB is low.

MON**x**_SYNCV

The Monitor Synchronization Status register, reflects the state of the monitor's state machine. When MON**x**_SYNCV is set high, the monitor's state machine is in synchronization for the STS-1 Path **x**. When MON**x**_SYNCV is low, the monitor is NOT in synchronization for the STS-1 Path **x**.
Note: The PRBS monitor will lock to an all 1s or all 0s pattern.
Note: For concatenated payloads, only the first STS-1 path of the STS-Nc MONx_SYNCV1 bit is valid.

Register 024CH, 064CH, 0A4CH and 0E4CH: DPRGM Counter Update

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9		Unused	
Bit 8		Unused	
Bit 7		Unused	
Bit 6		Unused	
Bit 5		Unused	
Bit 4		Unused	
Bit 3		Unused	
Bit 2		Unused	
Bit 1		Unused	
Bit 0	R	Reserved	X

The Counter Update register is provided at PRGM read address 0Ch when TRSB is high and BSB is low.

A write in this register or to the Master Configuration Register (0000H) will trigger the transfer of the error counters to holding registers where they can be read. The value written in the register is not important.

Indirect Register 00h: DPRGM Monitor STS-1 path Configuration

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10	R/W	Reserved	0
Bit 9	R/W	Reserved	0
Bit 8		Unused	
Bit 7		Unused	
Bit 6	R/W	SEQ_PRBSB	0-
Bit 5	R/W	B1E1_ENA	0
Bit 4		Unused	
Bit 3	W	RESYNC	0
Bit 2	R/W	INV_PRBS	0
Bit 1	R/W	AMODE	0
Bit 0	R/W	MON_ENA	0

PRGM Indirect Data Register (Register 01h) definition when accessing Indirect Address 0h (IADDR[3:0] is “0h” of register 00h).

MON_ENA

Monitor Enable register bit, enables the PRBS monitor for the STS-1 path specified in the PATH[3:0] of register 0h (PRGM Indirect Addressing). If MON_ENA is set to ‘1’, a PRBS sequence is generated and compare to the incoming one inserted in the payload of the SONET/SDH frame. If MON_ENA is low, the data at the input of the monitor is ignored.

AMODE

Sets the PRGM monitor in the Telecom bus mode. If the AMODE is high, the monitor is in Autonomous mode, and the incoming SONET/SDH payload is compared to the internally generated one. In Autonomous mode, the beginning of the SPE is always place next to the H3 byte (zero offset), so the J1 pulses are ignored. When AMODE is low, the SONET/SDH payload offset received on the line interface is maintain through the PRGM block. The TOH and the POH are outputted unmodified, but PRBS has been inserted in the payload.

INV_PRBS

Sets the monitor to invert the PRBS before comparing it to the internally generated payload. When set high, the PRBS bytes will be inverted, else they will be compared unmodified.

RESYNC

Sets the monitor to re-initialize the PRBS sequence. When set high, the monitor's state machine will be forced in the Out Of Sync state and automatically try to resynchronize to the incoming stream. In master/slave configuration, to re-initialize the PRBS, RESYNC has to be set high in the master PRGM only.

B1E1_ENA

When high, this bit enables the monitoring of the B1 and E1 bytes in the SONET/SDH frame. The incoming B1 byte is compared to a programmable register. The E1 byte is compared to the complement of the same value. When B1E1_ENA is high, the B1 and E1 bytes are monitored.

SEQ_PRBSB

This bit enables the monitoring of a PRBS or sequential pattern inserted in the payload. When low, the payload contains PRBS bytes, and when high, a sequential pattern is monitored.

Indirect Register 01h: DPRGM Monitor PRBS[22:7] Accumulator

Bit	Type	Function	Default
Bit 15	R/W	PRBS[22]	0
Bit 14	R/W	PRBS[21]	0
Bit 13	R/W	PRBS[20]	0
Bit 12	R/W	PRBS[19]	0
Bit 11	R/W	PRBS[18]	0
Bit 10	R/W	PRBS[17]	0
Bit 9	R/W	PRBS[16]	0
Bit 8	R/W	PRBS[15]	0
Bit 7	R/W	PRBS[14]	0
Bit 6	R/W	PRBS[13]	0
Bit 5	R/W	PRBS[12]	0
Bit 4	R/W	PRBS[11]	0
Bit 3	R/W	PRBS[10]	0
Bit 2	R/W	PRBS[9]	0
Bit 1	R/W	PRBS[8]	0
Bit 0	R/W	PRBS[7]	0

PRGM Indirect Data Register (Register 01h) definition when accessing Indirect Address 1h (IADDR[3:0] is “1h” of register 00h).

PRBS[22:7]

The PRBS[22:7] register, are the 16 MSBs of the LFSR state of the STS-1 path specified in the Indirect Addressing register. It is possible to write in this register to change the initial state of the register.

Indirect Register 02H: DPRGM Monitor PRBS[6:0] Accumulator

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9		Unused	
Bit 8		Unused	
Bit 7		Unused	
Bit 6	R/W	PRBS[6]	0
Bit 5	R/W	PRBS[5]	0
Bit 4	R/W	PRBS[4]	0
Bit 3	R/W	PRBS[3]	0
Bit 2	R/W	PRBS[2]	0
Bit 1	R/W	PRBS[1]	0
Bit 0	R/W	PRBS[0]	0

PRGM Indirect Data Register (Register 01h) definition when accessing Indirect Address 2h (IADDR[3:0] is “2h” of register 00h).

PRBS[7:0]

The PRBS[7:0] register, are the 6 LSBs of the LFSR state of the STS-1 path specified in the Indirect Addressing register. It is possible to write in this register to change the initial state of the register.

Indirect Register 03H: DPRGM Monitor B1/E1 value

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9		Unused	
Bit 8		Unused	
Bit 7	R/W	B1[7]	0
Bit 6	R/W	B1[6]	0
Bit 5	R/W	B1[5]	0
Bit 4	R/W	B1[4]	0
Bit 3	R/W	B1[3]	0
Bit 2	R/W	B1[2]	0
Bit 1	R/W	B1[1]	0
Bit 0	R/W	B1[0]	0

PRGM Indirect Data Register (Register 01h) definition when accessing Indirect Address 3h (IADDR[3:0] is “3h” of register 00h).

B1[7:0]

When enabled, the monitoring of the B1byte in the incoming SONET/SDH frame, is a simple comparison to the value in the B1[7:0] register. The same value is used for the monitoring of the E1 byte except its complement is used.

Indirect Register 04H: DPRGM Monitor Error count

Bit	Type	Function	Default
Bit 15	R	ERR_CNT[15]	X
Bit 14	R	ERR_CNT[14]	X
Bit 13	R	ERR_CNT[13]	X
Bit 12	R	ERR_CNT[12]	X
Bit 11	R	ERR_CNT[11]	X
Bit 10	R	ERR_CNT[10]	X
Bit 9	R	ERR_CNT[9]	X
Bit 8	R	ERR_CNT[8]	X
Bit 7	R	ERR_CNT[7]	X
Bit 6	R	ERR_CNT[6]	X
Bit 5	R	ERR_CNT[5]	X
Bit 4	R	ERR_CNT[4]	X
Bit 3	R	ERR_CNT[3]	X
Bit 2	R	ERR_CNT[2]	X
Bit 1	R	ERR_CNT[1]	X
Bit 0	R	ERR_CNT[0]	X

PRGM Indirect Data Register (Register 01h) definition when accessing Indirect Address 4h (IADDR[3:0] is “4h” of register 00h).

ERR_CNT[15:0]

The ERR_CNT[15:0] registers, is the number of error in the PRBS bytes detected during the monitoring. Errors are accumulated only when the monitor is in the synchronized state. Even if there is multiple errors within one PRBS byte, only one error is counted. The error counter is cleared and restarted after its value is transferred to the ERR_CNT[15:0] holding registers. No errors are missed during the transfer. The error counter will not wrap around after reaching FFFFh, it will saturate at this value.
Note: When losing synchronization, the PRBS monitor in the PRGM block incorrectly counts up to two additional byte errors.

Indirect Register 05H: DPRGM Monitor Received B1/E1 bytes

Bit	Type	Function	Default
Bit 15	R	REC_E1[7]	X
Bit 14	R	REC_E1[6]	X
Bit 13	R	REC_E1[5]	X
Bit 12	R	REC_E1[4]	X
Bit 11	R	REC_E1[3]	X
Bit 10	R	REC_E1[2]	X
Bit 9	R	REC_E1[1]	X
Bit 8	R	REC_E1[0]	X
Bit 7	R	REC_B1[7]	X
Bit 6	R	REC_B1[6]	X
Bit 5	R	REC_B1[5]	X
Bit 4	R	REC_B1[4]	X
Bit 3	R	REC_B1[3]	X
Bit 2	R	REC_B1[2]	X
Bit 1	R	REC_B1[1]	X
Bit 0	R	REC_B1[0]	X

PRGM Indirect Data Register (Register 01h) definition when accessing Indirect Address 5h (IADDR[3:0] is “5h” of register 00h).

REC_B1[7:0]

The Received B1 byte is the content of the B1 byte position in the SONET/SDH frame for this particular STS-1 path. Every time a B1 byte is received, it is copied in this register.

REC_E1[7:0]

The Received E1 byte is the content of the E1 byte position in the SONET/SDH frame for this particular STS-1 path. Every time a E1 byte is received, it is copied in this register.

Indirect Register 08H: DPRGM Generator STS-1 path Configuration

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13	R/W	Reserved	0
Bit 12	R/W	GEN_ENA	0
Bit 11		Unused	
Bit 10		Unused	
Bit 9	R/W	Reserved	0
Bit 8	R/W	DALARM_DIS	0
Bit 7	R/W	SS[1]	0
Bit 6	R/W	SS[0]	0
Bit 5	R/W	SEQ_PRBSB	0
Bit 4	R/W	B1E1_ENA	0
Bit 3	W	FORCE_ERR	0
Bit 2		Unused	
Bit 1	R/W	INV_PRBS	0
Bit 0	R/W	AMODE	0

PRGM Indirect Data Register (Register 01h) definition when accessing Indirect Address 8h (IADDR[3:0] is “8h” of register 00h).

AMODE

Sets the PRGM generator in the Telecom bus or in Autonomous mode. If the AMODE is high, the generator is in Autonomous mode, and the SONET/SDH frame is generated using only the J0 pulse. When AMODE is low, the SONET/SDH frame is received on the Telecom bus. The TOH and the POH are outputted unmodified, but PRBS is inserted in the payload.

INV_PRBS

Sets the generator to invert the PRBS before inserting it in the payload. When set high, the PRBS bytes will be inverted, else they will be inserted unmodified.

FORCE_ERR

The Force Error bit is used to force bit errors in the inserted pattern. When set high, the MSB of the next byte will be inverted, inducing a single bit error. The register clear itself when the operation is complete. A read operation will always result in a logic ‘0’.

B1E1_ENA

This bit enables the replacement of the B1 byte in the SONET/SDH frame, by a programmable value. The E1 byte is replaced by the complement of the same value. When B1E1_ENA is high, the B1 and E1 bytes are replaced in the frame, else they go through the PRGM unaltered. The B1/E1 byte insertion is independent of PRBS insertion.

SEQ_PRBSB

This bit enables the insertion of a PRBS sequence or a sequential pattern in the payload. When low, the payload is filled with PRBS bytes, and when high, a sequential pattern is inserted.

SS[1:0]

The SS bits signal, is the value to be inserted in bit 2 and 3 of the H1 byte of a concatenated pointer. This value is used when the PRGM is in processing concatenated payload and in autonomous mode.

DALARM_DIS

The Drop Bus DALARM Disable controls the DALARM port on a per STS-1/STM-0 basis. When low, the DALARM port reports the AIS-P insertion in the receive side for the corresponding STS-1/STM-0 path. When high, the DALARM port will not report AIS-P insertion in the receive stream for the corresponding STS-1/STM-0 path.

GEN_ENA

This bit specifies if PRBS is to be inserted. If GEN_ENA is high, patterns are generated and inserted, else no pattern is generated and the unmodified SONET/SDH input frame is outputted.

Indirect Register 09H: DPRGM Generator PRBS[22:7] Accumulator

Bit	Type	Function	Default
Bit 15	R/W	PRBS[22]	0
Bit 14	R/W	PRBS[21]	0
Bit 13	R/W	PRBS[20]	0
Bit 12	R/W	PRBS[19]	0
Bit 11	R/W	PRBS[18]	0
Bit 10	R/W	PRBS[17]	0
Bit 9	R/W	PRBS[16]	0
Bit 8	R/W	PRBS[15]	0
Bit 7	R/W	PRBS[14]	0
Bit 6	R/W	PRBS[13]	0
Bit 5	R/W	PRBS[12]	0
Bit 4	R/W	PRBS[11]	0
Bit 3	R/W	PRBS[10]	0
Bit 2	R/W	PRBS[9]	0
Bit 1	R/W	PRBS[8]	0
Bit 0	R/W	PRBS[7]	0

PRGM Indirect Data Register (Register 01h) definition when accessing Indirect Address 9h (IADDR[3:0] is “9h” of register 00h).

PRBS[22:7]

The PRBS[22:7] register, are the 16 MSBs of the LFSR state of the STS-1 path specified in the Indirect Addressing register. It is possible to write in this register to change the initial state of the register.

Indirect Register 0AH: DPRGM Generator PRBS[6:0] Accumulator

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9		Unused	
Bit 8		Unused	
Bit 7		Unused	
Bit 6	R/W	PRBS[6]	0
Bit 5	R/W	PRBS[5]	0
Bit 4	R/W	PRBS[4]	0
Bit 3	R/W	PRBS[3]	0
Bit 2	R/W	PRBS[2]	0
Bit 1	R/W	PRBS[1]	0
Bit 0	R/W	PRBS[0]	0

PRGM Indirect Data Register (Register 01h) definition when accessing Indirect Address Ah (IADDR[3:0] is “Ah” of register 00h).

PRBS[6:0]

The PRBS[6:0] register, are the 7 LSBs of the LFSR state of the STS-1 path specified in the Indirect Addressing register. It is possible to write in this register to change the initial state of the register.

Indirect Register 0Bh: DPRGM Generator B1/E1 value

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9		Unused	
Bit 8		Unused	
Bit 7	R/W	B1[7]	0
Bit 6	R/W	B1[6]	0
Bit 5	R/W	B1[5]	0
Bit 4	R/W	B1[4]	0
Bit 3	R/W	B1[3]	0
Bit 2	R/W	B1[2]	0
Bit 1	R/W	B1[1]	0
Bit 0	R/W	B1[0]	0

PRGM Indirect Data Register (Register 01h) definition when accessing Indirect Address Bh (IADDR[3:0] is “Bh” of register 00h).

B1[7:0]

When enabled, the value in this register is inserted in the B1byte position in the outgoing SONET/SDH frame. The complement of this value is also inserted at the E1 byte position.

Register 0260H, 0660H, 0A60H and 0E60H: SARC Indirect Address

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	0
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9		Unused	
Bit 8		Unused	
Bit 7		Unused	
Bit 6		Unused	
Bit 5		Unused	
Bit 4		Unused	
Bit 3	R/W	PATH[3]	0
Bit 2	R/W	PATH[2]	0
Bit 1	R/W	PATH[1]	0
Bit 0	R/W	PATH[0]	0

The Indirect Address Register is provided at SARC r/w address 00H.

PATH[3:0]

The STS-1/STM-0 path (PATH[3:0]) bits select which STS-1/STM-0 path is accessed by the current read or write from the following registers 08H, 09H, 0AH, 0CH, 0DH and 0EH.

PATH[3:0]	STS-1/STM-0 path #
0000	Invalid path
0001-1100	Path #1 to Path #12
1101-1111	Invalid path

Register 0262H, 0662H, 0A62H and 0E62H: SARC Section Configuration

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9		Unused	
Bit 8		Unused	
Bit 7		Unused	
Bit 6		Unused	
Bit 5		Unused	
Bit 4		Unused	
Bit 3		Unused	
Bit 2		Unused	
Bit 1	R/W	LRDI20	0
Bit 0	R/W	TLRCPEN	0

The Section Configuration Register is provided at SARC r/w address 02H.

TLRCPEN

The transmit line ring control port enable (TLRCPEN) bit enables the TRCP port. When TLRCPEN is set to logic 1, the APS, RDI-L and REI-L insertion indication are extracted from the TRCP port. When TRCPEN is set to logic 0, the APS, RDI-L and REI-L insertion indication are derived from the defect detected on the receive data stream.

LRDI20

The line remote defect indication (LRDI20) bit selects the line RDI persistence. When LRDI20 is set to logic 1, a new line RDI indication is transmitted for at least 20 frames. When LRDI20 is set to logic 0, a new line RDI indication is transmitted for at least 10 frames.

Register 0263H, 0663H, 0A63H and 0E63H: SARC Section Receive SALM Enable

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11	R/W	Reserved	0
Bit 10	R/W	Reserved	0
Bit 9	R/W	SFBEREN	0
Bit 8	R/W	SDBEREN	0
Bit 7	R/W	STIMEN	0
Bit 6	R/W	STIUEN	0
Bit 5	R/W	APSBFEN	0
Bit 4	R/W	LRDIEN	0
Bit 3	R/W	LAISEN	0
Bit 2	R/W	LOSEN	0
Bit 1	R/W	LOFEN	0
Bit 0	R/W	OOFEN	0

The Section Receive SALM Enable Register is provided at SARC r/w address 03H.

OOFEN

The OOF enable bit allows the out of frame defect to be ORed into the SALM output. When the OOFEN bit is set high, the corresponding defect indication is ORed with other defect indications to trigger the SALM output. When the OOFEN bit is set low, the corresponding defect indication does not affect the SALM output.

LOFEN

The LOF enable bit allows the loss of frame defect to be ORed into the SALM output. When the LOFEN bit is set high, the corresponding defect indication is ORed with other defect indications to trigger the SALM output. When the LOFEN bit is set low, the corresponding defect indication does not affect the SALM output.

LOSEN

The LOS enable bit allows the loss of signal defect to be ORed into the SALM output. When the LOSEN bit is set high, the corresponding defect indication is ORed with other defect indications to trigger the SALM output. When the LOSEN bit is set low, the corresponding defect indication does not affect the SALM output.

LAISEN

The LAIS enable bit allows the line alarm indication signal defect to be ORed into the SALM output. When the LAISEN bit is set high, the corresponding defect indication is ORed with other defect indications to trigger the SALM output. When the LAISEN bit is set low, the corresponding defect indication does not affect the SALM output.

LRDIEN

The LRDI enable bit allows the line remote defect indication defect to be ORed into the SALM output. When the LRDIEN bit is set high, the corresponding defect indication is ORed with other defect indications to trigger the SALM output. When the LRDIEN bit is set low, the corresponding defect indication does not affect the SALM output.

APSBFEN

The APSBF enable bit allows the APS byte failure defect to be ORed into the SALM output. When the APSBFEN bit is set high, the corresponding defect indication is ORed with other defect indications to trigger the SALM output. When the APSBFEN bit is set low, the corresponding defect indication does not affect the SALM output.

STIUEN

The STIU enable bit allows the section trace identifier unstable defect to be ORed into the SALM output. When the STIUEN bit is set high, the corresponding defect indication is ORed with other defect indications to trigger the SALM output. When the STIUEN bit is set low, the corresponding defect indication does not affect the SALM output.

STIMEN

The STIM enable bit allows the section trace identifier mismatch defect to be ORed into the SALM output. When the STIMEN bit is set high, the corresponding defect indication is ORed with other defect indications to trigger the SALM output. When the STIMEN bit is set low, the corresponding defect indication does not affect the SALM output.

SDBEREN

The SDBER enable bit allows the signal degrade BER defect to be ORed into the SALM output. When the SDBEREN bit is set high, the corresponding defect indication is ORed with other defect indications to trigger the SALM output. When the SDBEREN bit is set low, the corresponding defect indication does not affect the SALM output.

SFBEREN

The SFBER enable bit allows the signal failure BER defect to be ORed into the SALM output. When the SFBEREN bit is set high, the corresponding defect indication is ORed with other defect indications to trigger the SALM output. When the SFBEREN bit is set low, the corresponding defect indication does not affect the SALM output.

Register 0264H, 0664H, 0A64H and 0E64H: SARC Section Receive AIS-L Enable

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11	R/W	Reserved	0
Bit 10	R/W	Reserved	0
Bit 9	R/W	SFBEREN	0
Bit 8	R/W	SDBEREN	0
Bit 7	R/W	STIMEN	0
Bit 6	R/W	STIUEN	0
Bit 5	R/W	APSBFEN	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	LAISEN	0
Bit 2	R/W	LOSEN	0
Bit 1	R/W	LOFEN	0
Bit 0	R/W	OOFEN	0

The Section Receive AIS-L Enable Register is provided at SARC r/w address 04H.

OOFEN

The OOF enable bit allows the out of frame defect to be ORed into the receive AIS-L generation. When the OOFEN bit is set high, the corresponding defect indication is ORed with other defect indications to enable receive AIS-L generation. When the OOFEN bit is set low, the corresponding defect indication does not enable receive AIS-L generation.

LOFEN

The LOF enable bit allows the loss of frame defect to be ORed into the receive AIS-L generation. When the LOFEN bit is set high, the corresponding defect indication is ORed with other defect indications to enable receive AIS-L generation. When the LOFEN bit is set low, the corresponding defect indication does not enable receive AIS-L generation.

LOSEN

The LOS enable bit allows the loss of signal defect to be ORed into the receive AIS-L generation. When the LOSEN bit is set high, the corresponding defect indication is ORed with other defect indications to enable receive AIS-L generation. When the LOSEN bit is set low, the corresponding defect indication does not enable receive AIS-L generation.

LAISEN

The LAIS enable bit allows the line alarm indication signal defect to be ORed into the receive AIS-L generation. When the LAISEN bit is set high, the corresponding defect indication is ORed with other defect indications to enable receive AIS-L generation. When the LAISEN bit is set low, the corresponding defect indication does not enable receive AIS-L generation.

receive AIS-LAPSBFEN

The APSBF enable bit allows the APS byte failure defect to be ORed into the receive AIS-L generation. When the APSBFEN bit is set high, the corresponding defect indication is ORed with other defect indications to enable receive AIS-L generation. When the APSBFEN bit is set low, the corresponding defect indication does not enable receive AIS-L generation.

STIUEN

The STIU enable bit allows the section trace identifier unstable defect to be ORed into the receive AIS-L generation. When the STIUEN bit is set high, the corresponding defect indication is ORed with other defect indications to enable receive AIS-L generation. When the STIUEN bit is set low, the corresponding defect indication does not enable receive AIS-L generation.

STIMEN

The STIM enable bit allows the section trace identifier mismatch defect to be ORed into the receive AIS-L generation. When the STIMEN bit is set high, the corresponding defect indication is ORed with other defect indications to enable receive AIS-L generation. When the STIMEN bit is set low, the corresponding defect indication does not enable receive AIS-L generation.

SDBEREN

The SDBER enable bit allows the signal degrade BER defect to be ORed into the receive AIS-L generation. When the SDBEREN bit is set high, the corresponding defect indication is ORed with other defect indications to enable receive AIS-L generation. When the SDBEREN bit is set low, the corresponding defect indication does not enable receive AIS-L generation.

SFBEREN

The SFBER enable bit allows the signal failure BER defect to be ORed into the receive AIS-L generation. When the SFBEREN bit is set high, the corresponding defect indication is ORed with other defect indications to enable receive AIS-L generation. When the SFBEREN bit is set low, the corresponding defect indication does not enable receive AIS-L generation.

receive AIS-L

Register 0265H, 0665H, 0A65H and 0E65H: SARC Section Transmit RDI-L Enable

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11	R/W	Reserved	0
Bit 10	R/W	Reserved	0
Bit 9	R/W	SFBEREN	0
Bit 8	R/W	SDBEREN	0
Bit 7	R/W	STIMEN	0
Bit 6	R/W	STIUEN	0
Bit 5	R/W	APSBFEN	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	LAISEN	0
Bit 2	R/W	LOSEN	0
Bit 1	R/W	LOFEN	0
Bit 0	R/W	OOFEN	0

The Section Transmit RDI-L Enable Register is provided at SARC r/w address 05H.

OOFEN

The OOF enable bit allows the out of frame defect to be ORed into the transmit RDI-L generation. When the OOFEN bit is set high, the corresponding defect indication is ORed with other defect indications to enable transmit RDI-L generation. When the OOFEN bit is set low, the corresponding defect indication does not enable transmit RDI-L generation.

LOFEN

The LOF enable bit allows the loss of frame defect to be ORed into the transmit RDI-L generation. When the LOFEN bit is set high, the corresponding defect indication is ORed with other defect indications to enable transmit RDI-L generation. When the LOFEN bit is set low, the corresponding defect indication does not enable transmit RDI-L generation.

LOSEN

The LOS enable bit allows the loss of signal defect to be ORed into the transmit RDI-L generation. When the LOSEN bit is set high, the corresponding defect indication is ORed with other defect indications to enable transmit RDI-L generation. When the LOSEN bit is set low, the corresponding defect indication does not enable transmit RDI-L generation.

LAISEN

The LAIS enable bit allows the line alarm indication signal defect to be ORed into the transmit RDI-L generation. When the LAISEN bit is set high, the corresponding defect indication is ORed with other defect indications to enable transmit RDI-L generation. When the LAISEN bit is set low, the corresponding defect indication does not enable transmit RDI-L generation.

APSBFEN

The APSBF enable bit allows the APS byte failure defect to be ORed into the transmit RDI-L generation. When the APSBFEN bit is set high, the corresponding defect indication is ORed with other defect indications to enable transmit RDI-L generation. When the APSBFEN bit is set low, the corresponding defect indication does not enable transmit RDI-L generation.

STIUEN

The STIU enable bit allows the section trace identifier unstable defect to be ORed into the transmit RDI-L generation. When the STIUEN bit is set high, the corresponding defect indication is ORed with other defect indications to enable transmit RDI-L generation. When the STIUEN bit is set low, the corresponding defect indication does not enable transmit RDI-L generation.

STIMEN

The STIM enable bit allows the section trace identifier mismatch defect to be ORed into the transmit RDI-L generation. When the STIMEN bit is set high, the corresponding defect indication is ORed with other defect indications to enable transmit RDI-L generation. When the STIMEN bit is set low, the corresponding defect indication does not enable transmit RDI-L generation.

SDBEREN

The SDBER enable bit allows the signal degrade BER defect to be ORed into the transmit RDI-L generation. When the SDBEREN bit is set high, the corresponding defect indication is ORed with other defect indications to enable transmit RDI-L generation. When the SDBEREN bit is set low, the corresponding defect indication does not enable transmit RDI-L generation.

SFBEREN

The SFBER enable bit allows the signal failure BER defect to be ORed into the transmit RDI-L generation. When the SFBEREN bit is set high, the corresponding defect indication is ORed with other defect indications to enable transmit RDI-L generation. When the SFBEREN bit is set low, the corresponding defect indication does not enable transmit RDI-L generation.

Register 0268H, 0668H, 0A68H and 0E68H: SARC Path Configuration

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9		Unused	
Bit 8		Unused	
Bit 7	R/W	PRDIEN	0
Bit 6	R/W	PERDI20	0
Bit 5	R/W	TPRCPEN	0
Bit 4	R/W	PLOPTREND	0
Bit 3	R/W	PAISPTRCFG[1]	0
Bit 2	R/W	PAISPTRCFG[0]	0
Bit 1	R/W	PLOPTRCFG[1]	0
Bit 0	R/W	PLOPTRCFG[0]	0

The Path Configuration Register is provided at SARC r/w address 08H.

PLOPTRCFG[1:0]

The path loss of pointer configuration (PLOPTRCFG[1:0]) bits define the LOP-P defect. When PLOPTRCFG[1:0] is set to 00b, an LOP-P defect is declared when the pointer is in the LOP state and an LOP-P defect is removed when the pointer is not in the LOP state. When PLOPTRCFG[1:0] is set to 01b, an LOP-P defect is declared when the pointer or any of the concatenated pointers is in the LOP state and an LOP-P defect is removed when the pointer and all the concatenation pointers are not in the LOP state. When PLOPTRCFG[1:0] is set to 10b, an LOP-P defect is declared when the pointer or any of the concatenated pointers is in the LOP state or in the AIS state and an LOP-P defect is removed when the pointer and all the concatenation pointers are not in the LOP state or in the AIS state.

PAISPTRCFG[1:0]

The path AIS pointer configuration (PAISPTRCFG[1:0]) bits define the AIS-P defect. When PAISPTRCFG[1:0] is set to 00b, an AIS-P defect is declared when the pointer is in the AIS state and an AIS-P defect is removed when the pointer is not in the AIS state. When PAISPTRCFG[1:0] is set to 01b, an AIS-P defect is declared when the pointer or any of the concatenated pointers is in the AIS state and an AIS-P defect is removed when the pointer and all the concatenation pointers are not in the AIS state. When PAISPTRCFG[1:0] is set to 10b, an AIS-P defect is declared when the pointer and all the concatenated pointers are in the AIS state and an AIS-P defect is removed when the pointer or any of the concatenation pointers is not in the AIS state.

PLOPTREND

The path loss of pointer removal (PLOPTREND) bit controls the removal of a LOP-P defect when an AIS-P defect is declared. When PLOPTREND is set to logic 1, a LOP-P defect is terminated when an AIS-P defect is declared. When PLOPTREND is set to logic 0, a LOP-P defect is not terminated when an AIS-P defect is declared.

TPRCPEN

The transmit path ring control port enable (TPRCPEN) bit enables the TRCP port. When TPRPEN is set to logic 1, ERDI-P and REI-P insertion indication are extracted from the TRCP port. When TRCPEN is set to logic 0, ERDI-P and REI-P insertion indication are derived from the defect detected on the receive data stream.

PERDI20

The path enhance remote defect indication (PERDI20) bit selects the path ERDI persistence. When PERDI20 is set to logic 1, a new path ERDI indication is transmitted for at least 20 frames. When PERDI20 is set to logic 0, a new path ERDI indication is transmitted for at least 10 frames.

PRDIEN

The path remote defect indication enable (PRDIEN) bit selects between the 1 bit RDI code and the 3 bits ERDI code. When PRDIEN is set to logic 1, the 1 bit RDI code is transmitted. When PRDIEN is set to logic 0, the 3 bit ERDI code is transmitted.

Register 0269H, 0669H, 0A69H and 0E69H: SARC Path Receive RALM Enable

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13	R/W	Reserved	0
Bit 12	R/W	Reserved	0
Bit 11	R/W	PTIMEN	0
Bit 10	R/W	PTIUEN	0
Bit 9	R/W	PERDIEN	0
Bit 8	R/W	PRDIEN	0
Bit 7	R/W	PPDIEN	0
Bit 6	R/W	PUNEQEN	0
Bit 5	R/W	PPLMEN	0
Bit 4	R/W	PPLUEN	0
Bit 3	R/W	PAISPTREN	0
Bit 2	R/W	PLOPTREN	0
Bit 1	R/W	MSSALMEN	0
Bit 0	R/W	SALMEN	0

The Path Receive RALM Enable Register is provided at SARC r/w address 09H.

SALMEN

The SALM enable bit allows the receive section alarm to be ORed into the RALM output. When the SALMEN bit is set high, the corresponding alarm indication is ORed with other defect indications to trigger the RALM output. When the SALMEN bit is set low, the corresponding alarm indication does not affect the RALM output.

MSSALMEN

The master SALM enable bit allows the master receive section alarm to be ORed into the RALM output. When the MSSALMEN bit is set high, the corresponding alarm indication is ORed with other defect indications to trigger the RALM output. When the MSSALMEN bit is set low, the corresponding alarm indication does not affect the RALM output.

PLOPTREN

The PLOPTR enable bit allows the path loss of pointer defect to be ORed into the RALM output. When the PLOPTREN bit is set high, the corresponding defect indication is ORed with other defect indications to trigger the RALM output. When the PLOPTREN bit is set low, the corresponding defect indication does not affect the RALM output.

PAISPTREN

The PAISPTR enable bit allows the path AIS pointer defect to be ORed into the RALM output. When the PAISPTREN bit is set high, the corresponding defect indication is ORed with other defect indications to trigger the RALM output. When the PAISPTREN bit is set low, the corresponding defect indication does not affect the RALM output.

PPLUEN

The PPLU enable bit allows the path payload label unstable defect to be ORed into the RALM output. When the PPLUEN bit is set high, the corresponding defect indication is ORed with other defect indications to trigger the RALM output. When the PPLUEN bit is set low, the corresponding defect indication does not affect the RALM output.

PPLMEN

The PPLM enable bit allows the path payload label mismatch defect to be ORed into the RALM output. When the PPLMEN bit is set high, the corresponding defect indication is ORed with other defect indications to trigger the RALM output. When the PPLMEN bit is set low, the corresponding defect indication does not affect the RALM output.

PUNEQEN

The PUNEQ enable bit allows the path unequipped defect to be ORed into the RALM output. When the PUNEQEN bit is set high, the corresponding defect indication is ORed with other defect indications to trigger the RALM output. When the PUNEQEN bit is set low, the corresponding defect indication does not affect the RALM output.

PPDIEN

The PPDI enable bit allows the path payload defect indication defect to be ORed into the RALM output. When the PPDIEN bit is set high, the corresponding defect indication is ORed with other defect indications to trigger the RALM output. When the PPDIEN bit is set low, the corresponding defect indication does not affect the RALM output.

PRDIEN

The PRDI enable bit allows the path remote defect indication defect to be ORed into the RALM output. When the PRDIEN bit is set high, the corresponding defect indication is ORed with other defect indications to trigger the RALM output. When the PRDIEN bit is set low, the corresponding defect indication does not affect the RALM output.

PERDIEN

The PERDI enable bit allows the path enhanced remote defect indication defect to be ORed into the RALM output. When the PERDIEN bit is set high, the corresponding defect indication is ORed with other defect indications to trigger the RALM output. When the PERDIEN bit is set low, the corresponding defect indication does not affect the RALM output.

PTIUEN

The PTIU enable bit allows the path trace identifier unstable defect to be ORed into the RALM output. When the PTIUEN bit is set high, the corresponding defect indication is ORed with other defect indications to trigger the RALM output. When the PTIUEN bit is set low, the corresponding defect indication does not affect the RALM output.

PTIMEN

The PTIM enable bit allows the path trace identifier mismatch defect to be ORed into the RALM output. When the PTIMEN bit is set high, the corresponding defect indication is ORed with other defect indications to trigger the RALM output. When the PTIMEN bit is set low, the corresponding defect indication does not affect the RALM output.

Register 026AH, 066AH, 0A6AH and 0E6AH: SARC Path Receive AIS-P Enable

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13	R/W	Reserved	0
Bit 12	R/W	Reserved	0
Bit 11	R/W	PTIMEN	0
Bit 10	R/W	PTIUEN	0
Bit 9	R/W	Reserved	0
Bit 8	R/W	Reserved	0
Bit 7	R/W	PPDIEN	0
Bit 6	R/W	PUNEQEN	0
Bit 5	R/W	PPLMEN	0
Bit 4	R/W	PPLUEN	0
Bit 3	R/W	PAISPTREN	0
Bit 2	R/W	PLOPTREN	0
Bit 1	R/W	MSRLAISINSEN	0
Bit 0	R/W	RLAISINSEN	0

The Path Receive AIS-P Enable Register is provided at SARC r/w address 0AH.

RLAISINSEN

The RLAISINS enable bit allows the line AIS insertion indication to be ORed into the receive AIS-P generation. When the RLAISINSEN bit is set high, the corresponding insertion indication is ORed with other defect indications to enable receive AIS-P generation. When the RLAISINSEN bit is set low, the corresponding insertion indication does not enable receive AIS-P generation.

MSRLAISINSEN

The master RLAISINS enable bit allows the master line AIS insertion indication to be ORed into the receive AIS-P generation. When the RLAISINSEN bit is set high, the corresponding insertion indication is ORed with other defect indications to enable receive AIS-P generation. When the MSRLAISINSEN bit is set low, the corresponding insertion indication does not enable receive AIS-P generation.

PLOPTREN

The PLOPTR enable bit allows the path loss of pointer defect to be ORed into the receive AIS-P generation. When the PLOPTREN bit is set high, the corresponding defect indication is ORed with other defect indications to enable receive AIS-P generation. When the PLOPTREN bit is set low, the corresponding defect indication does not enable receive AIS-P generation.

PAISPTREN

The PAISPTR enable bit allows the path AIS pointer defect to be ORed into the receive AIS-P generation. When the PAISPTREN bit is set high, the corresponding defect indication is ORed with other defect indications to enable receive AIS-P generation. When the PAISPTREN bit is set low, the corresponding defect indication does not enable receive AIS-P generation.

PPLUEN

The PPLU enable bit allows the path payload label unstable defect to be ORed into the receive AIS-P generation. When the PPLUEN bit is set high, the corresponding defect indication is ORed with other defect indications to enable receive AIS-P generation. When the PPLUEN bit is set low, the corresponding defect indication does not enable receive AIS-P generation.

PPLMEN

The PPLM enable bit allows the path payload label mismatch defect to be ORed into the receive AIS-P generation. When the PPLMEN bit is set high, the corresponding defect indication is ORed with other defect indications to enable receive AIS-P generation. When the PPLMEN bit is set low, the corresponding defect indication does not enable receive AIS-P generation.

PUNEQEN

The PUNEQ enable bit allows the path unequipped defect to be ORed into the receive AIS-P generation. When the PUNEQEN bit is set high, the corresponding defect indication is ORed with other defect indications to enable receive AIS-P generation. When the PUNEQEN bit is set low, the corresponding defect indication does not enable receive AIS-P generation.

PPDIEN

The PPDI enable bit allows the path payload defect indication defect to be ORed into the receive AIS-P generation. When the PPDIEN bit is set high, the corresponding defect indication is ORed with other defect indications to enable receive AIS-P generation. When the PPDIEN bit is set low, the corresponding defect indication does not enable receive AIS-P generation.

PTIUEN

The PTIU enable bit allows the path trace identifier unstable defect to be ORed into the receive AIS-P generation. When the PTIUEN bit is set high, the corresponding defect indication is ORed with other defect indications to enable receive AIS-P generation. When the PTIUEN bit is set low, the corresponding defect indication does not enable receive AIS-P generation.

PTIMEN

The PTIM enable bit allows the path trace identifier mismatch defect to be ORed into the receive AIS-P generation. When the PTIMEN bit is set high, the corresponding defect indication is ORed with other defect indications to enable receive AIS-P generation. When the PTIMEN bit is set low, the corresponding defect indication does not enable receive AIS-P generation.

Register 026BH, 066BH, 0A6BH and 0E6BH: SARC TU3 Path Configuration

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9		Unused	
Bit 8		Unused	
Bit 7	R/W	PRDIEN	0
Bit 6	R/W	PERDI20	0
Bit 5	R/W	TPRCPEN	0
Bit 4	R/W	PLOPTREND	0
Bit 3		Unused	
Bit 2		Unused	
Bit 1		Unused	
Bit 0	R/W	PLOPTRCFG	0

The TU3 Path Configuration Register is provided at SARC r/w address 0BH.

PLOPTRCFG

The path loss of pointer configuration (PLOPTRCFG) bit defines the LOP-P defect. When PLOPTRCFG is set to zero, an LOP-P defect is declared when the pointer is in the LOP state and an LOP-P defect is removed when the pointer is not in the LOP state. When PLOPTRCFG is set to one, an LOP-P defect is declared when the pointer is in the LOP state or in the AIS state and an LOP-P defect is removed when the pointer is not in the LOP state or in the AIS state.

PLOPTREND

The path loss of pointer removal (PLOPTREND) bit controls the removal of a LOP-P defect when an AIS-P defect is declared. When PLOPTREND is set to logic 1, a LOP-P defect is terminated when an AIS-P defect is declared. When PLOPTREND is set to logic 0, a LOP-P defect is not terminated when an AIS-P defect is declared.

TPRCPEN

The transmit path ring control port enable (TPRCPEN) bit enables the TRCP port. When TPRPEN is set to logic 1, ERDI-P and REI-P insertion indication are extracted from the TRCP port. When TRCPEN is set to logic 0, ERDI-P and REI-P insertion indication are derived from the defect detected on the receive data stream.

PERDI20

The path enhance remote defect indication (PERDI20) bit selects the path ERDI persistence. When PERDI20 is set to logic 1, a new path ERDI indication is transmitted for at least 20 frames. When PERDI20 is set to logic 0, a new path ERDI indication is transmitted for at least 10 frames.

PRDIEN

The path remote defect indication enable (PRDIEN) bit selects between the 1 bit RDI code and the 3 bits ERDI code. When PRDIEN is set to logic 1, the 1 bit RDI code is transmitted. When PRDIEN is set to logic 0, the 3 bit ERDI code is transmitted.

Register 026CH, 066CH, 0A6CH and 0E6CH: SARC TU3 Path Receive RALM Enable

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13	R/W	Reserved	0
Bit 12	R/W	Reserved	0
Bit 11	R/W	PTIMEN	0
Bit 10	R/W	PTIUEN	0
Bit 9	R/W	PERDIEN	0
Bit 8	R/W	PRDIEN	0
Bit 7	R/W	PPDIEN	0
Bit 6	R/W	PUNEQEN	0
Bit 5	R/W	PPLMEN	0
Bit 4	R/W	PPLUEN	0
Bit 3	R/W	PAISPTREN	0
Bit 2	R/W	PLOPTREN	0
Bit 1	R/W	MSSALMEN	0
Bit 0	R/W	SALMEN	0

The TU3 Path Receive RALM Enable Register is provided at SARC r/w address 0CH.

SALMEN

The SALM enable bit allows the receive section alarm to be ORed into the RALM output. When the SALMEN bit is set high, the corresponding alarm indication is ORed with other defect indications to trigger the RALM output. When the SALMEN bit is set low, the corresponding alarm indication does not affect the RALM output.

MSSALMEN

The master SALM enable bit allows the master receive section alarm to be ORed into the RALM output. When the MSSALMEN bit is set high, the corresponding alarm indication is ORed with other defect indications to trigger the RALM output. When the MSSALMEN bit is set low, the corresponding alarm indication does not affect the RALM output.

PLOPTREN

The PLOPTR enable bit allows the path loss of pointer defect to be ORed into the RALM output. When the PLOPTREN bit is set high, the corresponding defect indication is ORed with other defect indications to trigger the RALM output. When the PLOPTREN bit is set low, the corresponding defect indication does not affect the RALM output.

PAISPTREN

The PAISPTR enable bit allows the path AIS pointer defect to be ORed into the RALM output. When the PAISPTREN bit is set high, the corresponding defect indication is ORed with other defect indications to trigger the RALM output. When the PAISPTREN bit is set low, the corresponding defect indication does not affect the RALM output.

PPLUEN

The PPLU enable bit allows the path payload label unstable defect to be ORed into the RALM output. When the PPLUEN bit is set high, the corresponding defect indication is ORed with other defect indications to trigger the RALM output. When the PPLUEN bit is set low, the corresponding defect indication does not affect the RALM output.

PPLMEN

The PPLM enable bit allows the path payload label mismatch defect to be ORed into the RALM output. When the PPLMEN bit is set high, the corresponding defect indication is ORed with other defect indications to trigger the RALM output. When the PPLMEN bit is set low, the corresponding defect indication does not affect the RALM output.

PUNEQEN

The PUNEQ enable bit allows the path unequipped defect to be ORed into the RALM output. When the PUNEQEN bit is set high, the corresponding defect indication is ORed with other defect indications to trigger the RALM output. When the PUNEQEN bit is set low, the corresponding defect indication does not affect the RALM output.

PPDIEN

The PPDI enable bit allows the path payload defect indication defect to be ORed into the RALM output. When the PPDIEN bit is set high, the corresponding defect indication is ORed with other defect indications to trigger the RALM output. When the PPDIEN bit is set low, the corresponding defect indication does not affect the RALM output.

PRDIEN

The PRDI enable bit allows the path remote defect indication defect to be ORed into the RALM output. When the PRDIEN bit is set high, the corresponding defect indication is ORed with other defect indications to trigger the RALM output. When the PRDIEN bit is set low, the corresponding defect indication does not affect the RALM output.

PERDIEN

The PERDI enable bit allows the path enhanced remote defect indication defect to be ORed into the RALM output. When the PERDIEN bit is set high, the corresponding defect indication is ORed with other defect indications to trigger the RALM output. When the PERDIEN bit is set low, the corresponding defect indication does not affect the RALM output.

PTIUEN

The PTIU enable bit allows the path trace identifier unstable defect to be ORed into the RALM output. When the PTIUEN bit is set high, the corresponding defect indication is ORed with other defect indications to trigger the RALM output. When the PTIUEN bit is set low, the corresponding defect indication does not affect the RALM output.

PTIMEN

The PTIM enable bit allows the path trace identifier mismatch defect to be ORed into the RALM output. When the PTIMEN bit is set high, the corresponding defect indication is ORed with other defect indications to trigger the RALM output. When the PTIMEN bit is set low, the corresponding defect indication does not affect the RALM output.

Register 026DH, 066DH, 0A6DH and 0E6DH: SARC TU3 Path Receive AIS-P Enable

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13	R/W	Reserved	0
Bit 12	R/W	Reserved	0
Bit 11	R/W	PTIMEN	0
Bit 10	R/W	PTIUEN	0
Bit 9	R/W	Reserved	0
Bit 8	R/W	Reserved	0
Bit 7	R/W	PPDIEN	0
Bit 6	R/W	PUNEQEN	0
Bit 5	R/W	PPLMEN	0
Bit 4	R/W	PPLUEN	0
Bit 3	R/W	PAISPTREN	0
Bit 2	R/W	PLOPTREN	0
Bit 1	R/W	MSRLAISINSEN	0
Bit 0	R/W	RLAISINSEN	0

The TU3 Path Receive AIS-P Enable Register is provided at SARC r/w address 0DH.

RLAISINSEN

The RLAISINS enable bit allows the line AIS insertion indication to be ORed into the receive AIS-P generation. When the RLAISINSEN bit is set high, the corresponding insertion indication is ORed with other defect indications to enable receive AIS-P generation. When the RLAISINSEN bit is set low, the corresponding insertion indication does not enable receive AIS-P generation.

MSRLAISINSEN

The master RLAISINS enable bit allows the master line AIS insertion indication to be ORed into the receive AIS-P generation. When the RLAISINSEN bit is set high, the corresponding insertion indication is ORed with other defect indications to enable receive AIS-P generation. When the MSRLAISINSEN bit is set low, the corresponding insertion indication does not enable receive AIS-P generation.

PLOPTREN

The PLOPTR enable bit allows the path loss of pointer defect to be ORed into the receive AIS-P generation. When the PLOPTREN bit is set high, the corresponding defect indication is ORed with other defect indications to enable receive AIS-P generation. When the PLOPTREN bit is set low, the corresponding defect indication does not enable receive AIS-P generation.

PAISPTREN

The PAISPTR enable bit allows the path AIS pointer defect to be ORed into the receive AIS-P generation. When the PAISPTREN bit is set high, the corresponding defect indication is ORed with other defect indications to enable receive AIS-P generation. When the PAISPTREN bit is set low, the corresponding defect indication does not enable receive AIS-P generation.

PPLUEN

The PPLU enable bit allows the path payload label unstable defect to be ORed into the receive AIS-P generation. When the PPLUEN bit is set high, the corresponding defect indication is ORed with other defect indications to enable receive AIS-P generation. When the PPLUEN bit is set low, the corresponding defect indication does not enable receive AIS-P generation.

PPLMEN

The PPLM enable bit allows the path payload label mismatch defect to be ORed into the receive AIS-P generation. When the PPLMEN bit is set high, the corresponding defect indication is ORed with other defect indications to enable receive AIS-P generation. When the PPLMEN bit is set low, the corresponding defect indication does not enable receive AIS-P generation.

PUNEQEN

The PUNEQ enable bit allows the path unequipped defect to be ORed into the receive AIS-P generation. When the PUNEQEN bit is set high, the corresponding defect indication is ORed with other defect indications to enable receive AIS-P generation. When the PUNEQEN bit is set low, the corresponding defect indication does not enable receive AIS-P generation.

PPDIEN

The PPDI enable bit allows the path payload defect indication defect to be ORed into the receive AIS-P generation. When the PPDIEN bit is set high, the corresponding defect indication is ORed with other defect indications to enable receive AIS-P generation. When the PPDIEN bit is set low, the corresponding defect indication does not enable receive AIS-P generation.

PTIUEN

The PTIU enable bit allows the path trace identifier unstable defect to be ORed into the receive AIS-P generation. When the PTIUEN bit is set high, the corresponding defect indication is ORed with other defect indications to enable receive AIS-P generation. When the PTIUEN bit is set low, the corresponding defect indication does not enable receive AIS-P generation.

PTIMEN

The PTIM enable bit allows the path trace identifier mismatch defect to be ORed into the receive AIS-P generation. When the PTIMEN bit is set high, the corresponding defect indication is ORed with other defect indications to enable receive AIS-P generation. When the PTIMEN bit is set low, the corresponding defect indication does not enable receive AIS-P generation.

Register 0270H, 0670H, 0A70H and 0E70H: SARC LOP Pointer Status

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11	R	PLOPTRV[12]	X
Bit 10	R	PLOPTRV[11]	X
Bit 9	R	PLOPTRV[10]	X
Bit 8	R	PLOPTRV[9]	X
Bit 7	R	PLOPTRV[8]	X
Bit 6	R	PLOPTRV[7]	X
Bit 5	R	PLOPTRV[6]	X
Bit 4	R	PLOPTRV[5]	X
Bit 3	R	PLOPTRV[4]	X
Bit 2	R	PLOPTRV[3]	X
Bit 1	R	PLOPTRV[2]	X
Bit 0	R	PLOPTRV[1]	X

The LOP Pointer Status Register is provided at SARC r/w address 10H.

PLOPTRV[12:1]

The path loss of pointer status (PLOPTRV[12:1]) bits indicate the current status of the LOP-P defect for STS-1/STM-0 paths #1 to #12. When PLOPTRCFG register bits are set to 00b, PLOPTRV is asserted when the pointer is in the LOP state and PLOPTRV is negated when the pointer is not in the LOP state. When PLOPTRCFG register bits are set to 01b, PLOPTRV is asserted when the pointer or any of the concatenated pointers is in the LOP state and PLOPTRV is negated when the pointer and all the concatenation pointers are not in the LOP state. When PLOPTRCFG register bits are set to 10b, PLOPTRV is asserted when the pointer or any of the concatenated pointers is in the LOP state or in the AIS state and PLOPTRV is negated when the pointer and all the concatenation pointers are not in the LOP state or in the AIS state. When the PLOPTREND register bit is set to one, PLOPPTRV is negated when a AIS-P defect is detected.

Register 0271H, 0671H, 0A71H and 0E71H: SARC LOP Pointer Interrupt Enable

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11	R/W	PLOPTRE[12]	0
Bit 10	R/W	PLOPTRE[11]	0
Bit 9	R/W	PLOPTRE[10]	0
Bit 8	R/W	PLOPTRE[9]	0
Bit 7	R/W	PLOPTRE[8]	0
Bit 6	R/W	PLOPTRE[7]	0
Bit 5	R/W	PLOPTRE[6]	0
Bit 4	R/W	PLOPTRE[5]	0
Bit 3	R/W	PLOPTRE[4]	0
Bit 2	R/W	PLOPTRE[3]	0
Bit 1	R/W	PLOPTRE[2]	0
Bit 0	R/W	PLOPTRE[1]	0

The LOP Pointer Interrupt Enable Register is provided at SARC r/w address 11H.

PLOPTRE[12:1]

The path loss of pointer interrupt enable (PLOPTRE[12:1]) bits control the activation of the interrupt output for STS-1/STM-0 paths #1 to #12. When any of these bit locations is set to logic 1, the corresponding pending interrupt will assert the interrupt output. When any of these bit locations is set to logic 0, the corresponding pending interrupt will not assert the interrupt output.

Register 0272H, 0672H, 0A72H and 0E72H: SARC LOP Pointer Interrupt Status

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11	R	PLOPTRI[12]	X
Bit 10	R	PLOPTRI[11]	X
Bit 9	R	PLOPTRI[10]	X
Bit 8	R	PLOPTRI[9]	X
Bit 7	R	PLOPTRI[8]	X
Bit 6	R	PLOPTRI[7]	X
Bit 5	R	PLOPTRI[6]	X
Bit 4	R	PLOPTRI[5]	X
Bit 3	R	PLOPTRI[4]	X
Bit 2	R	PLOPTRI[3]	X
Bit 1	R	PLOPTRI[2]	X
Bit 0	R	PLOPTRI[1]	X

The LOP Pointer Interrupt Status Register is provided at SARC r/w address 12H.

PLOPTRI[12:1]

The path loss of pointer interrupt status (PLOPTRI[12:1]) bits are event indicators for STS-1/STM-0 paths #1 to #12. PLOPTRI[12:1] are set to logic 1 to indicate any changes in the status of PLOPTRV[12:1]. These interrupt status bits are independent of the interrupt enable bits. PLOPTRI[12:1] are cleared to logic 0 when this register is read.

Register 0273H, 0673H, 0A73H and 0E73H: SARC AIS Pointer Status

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11	R	PAISPTRV[12]	X
Bit 10	R	PAISPTRV[11]	X
Bit 9	R	PAISPTRV[10]	X
Bit 8	R	PAISPTRV[9]	X
Bit 7	R	PAISPTRV[8]	X
Bit 6	R	PAISPTRV[7]	X
Bit 5	R	PAISPTRV[6]	X
Bit 4	R	PAISPTRV[5]	X
Bit 3	R	PAISPTRV[4]	X
Bit 2	R	PAISPTRV[3]	X
Bit 1	R	PAISPTRV[2]	X
Bit 0	R	PAISPTRV[1]	X

The AIS Pointer Status Register is provided at SARC r/w address 13H.

PAISPTRV[12:1]

The path AIS pointer status (PAISPTRV[12:1]) bits indicate the current status of the AIS-P defect for STS-1/STM-0 paths #1 to #12. When PAISPTRCFG register bits are set to 00b, PAISPTRV is asserted when the pointer is in the AIS state and PAISPTRV is negated when the pointer is not in the AIS state. When PAISPTRCFG register bits are set to 01b, PAISPTRV is asserted when the pointer or any of the concatenated pointers is in the AIS state and PAISPTRV is negated when the pointer and all the concatenation pointers are not in the AIS state. When PAISPTRCFG register bits are set to 10b, PAISPTRV is asserted when the pointer and all the concatenated pointers are in the AIS state and PAISPTRV is negated when the pointer or any of the concatenation pointers are not in the AIS state.

Register 0274H, 0674H, 0A74H and 0E74H: SARC AIS Pointer Interrupt Enable

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11	R/W	PAISPTRE[12]	0
Bit 10	R/W	PAISPTRE[11]	0
Bit 9	R/W	PAISPTRE[10]	0
Bit 8	R/W	PAISPTRE[9]	0
Bit 7	R/W	PAISPTRE[8]	0
Bit 6	R/W	PAISPTRE[7]	0
Bit 5	R/W	PAISPTRE[6]	0
Bit 4	R/W	PAISPTRE[5]	0
Bit 3	R/W	PAISPTRE[4]	0
Bit 2	R/W	PAISPTRE[3]	0
Bit 1	R/W	PAISPTRE[2]	0
Bit 0	R/W	PAISPTRE[1]	0

The AIS Pointer Interrupt Enable Register is provided at SARC r/w address 14H.

PAISPTRE[12:1]

The path AIS signal pointer interrupt enable (PAISPTRE[12:1]) bits control the activation of the interrupt output for STS-1/STM-0 paths #1 to #12. When any of these bit locations is set to logic 1, the corresponding pending interrupt will assert the interrupt output. When any of these bit locations is set to logic 0, the corresponding pending interrupt will not assert the interrupt output.

Register 0275H, 0675H, 0A75H and 0E75H: SARC AIS Pointer Interrupt Status

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11	R	PAISPTRI[12]	X
Bit 10	R	PAISPTRI[11]	X
Bit 9	R	PAISPTRI[10]	X
Bit 8	R	PAISPTRI[9]	X
Bit 7	R	PAISPTRI[8]	X
Bit 6	R	PAISPTRI[7]	X
Bit 5	R	PAISPTRI[6]	X
Bit 4	R	PAISPTRI[5]	X
Bit 3	R	PAISPTRI[4]	X
Bit 2	R	PAISPTRI[3]	X
Bit 1	R	PAISPTRI[2]	X
Bit 0	R	PAISPTRI[1]	X

The AIS Pointer Interrupt Status Register is provided at SARC r/w address 15H.

PAISPTRI[12:1]

The path AIS pointer interrupt status (PAISPTRI[12:1]) bits are event indicators for STS-1/STM-0 paths #1 to #12. PAISPTRI[12:1] are set to logic 1 to indicate any changes in the status of PAISPTRV[12:1]. These interrupt status bits are independent of the interrupt enable bits. PAISPTRI[12:1] are cleared to logic 0 when this register is read.

Register 0278H, 068DH, 0A78H and 0E78H: SARC TU3 LOP Pointer Status

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11	R	PLOPTRV[12]	X
Bit 10	R	PLOPTRV[11]	X
Bit 9	R	PLOPTRV[10]	X
Bit 8	R	PLOPTRV[9]	X
Bit 7	R	PLOPTRV[8]	X
Bit 6	R	PLOPTRV[7]	X
Bit 5	R	PLOPTRV[6]	X
Bit 4	R	PLOPTRV[5]	X
Bit 3	R	PLOPTRV[4]	X
Bit 2	R	PLOPTRV[3]	X
Bit 1	R	PLOPTRV[2]	X
Bit 0	R	PLOPTRV[1]	X

The TU3 LOP Pointer Status Register is provided at SARC r/w address 18H.

PLOPTRV[12:1]

The TU3 path loss of pointer status (PLOPTRV[12:1]) bits indicate the current status of the LOP-P defect for STS-1/STM-0 paths #1 to #12. When PLOPTRCFG register bit is set to zero, PLOPTRV is asserted when the TU3 pointer is in the LOP state and PLOPTRV is negated when the TU3 pointer is not in the LOP state. When PLOPTRCFG register bit is set to one, PLOPTRV is asserted when the TU3 pointer is in the LOP state or AIS state and PLOPTRV is negated when the TU3 pointer is not in the LOP state or AIS state. When the PLOPTREND register bit is set to one, PLOPPTRV is negated when a AIS-P defect is detected.

Register 0279H, 0679H, 0A79H and 0E79H: SARC TU3 LOP Pointer Interrupt Enable

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11	R/W	PLOPTRE[12]	0
Bit 10	R/W	PLOPTRE[11]	0
Bit 9	R/W	PLOPTRE[10]	0
Bit 8	R/W	PLOPTRE[9]	0
Bit 7	R/W	PLOPTRE[8]	0
Bit 6	R/W	PLOPTRE[7]	0
Bit 5	R/W	PLOPTRE[6]	0
Bit 4	R/W	PLOPTRE[5]	0
Bit 3	R/W	PLOPTRE[4]	0
Bit 2	R/W	PLOPTRE[3]	0
Bit 1	R/W	PLOPTRE[2]	0
Bit 0	R/W	PLOPTRE[1]	0

The TU3 LOP Pointer Interrupt Enable Register is provided at SARC r/w address 19H.

PLOPTRE[12:1]

The TU3 path loss of pointer interrupt enable (PLOPTRE[12:1]) bits control the activation of the interrupt output for STS-1/STM-0 paths #1 to #12. When any of these bit locations is set to logic 1, the corresponding pending interrupt will assert the interrupt output. When any of these bit locations is set to logic 0, the corresponding pending interrupt will not assert the interrupt output.

Register 027AH, 067AH, 0A7AH and 0E7AH: SARC TU3 LOP Pointer Interrupt Status

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11	R	PLOPTRI[12]	X
Bit 10	R	PLOPTRI[11]	X
Bit 9	R	PLOPTRI[10]	X
Bit 8	R	PLOPTRI[9]	X
Bit 7	R	PLOPTRI[8]	X
Bit 6	R	PLOPTRI[7]	X
Bit 5	R	PLOPTRI[6]	X
Bit 4	R	PLOPTRI[5]	X
Bit 3	R	PLOPTRI[4]	X
Bit 2	R	PLOPTRI[3]	X
Bit 1	R	PLOPTRI[2]	X
Bit 0	R	PLOPTRI[1]	X

The TU3 LOP Pointer Interrupt Status Register is provided at SARC r/w address 1AH.

PLOPTRI[12:1]

The TU3 path loss of pointer interrupt status (PLOPTRI[12:1]) bits are event indicators for STS-1/STM-0 paths #1 to #12. PLOPTRI[12:1] are set to logic 1 to indicate any changes in the status of PLOPTRV[12:1]. These interrupt status bits are independent of the interrupt enable bits. PLOPTRI[12:1] are cleared to logic 0 when this register is read.

Register 027BH, 067BH, 0A7BH and 0E7BH: SARC TU3 AIS Pointer Status

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11	R	PAISPTRV[12]	X
Bit 10	R	PAISPTRV[11]	X
Bit 9	R	PAISPTRV[10]	X
Bit 8	R	PAISPTRV[9]	X
Bit 7	R	PAISPTRV[8]	X
Bit 6	R	PAISPTRV[7]	X
Bit 5	R	PAISPTRV[6]	X
Bit 4	R	PAISPTRV[5]	X
Bit 3	R	PAISPTRV[4]	X
Bit 2	R	PAISPTRV[3]	X
Bit 1	R	PAISPTRV[2]	X
Bit 0	R	PAISPTRV[1]	X

The TU3 AIS Pointer Status Register is provided at SARC r/w address 1BH.

PAISPTRV[12:1]

The TU3 path AIS pointer status (PAISPTRV[12:1]) bits indicate the current status of the AIS-P defect for STS-1/STM-0 paths #1 to #12. PAISPTRV is asserted when the pointer is in the AIS state and PAISPTRV is negated when the pointer is not in the AIS state.

Register 027CH, 067CH, 0A7CH and 0E7CH: SARC TU3 AIS Pointer Interrupt Enable

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11	R/W	PAISPTRE[12]	0
Bit 10	R/W	PAISPTRE[11]	0
Bit 9	R/W	PAISPTRE[10]	0
Bit 8	R/W	PAISPTRE[9]	0
Bit 7	R/W	PAISPTRE[8]	0
Bit 6	R/W	PAISPTRE[7]	0
Bit 5	R/W	PAISPTRE[6]	0
Bit 4	R/W	PAISPTRE[5]	0
Bit 3	R/W	PAISPTRE[4]	0
Bit 2	R/W	PAISPTRE[3]	0
Bit 1	R/W	PAISPTRE[2]	0
Bit 0	R/W	PAISPTRE[1]	0

The TU3 AIS Pointer Interrupt Enable Register is provided at SARC r/w address 1CH.

PAISPTRE[12:1]

The TU3 path AIS pointer interrupt enable (PAISPTRE[12:1]) bits control the activation of the interrupt output for STS-1/STM-0 paths #1 to #12. When any of these bit locations is set to logic 1, the corresponding pending interrupt will assert the interrupt output. When any of these bit locations is set to logic 0, the corresponding pending interrupt will not assert the interrupt output.

Register 027DH, 067DH, 0A7DH and 0E7DH: SARC TU3 AIS Pointer Interrupt Status

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11	R	PAISPTRI[12]	X
Bit 10	R	PAISPTRI[11]	X
Bit 9	R	PAISPTRI[10]	X
Bit 8	R	PAISPTRI[9]	X
Bit 7	R	PAISPTRI[8]	X
Bit 6	R	PAISPTRI[7]	X
Bit 5	R	PAISPTRI[6]	X
Bit 4	R	PAISPTRI[5]	X
Bit 3	R	PAISPTRI[4]	X
Bit 2	R	PAISPTRI[3]	X
Bit 1	R	PAISPTRI[2]	X
Bit 0	R	PAISPTRI[1]	X

The TU3 AIS Pointer Interrupt Status Register is provided at SARC r/w address 1DH.

PAISPTRI[12:1]

The TU3 path AIS pointer interrupt status (PAISPTRI[12:1]) bits are event indicators for STS-1/STM-0 paths #1 to #12. PAISPTRI[12:1] are set to logic 1 to indicate any changes in the status of PAISPTRV[12:1]. These interrupt status bits are independent of the interrupt enable bits. PAISPTRI[12:1] are cleared to logic 0 when this register is read.

Register 0302H: DDLL Reset

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9		Unused	
Bit 8		Unused	
Bit 7		Unused	
Bit 6		Unused	
Bit 5		Unused	
Bit 4		Unused	
Bit 3		Unused	
Bit 2		Unused	
Bit 1		Unused	
Bit 0		Unused	

Any write to the DDLL Reset Register will reset the Drop Bus DLL

Register 1040H: STLI Clock Configuration

Bit	Type	Function	Default
Bit 15	R/W	ROTATEEN	1
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9		Unused	
Bit 8		Unused	
Bit 7		Unused	
Bit 6		Unused	
Bit 5		Unused	
Bit 4	R/W	TCLK4EN	0
Bit 3	R/W	TCLK3EN	0
Bit 2	R/W	TCLK2EN	0
Bit 1	R/W	TCLK1EN	0
Bit 0	R/W	TDCLKOEN	0

The Clock Configuration Register is provided at STLI r/w address 00H.

TDCLKOEN

The transmit clock enable (TDCLKOEN) bit controls the gating of the TDCLKO output clock. When TDCLKOEN is set to logic 1, the TDCLKO output clock operates normally. When TDCLKOEN is set to logic 0, the TDCLKO output clock is held low.

TCLK1EN

The transmit clock enable (TCLK1EN) bit controls the gating of the TCLK1 output clock. When TCLK1EN is set to logic 1, the TCLK1 output clock operates normally. When TCLK1EN is set to logic 0, the TCLK1 output clock is held low.

TCLK2EN

The transmit clock enable (TCLK2EN) bit controls the gating of the TCLK2 output clock. When TCLK2EN is set to logic 1, the TCLK2 output clock operates normally. When TCLK2EN is set to logic 0, the TCLK2 output clock is held low.

TCLK3EN

The transmit clock enable (TCLK3EN) bit controls the gating of the TCLK3 output clock. When TCLK3EN is set to logic 1, the TCLK3 output clock operates normally. When TCLK3EN is set to logic 0, the TCLK3 output clock is held low.

TCLK4EN

The transmit clock enable (TCLK4EN) bit controls the gating of the TCLK4 output clock. When TCLK4EN is set to logic 1, the TCLK4 output clock operates normally. When TCLK4EN is set to logic 0, the TCLK4 output clock is held low.

ROTATEEN

The rotate enable (ROTATEEN) bit controls the line rotation matrix when the SPECTRA-2488 is configured for OC-48 mode. When ROTATEEN is set to logic 1, the rotation matrix is active and the bytes on the TD[15:0] output bus are interleaved by the SPECTRA-2488. When ROTATEEN is set to logic 0, the rotation matrix is inactive and the interleaving is expected to be performed by the SERDES device. Most SERDES devices do not perform byte interleaving so ROTATEEN default to logic 1.Check with SERDES device to determine correct setting of this bit. This bit is not valid in quad OC-12 mode.

Register 1041H: STLI PGM Clock Configuration

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9		Unused	
Bit 8		Unused	
Bit 7		Unused	
Bit 6		Unused	
Bit 5		Unused	
Bit 4		Unused	
Bit 3	R/W	PGMTCLKSRC[1]	0
Bit 2	R/W	PGMTCLKSRC[0]	0
Bit 1	R/W	PGMTCLKSEL	0
Bit 0	R/W	PGMTCLKEN	0

The PGM Clock Configuration Register is provided at STLI r/w address 01H.

PGMTCLKEN

The programmable transmit clock enable (PGMTCLKEN) bit controls the gating of the PGMTCLK output clock. When PGMTCLKEN is set to logic one, the PGMTCLK output clock operates normally. When PGMTCLKEN is set to logic zero, the PGMTCLK output clock is held low.

PGMTCLKSEL

The programmable transmit clock frequency selection (PGMTCLKSEL) bit selects the frequency of the PGMTCLK output clock. When PGMTCLKSEL is set high, PGMTCLK is a nominal 8 KHz clock. When PGMTCLKSEL is set to logic zero, PGMTCLK is a nominal 19.44 MHz clock.

PGMTCLKSRC[1:0]

The programmable transmit clock source (PGMTCLKSRC[1:0]) bits select the source of the PGMTCLK output clock when the STLI is in quad STS-12 (STM-4) mode. When the STLI is in STS-48 (STM-16) mode, TDCLK is the source of the PGMTCLK output clock.

PGMTCLKSRC[1:0]	Source
00	TDCLK1
01	TDCLK2
10	TDCLK3
11	TDCLK4

Register 1080H, 1480H, 1880H and 1C80H: TRMP Configuration

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11	R/W	LREIBLK	0
Bit 10	R/W	LREIEN	1
Bit 9	R/W	APSEN	1
Bit 8	R/W	TLDTS	1
Bit 7	R/W	TLDEN	0
Bit 6	R/W	TSLDSEL	0
Bit 5	R/W	TSLDTS	1
Bit 4	R/W	TSLDEN	0
Bit 3	R/W	TRACEEN	0
Bit 2	R/W	J0Z0INCEN	0
Bit 1	R/W	Z0DEF	0
Bit 0	R/W	A1A2EN	1

The Configuration Register is provided at TRMP r/w address 00H.

A1A2EN

The A1A2 framing enable (A1A2EN) bit controls the insertion of the framing bytes in the data stream. When A1A2EN is set to logic 1, F6h and 28h are inserted in the A1 and A2 bytes according to the priority of Table 6. When A1A2EN is set to logic 0, the framing bytes are not inserted.

Z0DEF

The Z0 definition (Z0DEF) bit defines the Z0 growth bytes. When Z0DEF is set to logic 1, the Z0 bytes are defined according to ITU. The Z0 bytes are located in STS-1/STM-0 #2 to #4 in STS-12/STM-4 master mode and are located in STS-1/STM-0 #1 to #4 in STS-12/STM-4 slave mode. When Z0DEF is set to logic 0, The Z0 bytes are defined according to BELLCORE. The Z0 bytes are located in STS-1/STM-0 #2 to #12 in STS-12/STM-4 master mode and are located in STS-1/STM-0 #1 to #12 in STS-12/STM-4 slave mode.
Note: When Z0DEF is set to logic 1, the national bytes in STS-1/STM-0 #5 to #12 must be configured properly to avoid all zero or all one un scrambled sequence.

J0Z0INCEN

The J0 and Z0 increment enable (J0Z0INCEN) bit controls the insertion of an incremental pattern in the section trace and Z0 growth bytes. When J0Z0INCEN is set to logic 1, the corresponding STS-1/STM-0 path # is inserted in the J0 and Z0 bytes according to the priority of Table 6. When J0Z0INCEN is set to logic 0, no incremental pattern is inserted.

TRACEEN

The section trace enable (TRACEEN) bit controls the insertion of section trace in the data stream. When TRACEEN is set to logic 1, the section trace from the TTTP is inserted in the J0 byte of STS-1/STM-0 #1 according to the priority of Table 6. When TRACEEN is set to logic 0, the section trace from the TTTP is not inserted.

TSLDEN

The TSLD enable (TSLDEN) bit controls the insertion of section or line DCC in the data stream. When TSLDEN is set to logic 1, the section or line DCC from the serial TSLD port is inserted in the D1-D3 bytes or D4-D12 bytes of STS-1/STM-0 #1 according to the priority of Table 6. When TSLDEN is set to logic 0, the section or line DCC from the serial TSLD port is not inserted.

TSLDTS

The TSLD tri-state control (TSLDTS) bit controls the TSLDCLK output port. When TSLDTS is set to logic 1, the TSLDCLK output port is tri-state. When TSLDTS is set to logic 0, the TSLDCLK output port is enable.

TSLDSEL

The TSLD channel select (TSLDSEL) bit selects the contents of the TSLD port and the frequency of the TSLDCLK clock.

TSLDSEL	Contents	TSLDCLK
0	Section DCC (D1-D3)	Nominal 192 kHz
1	Line DCC (D4-D12)	Nominal 576 kHz

TLDEN

The TLD enable (TLDEN) bit controls the insertion of line DCC in the data stream. When TLDEN is set to logic 1, the line DCC from the serial TLD port is inserted in the D4-D12 bytes of STS-1/STM-0 #1 according to the priority of Table 6. When TLDEN is set to logic 0, the line DCC from the serial TLD port is not inserted.

TLDTS

The TLDTS tri-state control (TLDTS) bit controls the TLDCLK output port. When TLDTS is set to logic 1, the TLDCLK output port is tri-state. When TLDTS is set to logic 0, the TLDCLK output port is enable.

APSEN

The APS enable (APSEN) bit controls the insertion of automatic protection switching in the data stream. When APSEN is set to logic 1, the APS bytes from the RRMP are inserted in the K1/K2 bytes of STS-1/STM-0 #1 according to the priority of Table 6. When APSEN is set to logic 0, the APS bytes from the RRMP are not inserted.

LREIEN

The line REI enable (LREIEN) bit controls the insertion of line remote error indication in the data stream. When LREIEN is set to logic 1, the line REI from the RRMP are inserted in the M1 byte of STS-1/STM-0 #3 according to the priority of Table 6. When LREIEN is set to logic 0, the line REI from the RRMP are not inserted.

LREIBLK

The line REI block (LREIBLK) bit controls the generation of line remote error indication. When LREIBLK is set to logic 1, the line REI inserted in the M1 byte represents BIP-24 block errors (a maximum of 1 error per STS-3/STM-1 per frame). When LREIBLK is set to logic 0, the line REI inserted in the M1 byte represents BIP-8 errors (a maximum of 8 error per STS-1/STM-0 per frame).

Register 1081H, 1481H, 1881H and 1C81H: TRMP Register Insertion

Bit	Type	Function	Default
Bit 15	R/W	UNUSEDV	0
Bit 14	R/W	UNUSEDEN	0
Bit 13	R/W	NATIONALV	0
Bit 12	R/W	NATIONALEN	0
Bit 11		Unused	
Bit 10	R/W	E2REGEN	0
Bit 9	R/W	Z2REGEN	0
Bit 8	R/W	Z1REGEN	0
Bit 7	R/W	S1REGEN	0
Bit 6	R/W	D4D12REGEN	0
Bit 5	R/W	K1K2REGEN	0
Bit 4	R/W	D1D3REGEN	0
Bit 3	R/W	F1REGEN	0
Bit 2	R/W	E1REGEN	0
Bit 1	R/W	Z0REGEN	1
Bit 0	R/W	J0REGEN	1

The Register Insertion Register is provided at TRMP r/w address 01H.

J0REGEN

The J0 register enable (J0REGEN) bit controls the insertion of section trace in the data stream. When J0REGEN is set to logic 1, the section trace from the J0 register is inserted in the J0 byte of STS-1/STM-0 #1 according to the priority of Table 6. When J0REGEN is set to logic 0, the section trace from the J0 register is not inserted.

Z0REGEN

The Z0 register enable (Z0REGEN) bit controls the insertion of Z0 growth bytes in the data stream. When Z0REGEN is set to logic 1, the Z0 growth byte from the Z0 register is inserted in the Z0 bytes according to the priority of Table 6. When Z0REGEN is set to logic 0, the Z0 growth byte from the Z0 register is not inserted. The Z0DEF register bit defines the Z0 bytes.

E1REGEN

The E1 register enable (E1REGEN) bit controls the insertion of section order wire in the data stream. When E1REGEN is set to logic 1, the section order wire from the E1 register is inserted in the E1 byte of STS-1/STM-0 #1 according to the priority of Table 6. When E1REGEN is set to logic 0, the section order wire from the E1 register is not inserted.

F1REGEN

The F1 register enable (F1REGEN) bit controls the insertion of section user channel in the data stream. When F1REGEN is set to logic 1, the section user channel from the F1 register is inserted in the F1 byte of STS-1/STM-0 #1 according to the priority of Table 6. When F1REGEN is set to logic 0, the section user channel from the F1 register is not inserted.

D1D3REGEN

The D1 to D3 register enable (D1D3REGEN) bit controls the insertion of section data communication channel in the data stream. When D1D3REGEN is set to logic 1, the section DCC from the D1D3 register is inserted in the D1 to D3 bytes of STS-1/STM-0 #1 according to the priority of Table 6. When D1D3REGEN is set to logic 0, the section DCC from the D1D3 register is not inserted.

K1K2REGEN

The K1K2 register enable (K1K2REGEN) bit controls the insertion of automatic protection switching in the data stream. When K1K2REGEN is set to logic 1, the APS bytes from the K1K2 register are inserted in the K1, K2 bytes of STS-1/STM-0 #1 according to the priority of Table 6. When K1K2REGEN is set to logic 0, the APS bytes from the K1K2 register are not inserted.

D4D12REGEN

The D4 to D12 register enable (D4D12REGEN) bit controls the insertion of line data communication channel in the data stream. When D4D12REGEN is set to logic 1, the line DCC from the D4D12 register is inserted in the D4 to D12 bytes of STS-1/STM-0 #1 according to the priority of Table 6. When D4D12REGEN is set to logic 0, the line DCC from the D4D12 register is not inserted.

S1REGEN

The S1 register enable (S1REGEN) bit controls the insertion of the synchronization status message in the data stream. When S1REGEN is set to logic 1, the SSM from the S1 register is inserted in the S1 byte of STS-1/STM-0 #1 according to the priority of Table 6. When S1REGEN is set to logic 0, the SSM from the S1 register is not inserted.

Z1REGEN

The Z1 register enable (Z1REGEN) bit controls the insertion of Z1 growth bytes in the data stream. When Z1REGEN is set to logic 1, the Z1 byte from the Z1 register is inserted in the Z1 bytes according to the priority of Table 6. When Z1REGEN is set to logic 0, the Z1 byte from the Z1 register is not inserted.

Z2REGEN

The Z2 register enable (Z2REGEN) bit controls the insertion of Z2 growth bytes in the data stream. When Z2REGEN is set to logic 1, the Z2 byte from the Z2 register is inserted in the Z2 bytes according to the priority of Table 6. When Z2REGEN is set to logic 0, the Z2 byte from the Z2 register is not inserted.

E2REGEN

The E2 register enable (E2REGEN) bit controls the insertion of line order wire in the data stream. When E2REGEN is set to logic 1, the line order wire from the E2 register is inserted in the E2 byte of STS-1/STM-0 #1 according to the priority of Table 6. When E2REGEN is set to logic 0, the line order wire from the E2 register is not inserted.

NATIONALEN

The national enable (NATIONALEN) bit controls the insertion of national bytes in the data stream. When NATIONALEN is set to logic 1, an all one or an all zero pattern is inserted in the national bytes according to the priority of Table 6. When NATIONALEN is set to logic 0, no pattern is inserted. The Z0DEF register bit defines the national bytes of ROW #1.

NATIONALV

The national value (NATIONALV) bit controls the value inserted in the national bytes. When NATIONALV is set to logic 1, an all one pattern is inserted in the national bytes if enable via the NATIONALEN register bit. When NATIONALV is set to logic 0, an all zero pattern is inserted in the national bytes if enable via the NATIONALEN register bit.

UNUSEDEN

The unused enable (UNUSEDEN) bit controls the insertion of unused bytes in the data stream. When UNUSEDEN is set to logic 1, an all one or an all zero pattern is inserted in the unused bytes according to the priority of Table 6. When UNUSEDEN is set to logic 0, no pattern is inserted.

UNUSEDV

The unused value (UNUSEDV) bit controls the value inserted in the unused bytes. When UNUSEDV is set to logic 1, an all one pattern is inserted in the unused bytes if enable via the UNUSEDEN register bit. When UNUSEDV is set to logic 0, an all zero pattern is inserted in the unused bytes if enable via the UNUSEDEN register bit.

Register 1082H, 1482H, 1882H and 1C82H: TRMP Error Insertion

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9		Unused	
Bit 8	R/W	B2DIS	0
Bit 7	R/W	B1DIS	0
Bit 6	R/W	LOSINS	0
Bit 5	R/W	LAISINS	0
Bit 4	R/W	LRDIINS	0
Bit 3	R/W	A1ERR	0
Bit 2	R/W	HMASKEN	1
Bit 1	R/W	B2MASKEN	1
Bit 0	R/W	B1MASKEN	1

The Error Insertion Register is provided at TRMP r/w address 02H.

B1MASKEN

The B1 mask enable (B1MASKEN) bit selects the used of the B1 byte extracted from the TTOH port. When B1MASKEN is set to logic 1, the B1 byte extracted from the TTOH port is used as a mask to toggle bits in the calculated B1 byte (the B1 byte extracted from the TTOH port is xor with the calculated B1 byte). When B1MASKEN is set to logic 0, the B1 byte extracted from the TTOH port is inserted instead of the calculated B1 byte.

B2MASKEN

The B2 mask enable (B2MASKEN) bit selects the used of the B2 bytes extracted from the TTOH port. When B2MASKEN is set to logic 1, the B2 bytes extracted from the TTOH port are used as a mask to toggle bits in the calculated B2 bytes (the B2 bytes extracted from the TTOH port are xor with the calculated B2 bytes). When B2MASKEN is set to logic 0, the B2 bytes extracted from the TTOH port are inserted instead of the calculated B2 bytes.

HMASKEN

The H1/H2 mask enable (HMASKEN) bit selects the used of the H1/H2 bytes extracted from the TTOH port. When HMASKEN is set to logic 1, the H1/H2 bytes extracted from the TTOH port are used as a mask to toggle bits in the H1/H2 path payload pointer bytes (the H1/H2 bytes extracted from the TTOH port are xor with the path payload pointer bytes). When HMASKEN is set to logic 0, the H1/H2 bytes extracted from the TTOH port are inserted instead of the path payload pointer bytes.

A1ERR

The A1 error insertion (A1ERR) bit is used to introduce framing errors in the A1 bytes. When A1ERR is set to logic 1, 76h instead of F6h is inserted in all of the A1 bytes according to the priority of Table 6. When A1ERR is set to logic 0, no framing errors are introduced.

LRDIINS

The line RDI insertion (LRDIINS) bit is used to force a line remote defect indication in the data stream. When LRDIINS is set to logic 1, the 110 pattern is inserted in bits 6, 7 and 8 of the K2 byte of STS-1/STM-0 #1 to force a line RDI condition. When LRDIINS is set to logic 0, the line RDI condition is removed.

LAISINS

The line AIS insertion (LAISINS) bit is used to force a line alarm indication signal in the data stream. When LAISINS is set to logic 1, all ones are inserted in the line overhead and in the payload (all the bytes of the frame except the section overhead bytes) to force a line AIS condition. When LAISINS is set to logic 0, the line AIS condition is removed.

LOSINS

The LOS insertion (LOSINS) bit is used to force a loss of signal condition in the data stream. When LOSINS is set to logic 1, the data steam is set to all zero (after scrambling) to force a loss of signal condition. When LOSINS is set to logic 0, the loss of signal condition is removed.

B1DIS

The B1 disable insertion (B1DIS) bit is used to set the B1 byte in a pass through mode. When B1DIS is set to logic one, the B1 byte value source from the ADD bus is passed through transparently without being overwritten. When B1DIS is set to logic zero, a calculated B1 byte is inserted.

B2DIS

The B2 disable insertion (B2DIS) bit is used to set the B2 byte in a pass through mode. When B2DIS is set to logic one, the B2 byte value source from the ADD bus is passed through transparently without being overwritten. When B2DIS is set to logic zero, a calculated B2 byte is inserted.

Register 1083H, 1483H, 1883H and 1C83H: TRMP Transmit J0 and Z0

Bit	Type	Function	Default
Bit 15	R/W	J0V[7]	0
Bit 14	R/W	J0V[6]	0
Bit 13	R/W	J0V[5]	0
Bit 12	R/W	J0V[4]	0
Bit 11	R/W	J0V[3]	0
Bit 10	R/W	J0V[2]	0
Bit 9	R/W	J0V[1]	0
Bit 8	R/W	J0V[0]	1
Bit 7	R/W	Z0V[7]	1
Bit 6	R/W	Z0V[6]	1
Bit 5	R/W	Z0V[5]	0
Bit 4	R/W	Z0V[4]	0
Bit 3	R/W	Z0V[3]	1
Bit 2	R/W	Z0V[2]	1
Bit 1	R/W	Z0V[1]	0
Bit 0	R/W	Z0V[0]	0

The Transmit J0 and Z0 Register is provided at TRMP r/w address 03H.

Z0V[7:0]

The Z0 byte value (Z0V[7:0]) bits hold the Z0 growth byte to be inserted in the data stream. The Z0V[7:0] value is inserted in the Z0 bytes if the insertion is enabled via the Z0REGEN register bit. The Z0DEF register bit defines the Z0 bytes.

J0V[7:0]

The J0 byte value (J0V[7:0]) bits hold the section trace to be inserted in the data stream. The J0V[7:0] value is inserted in the J0 byte of STS-1/STM-0 #1 if the insertion is enabled via the J0REGEN register bit.

Register 1084H, 1484H, 1884H and 1C84H: TRMP Transmit E1 and F1

Bit	Type	Function	Default
Bit 15	R/W	E1V[7]	0
Bit 14	R/W	E1V[6]	0
Bit 13	R/W	E1V[5]	0
Bit 12	R/W	E1V[4]	0
Bit 11	R/W	E1V[3]	0
Bit 10	R/W	E1V[2]	0
Bit 9	R/W	E1V[1]	0
Bit 8	R/W	E1V[0]	0
Bit 7	R/W	F1V[7]	0
Bit 6	R/W	F1V[6]	0
Bit 5	R/W	F1V[5]	0
Bit 4	R/W	F1V[4]	0
Bit 3	R/W	F1V[3]	0
Bit 2	R/W	F1V[2]	0
Bit 1	R/W	F1V[1]	0
Bit 0	R/W	F1V[0]	0

The Transmit E1 and F1 Register is provided at TRMP r/w address 04H.

F1V[7:0]

The F1 byte value (F1V[7:0]) bits hold the section user channel to be inserted in the data stream. The F1V[7:0] value is inserted in the F1 byte of STS-1/STM-0 #1 if the insertion is enabled via the F1REGEN register bit.

E1V[7:0]

The E1 byte value (E1V[7:0]) bits hold the section order wire to be inserted in the data stream. The E1V[7:0] value is inserted in the E1 byte of STS-1/STM-0 #1 if the insertion is enabled via the E1REGEN register bit.

Register 1085H, 1485H, 1885H and 1C85H: TRMP Transmit D1D3 and D4D12

Bit	Type	Function	Default
Bit 15	R/W	D1D3V[7]	0
Bit 14	R/W	D1D3V[6]	0
Bit 13	R/W	D1D3V[5]	0
Bit 12	R/W	D1D3V[4]	0
Bit 11	R/W	D1D3V[3]	0
Bit 10	R/W	D1D3V[2]	0
Bit 9	R/W	D1D3V[1]	0
Bit 8	R/W	D1D3V[0]	0
Bit 7	R/W	D4D12V[7]	0
Bit 6	R/W	D4D12V[6]	0
Bit 5	R/W	D4D12V[5]	0
Bit 4	R/W	D4D12V[4]	0
Bit 3	R/W	D4D12V[3]	0
Bit 2	R/W	D4D12V[2]	0
Bit 1	R/W	D4D12V[1]	0
Bit 0	R/W	D4D12V[0]	0

The Transmit D1D3 and D4D12 Register is provided at TRMP r/w address 05H.

D4D12V[7:0]

The D4D12 byte value (D4D12V[7:0]) bits hold the line data communication channel to be inserted in the data stream. The D4D12V[7:0] value is inserted in the D4 to D12 bytes of STS-1/STM-0 #1 if the insertion is enabled via the D4D12REGEN register bit.

D1D3V[7:0]

The D1D3 byte value (D1D3V[7:0]) bits hold the section data communication channel to be inserted in the data stream. The D1D3V[7:0] value is inserted in the D1 to D3 bytes of STS-1/STM-0 #1 if the insertion is enabled via the D1D3REGEN register bit.

Register 1086H, 1486H, 1886H and 1C86H: TRMP Transmit K1 and K2

Bit	Type	Function	Default
Bit 15	R/W	K1V[7]	0
Bit 14	R/W	K1V[6]	0
Bit 13	R/W	K1V[5]	0
Bit 12	R/W	K1V[4]	0
Bit 11	R/W	K1V[3]	0
Bit 10	R/W	K1V[2]	0
Bit 9	R/W	K1V[1]	0
Bit 8	R/W	K1V[0]	0
Bit 7	R/W	K2V[7]	0
Bit 6	R/W	K2V[6]	0
Bit 5	R/W	K2V[5]	0
Bit 4	R/W	K2V[4]	0
Bit 3	R/W	K2V[3]	0
Bit 2	R/W	K2V[2]	0
Bit 1	R/W	K2V[1]	0
Bit 0	R/W	K2V[0]	0

The Transmit K1 and K2 Register is provided at TRMP r/w address 06H.

K1V[7:0], K2V[7:0]

The K1, K2 bytes value (K1V[7:0], K2V[7:0]) bits hold the APS bytes to be inserted in the data stream. The K1V[7:0], K2V[7:0] values are inserted in the K1, K2 bytes of STS-1/STM-0 #1 if the insertion is enabled via the K1K2REGEN register bit.

Register 1087H, 1487H, 1887H and 1C87H: TRMP Transmit S1 and Z1

Bit	Type	Function	Default
Bit 15	R/W	S1V[7]	0
Bit 14	R/W	S1V[6]	0
Bit 13	R/W	S1V[5]	0
Bit 12	R/W	S1V[4]	0
Bit 11	R/W	S1V[3]	0
Bit 10	R/W	S1V[2]	0
Bit 9	R/W	S1V[1]	0
Bit 8	R/W	S1V[0]	0
Bit 7	R/W	Z1V[7]	0
Bit 6	R/W	Z1V[6]	0
Bit 5	R/W	Z1V[5]	0
Bit 4	R/W	Z1V[4]	0
Bit 3	R/W	Z1V[3]	0
Bit 2	R/W	Z1V[2]	0
Bit 1	R/W	Z1V[1]	0
Bit 0	R/W	Z1V[0]	0

The Transmit S1 and Z1 Register is provided at TRMP r/w address 07.

Z1V[7:0]

The Z1 byte value (Z1V[7:0]) bits hold the Z1 growth byte to be inserted in the data stream. The Z1V[7:0] value is inserted in the Z1 byte if the insertion is enabled via the Z1REGEN register bit.

S1V[7:0]

The S1 byte value (S1V[7:0]) bits hold the synchronization status message to be inserted in the data stream. The S1V[7:0] value is inserted in the S1 byte of STS-1/STM-0 #1 if the insertion is enabled via the S1REGEN register bit.

Register 1088H, 1488H, 1888H and 1C88H: TRMP Transmit Z2 and E2

Bit	Type	Function	Default
Bit 15	R/W	Z2V[7]	0
Bit 14	R/W	Z2V[6]	0
Bit 13	R/W	Z2V[5]	0
Bit 12	R/W	Z2V[4]	0
Bit 11	R/W	Z2V[3]	0
Bit 10	R/W	Z2V[2]	0
Bit 9	R/W	Z2V[1]	0
Bit 8	R/W	Z2V[0]	0
Bit 7	R/W	E2V[7]	0
Bit 6	R/W	E2V[6]	0
Bit 5	R/W	E2V[5]	0
Bit 4	R/W	E2V[4]	0
Bit 3	R/W	E2V[3]	0
Bit 2	R/W	E2V[2]	0
Bit 1	R/W	E2V[1]	0
Bit 0	R/W	E2V[0]	0

The Transmit Z2 and E2 Register is provided at TRMP r/w address 08H.

E2V[7:0]

The E2 byte value (E2[7:0]) bits hold the line order wire to be inserted in the data stream. The E2V[7:0] value is inserted in the E2 byte of STS-1/STM-0 #1 if the insertion is enabled via the E2REGEN register bit.

Z2V[7:0]

The Z2 byte value (Z2V[7:0]) bits hold the Z2 growth byte to be inserted in the data stream. The Z2V[7:0] value is inserted in the Z2 byte if the insertion is enabled via the Z2REGEN register bit.

Register 1089H, 1489H, 1889H and 1C89H: TRMP Transmit H1 and H2 Mask

Bit	Type	Function	Default
Bit 15	R/W	H1MASK[7]	0
Bit 14	R/W	H1MASK[6]	0
Bit 13	R/W	H1MASK[5]	0
Bit 12	R/W	H1MASK[4]	0
Bit 11	R/W	H1MASK[3]	0
Bit 10	R/W	H1MASK[2]	0
Bit 9	R/W	H1MASK[1]	0
Bit 8	R/W	H1MASK[0]	0
Bit 7	R/W	H2MASK[7]	0
Bit 6	R/W	H2MASK[6]	0
Bit 5	R/W	H2MASK[5]	0
Bit 4	R/W	H2MASK[4]	0
Bit 3	R/W	H2MASK[3]	0
Bit 2	R/W	H2MASK[2]	0
Bit 1	R/W	H2MASK[1]	0
Bit 0	R/W	H2MASK[0]	0

The Transmit H1 and H2 Mask Register is provided at TRMP r/w address 09H.

H2MASK[7:0]

The H2 mask (H2MASK[7:0]) bits hold the H2 path payload pointer errors to be inserted in the data stream. The H2MASK[7:0] is XORed with the path payload pointer already in the data stream.

H1MASK[7:0]

The H1 mask (H1MASK[7:0]) bits hold the H1 path payload pointer errors to be inserted in the data stream. The H1MASK[7:0] is XORed with the path payload pointer already in the data stream.

Register 108AH, 148AH, 188AH and 1C8AH: TRMP Transmit B1 and B2 Mask

Bit	Type	Function	Default
Bit 15	R/W	B1MASK[7]	0
Bit 14	R/W	B1MASK[6]	0
Bit 13	R/W	B1MASK[5]	0
Bit 12	R/W	B1MASK[4]	0
Bit 11	R/W	B1MASK[3]	0
Bit 10	R/W	B1MASK[2]	0
Bit 9	R/W	B1MASK[1]	0
Bit 8	R/W	B1MASK[0]	0
Bit 7	R/W	B2MASK[7]	0
Bit 6	R/W	B2MASK[6]	0
Bit 5	R/W	B2MASK[5]	0
Bit 4	R/W	B2MASK[4]	0
Bit 3	R/W	B2MASK[3]	0
Bit 2	R/W	B2MASK[2]	0
Bit 1	R/W	B2MASK[1]	0
Bit 0	R/W	B2MASK[0]	0

The Transmit B1 and B2 Mask Register is provided at TRMP r/w address 0AH.

B2MASK[7:0]

The B2 mask (B2MASK[7:0]) bits hold the B2 BIP-8 errors to be inserted in the data stream. The B2MASK[7:0] is XORed with the calculated B2 before insertion in the B2 byte.

B1MASK[7:0]

The B1 mask (B1MASK[7:0]) bits hold the B1 BIP-8 errors to be inserted in the data stream. The B1MASK[7:0] is XORed with the calculated B1 before insertion in the B1 byte.

Register 10A0H, 14A0H, 18A0H and 1CA0H: TTTP SECTION Indirect Address

Bit	Type	Function	Default
Bit 15	R	BUSY	X
Bit 14	R/W	RWB	0
Bit 13		Unused	
Bit 12	R/W	IADDR[6]	0
Bit 11	R/W	IADDR[5]	0
Bit 10	R/W	IADDR[4]	0
Bit 9	R/W	IADDR[3]	0
Bit 8	R/W	IADDR[2]	0
Bit 7	R/W	IADDR[1]	0
Bit 6	R/W	IADDR[0]	0
Bit 5		Unused	
Bit 4		Unused	
Bit 3	R/W	PATH[3]	0
Bit 2	R/W	PATH[2]	0
Bit 1	R/W	PATH[1]	0
Bit 0	R/W	PATH[0]	0

The Indirect Address Register is provided at TTTP r/w address 00H.

PATH[3:0]

The STS-1/STM-0 path (PATH[3:0]) bits select which STS-1/STM-0 path is accessed by the current indirect transfer. When the TTTP generates section trace message, path #1 is valid.

PATH[3:0]	STS-1/STM-0 path #
0000	Invalid path
0001	SECTION
0010-1111	Invalid path

IADDR[6:0]

The indirect address location (IADDR[6:0]) bits select which indirect address location is accessed by the current indirect transfer.

Indirect Address IADDR[6:0]	Indirect Data
000 0000	Configuration
000 0001 to 011 1111	Invalid address
100 0000	First byte of the 1/16/64 byte trace
100 0001 to 111 1111	Other bytes of the 16/64 byte trace

RWB

The active high read and active low write (RWB) bit selects if the current access to the internal RAM is an indirect read or an indirect write. Writing to the Indirect Address Register initiates an access to the internal RAM. When RWB is set to logic 1, an indirect read access to the RAM is initiated. The data from the addressed location in the internal RAM will be transferred to the Indirect Data Register. When RWB is set to logic 0, an indirect write access to the RAM is initiated. The data from the Indirect Data Register will be transferred to the addressed location in the internal RAM.

BUSY

The active high RAM busy (BUSY) bit reports if a previously initiated indirect access to the internal RAM has been completed. BUSY is set to logic 1 upon writing to the Indirect Address Register. BUSY is set to logic 0, upon completion of the RAM access. This register should be polled to determine when new data is available in the Indirect Data Register.
Note: Maximum busy bit set time is 22 clock cycles.

Register 10A1H, 14A1H, 18A1H and 1CA1H: TTTP SECTION Indirect Data

Bit	Type	Function	Default
Bit 15	R/W	DATA[15]	0
Bit 14	R/W	DATA[14]	0
Bit 13	R/W	DATA[13]	0
Bit 12	R/W	DATA[12]	0
Bit 11	R/W	DATA[11]	0
Bit 10	R/W	DATA[10]	0
Bit 9	R/W	DATA[9]	0
Bit 8	R/W	DATA[8]	0
Bit 7	R/W	DATA[7]	0
Bit 6	R/W	DATA[6]	0
Bit 5	R/W	DATA[5]	0
Bit 4	R/W	DATA[4]	0
Bit 3	R/W	DATA[3]	0
Bit 2	R/W	DATA[2]	0
Bit 1	R/W	DATA[1]	0
Bit 0	R/W	DATA[0]	0

The Indirect Data Register is provided at TTTP r/w address 01H.

DATA[15:0]

The indirect access data (DATA[15:0]) bits hold the data transfer to or from the internal RAM during indirect access. When RWB is set to logic 1 (indirect read), the data from the addressed location in the internal RAM will be transfer to DATA[15:0]. BUSY should be polled to determine when the new data is available in DATA[15:0]. When RWB is set to logic 0 (indirect write), the data from DATA[15:0] will be transferred to the addressed location in the internal RAM. The indirect Data register must contain valid data before the indirect write is initiated by writing to the Indirect Address Register.

DATA[15:0] has a different meaning depending on which address of the internal RAM is being accessed.

Indirect Register 00H: TTTP SECTION Trace Configuration

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9		Unused	
Bit 8		Unused	
Bit 7		Unused	
Bit 6		Unused	
Bit 5		Unused	
Bit 4		Unused	
Bit 3		Unused	
Bit 2	R/W	ZEROEN	0
Bit 1	R/W	BYTEEN	0
Bit 0	R/W	LENGTH16	0

The Trace Configuration Indirect Register is provided at TTTP r/w indirect address 00H.

LENGTH16

The message length (LENGTH16) bit selects the length of the tail trace message to be transmitted. When LENGTH16 is set to logic 1, the length of the tail trace message is 16 byte. When LENGTH16 is set to logic 0, the length of the tail trace message is 64 byte.

BYTEEN

The single byte message enable (BYTEEN) bit enables the single byte tail trace message. When BYTEEN is set to logic 1, the length of the tail trace message is 1 byte. When BYTEEN is set to logic 0, the length of the tail trace message is determined by LENGTH16. BYTEEN has precedence over LENGTH16.

ZEROEN

The all zero message enable (ZEROEN) bit enables the transmission of an all zero tail trace message. When ZEROEN is set to logic 1, an all zero message is transmitted. When ZEROEN is set to logic 0, the RAM message is transmitted. The enabling and disabling of the all zero tail trace message is not done on message boundary since the receiver is required to perform filtering on the message.

Indirect Register 40H to 7FH: TTTP SECTION Trace

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9		Unused	
Bit 8		Unused	
Bit 7	R/W	TRACE[7]	X
Bit 6	R/W	TRACE[6]	X
Bit 5	R/W	TRACE[5]	X
Bit 4	R/W	TRACE[4]	X
Bit 3	R/W	TRACE[3]	X
Bit 2	R/W	TRACE[2]	X
Bit 1	R/W	TRACE[1]	X
Bit 0	R/W	TRACE[0]	X

The Trace Indirect Register is provided at TTTP r/w indirect address 4FH to 7FH.

TRACE[7:0]

The tail trace message (TRACE[7:0]) bits contain the tail trace message to be transmitted. When BYTEEN is set to logic 1, the message is stored at address 40h. When BYTEEN is set to logic 0 and LENGTH16 is set to logic 1, the message is stored between address 40h and 4Fh. When BYTEEN is set to logic 0 and LENGTH16 is set to logic 0, the message is stored between address 40h and 7Fh.

Register 10C0H, 14C0H, 18C0H and 1CC0H: TTTP PATH Indirect Address

Bit	Type	Function	Default
Bit 15	R	BUSY	X
Bit 14	R/W	RWB	0
Bit 13		Unused	
Bit 12	R/W	IADDR[6]	0
Bit 11	R/W	IADDR[5]	0
Bit 10	R/W	IADDR[4]	0
Bit 9	R/W	IADDR[3]	0
Bit 8	R/W	IADDR[2]	0
Bit 7	R/W	IADDR[1]	0
Bit 6	R/W	IADDR[0]	0
Bit 5		Unused	
Bit 4		Unused	
Bit 3	R/W	PATH[3]	0
Bit 2	R/W	PATH[2]	0
Bit 1	R/W	PATH[1]	0
Bit 0	R/W	PATH[0]	0

The Indirect Address Register is provided at TTTP r/w address 00H.

PATH[3:0]

The STS-1/STM-0 path (PATH[3:0]) bits select which STS-1/STM-0 path is accessed by the current indirect transfer. When the TTTP generates path trace messages, paths #1 to #12.

PATH[3:0]	STS-1/STM-0 path #
0000	Invalid path
0001-1100	Path #1 to Path #12
1101-1111	Invalid path

IADDR[6:0]

The indirect address location (IADDR[6:0]) bits select which indirect address location is accessed by the current indirect transfer.

Indirect Address IADDR[6:0]	Indirect Data
000 0000	Configuration
000 0001 to 011 1111	Invalid address
100 0000	First byte of the 1/16/64 byte trace
100 0001 to 111 1111	Other bytes of the 16/64 byte trace

RWB

The active high read and active low write (RWB) bit selects if the current access to the internal RAM is an indirect read or an indirect write. Writing to the Indirect Address Register initiates an access to the internal RAM. When RWB is set to logic 1, an indirect read access to the RAM is initiated. The data from the addressed location in the internal RAM will be transferred to the Indirect Data Register. When RWB is set to logic 0, an indirect write access to the RAM is initiated. The data from the Indirect Data Register will be transferred to the addressed location in the internal RAM.

BUSY

The active high RAM busy (BUSY) bit reports if a previously initiated indirect access to the internal RAM has been completed. BUSY is set to logic 1 upon writing to the Indirect Address Register. BUSY is set to logic 0, upon completion of the RAM access. This register should be polled to determine when new data is available in the Indirect Data Register.
Note: Maximum busy bit set time is 22 clock cycles.

Register 10C1H, 14C1H, 18C1H and 1CC1H: TTTP PATH Indirect Data

Bit	Type	Function	Default
Bit 15	R/W	DATA[15]	0
Bit 14	R/W	DATA[14]	0
Bit 13	R/W	DATA[13]	0
Bit 12	R/W	DATA[12]	0
Bit 11	R/W	DATA[11]	0
Bit 10	R/W	DATA[10]	0
Bit 9	R/W	DATA[9]	0
Bit 8	R/W	DATA[8]	0
Bit 7	R/W	DATA[7]	0
Bit 6	R/W	DATA[6]	0
Bit 5	R/W	DATA[5]	0
Bit 4	R/W	DATA[4]	0
Bit 3	R/W	DATA[3]	0
Bit 2	R/W	DATA[2]	0
Bit 1	R/W	DATA[1]	0
Bit 0	R/W	DATA[0]	0

The Indirect Data Register is provided at TTTP r/w address 01H.

DATA[15:0]

The indirect access data (DATA[15:0]) bits hold the data transfer to or from the internal RAM during indirect access. When RWB is set to logic 1 (indirect read), the data from the addressed location in the internal RAM will be transfer to DATA[15:0]. BUSY should be polled to determine when the new data is available in DATA[15:0]. When RWB is set to logic 0 (indirect write), the data from DATA[15:0] will be transferred to the addressed location in the internal RAM. The indirect Data register must contain valid data before the indirect write is initiated by writing to the Indirect Address Register.

DATA[15:0] has a different meaning depending on which address of the internal RAM is being accessed.

Indirect Register 00H: TTTP PATH Trace Configuration

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9		Unused	
Bit 8		Unused	
Bit 7		Unused	
Bit 6		Unused	
Bit 5		Unused	
Bit 4		Unused	
Bit 3		Unused	
Bit 2	R/W	ZEROEN	0
Bit 1	R/W	BYTEEN	0
Bit 0	R/W	LENGTH16	0

The Trace Configuration Indirect Register is provided at TTTP r/w indirect address 00H.

LENGTH16

The message length (LENGTH16) bit selects the length of the tail trace message to be transmitted. When LENGTH16 is set to logic 1, the length of the tail trace message is 16 byte. When LENGTH16 is set to logic 0, the length of the tail trace message is 64 byte.

BYTEEN

The single byte message enable (BYTEEN) bit enables the single byte tail trace message. When BYTEEN is set to logic 1, the length of the tail trace message is 1 byte. When BYTEEN is set to logic 0, the length of the tail trace message is determined by LENGTH16. BYTEEN has precedence over LENGTH16.

ZEROEN

The all zero message enable (ZEROEN) bit enables the transmission of an all zero tail trace message. When ZEROEN is set to logic 1, an all zero message is transmitted. When ZEROEN is set to logic 0, the RAM message is transmitted. The enabling and disabling of the all zero tail trace message is not done on message boundary since the receiver is required to perform filtering on the message.

Indirect Register 40H to 7FH: TTTP PATH Trace

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9		Unused	
Bit 8		Unused	
Bit 7	R/W	TRACE[7]	X
Bit 6	R/W	TRACE[6]	X
Bit 5	R/W	TRACE[5]	X
Bit 4	R/W	TRACE[4]	X
Bit 3	R/W	TRACE[3]	X
Bit 2	R/W	TRACE[2]	X
Bit 1	R/W	TRACE[1]	X
Bit 0	R/W	TRACE[0]	X

The Trace Indirect Register is provided at TTTP r/w indirect address 4FH to 7FH.

TRACE[7:0]

The tail trace message (TRACE[7:0]) bits contain the tail trace message to be transmitted. When BYTEEN is set to logic 1, the message is stored at address 40h. When BYTEEN is set to logic 0 and LENGTH16 is set to logic 1, the message is stored between address 40h and 4Fh. When BYTEEN is set to logic 0 and LENGTH16 is set to logic 0, the message is stored between address 40h and 7Fh.

Register 10E0H, 14E0H, 18E0H and 1CE0H: TTTP PATH TU3 Indirect Address

Bit	Type	Function	Default
Bit 15	R	BUSY	X
Bit 14	R/W	RWB	0
Bit 13		Unused	
Bit 12	R/W	IADDR[6]	0
Bit 11	R/W	IADDR[5]	0
Bit 10	R/W	IADDR[4]	0
Bit 9	R/W	IADDR[3]	0
Bit 8	R/W	IADDR[2]	0
Bit 7	R/W	IADDR[1]	0
Bit 6	R/W	IADDR[0]	0
Bit 5		Unused	
Bit 4		Unused	
Bit 3	R/W	PATH[3]	0
Bit 2	R/W	PATH[2]	0
Bit 1	R/W	PATH[1]	0
Bit 0	R/W	PATH[0]	0

The Indirect Address Register is provided at TTTP r/w address 00H.

PATH[3:0]

The STS-1/STM-0 path (PATH[3:0]) bits select which STS-1/STM-0 path is accessed by the current indirect transfer. When the TTTP generates path trace messages, paths #1 to #12 are valid.

PATH[3:0]	STS-1/STM-0 path #
0000	Invalid path
0001-1100	Path #1 to Path #12
1101-1111	Invalid path

IADDR[6:0]

The indirect address location (IADDR[6:0]) bits select which indirect address location is accessed by the current indirect transfer.

Indirect Address IADDR[6:0]	Indirect Data
000 0000	Configuration
000 0001 to 011 1111	Invalid address
100 0000	First byte of the 1/16/64 byte trace
100 0001 to 111 1111	Other bytes of the 16/64 byte trace

RWB

The active high read and active low write (RWB) bit selects if the current access to the internal RAM is an indirect read or an indirect write. Writing to the Indirect Address Register initiates an access to the internal RAM. When RWB is set to logic 1, an indirect read access to the RAM is initiated. The data from the addressed location in the internal RAM will be transferred to the Indirect Data Register. When RWB is set to logic 0, an indirect write access to the RAM is initiated. The data from the Indirect Data Register will be transferred to the addressed location in the internal RAM.

BUSY

The active high RAM busy (BUSY) bit reports if a previously initiated indirect access to the internal RAM has been completed. BUSY is set to logic 1 upon writing to the Indirect Address Register. BUSY is set to logic 0, upon completion of the RAM access. This register should be polled to determine when new data is available in the Indirect Data Register.
Note: Maximum busy bit set time is 22 clock cycles.

Register 10E1H, 14E1H, 18E1H and 1CE1H: TTTP PATH TU3 Indirect Data

Bit	Type	Function	Default
Bit 15	R/W	DATA[15]	0
Bit 14	R/W	DATA[14]	0
Bit 13	R/W	DATA[13]	0
Bit 12	R/W	DATA[12]	0
Bit 11	R/W	DATA[11]	0
Bit 10	R/W	DATA[10]	0
Bit 9	R/W	DATA[9]	0
Bit 8	R/W	DATA[8]	0
Bit 7	R/W	DATA[7]	0
Bit 6	R/W	DATA[6]	0
Bit 5	R/W	DATA[5]	0
Bit 4	R/W	DATA[4]	0
Bit 3	R/W	DATA[3]	0
Bit 2	R/W	DATA[2]	0
Bit 1	R/W	DATA[1]	0
Bit 0	R/W	DATA[0]	0

The Indirect Data Register is provided at TTTP r/w address 01H.

DATA[15:0]

The indirect access data (DATA[15:0]) bits hold the data transfer to or from the internal RAM during indirect access. When RWB is set to logic 1 (indirect read), the data from the addressed location in the internal RAM will be transfer to DATA[15:0]. BUSY should be polled to determine when the new data is available in DATA[15:0]. When RWB is set to logic 0 (indirect write), the data from DATA[15:0] will be transferred to the addressed location in the internal RAM. The indirect Data register must contain valid data before the indirect write is initiated by writing to the Indirect Address Register.

DATA[15:0] has a different meaning depending on which address of the internal RAM is being accessed.

Indirect Register 00H: TTTP PATH TU3 Trace Configuration

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9		Unused	
Bit 8		Unused	
Bit 7		Unused	
Bit 6		Unused	
Bit 5		Unused	
Bit 4		Unused	
Bit 3		Unused	
Bit 2	R/W	ZEROEN	0
Bit 1	R/W	BYTEEN	0
Bit 0	R/W	LENGTH16	0

The Trace Configuration Indirect Register is provided at TTTP r/w indirect address 00H.

LENGTH16

The message length (LENGTH16) bit selects the length of the tail trace message to be transmitted. When LENGTH16 is set to logic 1, the length of the tail trace message is 16 byte. When LENGTH16 is set to logic 0, the length of the tail trace message is 64 byte.

BYTEEN

The single byte message enable (BYTEEN) bit enables the single byte tail trace message. When BYTEEN is set to logic 1, the length of the tail trace message is 1 byte. When BYTEEN is set to logic 0, the length of the tail trace message is determined by LENGTH16. BYTEEN has precedence over LENGTH16.

ZEROEN

The all zero message enable (ZEROEN) bit enables the transmission of an all zero tail trace message. When ZEROEN is set to logic 1, an all zero message is transmitted. When ZEROEN is set to logic 0, the RAM message is transmitted. The enabling and disabling of the all zero tail trace message is not done on message boundary since the receiver is required to perform filtering on the message.

Indirect Register 40H to 7FH: TTTP PATH TU3 Trace

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9		Unused	
Bit 8		Unused	
Bit 7	R/W	TRACE[7]	X
Bit 6	R/W	TRACE[6]	X
Bit 5	R/W	TRACE[5]	X
Bit 4	R/W	TRACE[4]	X
Bit 3	R/W	TRACE[3]	X
Bit 2	R/W	TRACE[2]	X
Bit 1	R/W	TRACE[1]	X
Bit 0	R/W	TRACE[0]	X

The Trace Indirect Register is provided at TTTP r/w indirect address 4FH to 7FH.

TRACE[7:0]

The tail trace message (TRACE[7:0]) bits contain the tail trace message to be transmitted. When BYTEEN is set to logic 1, the message is stored at address 40h. When BYTEEN is set to logic 0 and LENGTH16 is set to logic 1, the message is stored between address 40h and 4Fh. When BYTEEN is set to logic 0 and LENGTH16 is set to logic 0, the message is stored between address 40h and 7Fh.

Register 1100H, 1500H, 1900H and 1D00H: THPP Indirect Address

Bit	Type	Function	Default
Bit 15	R	BUSY	X
Bit 14	R/W	RWB	0
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9	R/W	IADDR[3]	0
Bit 8	R/W	IADDR[2]	0
Bit 7	R/W	IADDR[1]	0
Bit 6	R/W	IADDR[0]	0
Bit 5		Unused	
Bit 4		Unused	
Bit 3	R/W	PATH[3]	0
Bit 2	R/W	PATH[2]	0
Bit 1	R/W	PATH[1]	0
Bit 0	R/W	PATH[0]	0

The Indirect Addressing Register is provided at THPP r/w address 00H.

PATH[3:0]

The STS-1/STM-0 path (PATH[3:0]) bits select which STS-1/STM-0 path is accessed by the current indirect transfer.

PATH[3:0]	STS-1/STM-0 path #
0000	Invalid path
0001-1100	Path #1 to Path #12
1101-1111	Invalid path

IADDR[3:0]

The indirect address (IADDR[3:0]) bits select which address location is accessed by the current indirect transfer.

IADDR[3:0]	Indirect Register
0000	THPP Control Register
0001	THPP Source & Pointer Control
0010	Unused
0011	Unused
0100	THPP Fixed stuff byte and B3MASK
0101	THPP J1 and C2 POH

IADDR[3:0]	Indirect Register
0110	THPP G1 POH and H4MASK
0111	THPP F2 and Z3 POH
1000	THPP Z4 and Z5 POH
1001 to 1111	Unused

RWB

The active high read and active low write (RWB) bit selects if the current access to the internal RAM is an indirect read or an indirect write. Writing to the Indirect Address Register initiates an access to the internal RAM. When RWB is set to logic 1, an indirect read access to the RAM is initiated. The data from the addressed location in the internal RAM will be transferred to the Indirect Data Register. When RWB is set to logic 0, an indirect write access to the RAM is initiated. The data from the Indirect Data Register will be transferred to the addressed location in the internal RAM.

BUSY

The BUSY (BUSY) bit reports the status of an indirect read/write access to the time sliced ram. BUSY is set to logic 1 upon writing to the Indirect Addressing Register. BUSY is set to logic 0, upon completion of the RAM transfer. This register should be polled to determine when new data is available in the Indirect Data Register.
Note: Maximum busy bit set time is 22 clock cycles.

Register 1101H, 1501H, 1901H and 1D01H: THPP Indirect Data

Bit	Type	Function	Default
Bit 15	R/W	DATA[15]	0
Bit 14	R/W	DATA[14]	0
Bit 13	R/W	DATA[13]	0
Bit 12	R/W	DATA[12]	0
Bit 11	R/W	DATA[11]	0
Bit 10	R/W	DATA[10]	0
Bit 9	R/W	DATA[9]	0
Bit 8	R/W	DATA[8]	0
Bit 7	R/W	DATA[7]	0
Bit 6	R/W	DATA[6]	0
Bit 5	R/W	DATA[5]	0
Bit 4	R/W	DATA[4]	0
Bit 3	R/W	DATA[3]	0
Bit 2	R/W	DATA[2]	0
Bit 1	R/W	DATA[1]	0
Bit 0	R/W	DATA[0]	0

The Indirect Data Register is provided at THPP r/w address 01H.

DATA[15:0]

The indirect access data (DATA[15:0]) bits hold the data transfer to or from the internal RAM during indirect access. When RWB is set to logic 1 (indirect read), the data from the addressed location in the internal RAM will be transferred to DATA[15:0]. BUSY should be polled to determine when the new data is available in DATA[15:0]. When RWB is set to logic 0 (indirect write), the data from DATA[15:0] will be transferred to the addressed location in the internal RAM. The indirect Data register must contain valid data before the indirect write is initiated by writing to the Indirect Address Register.

DATA[15:0] has a different meaning depending on which address of the internal RAM is being accessed.

Register 1102H, 1502H, 1902H and 1D02H: THPP Payload Configuration

Bit	Type	Function	Default
Bit 15	R/W	STS12CSL	0
Bit 14	R/W	STS12C	0
Bit 13	R/W	Reserved	0
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9		Unused	
Bit 8		Unused	
Bit 7	R/W	Reserved	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	STS3C[4]	0
Bit 2	R/W	STS3C[3]	0
Bit 1	R/W	STS3C[2]	0
Bit 0	R/W	STS3C[1]	0

The Payload Configuration Register is provided at THPP r/w address 02H.

STS3C[1]

The STS-3c (VC-4) payload configuration (STS3C[1]) bit selects the payload configuration. When STS3C[1] is set to logic 1, the STS-1/STM-0 paths #1, #5 and #9 are part of a STS-3c (VC-4) payload. When STS3C[1] is set to logic 0, the paths are STS-1 (VC-3) payloads. When STS12C is set to logic 1, STS3C[1] must be set to logic 0.

STS3C[2]

The STS-3c (VC-4) payload configuration (STS3C[2]) bit selects the payload configuration. When STS3C[2] is set to logic 1, the STS-1/STM-0 paths #2, #6 and #10 are part of a STS-3c (VC-4) payload. When STS3C[2] is set to logic 0, the paths are STS-1 (VC-3) payloads. When STS12C is set to logic 1, STS3C[2] must be set to logic 0.

STS3C[3]

The STS-3c (VC-4) payload configuration (STS3C[3]) bit selects the payload configuration. When STS3C[3] is set to logic 1, the STS-1/STM-0 paths #3, #7 and #11 are part of a STS-3c (VC-4) payload. When STS3C[3] is set to logic 0, the paths are STS-1 (VC-3) payloads. When STS12C is set to logic 1, STS3C[3] must be set to logic 0.

STS3C[4]

The STS-3c (VC-4) payload configuration (STS3C[4]) bit selects the payload configuration. When STS3C[4] is set to logic 1, the STS-1/STM-0 paths #4, #8 and #12 are part of a STS-3c (VC-4) payload. When STS3C[4] is set to logic 0, the paths are STS-1 (VC-3) payloads. When STS12C is set to logic 1, STS3C[4] must be set to logic 0.

STS12C

The STS-12c (VC-4-4c) payload configuration (STS12C) bit selects the payload configuration. When STS12C is set to logic 1, the STS-1/STM-0 paths #1 to #12 are part of a STS-12c (VC-4-4c) payload. When STS12C is set to logic 0, the STS-1/STM-0 paths are defined with the STS3C[1:4] register bit.

STS12CSL

The slave STS-12c (VC-4-4c) payload configuration (STS12CSL) bit selects the slave payload configuration. When STS12CSL is set to logic 1, the STS-1/STM-0 paths #1 to #12 are part of a STS-12c (VC-4-4c) slave payload. When STS12CSL is set to logic 0, the STS-1/STM-0 paths #1 to # 12 are part of a STS-12c (VC-4-4c) master payload. When STS12C is set to logic 0, the STS12CSL must be set to logic 0.

Indirect Register 00H: THPP Control

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9		Unused	
Bit 8		Unused	
Bit 7	R/W	Reserved	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	TDIS	0
Bit 4		Unused	
Bit 3	R/W	FSBEN	0
Bit 2	R/W	PREIEBLK	0
Bit 1	R/W	EXCFS	0
Bit 0		Unused	

The THPP Control Indirect Register is provided at THPP r/w indirect address 00H.

EXCFS

When EXCFS is logic high, the fixed stuff columns in the STS-1 (VC-3) format are excluded from BIP-8 calculations. When EXCFS is logic low, the fixed stuff columns in the STS-1 (VC-3) format are included in the BIP calculations.

PREIEBLK

When PREIEBLK is logic high, the REI-P value source from the RHPP represents BIP-8 block errors, i.e. the REI-P value allowed in G1 is either 0 or 1. When PREIEBLK is logic low, the REI-P value source from the RHPP represents BIP-8 errors, i.e. the REI-P value allowed in G1 is from 0 to 8.

FSBEN

When FSBEN is logic high, the THPP overwrites the fixed stuff bytes with the register value FSB[7:0]. When FSBEN is logic low, the fixed stuff bytes are not over written.

TDIS

When TDIS is logic high, the path overhead bytes are passed through the THPP transparently from the ADD TelecomBus without being overwritten by the THPP. When TDIS is logic low, the THPP can insert path overhead bytes.

Indirect Register 01H: THPP Source and Pointer Control

Bit	Type	Function	Default
Bit 15	R/W	UNEQV	0
Bit 14	R/W	UNEQ	0
Bit 13	R/W	H4MASK	0
Bit 12	R/W	B3MASK	0
Bit 11	R/W	ENG1REC	1
Bit 10	R/W	H4REGMASK	0
Bit 9	R/W	PTBJ1	0
Bit 8	R/W	SRCZ5	0
Bit 7	R/W	SRCZ4	0
Bit 6	R/W	SRCZ3	0
Bit 5	R/W	SRCF2	0
Bit 4	R/W	SRCG1	0
Bit 3	R/W	SRCH4	0
Bit 2	R/W	SRCC2	0
Bit 1	R/W	SRCJ1	0
Bit 0	R/W	IBER	0

The THPP Control Indirect Register is provided at THPP r/w indirect address 01H.

IBER

When the IBER is logic high, the G1 byte is passed through the THPP transparently from the ADD Telecom Bus. When IBER is logic zero, the G1 byte can be modified by the THPP.

SRCJ1, SRCC2, SRCH4, SRCG1, SRCF2, SRCZ3, SRCZ4, SRCZ5

The SRCxx bits are used to determine the source of the path overhead bytes. When a logic high is written to SRCJ1, the J1 byte inserted in the transmit data stream is source from the internal J1 register. When a logic low is written to SRCJ1, the J1 byte inserted in the transmit data stream is not source from internal register.

PTBJ1

When PTBJ1 is logic high, the J1 byte is source from the TTTP. When PTBJ1 is logic low, the J1 byte is not source from the TTTP.

H4REGMASK

When H4REGMASK is logic high, the H4[7:0] byte in the H4 register is used as an error mask on the H4 byte. When H4REGMASK is logic low, the H4[7:0] byte in the H4 register is inserted in the transmit data stream.

ENG1REC

When ENG1REC is logic high, the ERDI-P and REI-P from the RHPP are inserted into the G1 path overhead byte.. When ENG1REC is logic low, the ERDI-P and REI-P from the RHPP are not inserted.

B3MASK

When B3MASK is logic high, the B3 byte received on the TPOH (valid only if TPOHEN is logic high) port is used as a mask for the B3 byte. When B3MASK is logic low, the B3 byte received on the TPOH (valid only if TPOHEN is logic high) port is inserted in the transmit data stream.

H4MASK

When H4MASK is logic high, the H4 byte received on the TPOH (valid only if TPOHEN is logic high) port is used as a mask for the H4 byte. When H4MASK is logic low, the H4 byte received on the TPOH (valid only if TPOHEN is logic high) port is inserted in the transmit data stream.

UNEQ

The unequipped bit (UNEQ) controls the insertion of an all one or an all zero pattern in the path overhead and in the payload, the fixed stuff bytes are excluded from insertion. When UNEQ is set to logic one, an all one or an all zero pattern is inserted in the path overhead and in the payload. When UNEQ is set logic 0, no pattern is inserted.

UNEQV

The unequipped value (UNEQV) bit controls the value inserted in the path overhead and in the payload. When UNEQV is set to logic 1, an all one pattern is inserted in the path overhead and in the payload if enable via the UNEQ register bit. When UNEQV is set to logic 0, an all zero pattern is inserted in the path overhead and in the payload if enable via the UNEQ register bit.

Indirect Register 04H: THPP Fixed Stuff and B3 Mask

Bit	Type	Function	Default
Bit 15	R/W	B3MASK[7]	0
Bit 14	R/W	B3MASK[6]	0
Bit 13	R/W	B3MASK[5]	0
Bit 12	R/W	B3MASK[4]	0
Bit 11	R/W	B3MASK[3]	0
Bit 10	R/W	B3MASK[2]	0
Bit 9	R/W	B3MASK[1]	0
Bit 8	R/W	B3MASK[0]	0
Bit 7	R/W	FSB[7]	0
Bit 6	R/W	FSB[6]	0
Bit 5	R/W	FSB[5]	0
Bit 4	R/W	FSB[4]	0
Bit 3	R/W	FSB[3]	0
Bit 2	R/W	FSB[2]	0
Bit 1	R/W	FSB[1]	0
Bit 0	R/W	FSB[0]	0

FSB[7:0]

When FSBEN is logic one, the THPP replaces the fixed stuff bytes with the byte from this register.

B3MASK[7:0]

The calculated B3 byte to be inserted in the path overhead is XORed with this register byte to allow the user to insert errors in B3.

Indirect Register 05H: THPP J1 and C2

Bit	Type	Function	Default
Bit 15	R/W	C2[7]	0
Bit 14	R/W	C2[6]	0
Bit 13	R/W	C2[5]	0
Bit 12	R/W	C2[4]	0
Bit 11	R/W	C2[3]	0
Bit 10	R/W	C2[2]	0
Bit 9	R/W	C2[1]	0
Bit 8	R/W	C2[0]	0
Bit 7	R/W	J1[7]	0
Bit 6	R/W	J1[6]	0
Bit 5	R/W	J1[5]	0
Bit 4	R/W	J1[4]	0
Bit 3	R/W	J1[3]	0
Bit 2	R/W	J1[2]	0
Bit 1	R/W	J1[1]	0
Bit 0	R/W	J1[0]	0

J1[7:0]

When SRCJ1 is logic high, this byte is inserted in the J1 path overhead byte position.

C2[7:0]

When SRCC2 is logic high, this byte is inserted in the C2 path overhead byte position.

Indirect Register 06H: THPP G1 and H4 mask

Bit	Type	Function	Default
Bit 15	R/W	H4[7]	0
Bit 14	R/W	H4[6]	0
Bit 13	R/W	H4[5]	0
Bit 12	R/W	H4[4]	0
Bit 11	R/W	H4[3]	0
Bit 10	R/W	H4[2]	0
Bit 9	R/W	H4[1]	0
Bit 8	R/W	H4[0]	0
Bit 7	R/W	G1[7]	0
Bit 6	R/W	G1[6]	0
Bit 5	R/W	G1[5]	0
Bit 4	R/W	G1[4]	0
Bit 3	R/W	G1[3]	0
Bit 2	R/W	G1[2]	0
Bit 1	R/W	G1[1]	0
Bit 0	R/W	G1[0]	0

G1[7:0]

When SRCG1 is logic high, this byte is inserted in the G1 path overhead byte position.

H4[7:0]

The logical value of the H4REGMASK register bit determines if this byte is to be inserted in the H4 path overhead byte position or is to be used as an error mask.

Indirect Register 07H: THPP F2 and Z3

Bit	Type	Function	Default
Bit 15	R/W	F2[7]	0
Bit 14	R/W	F2[6]	0
Bit 13	R/W	F2[5]	0
Bit 12	R/W	F2[4]	0
Bit 11	R/W	F2[3]	0
Bit 10	R/W	F2[2]	0
Bit 9	R/W	F2[1]	0
Bit 8	R/W	F2[0]	0
Bit 7	R/W	Z3[7]	0
Bit 6	R/W	Z3[6]	0
Bit 5	R/W	Z3[5]	0
Bit 4	R/W	Z3[4]	0
Bit 3	R/W	Z3[3]	0
Bit 2	R/W	Z3[2]	0
Bit 1	R/W	Z3[1]	0
Bit 0	R/W	Z3[0]	0

F2[7:0]

When SRCF2 is logic high, this byte is inserted in the F2 path overhead byte position.

Z3[7:0]

When SRCZ3 is logic high, this byte is inserted in the Z3 path overhead byte position.

Indirect Register 08H: THPP Z4 and Z5

Bit	Type	Function	Default
Bit 15	R/W	Z4[7]	0
Bit 14	R/W	Z4[6]	0
Bit 13	R/W	Z4[5]	0
Bit 12	R/W	Z4[4]	0
Bit 11	R/W	Z4[3]	0
Bit 10	R/W	Z4[2]	0
Bit 9	R/W	Z4[1]	0
Bit 8	R/W	Z4[0]	0
Bit 7	R/W	Z5[7]	0
Bit 6	R/W	Z5[6]	0
Bit 5	R/W	Z5[5]	0
Bit 4	R/W	Z5[4]	0
Bit 3	R/W	Z5[3]	0
Bit 2	R/W	Z5[2]	0
Bit 1	R/W	Z5[1]	0
Bit 0	R/W	Z5[0]	0

Z4[7:0]

When SRCZ4 is logic high, this byte is inserted in the Z4 path overhead byte position.

Z5[7:0]

When SRCZ5 is logic high, this byte is inserted in the Z5 path overhead byte position.

Register 1180H, 1580H, 1980H and 1D80H: THPP TU3 Indirect Address

Bit	Type	Function	Default
Bit 15	R	BUSY	X
Bit 14	R/W	RWB	0
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9	R/W	IADDR[3]	0
Bit 8	R/W	IADDR[2]	0
Bit 7	R/W	IADDR[1]	0
Bit 6	R/W	IADDR[0]	0
Bit 5		Unused	
Bit 4		Unused	
Bit 3	R/W	PATH[3]	0
Bit 2	R/W	PATH[2]	0
Bit 1	R/W	PATH[1]	0
Bit 0	R/W	PATH[0]	0

The Indirect Addressing Register is provided at THPP r/w address 00H.

PATH[3:0]

The STS-1/STM-0 path (PATH[3:0]) bits select which STS-1/STM-0 path is accessed by the current indirect transfer.

PATH[3:0]	STS-1/STM-0 path #
0000	Invalid path
0001-1100	Path #1 to Path #12
1101-1111	Invalid path

IADDR[3:0]

The indirect address (IADDR[3:0]) bits select which address location is accessed by the current indirect transfer.

IADDR[3:0]	Indirect Register
0000	THPP Control Register
0001	THPP Source & Pointer Control
0010	Unused
0011	Unused
0100	THPP Fixed stuff byte and B3MASK
0101	THPP J1 and C2 POH

IADDR[3:0]	Indirect Register
0110	THPP G1 POH and H4MASK
0111	THPP F2 and Z3 POH
1000	THPP Z4 and Z5 POH
1001 to 1111	Unused

RWB

The active high read and active low write (RWB) bit selects if the current access to the internal RAM is an indirect read or an indirect write. Writing to the Indirect Address Register initiates an access to the internal RAM. When RWB is set to logic 1, an indirect read access to the RAM is initiated. The data from the addressed location in the internal RAM will be transferred to the Indirect Data Register. When RWB is set to logic 0, an indirect write access to the RAM is initiated. The data from the Indirect Data Register will be transferred to the addressed location in the internal RAM.

BUSY

The BUSY (BUSY) bit reports the status of an indirect read/write access to the time sliced ram. BUSY is set to logic 1 upon writing to the Indirect Addressing Register. BUSY is set to logic 0, upon completion of the RAM transfer. This register should be polled to determine when new data is available in the Indirect Data Register.
Note: Maximum busy bit set time is 22 clock cycles.

Register 1181H, 1581H, 1981H and 1D81H: THPP TU3 Indirect Data

Bit	Type	Function	Default
Bit 15	R/W	DATA[15]	0
Bit 14	R/W	DATA[14]	0
Bit 13	R/W	DATA[13]	0
Bit 12	R/W	DATA[12]	0
Bit 11	R/W	DATA[11]	0
Bit 10	R/W	DATA[10]	0
Bit 9	R/W	DATA[9]	0
Bit 8	R/W	DATA[8]	0
Bit 7	R/W	DATA[7]	0
Bit 6	R/W	DATA[6]	0
Bit 5	R/W	DATA[5]	0
Bit 4	R/W	DATA[4]	0
Bit 3	R/W	DATA[3]	0
Bit 2	R/W	DATA[2]	0
Bit 1	R/W	DATA[1]	0
Bit 0	R/W	DATA[0]	0

The Indirect Data Register is provided at THPP r/w address 01H.

DATA[15:0]

The indirect access data (DATA[15:0]) bits hold the data transfer to or from the internal RAM during indirect access. When RWB is set to logic 1 (indirect read), the data from the addressed location in the internal RAM will be transferred to DATA[15:0]. BUSY should be polled to determine when the new data is available in DATA[15:0]. When RWB is set to logic 0 (indirect write), the data from DATA[15:0] will be transferred to the addressed location in the internal RAM. The indirect Data register must contain valid data before the indirect write is initiated by writing to the Indirect Address Register.

DATA[15:0] has a different meaning depending on which address of the internal RAM is being accessed.

Register 1182H, 1582H, 1982H and 1D82H: THPP TU3 Payload Configuration

Bit	Type	Function	Default
Bit 15	R/W	Reserved	0
Bit 14	R/W	Reserved	0
Bit 13	R/W	Reserved	0
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9		Unused	
Bit 8		Unused	
Bit 7	R/W	TUG3[4]	0
Bit 6	R/W	TUG3[3]	0
Bit 5	R/W	TUG3[2]	0
Bit 4	R/W	TUG3[1]	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	Reserved	0

The Payload Configuration Register is provided at THPP r/w address 02H.

TUG3[1]

The TUG3 payload configuration (TUG3[1]) bit selects the payload configuration. When TUG3[1] is set to logic 1, the STS-1/STM-0 paths #1, #5 and #9 are part of a TUG3 payload. When TUG3[1] is set to logic 0, the paths are not part of a TUG3 payloads.

TUG3[2]

The TUG3 payload configuration (TUG3[2]) bit selects the payload configuration. When TUG3[2] is set to logic 1, the STS-1/STM-0 paths #2, #6 and #10 are part of a TUG3 payload. When TUG3[2] is set to logic 0, the paths are not part of a TUG3 payloads.

TUG3[3]

The TUG3 payload configuration (TUG3[3]) bit selects the payload configuration. When TUG3[3] is set to logic 1, the STS-1/STM-0 paths #3, #7 and #11 are part of a TUG3 payload. When TUG3[3] is set to logic 0, the paths are not part of a TUG3 payloads.

TUG3[4]

The TUG3 payload configuration (TUG3[4]) bit selects the payload configuration. When TUG3[4] is set to logic 1, the STS-1/STM-0 paths #4, #8 and #12 are part of a TUG3 payload. When TUG3[4] is set to logic 0, the paths are not part of a TUG3 payloads.

Indirect Register 00H: THPP TU3 Control

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9		Unused	
Bit 8		Unused	
Bit 7	R/W	Reserved	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	TDIS	0
Bit 4		Unused	
Bit 3	R/W	FSBEN	0
Bit 2	R/W	PREIEBLK	0
Bit 1	R/W	EXCFS	0
Bit 0		Unused	

The THPP Control Indirect Register is provided at THPP r/w indirect address 00H.

EXCFS

When EXCFS is logic high, the fixed stuff columns in the STS-1 (VC-3) format are excluded from BIP-8 calculations. When EXCFS is logic low, the fixed stuff columns in the STS-1 (VC-3) format are included in the BIP calculations.

PREIEBLK

When PREIEBLK is logic high, the REI-P value source from the RHPP represents BIP-8 block errors, i.e. the REI-P value allowed in G1 is either 0 or 1. When PREIEBLK is logic low, the REI-P value source from the RHPP represents BIP-8 errors, i.e. the REI-P value allowed in G1 is from 0 to 8.

FSBEN

When FSBEN is logic high, the THPP overwrites the fixed stuff bytes with the register value FSB[7:0]. When FSBEN is logic low, the fixed stuff bytes are not over written.

TDIS

When TDIS is logic high, the path overhead bytes are passed through the THPP transparently from the ADD TelecomBus without being overwritten by the THPP. When TDIS is logic low, the THPP can insert path overhead bytes.

Indirect Register 01H: THPP TU3 Source and Pointer Control

Bit	Type	Function	Default
Bit 15	R/W	UNEQV	0
Bit 14	R/W	UNEQ	0
Bit 13	R/W	H4MASK	0
Bit 12	R/W	B3MASK	0
Bit 11	R/W	ENG1REC	1
Bit 10	R/W	H4REGMASK	0
Bit 9	R/W	PTBJ1	0
Bit 8	R/W	SRCZ5	0
Bit 7	R/W	SRCZ4	0
Bit 6	R/W	SRCZ3	0
Bit 5	R/W	SRCF2	0
Bit 4	R/W	SRCG1	0
Bit 3	R/W	SRCH4	0
Bit 2	R/W	SRCC2	0
Bit 1	R/W	SRCJ1	0
Bit 0	R/W	IBER	0

The THPP Control Indirect Register is provided at THPP r/w indirect address 01H.

IBER

When the IBER is logic high, the G1 byte is passed through the THPP transparently from the ADD Telecom Bus. When IBER is logic zero, the G1 byte can be modified by the THPP.

SRCJ1, SRCC2, SRCH4, SRCG1, SRCF2, SRCZ3, SRCZ4, SRCZ5

The SRCxx bits are used to determine the source of the path overhead bytes. When a logic high is written to SRCJ1, the J1 byte inserted in the transmit data stream is source from the internal J1 register. When a logic low is written to SRCJ1, the J1 byte inserted in the transmit data stream is not source from internal register.

PTBJ1

When PTBJ1 is logic high, the J1 byte is source from the TTTP. When PTBJ1 is logic low, the J1 byte is not source from the TTTP.

H4REGMASK

When H4REGMASK is logic high, the H4[7:0] byte in the H4 register is used as an error mask on the H4 byte. When H4REGMASK is logic low, the H4[7:0] byte in the H4 register is inserted in the transmit data stream.

ENG1REC

When ENG1REC is logic high, the ERDI-P and REI-P from the RHPP are inserted into the G1 path overhead byte.. When ENG1REC is logic low, the ERDI-P and REI-P from the RHPP are not inserted.

B3MASK

When B3MASK is logic high, the B3 byte received on the TPOH (valid only if TPOHEN is logic high) port is used as a mask for the B3 byte. When B3MASK is logic low, the B3 byte received on the TPOH (valid only if TPOHEN is logic high) port is inserted in the transmit data stream.

H4MASK

When H4MASK is logic high, the H4 byte received on the TPOH (valid only if TPOHEN is logic high) port is used as a mask for the H4 byte. When H4MASK is logic low, the H4 byte received on the TPOH (valid only if TPOHEN is logic high) port is inserted in the transmit data stream.

UNEQ

The unequipped bit (UNEQ) controls the insertion of an all one or an all zero pattern in the path overhead and in the payload, the fixed stuff bytes are excluded from insertion. When UNEQ is set to logic one, an all one or an all zero pattern is inserted in the path overhead and in the payload. When UNEQ is set logic 0, no pattern is inserted.

UNEQV

The unequipped value (UNEQV) bit controls the value inserted in the path overhead and in the payload. When UNEQV is set to logic 1, an all one pattern is inserted in the path overhead and in the payload if enable via the UNEQ register bit. When UNEQV is set to logic 0, an all zero pattern is inserted in the path overhead and in the payload if enable via the UNEQ register bit.

Indirect Register 04H: THPP TU3 Fixed Stuff and B3 Mask

Bit	Type	Function	Default
Bit 15	R/W	B3MASK[7]	0
Bit 14	R/W	B3MASK[6]	0
Bit 13	R/W	B3MASK[5]	0
Bit 12	R/W	B3MASK[4]	0
Bit 11	R/W	B3MASK[3]	0
Bit 10	R/W	B3MASK[2]	0
Bit 9	R/W	B3MASK[1]	0
Bit 8	R/W	B3MASK[0]	0
Bit 7	R/W	FSB[7]	0
Bit 6	R/W	FSB[6]	0
Bit 5	R/W	FSB[5]	0
Bit 4	R/W	FSB[4]	0
Bit 3	R/W	FSB[3]	0
Bit 2	R/W	FSB[2]	0
Bit 1	R/W	FSB[1]	0
Bit 0	R/W	FSB[0]	0

FSB[7:0]

When FSBEN is logic one, the THPP replaces the fixed stuff bytes with the byte from this register.

B3MASK[7:0]

The calculated B3 byte to be inserted in the path overhead is XORed with this register byte to allow the user to insert errors in B3.

Indirect Register 05H: THPP TU3 J1 and C2

Bit	Type	Function	Default
Bit 15	R/W	C2[7]	0
Bit 14	R/W	C2[6]	0
Bit 13	R/W	C2[5]	0
Bit 12	R/W	C2[4]	0
Bit 11	R/W	C2[3]	0
Bit 10	R/W	C2[2]	0
Bit 9	R/W	C2[1]	0
Bit 8	R/W	C2[0]	0
Bit 7	R/W	J1[7]	0
Bit 6	R/W	J1[6]	0
Bit 5	R/W	J1[5]	0
Bit 4	R/W	J1[4]	0
Bit 3	R/W	J1[3]	0
Bit 2	R/W	J1[2]	0
Bit 1	R/W	J1[1]	0
Bit 0	R/W	J1[0]	0

J1[7:0]

When SRCJ1 is logic high, this byte is inserted in the J1 path overhead byte position.

C2[7:0]

When SRCC2 is logic high, this byte is inserted in the C2 path overhead byte position.

Indirect Register 06H: THPP TU3 G1 and H4 mask

Bit	Type	Function	Default
Bit 15	R/W	H4[7]	0
Bit 14	R/W	H4[6]	0
Bit 13	R/W	H4[5]	0
Bit 12	R/W	H4[4]	0
Bit 11	R/W	H4[3]	0
Bit 10	R/W	H4[2]	0
Bit 9	R/W	H4[1]	0
Bit 8	R/W	H4[0]	0
Bit 7	R/W	G1[7]	0
Bit 6	R/W	G1[6]	0
Bit 5	R/W	G1[5]	0
Bit 4	R/W	G1[4]	0
Bit 3	R/W	G1[3]	0
Bit 2	R/W	G1[2]	0
Bit 1	R/W	G1[1]	0
Bit 0	R/W	G1[0]	0

G1[7:0]

When SRCG1 is logic high, this byte is inserted in the G1 path overhead byte position.

H4[7:0]

The logical value of the H4REGMASK register bit determines if this byte is to be inserted in the H4 path overhead byte position or is to be used as an error mask.

Indirect Register 07H: THPP TU3 F2 and Z3

Bit	Type	Function	Default
Bit 15	R/W	F2[7]	0
Bit 14	R/W	F2[6]	0
Bit 13	R/W	F2[5]	0
Bit 12	R/W	F2[4]	0
Bit 11	R/W	F2[3]	0
Bit 10	R/W	F2[2]	0
Bit 9	R/W	F2[1]	0
Bit 8	R/W	F2[0]	0
Bit 7	R/W	Z3[7]	0
Bit 6	R/W	Z3[6]	0
Bit 5	R/W	Z3[5]	0
Bit 4	R/W	Z3[4]	0
Bit 3	R/W	Z3[3]	0
Bit 2	R/W	Z3[2]	0
Bit 1	R/W	Z3[1]	0
Bit 0	R/W	Z3[0]	0

F2[7:0]

When SRCF2 is logic high, this byte is inserted in the F2 path overhead byte position.

Z3[7:0]

When SRCZ3 is logic high, this byte is inserted in the Z3 path overhead byte position.

Indirect Register 08H: THPP TU3 Z4 and Z5

Bit	Type	Function	Default
Bit 15	R/W	Z4[7]	0
Bit 14	R/W	Z4[6]	0
Bit 13	R/W	Z4[5]	0
Bit 12	R/W	Z4[4]	0
Bit 11	R/W	Z4[3]	0
Bit 10	R/W	Z4[2]	0
Bit 9	R/W	Z4[1]	0
Bit 8	R/W	Z4[0]	0
Bit 7	R/W	Z5[7]	0
Bit 6	R/W	Z5[6]	0
Bit 5	R/W	Z5[5]	0
Bit 4	R/W	Z5[4]	0
Bit 3	R/W	Z5[3]	0
Bit 2	R/W	Z5[2]	0
Bit 1	R/W	Z5[1]	0
Bit 0	R/W	Z5[0]	0

Z4[7:0]

When SRCZ4 is logic high, this byte is inserted in the Z4 path overhead byte position.

Z5[7:0]

When SRCZ5 is logic high, this byte is inserted in the Z5 path overhead byte position.

Register 1200H, 1600H, 1A00H and 1E00H: TSVCA Indirect Address

Bit	Type	Function	Default
Bit 15	R	BUSY	X
Bit 14	R/W	RWB	0
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9		Unused	
Bit 8		Unused	
Bit 7	R/W	IADDR[1]	0
Bit 6	R/W	IADDR[0]	0
Bit 5		Unused	
Bit 4		Unused	
Bit 3	R/W	PATH[3]	0
Bit 2	R/W	PATH[2]	0
Bit 1	R/W	PATH[1]	0
Bit 0	R/W	PATH[0]	0

The Indirect Address Register is provided at SVCA r/w address 00H.

RWB

The active high read and active low write (RWB) bit selects if the current access to the internal RAM is an indirect read or an indirect write. Writing to the Indirect Address Register initiates an access to the internal RAM. When RWB is set to logic 1, an indirect read access to the RAM is initiated. The data from the addressed location in the internal RAM will be transferred to the Indirect Data Register. When RWB is set to logic 0, an indirect write access to the RAM is initiated. The data from the Indirect Data Register will be transferred to the addressed location in the internal RAM.

BUSY

The active high RAM busy (BUSY) bit reports if a previously initiated indirect access to the internal RAM has been completed. BUSY is set to logic 1 upon writing to the Indirect Address Register. BUSY is set to logic 0, upon completion of the RAM access. This register should be polled to determine when new data is available in the Indirect Data Register.
Note: Maximum busy bit set time is 22 clock cycles.

PATH[3:0]

The STS-1/STM-0 path (PATH[3:0]) bits select which STS-1/STM-0 path is accessed by the current indirect transfer. Some indirect registers are valid only when the PATH[3:0] have certain values.

PATH[3:0]	STS-1/STM-0 path #
0000	Invalid path
0001-1100	Path #1 to Path #12
1101-1111	Invalid path

IADDR[1:0]

The indirect address location (IADDR[1:0]) bits select which address location is accessed by the current indirect transfer.

IADDR[1:0]	Indirect Register
00	SVCA Outgoing Positive Justification Performance Monitor
01	SVCA Outgoing Negative Justification Performance Monitor
10	SVCA Diagnostic/Configuration Register
11	AU-4 pointer

Register 1201H, 1601H, 1A01H and 1E01H: TSVCA Indirect Data

Bit	Type	Function	Default
Bit 15	R/W	DATA[15]	0
Bit 14	R/W	DATA[14]	0
Bit 13	R/W	DATA[13]	0
Bit 12	R/W	DATA[12]	0
Bit 11	R/W	DATA[11]	0
Bit 10	R/W	DATA[10]	0
Bit 9	R/W	DATA[9]	0
Bit 8	R/W	DATA[8]	0
Bit 7	R/W	DATA[7]	0
Bit 6	R/W	DATA[6]	0
Bit 5	R/W	DATA[5]	0
Bit 4	R/W	DATA[4]	0
Bit 3	R/W	DATA[3]	0
Bit 2	R/W	DATA[2]	0
Bit 1	R/W	DATA[1]	0
Bit 0	R/W	DATA[0]	0

The Indirect Data Register is provided at SVCA r/w address 01H.

DATA[15:0]

The indirect access data (DATA[15:0]) bits hold the data transfer to or from the internal RAM during indirect access. When RWB is set to logic 1 (indirect read), the data from the addressed location in the internal RAM will be transferred to DATA[15:0]. BUSY should be polled to determine when the new data is available in DATA[15:0]. When RWB is set to logic 0 (indirect write), the data from DATA[15:0] will be transferred to the addressed location in the internal RAM. The indirect Data register must contain valid data before the indirect write is initiated by writing to the Indirect Address Register.

DATA[15:0] has a different meaning depending on which address of the internal RAM is being accessed.

Register 1202H, 1602H, 1A02H and 1E02H: TSVCA Payload Configuration

Bit	Type	Function	Default
Bit 15	R/W	STS12CSL	0
Bit 14	R/W	STS12C	0
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9		Unused	
Bit 8		Unused	
Bit 7	R/W	TUG3[4]	0
Bit 6	R/W	TUG3[3]	0
Bit 5	R/W	TUG3[2]	0
Bit 4	R/W	TUG3[1]	0
Bit 3	R/W	STS3C[4]	0
Bit 2	R/W	STS3C[3]	0
Bit 1	R/W	STS3C[2]	0
Bit 0	R/W	STS3C[1]	0

The Payload Configuration Register is provided at SVCA r/w address 02H.

STS3C[1]

The STS-3c (VC-4) payload configuration (STS3C[1]) bit selects the payload configuration. When STS3C[1] is set to logic 1, the STS-1/STM-0 paths #1, #5 and #9 are part of an STS-3c (VC-4) payload. When STS3C[1] is set to logic 0, the paths are STS-1 (VC-3) payloads. When STS12C is set to logic 1, STS3C[1] must be set to logic 0.

STS3C[2]

The STS-3c (VC-4) payload configuration (STS3C[2]) bit selects the payload configuration. When STS3C[2] is set to logic 1, the STS-1/STM-0 paths #2, #6 and #10 are part of an STS-3c (VC-4) payload. When STS3C[2] is set to logic 0, the paths are STS-1 (VC-3) payloads. When STS12C is set to logic 1, STS3C[2] must be set to logic 0.

STS3C[3]

The STS-3c (VC-4) payload configuration (STS3C[3]) bit selects the payload configuration. When STS3C[3] is set to logic 1, the STS-1/STM-0 paths #3, #7 and #11 are part of an STS-3c (VC-4) payload. When STS3C[3] is set to logic 0, the paths are STS-1 (VC-3) payloads. When STS12C is set to logic 1, STS3C[3] must be set to logic 0.

STS3C[4]

The STS-3c (VC-4) payload configuration (STS3C[4]) bit selects the payload configuration. When STS3C[4] is set to logic 1, the STS-1/STM-0 paths #4, #8 and #12 are part of an STS-3c (VC-4) payload. When STS3C[4] is set to logic 0, the paths are STS-1 (VC-3) payloads. When STS12C is set to logic 1, STS3C[4] must be set to logic 0.

TUG3[1]

The TUG3 payload configuration (TUG3[1]) bit selects the payload configuration. When TUG3[1] is set to logic 1, the STS-1/STM-0 paths #1, #5 and #9 are part of a TUG3 payload. When TUG3[1] is set to logic 0, the paths are not part of a TUG3 payload. When STS12C is set to logic 1, TUG3[1] must be set to logic 0.

TUG3[2]

The TUG3 payload configuration (TUG3[2]) bit selects the payload configuration. When TUG3[2] is set to logic 1, the STS-1/STM-0 paths #2, #6 and #10 are part of a TUG3 payload. When TUG3[2] is set to logic 0, the paths are not part of a TUG3 payload. When STS12C is set to logic 1, TUG3[2] must be set to logic 0.

TUG3[3]

The TUG3 payload configuration (TUG3[3]) bit selects the payload configuration. When TUG3[3] is set to logic 1, the STS-1/STM-0 paths #3, #7 and #11 are part of a TUG3 payload. When TUG3[3] is set to logic 0, the paths are not part of a TUG3 payload. When STS12C is set to logic 1, TUG3[3] must be set to logic 0.

TUG3[4]

The TUG3 payload configuration (TUG3[4]) bit selects the payload configuration. When TUG3[4] is set to logic 1, the STS-1/STM-0 paths #4, #8 and #12 are part of a TUG3 payload. When TUG3[4] is set to logic 0, the paths are not part of a TUG3 payload. When STS12C is set to logic 1, TUG3[4] must be set to logic 0.

STS12C

The STS-12c (VC-4-4c) payload configuration (STS12C) bit selects the payload configuration. When STS12C is set to logic 1, the STS-1/STM-0 paths #1 to #12 are part of an STS-12c (VC-4-4c) payload. When STS12C is set to logic 0, the STS-1/STM-0 paths are defined with the STS3C[1:4] register bit.

STS12CSL

The slave STS-12c (VC-4-4c) payload configuration (STS12CSL) bit selects the slave payload configuration. When STS12CSL is set to logic 1, the STS-1/STM-0 paths #1 to #12 are part of a STS-12c (VC-4-4c) slave payload. When STS12CSL is set to logic 0, the STS-1/STM-0 paths #1 to #12 are part of a STS-12c (VC-4-4c) master payload. When STS12C is set to logic 0, STS12CSL must be set to logic 0.

Register 1203H, 1603H, 1A03H and 1E03H: TSVCA Positive Pointer Justification Interrupt Status

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11	R	PPJI[12]	0
Bit 10	R	PPJI[11]	0
Bit 9	R	PPJI[10]	0
Bit 8	R	PPJI[9]	0
Bit 7	R	PPJI[8]	0
Bit 6	R	PPJI[7]	0
Bit 5	R	PPJI[6]	0
Bit 4	R	PPJI[5]	0
Bit 3	R	PPJI[4]	0
Bit 2	R	PPJI[3]	0
Bit 1	R	PPJI[2]	0
Bit 0	R	PPJI[1]	0

The Positive Pointer Justification Interrupt Status Register is provided at SVCA r/w address 03H.

PPJI[12:1]

The positive pointer justification interrupt status (PPJI[12:1]) bits are event indicators for STS-1/STM-0 paths #1 to #12. PPJI[12:1] are set to logic 1 to indicate a positive pointer justification event in the outgoing data stream. These interrupt status bits are independent of the interrupt enable bits. PPJI[12:1] are cleared to logic 0 when this register is read.

Register 1204H, 1604H, 1A04H and 1E04H: TSVCA Negative Pointer Justification Interrupt Status

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11	R	NPJI[12]	0
Bit 10	R	NPJI[11]	0
Bit 9	R	NPJI[10]	0
Bit 8	R	NPJI[9]	0
Bit 7	R	NPJI[8]	0
Bit 6	R	NPJI[7]	0
Bit 5	R	NPJI[6]	0
Bit 4	R	NPJI[5]	0
Bit 3	R	NPJI[4]	0
Bit 2	R	NPJI[3]	0
Bit 1	R	NPJI[2]	0
Bit 0	R	NPJI[1]	0

The Negative Pointer Justification Interrupt Status Register is provided at SVCA r/w address 04H.

NPJI[12:1]

The negative pointer justification interrupt status (NPJI[12:1]) bits are event indicators for STS-1/STM-0 paths #1 to #12. NPJI[12:1] are set to logic 1 to indicate a negative pointer justification event in the outgoing data stream. These interrupt status bits are independent of the interrupt enable bits. NPJI[12:1] are cleared to logic 0 when this register is read.

Register 1205H, 1605H, 1A05H and 1E05H: TSVCA FIFO Overflow Interrupt Status

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11	R	FOVRI[12]	0
Bit 10	R	FOVRI[11]	0
Bit 9	R	FOVRI[10]	0
Bit 8	R	FOVRI[9]	0
Bit 7	R	FOVRI[8]	0
Bit 6	R	FOVRI[7]	0
Bit 5	R	FOVRI[6]	0
Bit 4	R	FOVRI[5]	0
Bit 3	R	FOVRI[4]	0
Bit 2	R	FOVRI[3]	0
Bit 1	R	FOVRI[2]	0
Bit 0	R	FOVRI[1]	0

The FIFO overflow Event Interrupt Status Register is provided at SVCA r/w address 05H.

FOVRI[12:1]

The FIFO overflow event interrupt status (FOVRI[12:1]) bits are event indicators for STS-1/STM-0 paths #1 to #12. FOVRI[12:1] are set to logic 1 to indicate a FIFO overflow event. These interrupt status bits are independent of the interrupt enable bits. FOVRI[12:1] are cleared to logic 0 when this register is read.

Register 1206H, 1606H, 1A06H and 1E06H: TSVCA FIFO Underflow Interrupt Status

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11	R	FUDRI[12]	0
Bit 10	R	FUDRI[11]	0
Bit 9	R	FUDRI[10]	0
Bit 8	R	FUDRI[9]	0
Bit 7	R	FUDRI[8]	0
Bit 6	R	FUDRI[7]	0
Bit 5	R	FUDRI[6]	0
Bit 4	R	FUDRI[5]	0
Bit 3	R	FUDRI[4]	0
Bit 2	R	FUDRI[3]	0
Bit 1	R	FUDRI[2]	0
Bit 0	R	FUDRI[1]	0

The FIFO underflow Event Interrupt Status Register is provided at SVCA r/w address 06H.

FUDRI[12:1]

The FIFO underflow event interrupt status (FUDR[12:1]) bits are event indicators for STS-1/STM-0 paths #1 to #12. FUDRI[12:1] are set to logic 1 to indicate a FIFO underflow event. These interrupt status bits are independent of the interrupt enable bits. FUDRI[12:1] are cleared to logic 0 when this register is read.

Register 1207H, 1607H, 1A07H and 1E07H: TSVCA Pointer Justification Interrupt Enable

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11	R/W	PJIE[12]	0
Bit 10	R/W	PJIE[11]	0
Bit 9	R/W	PJIE[10]	0
Bit 8	R/W	PJIE[9]	0
Bit 7	R/W	PJIE[8]	0
Bit 6	R/W	PJIE[7]	0
Bit 5	R/W	PJIE[6]	0
Bit 4	R/W	PJIE[5]	0
Bit 3	R/W	PJIE[4]	0
Bit 2	R/W	PJIE[3]	0
Bit 1	R/W	PJIE[2]	0
Bit 0	R/W	PJIE[1]	0

The Pointer Justification Interrupt Enable Register is provided at SVCA direct r/w address 07H.

PJIEN[12:1]

The pointer justification event interrupt enable (PJIE[12:1]) bits controls the activation of the interrupt output for STS-1/STM-0 paths #1 to #12. When any of these bit locations is set to logic 1, the corresponding pending interrupt will assert the interrupt output. When any of these bit locations is set to logic 0, the corresponding pending interrupt will not assert the interrupt output.

Register 1208H, 1608H, 1A08H and 1E08H TSVCA FIFO Interrupt Enable

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11	R/W	FIE[12]	0
Bit 10	R/W	FIE[11]	0
Bit 9	R/W	FIE[10]	0
Bit 8	R/W	FIE[9]	0
Bit 7	R/W	FIE[8]	0
Bit 6	R/W	FIE[7]	0
Bit 5	R/W	FIE[6]	0
Bit 4	R/W	FIE[5]	0
Bit 3	R/W	FIE[4]	0
Bit 2	R/W	FIE[3]	0
Bit 1	R/W	FIE[2]	0
Bit 0	R/W	FIE[1]	0

The FIFO Event Interrupt Enable Register is provided at SVCA r/w address 08H.

FIEN[12:1]

The FIFO event interrupt enable (FIE[12:1]) bits controls the activation of the interrupt output for STS-1/STM-0 paths #1 to #12 caused by a FIFO overflow of a FIFO underflow. When any of these bit locations is set to logic 1, the corresponding pending interrupt will assert the interrupt output. When any of these bit locations is set to logic 0, the corresponding pending interrupt will not assert the interrupt output.

Register 120AH, 160AH, 1A0AH and 1E0AH: TSVCA Misc

Bit	Type	Function	Default
Bit 15	R/W	ESDIS	0
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11	R/W	CLRFS[12]	0
Bit 10	R/W	CLRFS[11]	0
Bit 9	R/W	CLRFS[10]	0
Bit 8	R/W	CLRFS[9]	0
Bit 7	R/W	CLRFS[8]	0
Bit 6	R/W	CLRFS[7]	0
Bit 5	R/W	CLRFS[6]	0
Bit 4	R/W	CLRFS[5]	0
Bit 3	R/W	CLRFS[4]	0
Bit 2	R/W	CLRFS[3]	0
Bit 1	R/W	CLRFS[2]	0
Bit 0	R/W	CLRFS[1]	0

The FIFO Fixed Stuff register provides miscellaneous control bits. It is provided at r/w address 10H.

ESDIS

When set high, forces the SVCA to bypass the internal FIFO. The input data is not buffered inside the FIFO and is not re-aligned to a new transport frame but simply clocked out on the next rising edge.

CLRFS

The Clear Fixed Stuff (CLRFS) enables the regeneration of fixed stuff columns (#30, #59) of an STS-1/VC-3. When set to logic one, STS-1/VC-3 incoming fixed stuff columns (#30, #59) are discarded and regenerated (set to 00h) on the outgoing stream. When set to logic 0, these fixed stuff columns are relayed through the SVCA.

Register 120BH, 160BH, 1A0BH and 1E0BH: TSVCA Counter Update

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9		Unused	
Bit 8		Unused	
Bit 7		Unused	
Bit 6		Unused	
Bit 5		Unused	
Bit 4		Unused	
Bit 3		Unused	
Bit 2		Unused	
Bit 1		Unused	
Bit 0		Unused	

The Performance monitor transfer register is provided at r/w address 1X0BH. Any write to this register or to the Master Configuration Register (0000H) triggers a transfer of all performance monitor counters to holding registers that can be read by the ecbi interface.

Indirect Register 00H: TSVCA Positive Justifications Performance Monitor

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12	R	PJPMON[12]	0
Bit 11	R	PJPMON[11]	0
Bit 10	R	PJPMON[10]	0
Bit 9	R	PJPMON[9]	0
Bit 8	R	PJPMON[8]	0
Bit 7	R	PJPMON[7]	0
Bit 6	R	PJPMON[6]	0
Bit 5	R	PJPMON[5]	0
Bit 4	R	PJPMON[4]	0
Bit 3	R	PJPMON[3]	0
Bit 2	R	PJPMON[2]	0
Bit 1	R	PJPMON[1]	0
Bit 0	R	PJPMON[0]	0

The Outgoing Positive justifications performance monitor is provided at SVCA indirect r/w address 00H.

PJPMON[12:0]

This register reports the number of positive pointer justification events that occurred on the outgoing side in the previous accumulation interval.

Indirect Register 01H: TSVCA Negative Justifications Performance Monitor

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12	R	NJPMON[12]	0
Bit 11	R	NJPMON[11]	0
Bit 10	R	NJPMON[10]	0
Bit 9	R	NJPMON[9]	0
Bit 8	R	NJPMON[8]	0
Bit 7	R	NJPMON[7]	0
Bit 6	R	NJPMON[6]	0
Bit 5	R	NJPMON[5]	0
Bit 4	R	NJPMON[4]	0
Bit 3	R	NJPMON[3]	0
Bit 2	R	NJPMON[2]	0
Bit 1	R	NJPMON[1]	0
Bit 0	R	NJPMON[0]	0

The outgoing Negative justifications performance monitor is provided at SVCA indirect r/w address 01H.

NJPMON[12:0]

This register reports the number of negative pointer justification events that occurred on the outgoing side in the previous accumulation interval.

Indirect Register 02H: TSVCA Diagnostic/Configuration

Bit	Type	Function	Default
Bit 15	R/W	PTRRST	0
Bit 14	R/W	PTRSS[1]	0
Bit 13	R/W	PTRSS[0]	0
Bit 12	R/W	JUS3DIS	0
Bit 11	R/W	PTRDD[1]	0
Bit 10	R/W	PTRDD[2]	0
Bit 9		Unused	
Bit 8		Unused	
Bit 7		Unused	
Bit 6		Unused	
Bit 5	R/W	Diag_NDFREQ	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	Diag_PAIS	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	Reserved	0

The SVCA Diagnostic Register is provided at SVCA r/w address 02H. These bits should be set to their default values during normal operation of the SVCA.

Diag_PAIS

When set high, the Diag_PAIS bit forces the SVCA to insert path AIS in the selected outgoing stream for at least three consecutive frames. AIS is inserted by writing an all ones pattern in the transport overhead bytes H1, H2, and H3, as well as in the entire STS synchronous payload envelope. The first frame after PAIS negates will contain a new data flag in the transport overhead H1 byte.

Diag_NDFREQ

When set high, Diag_NDFREQ bit forces the SVCA to insert a NEW DATA FLAG indication in the frame regardless of the state of the pointer generation state machine.

PTRDD[1:0]

The PTRDD[1:0] defines the STS-N/AU-N concatenation pointer bits DD. ITU requires that DD be set to 10 when processing AU-4, AU-3 or TU-3. On the other side, BELLCORE does not specify these two bits.

JUST3DIS

When set high, JUST3DIS allows the SVCA to perform 1 justification per frame when necessary. When set to zero, pointer justifications are allowed only every 4 frames.

PTRSS[1:0]

The PTRSS[1:0] defines the STS-N/AU-N pointer bits SS. ITU requires that SS be set to 10 when processing AU-4, AU-3 or TU-3. On the other side, BELLCORE does not specify these two bits. The ss bits are set to 00 when processing a slave sts-1.

PTR_RST

When set high, Incoming and outgoing pointers are reset to their default values. This bit is level sensitive.

Indirect Register 03H: TSVCA AU-4 pointer

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9	R/W	AU4PTR[9]	0
Bit 8	R/W	AU4PTR[8]	0
Bit 7	R/W	AU4PTR[7]	0
Bit 6	R/W	AU4PTR[6]	0
Bit 5	R/W	AU4PTR[5]	0
Bit 4	R/W	AU4PTR[4]	0
Bit 3	R/W	AU4PTR[3]	0
Bit 2	R/W	AU4PTR[2]	0
Bit 1	R/W	AU4PTR[1]	0
Bit 0	R/W	AU4PTR[0]	0

The FIFO AU4PTR is provided at SVCA indirect r/w address 03H.

AU4PTR[9:0]

This register holds the AU-4 pointer when three TUG-3 are carried within a VC-4.

Register 1220H: ASTSI Indirect Address

Bit	Type	Function	Default
Bit 15	R	BUSY	X
Bit 14	R/W	RWB	0
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10	R/W	PAGE	0
Bit 9		Unused	
Bit 8		Unused	
Bit 7	R/W	TSOUT[3]	0
Bit 6	R/W	TSOUT[2]	0
Bit 5	R/W	TSOUT[1]	0
Bit 4	R/W	TSOUT[0]	0
Bit 3		Unused	
Bit 2		Unused	
Bit 1	R/W	DOUTSEL[1]	0
Bit 0	R/W	DOUTSEL[0]	0

This register provides the slice number; the time-slot number and the control page select used to access the control pages. Writing to this register triggers an indirect register access. This register cannot be written to when an indirect register access is in progress.

DOUTSEL[1:0]

The Slice Output Select (DOUTSEL[1:0]) bits select the slice accessed by the current indirect transfer.

DOUTSEL[1:0]	DOUT
00	Slice #1
01	Slice #2
10	Slice #3
11	Slice #4

TSOUT[3:0]

The indirect STS-1/STM-0 output time slot (TSOUT[3:0]) bits indicate the STS-1/STM-0 output time slot accessed in the current indirect access. Time slots #1 to #12 are valid.

TSOUT[3:0]	STS-1/STM-0 time slot #
0000	Invalid time slot
0001-1100	Time slot #1 to time slot #12
1101-1111	Invalid time slot

PAGE

The page (PAGE) bit selects which control page is accessed in the current indirect transfer. Two pages are defined: page 0 and page 1.

PAGE	Control Page
0	Page 0
1	Page 1

RWB

The indirect access control bit (RWB) selects between a configure (write) or interrogate (read) access to the control pages. Writing logic 0 to RWB triggers an indirect write operation. Data to be written is taken for the STSI Indirect Data register. Writing logic 1 to RWB triggers an indirect read operation. The data read from the control pages is stored in the STSI Indirect Data register after the BUSY bit has cleared.

BUSY

The indirect access status bit (BUSY) reports the progress of an indirect access. BUSY is set to logic 1 when this register is written, triggering an access. It remains logic 1 until the access is complete at which time it is set to logic 0. This register should be polled to determine when new data is available in the Indirect Data Register or when another write access can be initiated.
Note: Maximum busy bit set time is 10 clock cycles.

Register 1221H: ASTSI Indirect Data

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13	R/W	Reserved	0
Bit 12	R/W	Reserved	0
Bit 11	R/W	Reserved	0
Bit 10	R/W	Reserved	0
Bit 9	R/W	Reserved	0
Bit 8	R/W	Reserved	0
Bit 7	R/W	TSIN[3]	0
Bit 6	R/W	TSIN[2]	0
Bit 5	R/W	TSIN[1]	0
Bit 4	R/W	TSIN[0]	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	DINSEL[1]	0
Bit 0	R/W	DINSEL[0]	0

This register contains the data read from the control pages after an indirect read operation or the data to be written to the control pages in an indirect write operation. The data to be written to the control pages must be set up in this register before triggering a write. The STSI Indirect Data register reflects the last value read or written until the completion of a subsequent indirect read operation. This register cannot be written to while an indirect register access is in progress.

DINSEL[1:0]

The Slice Input Select (DINSEL[1:0]) field reports the slice number read from or written to an indirect register location.

DINSEL[1:0]	Data Stream
00	Slice #1
01	Slice #2
10	Slice #3
11	Slice #4

TSIN[3:0]

The STS-1/STM-0 Input Time Slot (TSIN[3:0]) field reports the time-slot number read from or written to an indirect register location.

TSIN[3:0]	STS-1/STM-0 time slot #
0000	Invalid time slot
0001-1100	Time slot #1 to time slot #12
1101-1111	Invalid time slot

Register 1222H: ASTSI Configuration

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9		Unused	
Bit 8		Unused	
Bit 7		Unused	
Bit 6		Unused	
Bit 5		Unused	
Bit 4		Unused	
Bit 3	R	ACTIVE	X
Bit 2	R/W	PSEL	0
Bit 1	R/W	J0RORDR	0
Bit 0	R/W	COAPE	0

COAPE

The change of active page interrupt enable (COAPE) bit enables/disables the change of active page interrupt output. When the COAPE bit is set to logic 1, an interrupt is generated when the active page changes from page 0 to page 1 or from page 1 to page 0. These interrupts are masked when COAPE is set to logic 0.

J0RORDR

The J0 Reorder (J0RORDR) bit enables/disables the reordering of the J0/Z0 bytes. This configuration bit only has an effect when the STSI is in the dynamic switching mode – if the STSI is in any of the static switching modes then the value of this bit is ignored. When this bit is set to logic 0 the J0/Z0 bytes are not reordered by the STSI. When this bit is set to logic 1, normal reordering of the J0/Z0 bytes is enabled.

PSEL

The page select (PSEL) bit is used in the selection of the current active page. This bit is logically XORed with the value of the external CMP port to determine which control page is currently active.

ACTIVE

The active page indication (ACTIVE) bit indicates which control page is currently active. When this bit is logic 0 then page 0 is controlling the dynamic mux. When this bit is logic 1 then page 1 is controlling the dynamic mux.

Register 1223H: ASTSI Interrupt Status

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9		Unused	
Bit 8		Unused	
Bit 7		Unused	
Bit 6		Unused	
Bit 5		Unused	
Bit 4		Unused	
Bit 3		Unused	
Bit 2		Unused	
Bit 1		Unused	
Bit 0	R	COAPI	X

COAPI

The change of active page interrupt statue bit (COAPI) reports the status of the change of active page interrupt. COAPI is set to logic 1 when the active control page changes from page 0 to page 1 or from page 1 to page 0. COAPI is cleared immediately following a read to this register when WCIMODE is logic 0. When WCIMODE is logic 1, COAPI is cleared immediately following a **write** (regardless of value) to this register. COAPI remains valid when the interrupt is not enabled (COAPE set to logic 0) and may be polled to detect change of active control page events.

Register 1240H, 1640H, 1A40H and 1E40H: APRGM Indirect Address

Bit	Type	Function	Default
Bit 15	R	BUSY	X
Bit 14	R/W	RDWRB	0
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9	R/W	IADDR[3]	0
Bit 8	R/W	IADDR[2]	0
Bit 7	R/W	IADDR[1]	0
Bit 6	R/W	IADDR[0]	0
Bit 5		Unused	
Bit 4		Unused	
Bit 3	R/W	PATH[3]	0
Bit 2	R/W	PATH[2]	0
Bit 1	R/W	PATH[1]	0
Bit 0	R/W	PATH[0]	0

The PRGM Indirect Address Register is provided at PRGM r/w address 00h when TRSB is high and BSB is low.

PATH[3:0]

The PATH[3:0] bits select which time-multiplexed division is accessed by the current indirect transfer.

PATH[3:0]	time division #
0000	Invalid path
0001-1100	path #1 to path #12
1101-1111	Invalid path

IADDR[3:0]

The indirect address select which indirect register is access by the current indirect transfer. Six indirect registers are defined for the monitor (IADDR[3] = '0') : the configuration, the PRBS[22:7], the PRBS[6:0], the B1/E1 value, the Monitor error count and the received B1/E1 byte.

IADDR[3:0]	RAM page
0000	STS-1 path Configuration
0001	PRBS[22:7]
0010	PRBS[6:0]
0011	B1/E1 value
0100	Monitor error count
0101	Received B1 and E1

Four indirect registers are defined for the generator (IADDR [3] = '1') : the configuration, the PRBS[22:7], the PRBS[6:0] and the B1/E1 value.

IADDR[3:0]	RAM page
1000	STS-1 path Configuration
1001	PRBS[22:7]
1010	PRBS[6:0]
1011	B1/E1 value

RDWRB

The active high read and active low write (RDWRB) bit selects if the current access to the indirect register is an indirect read or an indirect write. Writing to the Indirect Address Register initiates an access to the indirect register. When RDWRB is set to logic 1, an indirect read access to the indirect register is initiated. The data from the addressed location will be transfer to the Indirect Data Register. When RDWRB is set to logic 0, an indirect write access to the indirect register is initiated. The data from the Indirect Data Register will be transfer to the addressed location.

BUSY

The active high busy (BUSY) bit reports if a previously initiated indirect access has been completed. BUSY is set to logic 1 upon writing to the Indirect Address Register. BUSY is set to logic 0, upon completion of the access. This register should be polled to determine when new data is available in the Indirect Data Register.
Note: Maximum busy bit set time is 22 clock cycles.

Register 1241H, 1641H, 1A41H and 1E41H: APRGM Indirect Data

Bit	Type	Function	Default
Bit 15	R/W	DATA[15]	0
Bit 14	R/W	DATA[14]	0
Bit 13	R/W	DATA[13]	0
Bit 12	R/W	DATA[12]	0
Bit 11	R/W	DATA[11]	0
Bit 10	R/W	DATA[10]	0
Bit 9	R/W	DATA[9]	0
Bit 8	R/W	DATA[8]	0
Bit 7	R/W	DATA[7]	0
Bit 6	R/W	DATA[6]	0
Bit 5	R/W	DATA[5]	0
Bit 4	R/W	DATA[4]	0
Bit 3	R/W	DATA[3]	0
Bit 2	R/W	DATA[2]	0
Bit 1	R/W	DATA[1]	0
Bit 0	R/W	DATA[0]	0

The PRGM Indirect Data Register is provided at PRGM r/w address 01h when TRSB is high and BSB is low.

DATA[15:0]

The indirect access data (DATA[15:0]) bits hold the data transfer to or from during indirect access. When RDWRB is set to logic 1 (indirect read), the data from the addressed location will be transfer to DATA[15:0]. BUSY should be polled to determine when the new data is available in DATA[15:0]. When RDWRB is set to logic 0 (indirect write), the data from DATA[15:0] will be transfer to the addressed location. The indirect Data register must contain valid data before the indirect write is initiated by writing to the Indirect Address Register.

DATA[15:0] has a different meaning depending on which indirect register is being accessed.

Register 1242H, 1642H, 1A42H and 1E42H: APRGM Generator Payload Configuration

Bit	Type	Function	Default
Bit 15	R/W	GEN_STS12CSL	0
Bit 14	R/W	GEN_STS12C	0
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10	R/W	GEN_MSSLEN[2]	0
Bit 9	R/W	GEN_MSSLEN[1]	0
Bit 8	R/W	GEN_MSSLEN[0]	0
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R/W	GEN_STS3C[4]	0
Bit 2	R/W	GEN_STS3C[3]	0
Bit 1	R/W	GEN_STS3C[2]	0
Bit 0	R/W	GEN_STS3C[1]	0

The Generator Payload Configuration register is provided at PRGM read address 02h when TRSB is high and BSB is low.

GEN_STS3C[1]

The STS-3c (VC-4) payload configuration (GEN_STS3C[1]) bit selects the payload configuration. When GEN_STS3C[1] is set to logic 1, the STS-1/STM-0 paths #1, #5 and #9 are part of a STS-3c (VC-4) payload. When GEN_STS3C[1] is set to logic 0, the paths are STS-1 (VC-3) payloads. When GEN_STS12C is set to logic 1, GEN_STS3C[1] must be set to logic 0.

GEN_STS3C[2]

The STS-3c (VC-4) payload configuration (GEN_STS3C[2]) bit selects the payload configuration. When GEN_STS3C[2] is set to logic 1, the STS-1/STM-0 paths #2, #6 and #10 are part of a STS-3c (VC-4) payload. When GEN_STS3C[2] is set to logic 0, the paths are STS-1 (VC-3) payloads. When GEN_STS12C is set to logic 1, GEN_STS3C[2] must be set to logic 0.

GEN_STS3C[3]

The STS-3c (VC-4) payload configuration (GEN_STS3C[3]) bit selects the payload configuration. When GEN_STS3C[3] is set to logic 1, the STS-1/STM-0 paths #3, #7 and #11 are part of a STS-3c (VC-4) payload. When GEN_STS3C[3] is set to logic 0, the paths are STS-1 (VC-3) payloads. When GEN_STS12C is set to logic 1, GEN_STS3C[3] must be set to logic 0.

GEN_STS3C[4]

The STS-3c (VC-4) payload configuration (GEN_STS3C[4]) bit selects the payload configuration. When GEN_STS3C[4] is set to logic 1, the STS-1/STM-0 paths #4, #8 and #12 are part of a STS-3c (VC-4) payload. When GEN_STS3C[4] is set to logic 0, the paths are STS-1 (VC-3) payloads. When GEN_STS12C is set to logic 1, GEN_STS3C[4] must be set to logic 0.

GEN_MSSLEN[2:0]

The Master/Slave Configuration Enable enables the master/slave configuration of the PRGM's generator.

GEN_MSSLEN[2:0]	Configuration
000	ms/sl configuration disable (STS-12/STM-4)
001	ms/sl configuration enable 2 PRGMs (STS-24/STM-8)
010	ms/sl configuration enable 3 PRGMs (STS-36/STM-12)
011	ms/sl configuration enable 4 PRGMs (STS-48/STM-16)
100 - 111	Invalid configuration

GEN_MSSLEN[2:0] must be set to "000" for rates STS-12c and below.

GEN_STS12C

The STS-12c (VC-4-4c) payload configuration (GEN_STS12C) bit selects the payload configuration. When GEN_STS12C is set to logic 1, the STS-1/STM-0 paths #1 to #12 are part of the same concatenated payload defined by GEN_MSSLEN. When GEN_STS12C is set to logic 0, the STS-1/STM-0 paths are defined with the GEN_STS3C[1:4] register bit.

GEN_STS12CSL

The slave STS-12c (VC-4-4c) payload configuration (GEN_STS12CSL) bit selects the slave payload configuration. When GEN_STS12CSL is set to logic 1, the STS-1/STM-0 paths #1 to #12 are part of a slave payload. When GEN_STS12CSL is set to logic 0, the STS-1/STM-0 paths are part of a master payload. When GEN_STS12C is set to logic 0, GEN_STS12CSL must be set to logic 0.

Register 1243H, 1643H, 1A43H and 1E43H: APRGM Monitor Payload Configuration

Bit	Type	Function	Default
Bit 15	R/W	MON_STS12CSL	0
Bit 14	R/W	MON_STS12C	0
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10	R/W	MON_MSSLEN[2]	0
Bit 9	R/W	MON_MSSLEN[1]	0
Bit 8	R/W	MON_MSSLEN[0]	0
Bit 7		Unused	X
Bit 6	R/W	Reserved	0
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R/W	MON_STS3C[4]	0
Bit 2	R/W	MON_STS3C[3]	0
Bit 1	R/W	MON_STS3C[2]	0
Bit 0	R/W	MON_STS3C[1]	0

The Monitor Payload Configuration register is provided at PRGM read address 03h when TRSB is high and BSB is low.

MON_STS3C[1]

The STS-3c (VC-4) payload configuration (MON_STS3C[1]) bit selects the payload configuration. When MON_STS3C[1] is set to logic 1, the STS-1/STM-0 paths #1, #5 and #9 are part of a STS-3c/VC-4 payload. When MON_STS3C[1] is set to logic 0, the paths are STS-1/VC-3 payloads. When MON_STS12C is set to logic 1, MON_STS3C[1] must be set to logic 0.

MON_STS3C[2]

The STS-3c (VC-4) payload configuration (MON_STS3C[2]) bit selects the payload configuration. When MON_STS3C[2] is set to logic 1, the STS-1/STM-0 paths #2, #6 and #10 are part of a STS-3c/VC-4 payload. When MON_STS3C[2] is set to logic 0, the paths are STS-1/VC-3 payloads. When MON_STS12C is set to logic 1, MON_STS3C[2] must be set to logic 0.

MON_STS3C[3]

The STS-3c (VC-4) payload configuration (MON_STS3C[3]) bit selects the payload configuration. When MON_STS3C[3] is set to logic 1, the STS-1/STM-0 paths #3, #7 and #11 are part of a MON_STS-3c/VC-4 payload. When MON_STS3C[3] is set to logic 0, the paths are STS-1 (VC-3) payloads. When MON_STS12C is set to logic 1, MON_STS3C[3] must be set to logic 0.

MON_STS3C[4]

The STS-3c (VC-4) payload configuration (MON_STS3C[4]) bit selects the payload configuration. When MON_STS3C[4] is set to logic 1, the STS-1/STM-0 paths #4, #8 and #12 are part of a STS-3c/VC-4 payload. When MON_STS3C[4] is set to logic 0, the paths are STS-1/VC-3 payloads. When MON_STS12C is set to logic 1, MON_STS3C[4] must be set to logic 0.

To initialize the performance to counter to FFFAh, the ERR_CNT_TEST bit must be set high, and a LCLK pulse must be generated.

MON_MSSLEN[2:0]

The Master/Slave Configuration Enable enables the master/slave configuration of the PRGM's monitor.

GEN_MSSLEN[2:0]	Configuration
000	ms/sl configuration disable (STS-12/STM-4)
001	ms/sl configuration enable 2 PRGMs (STS-24/STM-8)
010	ms/sl configuration enable 3 PRGMs (STS-36/STM-12)
011	ms/sl configuration enable 4 PRGMs (STS-48/STM-16)
100 – 111	Invalid configuration

MON_MSSLEN[2:0] must be set to "000" for rates STS-12c and below.

MON_STS12C

The STS-12c (VC-4-4c) payload configuration (MON_STS12C) bit selects the payload configuration. When MON_STS12C is set to logic 1, the STS-1/STM-0 paths #1 to #12 are part of the same concatenated payload defined by MON_MSSLEN. When MON_STS12C is set to logic 0, the STS-1/STM-0 paths are defined with the MON_STS3C[3:0] register bit.

MON_STS12CSL

The slave STS-12c (VC-4-4c) payload configuration (MON_STS12CSL) bit selects the slave payload configuration. When MON_STS12CSL is set to logic 1, the STS-1/STM-0 paths #1 to #12 are part of a slave payload. When MON_STS12CSL is set to logic 0, the STS-1/STM-0 paths are part of a master payload. When MON_STS12C is set to logic 0, MON_STS12CSL must be set to logic 0.

Register 1244H, 1644H, 1A44H and 1E44H: APRGM Monitor Byte Error Interrupt Status

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11	R	MON12_ERRI	X
Bit 10	R	MON11_ERRI	X
Bit 9	R	MON10_ERRI	X
Bit 8	R	MON9_ERRI	X
Bit 7	R	MON8_ERRI	X
Bit 6	R	MON7_ERRI	X
Bit 5	R	MON6_ERRI	X
Bit 4	R	MON5_ERRI	X
Bit 3	R	MON4_ERRI	X
Bit 2	R	MON3_ERRI	X
Bit 1	R	MON2_ERRI	X
Bit 0	R	MON1_ERRI	X

The Monitor Byte Error Interrupt Status register is provided at PRGM read address 04h when TRSB is high and BSB is low.

MON**x**_ERRI

The Monitor Byte Error Interrupt Status register, is the status of the interrupt generated by each of the 12 STS-1 paths when an error has been detected. The MON**x**_ERRI is set high when the monitor is in the synchronized state and when an error in a PRBS byte is detected in the STS-1 path **x**. This bit is independent of MON**x**_ERRE, and is cleared after it's been read.

Register 1245H, 1645H, 1A45H and 1E45H: APRGM Monitor Byte Error Interrupt Enable

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11	R/W	MON12_ERRE	0
Bit 10	R/W	MON11_ERRE	0
Bit 9	R/W	MON10_ERRE	0
Bit 8	R/W	MON9_ERRE	0
Bit 7	R/W	MON8_ERRE	0
Bit 6	R/W	MON7_ERRE	0
Bit 5	R/W	MON6_ERRE	0
Bit 4	R/W	MON5_ERRE	0
Bit 3	R/W	MON4_ERRE	0
Bit 2	R/W	MON3_ERRE	0
Bit 1	R/W	MON2_ERRE	0
Bit 0	R/W	MON1_ERRE	0

The Monitor Byte Error Interrupt Enable register is provided at PRGM r/w address 05h when TRSB is high and BSB is low.

MON**x**_ERRE

The Monitor Byte Error Interrupt Enable register, enables the interrupt for each of the 12 STS-1 paths. When MON**x**_ERRE is set high, allows the Byte Error Interrupt to generate an external interrupt.

Register 1246H, 1646H, 1A46H and 1E46H: APRGM Monitor B1/E1 Bytes Interrupt Status

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11	R	MON12_B1E1I	X
Bit 10	R	MON11_B1E1I	X
Bit 9	R	MON10_B1E1I	X
Bit 8	R	MON9_B1E1I	X
Bit 7	R	MON8_B1E1I	X
Bit 6	R	MON7_B1E1I	X
Bit 5	R	MON6_B1E1I	X
Bit 4	R	MON5_B1E1I	X
Bit 3	R	MON4_B1E1I	X
Bit 2	R	MON3_B1E1I	X
Bit 1	R	MON2_B1E1I	X
Bit 0	R	MON1_B1E1I	X

The Monitor B1/E1Bytes Interrupt Status register is provided at PRGM read address 06h when TRSB is high and BSB is low.

MON**x**_B1E1I

The Monitor B1/E1Bytes Interrupt Status register, is the status of the interrupt generated by each of the 12 STS-1 paths when a change in the status of the comparison has been detected on the B1/E1 bytes. The MON**x**_B1E1I is set high when the monitor is in the synchronized state and when the status change is detected on either the B1 or E1 bytes in the STS-1 path **x**. For example, if a mismatch is detected and the previous comparison was a match, the MON**x**_B1E1I will be set high. But if a mismatch is detected and the previous comparison was a mismatch, the MON**x**_B1E1I will keep its previous value. This bit is independent of MON**x**_B1E1E, and is cleared after it's been read.

Register 1247H, 1647H, 1A47H and 1E47H: APRGM Monitor B1/E1 Bytes Interrupt Enable

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11	R/W	MON12_B1E1E	0
Bit 10	R/W	MON11_ B1E1E	0
Bit 9	R/W	MON10_ B1E1E	0
Bit 8	R/W	MON9_ B1E1E	0
Bit 7	R/W	MON8_ B1E1E	0
Bit 6	R/W	MON7_ B1E1E	0
Bit 5	R/W	MON6_ B1E1E	0
Bit 4	R/W	MON5_ B1E1E	0
Bit 3	R/W	MON4_ B1E1E	0
Bit 2	R/W	MON3_ B1E1E	0
Bit 1	R/W	MON2_ B1E1E	0
Bit 0	R/W	MON1_ B1E1E	0

The Monitor B1/E1Bytes Interrupt Enable register is provided at PRGM r/w address 07h when TRSB is high and BSB is low.

MON**x**_B1E1E

The Monitor B1/E1 Bytes Interrupt Enable register, enables the interrupt for each of the 12 STS-1 paths. When MON**x**_B1E1E is set high, allows the B1/E1Bytes Interrupt to generate an external interrupt.

Register 1249H, 1649H, 1A49H and 1E49H: APRGM Monitor Synchronization Interrupt Status

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11	R	MON12_SYNCI	X
Bit 10	R	MON11_SYNCI	X
Bit 9	R	MON10_SYNCI	X
Bit 8	R	MON9_SYNCI	X
Bit 7	R	MON8_SYNCI	X
Bit 6	R	MON7_SYNCI	X
Bit 5	R	MON6_SYNCI	X
Bit 4	R	MON5_SYNCI	X
Bit 3	R	MON4_SYNCI	X
Bit 2	R	MON3_SYNCI	X
Bit 1	R	MON2_SYNCI	X
Bit 0	R	MON1_SYNCI	X

The Monitor Synchronization Interrupt Status register is provided at PRGM read address 09h when TRSB is high and BSB is low.1

MON**x**_SYNCI

The Monitor Synchronization Interrupt Status register, is set high when a change occurs in the monitor's synchronization status. Whenever a state machine of the **x** STS-1 path goes from Synchronized to Out Of Synchronization state or vice-versa, the MON**x**_SYNCI is set high. This bit is independent of MONx_SYNCE, and is cleared after it's been read.

Register 124AH, 164AH, 1A4AH and 1E4AH: APRGM Monitor Synchronization Interrupt Enable

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11	R/W	MON12_SYNCE	0
Bit 10	R/W	MON11_SYNCE	0
Bit 9	R/W	MON10_SYNCE	0
Bit 8	R/W	MON9_SYNCE	0
Bit 7	R/W	MON8_SYNCE	0
Bit 6	R/W	MON7_SYNCE	0
Bit 5	R/W	MON6_SYNCE	0
Bit 4	R/W	MON5_SYNCE	0
Bit 3	R/W	MON4_SYNCE	0
Bit 2	R/W	MON3_SYNCE	0
Bit 1	R/W	MON2_SYNCE	0
Bit 0	R/W	MON1_SYNCE	0

The Monitor Synchronization Interrupt Enable register is provided at PRGM r/w address 0Ah when TRSB is high and BSB is low.

MON**x**_SYNCE

The Monitor Synchronization Interrupt Enable register, allows each individual STS-1 path to generate an external interrupt on INT. When MON**x**_SYNCE is set high, whenever a change occurs in the synchronization state of the monitor in STS-1 path **x**, generates an interrupt.

Register 124BH, 164BH, 1A4BH and 1E4BH: APRGM Monitor Synchronization Status

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11	R	MON12_SYNCV	X
Bit 10	R	MON11_SYNCV	X
Bit 9	R	MON10_SYNCV	X
Bit 8	R	MON9_SYNCV	X
Bit 7	R	MON8_SYNCV	X
Bit 6	R	MON7_SYNCV	X
Bit 5	R	MON6_SYNCV	X
Bit 4	R	MON5_SYNCV	X
Bit 3	R	MON4_SYNCV	X
Bit 2	R	MON3_SYNCV	X
Bit 1	R	MON2_SYNCV	X
Bit 0	R	MON1_SYNCV	X

The Monitor Synchronization Status register is provided at PRGM read address 0Bh when TRSB is high and BSB is low.

MON**x**_SYNCV

The Monitor Synchronization Status register, reflects the state of the monitor's state machine. When MON**x**_SYNCV is set high, the monitor's state machine is in synchronization for the STS-1 Path **x**. When MON**x**_SYNCV is low, the monitor is NOT in synchronization for the STS-1 Path **x**.
Note: The PRBS monitor will lock to an all 1s or all 0s pattern.
Note: For concatenated payloads, only the first STS-1 path of the STS-Nc MONx_SYNCV1 bit is valid.

Register 124CH, 164CH, 1A4CH and 1E4CH: APRGM Counter Update

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9		Unused	
Bit 8		Unused	
Bit 7		Unused	
Bit 6		Unused	
Bit 5		Unused	
Bit 4		Unused	
Bit 3		Unused	
Bit 2		Unused	
Bit 1		Unused	
Bit 0	R	Reserved	X

The Counter Update register is provided at PRGM read address 0Ch when TRSB is high and BSB is low.

A write in this register or to the Master Configuration Register (0000H) will trigger the transfer of the error counters to holding registers where they can be read. The value written in the register is not important.

Indirect Register 00h: APRGM Monitor STS-1 path Configuration

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10	R/W	Reserved	0
Bit 9	R/W	Reserved	0
Bit 8		Unused	
Bit 7		Unused	
Bit 6	R/W	SEQ_PRBSB	0-
Bit 5	R/W	B1E1_ENA	0
Bit 4		Unused	
Bit 3	W	RESYNC	0
Bit 2	R/W	INV_PRBS	0
Bit 1	R/W	AMODE	0
Bit 0	R/W	MON_ENA	0

PRGM Indirect Data Register (Register 01h) definition when accessing Indirect Address 0h (IADDR[3:0] is “0h” of register 00h).

MON_ENA

Monitor Enable register bit, enables the PRBS monitor for the STS-1 path specified in the PATH[3:0] of register 0h (PRGM Indirect Addressing). If MON_ENA is set to ‘1’, a PRBS sequence is generated and compare to the incoming one inserted in the payload of the SONET/SDH frame. If MON_ENA is low, the data at the input of the monitor is ignored.

AMODE

Sets the PRGM monitor in the Telecom bus mode. If the AMODE is high, the monitor is in Autonomous mode, and the incoming SONET/SDH payload is compared to the internally generated one. In Autonomous mode, the beginning of the SPE is always place next to the H3 byte (zero offset), so the J1 pulses are ignored. When AMODE is low, the SONET/SDH payload offset received on the system interface is maintain through the PRGM block.. The TOH and the POH are outputted unmodified, but PRBS has been inserted in the payload.

Note: For proper operation when the AJ0J1_FP port contains no valid framing, the AFPEN mode (bit 14 of register 0016H) must be configure and the AFPMASK mask (bit 15 of register 001DH) must be enable.

INV_PRBS

Sets the monitor to invert the PRBS before comparing it to the internally generated payload. When set high, the PRBS bytes will be inverted, else they will be compared unmodified.

RESYNC

Sets the monitor to re-initialize the PRBS sequence. When set high, the monitor's state machine will be forced in the Out Of Sync state and automatically try to resynchronize to the incoming stream. In master/slave configuration, to re-initialize the PRBS, RESYNC has to be set high in the master PRGM only.

B1E1_ENA

When high, this bit enables the monitoring of the B1 and E1 bytes in the SONET/SDH frame. The incoming B1 byte is compared to a programmable register. The E1 byte is compared to the complement of the same value. When B1E1_ENA is high, the B1 and E1 bytes are monitored.

SEQ_PRBSB

This bit enables the monitoring of a PRBS or sequential pattern inserted in the payload. When low, the payload contains PRBS bytes, and when high, a sequential pattern is monitored.

Indirect Register 01h: APRGM Monitor PRBS[22:7] Accumulator

Bit	Type	Function	Default
Bit 15	R/W	PRBS[22]	0
Bit 14	R/W	PRBS[21]	0
Bit 13	R/W	PRBS[20]	0
Bit 12	R/W	PRBS[19]	0
Bit 11	R/W	PRBS[18]	0
Bit 10	R/W	PRBS[17]	0
Bit 9	R/W	PRBS[16]	0
Bit 8	R/W	PRBS[15]	0
Bit 7	R/W	PRBS[14]	0
Bit 6	R/W	PRBS[13]	0
Bit 5	R/W	PRBS[12]	0
Bit 4	R/W	PRBS[11]	0
Bit 3	R/W	PRBS[10]	0
Bit 2	R/W	PRBS[9]	0
Bit 1	R/W	PRBS[8]	0
Bit 0	R/W	PRBS[7]	0

PRGM Indirect Data Register (Register 01h) definition when accessing Indirect Address 1h (IADDR[3:0] is “1h” of register 00h).

PRBS[22:7]

The PRBS[22:7] register, are the 16 MSBs of the LFSR state of the STS-1 path specified in the Indirect Addressing register. It is possible to write in this register to change the initial state of the register.

Indirect Register 02h: APRGM Monitor PRBS[6:0] Accumulator

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9		Unused	
Bit 8		Unused	
Bit 7		Unused	
Bit 6	R/W	PRBS[6]	0
Bit 5	R/W	PRBS[5]	0
Bit 4	R/W	PRBS[4]	0
Bit 3	R/W	PRBS[3]	0
Bit 2	R/W	PRBS[2]	0
Bit 1	R/W	PRBS[1]	0
Bit 0	R/W	PRBS[0]	0

PRGM Indirect Data Register (Register 01h) definition when accessing Indirect Address 2h (IADDR[3:0] is “2h” of register 00h).

PRBS[7:0]

The PRBS[7:0] register, are the 6 LSBs of the LFSR state of the STS-1 path specified in the Indirect Addressing register. It is possible to write in this register to change the initial state of the register.

Indirect Register 03H: APRGM Monitor B1/E1 value

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9		Unused	
Bit 8		Unused	
Bit 7	R/W	B1[7]	0
Bit 6	R/W	B1[6]	0
Bit 5	R/W	B1[5]	0
Bit 4	R/W	B1[4]	0
Bit 3	R/W	B1[3]	0
Bit 2	R/W	B1[2]	0
Bit 1	R/W	B1[1]	0
Bit 0	R/W	B1[0]	0

PRGM Indirect Data Register (Register 01h) definition when accessing Indirect Address 3h (IADDR[3:0] is “3h” of register 00h).

B1[7:0]

When enabled, the monitoring of the B1byte in the incoming SONET/SDH frame, is a simple comparison to the value in the B1[7:0] register. The same value is used for the monitoring of the E1 byte except its complement is used.

Indirect Register 04H: APRGM Monitor Error count

Bit	Type	Function	Default
Bit 15	R	ERR_CNT[15]	X
Bit 14	R	ERR_CNT[14]	X
Bit 13	R	ERR_CNT[13]	X
Bit 12	R	ERR_CNT[12]	X
Bit 11	R	ERR_CNT[11]	X
Bit 10	R	ERR_CNT[10]	X
Bit 9	R	ERR_CNT[9]	X
Bit 8	R	ERR_CNT[8]	X
Bit 7	R	ERR_CNT[7]	X
Bit 6	R	ERR_CNT[6]	X
Bit 5	R	ERR_CNT[5]	X
Bit 4	R	ERR_CNT[4]	X
Bit 3	R	ERR_CNT[3]	X
Bit 2	R	ERR_CNT[2]	X
Bit 1	R	ERR_CNT[1]	X
Bit 0	R	ERR_CNT[0]	X

PRGM Indirect Data Register (Register 01h) definition when accessing Indirect Address 4h (IADDR[3:0] is “4h” of register 00h).

ERR_CNT[15:0]

The ERR_CNT[15:0] registers, is the number of error in the PRBS bytes detected during the monitoring. Errors are accumulated only when the monitor is in the synchronized state. Even if there is multiple errors within one PRBS byte, only one error is counted. The error counter is cleared and restarted after its value is transferred to the ERR_CNT[15:0] holding registers. No errors are missed during the transfer. The error counter will not wrap around after reaching FFFFh, it will saturate at this value.
Note: When losing synchronization, the PRBS monitor in the PRGM block incorrectly counts up to two additional byte errors.

Indirect Register 05H: APRGM Monitor Received B1/E1 bytes

Bit	Type	Function	Default
Bit 15	R	REC_E1[7]	X
Bit 14	R	REC_E1[6]	X
Bit 13	R	REC_E1[5]	X
Bit 12	R	REC_E1[4]	X
Bit 11	R	REC_E1[3]	X
Bit 10	R	REC_E1[2]	X
Bit 9	R	REC_E1[1]	X
Bit 8	R	REC_E1[0]	X
Bit 7	R	REC_B1[7]	X
Bit 6	R	REC_B1[6]	X
Bit 5	R	REC_B1[5]	X
Bit 4	R	REC_B1[4]	X
Bit 3	R	REC_B1[3]	X
Bit 2	R	REC_B1[2]	X
Bit 1	R	REC_B1[1]	X
Bit 0	R	REC_B1[0]	X

PRGM Indirect Data Register (Register 01h) definition when accessing Indirect Address 5h (IADDR[3:0] is “5h” of register 00h).

REC_B1[7:0]

The Received B1 byte is the content of the B1 byte position in the SONET/SDH frame for this particular STS-1 path. Every time a B1 byte is received, it is copied in this register.

REC_E1[7:0]

The Received E1 byte is the content of the E1 byte position in the SONET/SDH frame for this particular STS-1 path. Every time a E1 byte is received, it is copied in this register.

Indirect Register 08H: APRGM Generator STS-1 path Configuration

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13	R/W	Reserved	0
Bit 12	R/W	GEN_ENA	0
Bit 11		Unused	
Bit 10		Unused	
Bit 9		Reserved	
Bit 8		APAIS_DIS	
Bit 7	R/W	SS[1]	0
Bit 6	R/W	SS[0]	0
Bit 5	R/W	SEQ_PRBSB	0
Bit 4	R/W	B1E1_ENA	0
Bit 3	W	FORCE_ERR	0
Bit 2		Unused	
Bit 1	R/W	INV_PRBS	0
Bit 0	R/W	AMODE	0

PRGM Indirect Data Register (Register 01h) definition when accessing Indirect Address 8h (IADDR[3:0] is “8h” of register 00h).

AMODE

Sets the PRGM generator in the Telecom bus or in Autonomous mode. If the AMODE is high, the generator is in Autonomous mode, and the SONET/SDH frame is generated using only the J0 pulse. When AMODE is low, the SONET/SDH frame is received on the Telecom bus. The TOH and the POH are outputted unmodified, but PRBS is inserted in the payload.

Note: For proper operation when the AJ0J1_FP port contains no valid framing, the AFPEN mode (bit 14 of register 0016H) must be configure and the AFPMASK mask (bit 15 of register 001DH) must be enable.

INV_PRBS

Sets the generator to invert the PRBS before inserting it in the payload. When set high, the PRBS bytes will be inverted, else they will be inserted unmodified.

FORCE_ERR

The Force Error bit is used to force bit errors in the inserted pattern. When set high, the MSB of the next byte will be inverted, inducing a single bit error. The register clear itself when the operation is complete. A read operation will always result in a logic ‘0’.

B1E1_ENA

This bit enables the replacement of the B1 byte in the SONET/SDH frame, by a programmable value. The E1 byte is replaced by the complement of the same value. When B1E1_ENA is high, the B1 and E1 bytes are replaced in the frame, else they go through the PRGM unaltered. The B1/E1 byte insertion is independent of PRBS insertion.

SEQ_PRBSB

This bit enables the insertion of a PRBS sequence or a sequential pattern in the payload. When low, the payload is filled with PRBS bytes, and when high, a sequential pattern is inserted.

SS[1:0]

The SS bits signal, is the value to be inserted in bit 2 and 3 of the H1 byte of a concatenated pointer. This value is used when the PRGM is in processing concatenated payload and in autonomous mode.

APAIS_DIS

The Add Bus AIS-P Disable controls the APAIS port on a per STS-1/STM-0 basis. When low, the APAIS port controls the insertion of AIS-P in the transmit side for the corresponding STS-1/STM-0 path. When high, the APAIS port will not insert AIS-P in the transmit side for the corresponding STS-1/STM-0 path.

GEN_ENA

This bit specifies if PRBS is to be inserted. If GEN_ENA is high, patterns are generated and inserted, else no pattern is generated and the unmodified SONET/SDH input frame is outputted.

Indirect Register 09H: APRGM Generator PRBS[22:7] Accumulator

Bit	Type	Function	Default
Bit 15	R/W	PRBS[22]	0
Bit 14	R/W	PRBS[21]	0
Bit 13	R/W	PRBS[20]	0
Bit 12	R/W	PRBS[19]	0
Bit 11	R/W	PRBS[18]	0
Bit 10	R/W	PRBS[17]	0
Bit 9	R/W	PRBS[16]	0
Bit 8	R/W	PRBS[15]	0
Bit 7	R/W	PRBS[14]	0
Bit 6	R/W	PRBS[13]	0
Bit 5	R/W	PRBS[12]	0
Bit 4	R/W	PRBS[11]	0
Bit 3	R/W	PRBS[10]	0
Bit 2	R/W	PRBS[9]	0
Bit 1	R/W	PRBS[8]	0
Bit 0	R/W	PRBS[7]	0

PRGM Indirect Data Register (Register 01h) definition when accessing Indirect Address 9h (IADDR[3:0] is “9h” of register 00h).

PRBS[22:7]

The PRBS[22:7] register, are the 16 MSBs of the LFSR state of the STS-1 path specified in the Indirect Addressing register. It is possible to write in this register to change the initial state of the register.

Indirect Register 0AH: APRGM Generator PRBS[6:0] Accumulator

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9		Unused	
Bit 8		Unused	
Bit 7		Unused	
Bit 6	R/W	PRBS[6]	0
Bit 5	R/W	PRBS[5]	0
Bit 4	R/W	PRBS[4]	0
Bit 3	R/W	PRBS[3]	0
Bit 2	R/W	PRBS[2]	0
Bit 1	R/W	PRBS[1]	0
Bit 0	R/W	PRBS[0]	0

PRGM Indirect Data Register (Register 01h) definition when accessing Indirect Address Ah (IADDR[3:0] is “Ah” of register 00h).

PRBS[6:0]

The PRBS[6:0] register, are the 7 LSBs of the LFSR state of the STS-1 path specified in the Indirect Addressing register. It is possible to write in this register to change the initial state of the register.

Indirect Register 0Bh: APRGM Generator B1/E1 value

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9		Unused	
Bit 8		Unused	
Bit 7	R/W	B1[7]	0
Bit 6	R/W	B1[6]	0
Bit 5	R/W	B1[5]	0
Bit 4	R/W	B1[4]	0
Bit 3	R/W	B1[3]	0
Bit 2	R/W	B1[2]	0
Bit 1	R/W	B1[1]	0
Bit 0	R/W	B1[0]	0

PRGM Indirect Data Register (Register 01h) definition when accessing Indirect Address Bh (IADDR[3:0] is “Bh” of register 00h).

B1[7:0]

When enabled, the value in this register is inserted in the B1byte position in the outgoing SONET/SDH frame. The complement of this value is also inserted at the E1 byte position.

Register 1280H, 1680H, 1A80H and 1E80H: TAPI Indirect Address

Bit	Type	Function	Default
Bit 15	R	BUSY	X
Bit 14	R/W	RWB	0
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9	R/W	IADDR[3]	0
Bit 8	R/W	IADDR[2]	0
Bit 7	R/W	IADDR[1]	0
Bit 6	R/W	IADDR[0]	0
Bit 5		Unused	
Bit 4		Unused	
Bit 3	R/W	PATH[3]	0
Bit 2	R/W	PATH[2]	0
Bit 1	R/W	PATH[1]	0
Bit 0	R/W	PATH[0]	0

The Indirect Address Register is provided at TAPI r/w address 00H.

PATH[3:0]

The STS-1/STM-0 path (PATH[3:0]) bits select which STS-1/STM-0 path is accessed by the current indirect transfer.

PATH[3:0]	STS-1/STM-0 path #
0000	Invalid path
0001-1100	Path #1 to Path #12
1101-1111	Invalid path

IADDR[3:0]

The indirect address location (IADDR[3:0]) bits select which address location is accessed by the current indirect transfer.

Indirect Address ADDR[3:0]	Indirect Data
0000	Pointer Interpreter Configuration
0001	Error Monitor Configuration
0010	Pointer Value and ERDI
0011	Captured and Accepted PSL

Indirect Address ADDR[3:0]	Indirect Data
0100	Expected PSL and PDI
0101	Pointer Interpreter status
0110	Path BIP Error Counter
0111	Path REI Error Counter
1000	Path Negative Justification Event Counter
1001	Path Positive Justification Event Counter
1010 to 1111	Unused

RWB

The active high read and active low write (RWB) bit selects if the current access to the internal RAM is an indirect read or an indirect write. Writing to the Indirect Address Register initiates an access to the internal RAM. When RWB is set to logic 1, an indirect read access to the RAM is initiated. The data from the addressed location in the internal RAM will be transferred to the Indirect Data Register. When RWB is set to logic 0, an indirect write access to the RAM is initiated. The data from the Indirect Data Register will be transferred to the addressed location in the internal RAM.

BUSY

The active high RAM busy (BUSY) bit reports if a previously initiated indirect access to the internal RAM has been completed. BUSY is set to logic 1 upon writing to the Indirect Address Register. BUSY is set to logic 0, upon completion of the RAM access. This register should be polled to determine when new data is available in the Indirect Data Register.
Note: Maximum busy bit set time is 22 clock cycles.

Register 1281H, 1681H, 1A81H and 1E81H: TAPI Indirect Data

Bit	Type	Function	Default
Bit 15	R/W	DATA[15]	0
Bit 14	R/W	DATA[14]	0
Bit 13	R/W	DATA[13]	0
Bit 12	R/W	DATA[12]	0
Bit 11	R/W	DATA[11]	0
Bit 10	R/W	DATA[10]	0
Bit 9	R/W	DATA[9]	0
Bit 8	R/W	DATA[8]	0
Bit 7	R/W	DATA[7]	0
Bit 6	R/W	DATA[6]	0
Bit 5	R/W	DATA[5]	0
Bit 4	R/W	DATA[4]	0
Bit 3	R/W	DATA[3]	0
Bit 2	R/W	DATA[2]	0
Bit 1	R/W	DATA[1]	0
Bit 0	R/W	DATA[0]	0

The Indirect Data Register is provided at TAPI r/w address 01H.

DATA[15:0]

The indirect access data (DATA[15:0]) bits hold the data transfer to or from the internal RAM during indirect access. When RWB is set to logic 1 (indirect read), the data from the addressed location in the internal RAM will be transferred to DATA[15:0]. BUSY should be polled to determine when the new data is available in DATA[15:0]. When RWB is set to logic 0 (indirect write), the data from DATA[15:0] will be transferred to the addressed location in the internal RAM. The indirect Data register must contain valid data before the indirect write is initiated by writing to the Indirect Address Register.

DATA[15:0] has a different meaning depending on which address of the internal RAM is being accessed.

Register 1282H, 1682H, 1A82H and 1E82H: TAPI Payload Configuration

Bit	Type	Function	Default
Bit 15	R/W	STS12CSL	0
Bit 14	R/W	STS12C	0
Bit 13			
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9		Unused	
Bit 8	R/W	Reserved	0
Bit 7	R/W	Reserved	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	STS3C[4]	0
Bit 2	R/W	STS3C[3]	0
Bit 1	R/W	STS3C[2]	0
Bit 0	R/W	STS3C[1]	0

The Payload Configuration Register is provided at TAPI r/w address 02H.

STS3C[1]

The STS-3c (VC-4) payload configuration (STS3C[1]) bit selects the payload configuration. When STS3C[1] is set to logic 1, the STS-1/STM-0 paths #1, #5 and #9 are part of a STS-3c (VC-4) payload. When STS3C[1] is set to logic 0, the paths are STS-1 (VC-3) payloads. The STS12C register bit has precedence over the STS3C[1] register bit.

STS3C[2]

The STS-3c (VC-4) payload configuration (STS3C[2]) bit selects the payload configuration. When STS3C[2] is set to logic 1, the STS-1/STM-0 paths #2, #6 and #10 are part of a STS-3c (VC-4) payload. When STS3C[2] is set to logic 0, the paths are STS-1 (VC-3) payloads. The STS12C register bit has precedence over the STS3C[2] register bit.

STS3C[3]

The STS-3c (VC-4) payload configuration (STS3C[3]) bit selects the payload configuration. When STS3C[3] is set to logic 1, the STS-1/STM-0 paths #3, #7 and #11 are part of a STS-3c (VC-4) payload. When STS3C[3] is set to logic 0, the paths are STS-1 (VC-3) payloads. The STS12C register bit has precedence over the STS3C[3] register bit.

STS3C[4]

The STS-3c (VC-4) payload configuration (STS3C[4]) bit selects the payload configuration. When STS3C[4] is set to logic 1, the STS-1/STM-0 paths #4, #8 and #12 are part of a STS-3c (VC-4) payload. When STS3C[4] is set to logic 0, the paths are STS-1 (VC-3) payloads. The STS12C register bit has precedence over the STS3C[4] register bit.

STS12C

The STS-12c (VC-4-4c) payload configuration (STS12C) bit selects the payload configuration. When STS12C is set to logic 1, the STS-1/STM-0 paths #1 to #12 are part of a STS-12c (VC-4-4c) payload. When STS12C is set to logic 0, the STS-1/STM-0 paths are defined with the STS3C[1:4] register bit. The STS12C register bit has precedence over the STS3C[1:4] register bit.

STS12CSL

The slave STS-12c (VC-4-4c) payload configuration (STS12CSL) bit selects the slave payload configuration. When STS12CSL is set to logic 1, the STS-1/STM-0 paths #1 to #12 are part of a STS-12c (VC-4-4c) slave payload. When STS12CSL is set to logic 0, the STS-1/STM-0 paths #1 to # 12 are part of a STS-12c (VC-4-4c) master payload. When STS12C is set to logic 0, the STS12CSL register bit has no effect.

Register 1283H, 1683H, 1A83H and 1E83H: TAPI Counters update

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9		Unused	
Bit 8		Unused	
Bit 7		Unused	
Bit 6		Unused	
Bit 5		Unused	
Bit 4		Unused	
Bit 3		Unused	
Bit 2		Unused	
Bit 1		Unused	
Bit 0		Unused	

Any write to the TAPI Counters Update Register (address 0X03H) or to the Master Configuration Register (0000H) will trigger the transfer of all counter values to their holding registers.

Register 1284H, 1684H, 1A84H and 1E84H: TAPI Path Interrupt Status

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11	R	P_INT[12]	X
Bit 10	R	P_INT[11]	X
Bit 9	R	P_INT[10]	X
Bit 8	R	P_INT[9]	X
Bit 7	R	P_INT[8]	X
Bit 6	R	P_INT[7]	X
Bit 5	R	P_INT[6]	X
Bit 4	R	P_INT[5]	X
Bit 3	R	P_INT[4]	X
Bit 2	R	P_INT[3]	X
Bit 1	R	P_INT[2]	X
Bit 0	R	P_INT[1]	X

The Path Interrupt Status Register is provided at TAPI read address 04H.

P_INT[1:12]

The Path Interrupt Status bit (P_INT[1:12]) tells which path(s) have interrupts that are still active. Reading from this register will not clear any of the interrupts, it is simply added to reduce the average number of accesses required to service interrupts.

Register 1285H, 1685H, 1A85H and 1E85H: TAPI Pointer Concatenation Processing Disable

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11	R/W	PTRCDIS[12]	0
Bit 10	R/W	PTRCDIS[11]	0
Bit 9	R/W	PTRCDIS[10]	0
Bit 8	R/W	PTRCDIS[9]	0
Bit 7	R/W	PTRCDIS[8]	0
Bit 6	R/W	PTRCDIS[7]	0
Bit 5	R/W	PTRCDIS[6]	0
Bit 4	R/W	PTRCDIS[5]	0
Bit 3	R/W	PTRCDIS[4]	0
Bit 2	R/W	PTRCDIS[3]	0
Bit 1	R/W	PTRCDIS[2]	0
Bit 0	R/W	PTRCDIS[1]	0

The Pointer Concatenation processing Disable Register is provided at TAPI r/w address 05H.

PTRCDIS[1:12]

The concatenation pointer processing disable (PTRCDIS[1:12]) bits disable the path concatenation pointer interpreter state machine. When PTRCDIS[n] is set to logic 1, the path concatenation pointer interpreter state-machine (for the path n) is disabled and excluded from the LOPC-P, AISC-P and ALLAISC-P defect declaration. When PTRCDIS is set to logic 0, the path concatenation pointer interpreter state-machine is enabled and included in the LOPC-P, AISC-P and ALLAISC-P defect declaration.

Register 1288H, 1688H, 1A88H and 1E88H: TAPI Pointer Interpreter Status(STS1/STM0 #1)
Register 1290H, 1690H, 1A90H and 1E90H: TAPI Pointer Interpreter Status (STS1/STM0 #2)
Register 1298H, 1698H, 1A98H and 1E98H: TAPI Pointer Interpreter Status (STS1/STM0 #3)
Register 12A0H, 16A0H, 1AA0H and 1EA0H: TAPI Pointer Interpreter Status (STS1/STM0 #4)
Register 12A8H, 16A8H, 1AA8H and 1EA8H: TAPI Pointer Interpreter Status (STS1/STM0 #5)
Register 12B0H, 16B0H, 1AB0H and 1EB0H: TAPI Pointer Interpreter Status (STS1/STM0 #6)
Register 12B8H, 16B8H, 1AB8H and 1EB8H: TAPI Pointer Interpreter Status (STS1/STM0 #7)
Register 12C0H, 16C0H, 1AC0H and 1EC0H: TAPI Pointer Interpreter Status (STS1/STM0 #8)
Register 12C8H, 16C8H, 1AC8H and 1EC8H: TAPI Pointer Interpreter Status (STS1/STM0 #9)
Register 12D0H, 16D0H, 1AD0H and 1ED0H: TAPI Pointer Interpreter Status (STS1/STM0 #10)
Register 12D8H, 16D8H, 1AD8H and 1ED8H: TAPI Pointer Interpreter Status (STS1/STM0 #11)
Register 12E0H, 16E0H, 1AE0H and 1EE0H: TAPI Pointer Interpreter Status (STS1/STM0 #12)

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9		Unused	
Bit 8		Unused	
Bit 7		Unused	
Bit 6		Unused	
Bit 5	R	PAISCV	X
Bit 4	R	PLOPCV	X
Bit 3	R	PAISV	X
Bit 2	R	PLOPV	X
Bit 1		Unused	
Bit 0		Unused	

The Pointer Interpreter Status Register is provided at TAPI r/w address 08H 10H 18H 20H 28H 30H 38H 40H 48H 50H 58H and 60H.

PLOPV

The path lost of pointer state (PLOPV) bit indicates the current status of the pointer interpreter state machine. PLOPV is set to logic 1 when the state machine is in the LOP_state. PLOPV is set to logic 0 when the state machine is not in the LOP_state.

PAISV

The path alarm indication signal state (PAISV) bit indicates the current status of the pointer interpreter state machine. PAISV is set to logic 1 when the state machine is in the AIS_state. PAISV is set to logic 0 when the state machine is not in the AIS_state.

PLOPCV

The path lost of pointer concatenation state (PLOPCV) bit indicates the current status of the concatenation pointer interpreter state machine. PLOPCV is set to logic 1 when the state machine is in the LOPC_state. PLOPCV is set to logic 0 when the state machine is not in the LOPC_state.

PAISCV

The path concatenation alarm indication signal state (PAISCV) bit indicates the current status of the concatenation pointer interpreter state machine. PAISCV is set to logic 1 when the state machine is in the AISC_state. PAISCV is set to logic 0 when the state machine is not in the LOPC_state.

Register 1289H, 1689H, 1A89H and 1E89H: TAPI Pointer Interpreter Interrupt Enable (STS1/STM0 #1)
Register 1291H, 1691H, 1A91H and 1E91H: TAPI Pointer Interpreter Interrupt Enable (STS1/STM0 #2)
Register 1299H, 1699H, 1A99H and 1E99H: TAPI Pointer Interpreter Interrupt Enable (STS1/STM0 #3)
Register 12A1H, 16A1H, 1AA1H and 1EA1H: TAPI Pointer Interpreter Interrupt Enable (STS1/STM0 #4)
Register 12A9H, 16A9H, 1AA9H and 1EA9H: TAPI Pointer Interpreter Interrupt Enable (STS1/STM0 #5)
Register 12B1H, 16B1H, 1AB1H and 1EB1H: TAPI Pointer Interpreter Interrupt Enable (STS1/STM0 #6)
Register 12B9H, 16B9H, 1AB9H and 1EB9H: TAPI Pointer Interpreter Interrupt Enable (STS1/STM0 #7)
Register 12C1H, 16C1H, 1AC1H and 1EC1H: TAPI Pointer Interpreter Interrupt Enable (STS1/STM0 #8)
Register 12C9H, 16C9H, 1AC9H and 1EC9H: TAPI Pointer Interpreter Interrupt Enable (STS1/STM0 #9)
Register 12D1H, 16D1H, 1AD1H and 1ED1H: TAPI Pointer Interpreter Interrupt Enable (STS1/STM0 #10)
Register 12D9H, 16D9H, 1AD9H and 1ED9H: TAPI Pointer Interpreter Interrupt Enable (STS1/STM0 #11)
Register 12E1H, 16E1H, 1AE1H and 1EE1H: TAPI Pointer Interpreter Interrupt Enable (STS1/STM0 #12)

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9		Unused	
Bit 8		Unused	
Bit 7		Unused	
Bit 6		Unused	
Bit 5	R/W	PAISCE	0
Bit 4	R/W	PLOPCE	0
Bit 3	R/W	PAISE	0
Bit 2	R/W	PLOPE	0
Bit 1		Unused	
Bit 0	R/W	PTRJEE	0

The Pointer Interpreter Interrupt Enable Register is provided at TAPI r/w address 09H 11H 19H 21H 29H 31H 39H 41H 49H 51H 59H and 61H.

PTRJEE

The pointer justification event interrupt enable (PTRJEE) bit control the activation of the interrupt output. When PTRJEE is set to logic 1, the NJEI and PJEI pending interrupt will assert the interrupt output. When PTRJEE is set to logic 0, the NJEI and PJEI pending interrupt will not assert the interrupt output.

PLOPE

The path loss of pointer interrupt enable (PLOPE) bit controls the activation of the interrupt output. When PLOPE is set to logic 1, the PLOPI pending interrupt will assert the interrupt output. When PLOPE is set to logic 0, the PLOPI pending interrupt will not assert the interrupt output.

PAISE

The path alarm indication signal interrupt enable (PAISE) bit controls the activation of the interrupt output. When PAISE is set to logic 1, the PAISI pending interrupt will assert the interrupt output. When PAISE is set to logic 0, the PAISI pending interrupt will not assert the interrupt output.

PLOPCE

The path loss of pointer concatenation interrupt enable (PLOPCE) bit controls the activation of the interrupt output. When PLOPCE is set to logic 1, the PLOPCI pending interrupt will assert the interrupt output. When PLOPCE is set to logic 0, the PLOPCI pending interrupt will not assert the interrupt output.

PAISCE

The path concatenation alarm indication signal interrupt enable (PAISCE) bit controls the activation of the interrupt output. When PAISCE is set to logic 1, the PAISCI pending interrupt will assert the interrupt output. When PAISCE is set to logic 0, the PAISCI pending interrupt will not assert the interrupt output.

Register 128AH, 168AH, 1A8AH and 1E8AH: TAPI Pointer Interpreter Interrupt Status (STS1/STM0 #1)
Register 1292H, 1692H, 1A92H and 1E92H: TAPI Pointer Interpreter Interrupt Status (STS1/STM0 #2)
Register 129AH, 169AH, 1A9AH and 1E9AH: TAPI Pointer Interpreter Interrupt Status (STS1/STM0 #3)
Register 12A2H, 16A2H, 1AA2H and 1EA2H: TAPI Pointer Interpreter Interrupt Status (STS1/STM0 #4)
Register 12AAH, 16AAH, 1AAAH and 1EAAH: TAPI Pointer Interpreter Interrupt Status (STS1/STM0 #5)
Register 12B2H, 16B2H, 1AB2H and 1EB2H: TAPI Pointer Interpreter Interrupt Status (STS1/STM0 #6)
Register 12BAH, 16BAH, 1ABAH and 1EBAH: TAPI Pointer Interpreter Interrupt Status (STS1/STM0 #7)
Register 12C2H, 16C2H, 1AC2H and 1EC2H: TAPI Pointer Interpreter Interrupt Status (STS1/STM0 #8)
Register 12CAH, 16CAH, 1ACAH and 1ECAH: TAPI Pointer Interpreter Interrupt Status (STS1/STM0 #9)
Register 12D2H, 16D2H, 1AD2H and 1ED2H: TAPI Pointer Interpreter Interrupt Status (STS1/STM0 #10)
Register 12DAH, 16DAH, 1ADAH and 1EDAH: TAPI Pointer Interpreter Interrupt Status (STS1/STM0 #11)
Register 12E2H, 16E2H, 1AE2H and 1EE2H: TAPI Pointer Interpreter Interrupt Status (STS1/STM0 #12)

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9		Unused	
Bit 8		Unused	
Bit 7		Unused	
Bit 6		Unused	
Bit 5	R	PAISCI	X
Bit 4	R	PLOPCI	X
Bit 3	R	PAISI	X
Bit 2	R	PLOPI	X
Bit 1	R	PJEI	X
Bit 0	R	NJEI	X

The Pointer Interpreter Interrupt Status Register is provided at TAPI r/w address 0AH 12H 1AH 22H 2AH 32H 3AH 42H 4AH 52H 5AH and 62H.

NJEI

The negative pointer justification event interrupt status (NJEI) bit is an event indicator. NJEI is set to logic 1 to indicate a negative pointer justification event. The interrupt status bit is independent of the interrupt enable bit. NJEI is cleared to logic 0 when this register is read.

PJEI

The positive pointer justification event interrupt status (PJEI) bit is an event indicator. PJEI is set to logic 1 to indicate a positive pointer justification event. The interrupt status bit is independent of the interrupt enable bit. PJEI is cleared to logic 0 when this register is read.

PLOPI

The path loss of pointer interrupt status (PLOPI) bit is an event indicator. PLOPI is set to logic 1 to indicate any change in the status of PLOPV (entry to the LOP_state or exit from the LOP_state). The interrupt status bit is independent of the interrupt enable bit. PLOPI is cleared to logic 0 when this register is read.

PAISI

The path alarm indication signal interrupt status (PAISI) bit is an event indicator. PAISI is set to logic 1 to indicate any change in the status of PAISV (entry to the AIS_state or exit from the AIS_state). The interrupt status bit is independent of the interrupt enable bit. PAISI is cleared to logic 0 when this register is read.

PLOPCI

The path loss of pointer concatenation interrupt status (PLOPCI) bit is an event indicator. PLOPCI is set to logic 1 to indicate any change in the status of PLOPCV (entry to the LOPC_state or exit from the LOPC_state). The interrupt status bit is independent of the interrupt enable bit. PLOPCI is cleared to logic 0 when this register is read.

PAISCI

The path concatenation alarm indication signal interrupt status (PAISCI) bit is an event indicator. PAISCI is set to logic 1 to indicate any change in the status of PAISCV (entry to the AISC_state or exit from the AISC_state). The interrupt status bit is independent of the interrupt enable bit. PAISCI is cleared to logic 0 when this register is read.

Register 128BH, 168BH, 1A8BH and 1E8BH: TAPI Error Monitor Status (STS1/STM0 #1)
Register 1293H, 1693H, 1A93H and 1E93H: TAPI Error Monitor Status (STS1/STM0 #2)
Register 129BH, 169BH, 1A9BH and 1E9BH: TAPI Error Monitor Status (STS1/STM0 #3)
Register 12A3H, 16A3H, 1AA3H and 1EA3H: TAPI Error Monitor Status (STS1/STM0 #4)
Register 12ABH, 16ABH, 1AABH and 1EABH: TAPI Error Monitor Status (STS1/STM0 #5)
Register 12B3H, 16B3H, 1AB3H and 1EB3H: TAPI Error Monitor Status (STS1/STM0 #6)
Register 12BBH, 16BBH, 1ABBH and 1EBBH: TAPI Error Monitor Status (STS1/STM0 #7)
Register 12C3H, 16C3H, 1AC3H and 1EC3H: TAPI Error Monitor Status (STS1/STM0 #8)
Register 12CBH, 16CBH, 1ACBH and 1ECBH: TAPI Error Monitor Status (STS1/STM0 #9)
Register 12D3H, 16D3H, 1AD3H and 1ED3H: TAPI Error Monitor Status (STS1/STM0 #10)
Register 12DBH, 16DBH, 1ADBH and 1EDBH: TAPI Error Monitor Status (STS1/STM0 #11)
Register 12E3H, 16E3H, 1AE3H and 1EE3H: TAPI Error Monitor Status (STS1/STM0 #12)

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9		Unused	
Bit 8		Unused	
Bit 7		Unused	
Bit 6	R	PERDIV	X
Bit 5	R	PRDIV	X
Bit 4	R	PPDIV	X
Bit 3	R	PUNEQV	X
Bit 2	R	PPLMV	X
Bit 1	R	PPLUV	X
Bit 0		Unused	

The Error Monitor Status Register is provided at TAPI r/w address 0BH 13H 1BH 23H 2BH 33H 3BH 43H 4BH 53H 5BH and 63H.

Note: The Error Monitor Status bits are don't care for slave time slots.

PPLUV

The path payload label unstable status (PPLUV) bit indicates the current status of the PLU-P defect.

Algorithm 1: PPLUV is set to logic 0.

Algorithm 2: PPLUV is set to logic 1 when a total of 5 received PSL differs from the previously accepted PSL without any persistent PSL in between. PPLUV is set to logic 0 when a persistent PSL is found. A persistent PSL is found when the same PSL is received for 3 or 5 consecutive frames.

PPLMV

The path payload label mismatch status (PPLMV) bit indicates the current status of the PLM-P defect.

Algorithm 1: PPLMV is set to logic 1 when the received PSL does not match, according to Table 3, the expected PSL for 3 or 5 consecutive frames (selectable with the PSL5 register bit). PPLMV is set to logic 0 when the received PSL matches, according to Table 3, the expected PSL for 3 or 5 consecutive frames.

Algorithm 2: PPLMV is set to logic 1 when the accepted PSL does not match, according to Table 3, the expected PSL. PPLMV is set to logic 0 when the accepted PSL matches, according to Table 3, the expected PSL.

PUNEQV

The path unequipped status (PUNEQV) bit indicates the current status of the UNEQ-P defect.

PUNEQV is set to logic 1 when the received PSL indicates unequipped, according to Table 3, for 3 or 5 consecutive frames (selectable with the PSL5 register bit). An PUNEQV is set to logic 0 when the received PSL indicates not unequipped, according to Table 3, for 3 or 5 consecutive frames.

PPDIV

The path payload defect indication status (PPDIV) bit indicates the current status of the PPDI-P defect.

Algorithm 1: PPDIV is set to logic one when the received PSL is a defect, according to Table 3, for 3 or 5 consecutive frames (selectable with the PSL5 register bit). PPDIV is set to logic 0 when the received PSL is not a defect, according to Table 3, for 3 or 5 consecutive frames.

Algorithm 2: PPDIV is set to logic 1 when the accepted PSL is a defect, according to Table 3. PPDI is set to logic 0 when the accepted PSL is not a defect, according to Table 3.

PRDIV

The path remote defect indication status (PRDIV) bit indicates the current status of the RDI-P defect. PRDIV is set to logic 1 when bit 5 of the G1 byte is set high for five or ten consecutive frames (selectable with the PRDI10 register bit). PRDIV is set to logic 0 when bit 5 of the G1 byte is set low for five or ten consecutive frames.

PERDIV

The path enhanced remote defect indication status (PERDIV) bit indicates the current status of the ERDI-P defect. PERDIV is set to logic 1 when the same 010, 100, 101, 110 or 111 pattern is detected in bits 5, 6 and 7 of the G1 byte for five or ten consecutive frames (selectable with the PRDI10 register bit). PERDIV is set to logic 0 when the same 000, 001 or 011 pattern is detected in bits 5, 6 and 7 of the G1 byte for five or ten consecutive frames.

Register 128CH, 168CH, 1A8CH and 1E8CH: TAPI Error Monitor Interrupt Enable (STS1/STM0 #1)
Register 1294H, 1694H, 1A94H and 1E94H: TAPI Error Monitor Interrupt Enable (STS1/STM0 #2)
Register 129CH, 169CH, 1A9CH and 1E9CH: TAPI Error Monitor Interrupt Enable (STS1/STM0 #3)
Register 12A4H, 16A4H, 1AA4H and 1EA4H: TAPI Error Monitor Interrupt Enable (STS1/STM0 #4)
Register 12ACH, 16ACH, 1AACH and 1EACH: TAPI Error Monitor Interrupt Enable (STS1/STM0 #5)
Register 12B4H, 16B4H, 1AB4H and 1EB4H: TAPI Error Monitor Interrupt Enable (STS1/STM0 #6)
Register 12BCH, 16BCH, 1ABCH and 1EBCH: TAPI Error Monitor Interrupt Enable (STS1/STM0 #7)
Register 12C4H, 16C4H, 1AC4H and 1EC4H: TAPI Error Monitor Interrupt Enable (STS1/STM0 #8)
Register 12CCH, 16CCH, 1ACCH and 1ECCH: TAPI Error Monitor Interrupt Enable (STS1/STM0 #9)
Register 12D4H, 16D4H, 1AD4H and 1ED4H: TAPI Error Monitor Interrupt Enable (STS1/STM0 #10)
Register 12DCH, 16DCH, 1ADCH and 1EDCH: TAPI Error Monitor Interrupt Enable (STS1/STM0 #11)
Register 12E4H, 16E4H, 1AE4H and 1EE4H: TAPI Error Monitor Interrupt Enable (STS1/STM0 #12)

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9	R/W	PREIEE	0
Bit 8	R/W	PBIPEE	0
Bit 7	R/W	COPERDIE	0
Bit 6	R/W	PERDIE	0
Bit 5	R/W	PRDIE	0
Bit 4	R/W	PPDIE	0
Bit 3	R/W	PUNEQE	0
Bit 2	R/W	PPLME	0
Bit 1	R/W	PPLUE	0
Bit 0	R/W	COPSLE	0

The Error Monitor Interrupt Enable Register is provided at TAPI r/w address 0CH 14H 1CH 24H 2CH 34H 3CH 44H 4CH 54H 5CH and 64H.

COPSLE

The change of path payload signal label interrupt enable (COPSLE) bit controls the activation of the interrupt output. When COPSLE is set to logic 1, the COPSLI pending interrupt will assert the interrupt output. When COPSLE is set to logic 0, the COPSLI pending interrupt will not assert the interrupt output.

PPLUE

The path payload label unstable interrupt enable (PPLUE) bit controls the activation of the interrupt output. When PPLUE is set to logic 1, the PPLUI pending interrupt will assert the interrupt output. When PPLUE is set to logic 0, the PPLUI pending interrupt will not assert the interrupt output.

PPLME

The path payload label mismatch interrupt enable (PPLME) bit controls the activation of the interrupt output. When PPLME is set to logic 1, the PPLMI pending interrupt will assert the interrupt output. When PPLME is set to logic 0, the PPLMI pending interrupt will not assert the interrupt output.

PUNEQE

The path payload unequipped interrupt enable (PUNEQE) bit controls the activation of the interrupt output. When PUNEQE is set to logic 1, the PUNEQI pending interrupt will assert the interrupt output. When PUNEQE is set to logic 0, the PUNEQI pending interrupt will not assert the interrupt output.

PPDIE

The path payload defect indication interrupt enable (PPDIE) bit controls the activation of the interrupt output. When PPDIE is set to logic 1, the PPDI pending interrupt will assert the interrupt output. When PPDIE is set to logic 0, the PPDI pending interrupt will not assert the interrupt output.

PRDIE

The path remote defect indication interrupt enable (PRDIE) bit controls the activation of the interrupt output. When PRDIE is set to logic 1, the PRDII pending interrupt will assert the interrupt output. When PRDIE is set to logic 0, the PRDII pending interrupt will not assert the interrupt output.

PERDIE

The path enhanced remote defect indication interrupt enable (PERDIE) bit controls the activation of the interrupt output. When PERDIE is set to logic 1, the PERDII pending interrupt will assert the interrupt output. When PERDIE is set to logic 0, the PERDII pending interrupt will not assert the interrupt output.

COPERDIE

The change of path enhanced remote defect indication interrupt enable (COPERDIE) bit controls the activation of the interrupt output. When COPERDIE is set to logic 1, the COPERDII pending interrupt will assert the interrupt output. When COPERDIE is set to logic 0, the COPERDII pending interrupt will not assert the interrupt output.

PBIPEE

The path BIP-8 error interrupt enable (PBIPEE) bit controls the activation of the interrupt output. When PBIPEE is set to logic 1, the PBIPEI pending interrupt will assert the interrupt output. When PBIPEE is set to logic 0, the PBIPEI pending interrupt will not assert the interrupt output.

PREIEE

The path REI error interrupt enable (PREIEE) bit controls the activation of the interrupt output. When PREIEE is set to logic 1, the PREIEI pending interrupt will assert the interrupt output. When PREIEE is set to logic 0, the PREIEI pending interrupt will not assert the interrupt output.

Register 128DH, 168DH, 1A8DH and 1E8DH: TAPI Error Monitor Interrupt Status (STS1/STM0 #1)
Register 1295H, 1695H, 1A95H and 1E95H: TAPI Error Monitor Interrupt Status (STS1/STM0 #2)
Register 129DH, 169DH, 1A9DH and 1E9DH: TAPI Error Monitor Interrupt Status (STS1/STM0 #3)
Register 12A5H, 16A5H, 1AA5H and 1EA5H: TAPI Error Monitor Interrupt Status (STS1/STM0 #4)
Register 12ADH, 16ADH, 1AADH and 1EADH: TAPI Error Monitor Interrupt Status (STS1/STM0 #5)
Register 12B5H, 16B5H, 1AB5H and 1EB5H: TAPI Error Monitor Interrupt Status (STS1/STM0 #6)
Register 12BDH, 16BDH, 1ABDH and 1EBDH: TAPI Error Monitor Interrupt Status (STS1/STM0 #7)
Register 12C5H, 16C5H, 1AC5H and 1EC5H: TAPI Error Monitor Interrupt Status (STS1/STM0 #8)
Register 12CDH, 16CDH, 1ACDH and 1ECDH: TAPI Error Monitor Interrupt Status (STS1/STM0 #9)
Register 12D5H, 16D5H, 1AD5H and 1ED5H: TAPI Error Monitor Interrupt Status (STS1/STM0 #10)
Register 12DDH, 16DDH, 1ADDH and 1EDDH: TAPI Error Monitor Interrupt Status (STS1/STM0 #11)
Register 12E5H, 16E5H, 1AE5H and 1EE5H: TAPI Error Monitor Interrupt Status (STS1/STM0 #12)

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9	R	PREIEI	X
Bit 8	R	PBIPEI	X
Bit 7	R	COPERDII	X
Bit 6	R	PERDII	X
Bit 5	R	PRDII	X
Bit 4	R	PPDII	X
Bit 3	R	PUNEQI	X
Bit 2	R	PPLMI	X
Bit 1	R	PPLUI	X
Bit 0	R	COPSLI	X

The Error Monitor Interrupt Status Register is provided at TAPI r/w address 0DH 15H 1DH 25H 2DH 35H 3DH 45H 4DH 55H 5DH and 65H.

COPSLI

The change of path payload signal label interrupt status (COPSLI) bit is an event indicator. COPSLI is set to logic 1 to indicate a new PSL-P value. The interrupt status bit is independent of the interrupt enable bit. COPSLI is cleared to logic 0 when this register is read. ALGO2 register bit has no effect on COPSLI.

PPLUI

The path payload label unstable interrupt status (PPLUI) bit is an event indicator. PPLUI is set to logic 1 to indicate any change in the status of PPLUV (stable to unstable or unstable to stable). The interrupt status bit is independent of the interrupt enable bit. PPLUI is cleared to logic 0 when this register is read.

PPLMI

The path payload label mismatch interrupt status (PPLMI) bit is an event indicator. PPLMI is set to logic 1 to indicate any change in the status of PPLMV (match to mismatch or mismatch to match). The interrupt status bit is independent of the interrupt enable bit. PPLMI is cleared to logic 0 when this register is read.

PUNEQI

The path payload unequipped interrupt status (PUNEQI) bit is an event indicator. PUNEQI is set to logic 1 to indicate any change in the status of PUNEQV (equipped to unequipped or unequipped to equipped). The interrupt status bit is independent of the interrupt enable bit. PUNEQI is cleared to logic 0 when this register is read.

PPDII

The path payload defect indication interrupt status (PPDII) bit is an event indicator. PPDII is set to logic 1 to indicate any change in the status of PPDIV (no defect to payload defect or payload defect to no defect). The interrupt status bit is independent of the interrupt enable bit. PPDII is cleared to logic 0 when this register is read.

PRDII

The path remote defect indication interrupt status (PRDII) bit is an event indicator. PRDII is set to logic 1 to indicate any change in the status of PRDIV (no defect to RDI defect or RDI defect to no defect). The interrupt status bit is independent of the interrupt enable bit. PRDII is cleared to logic 0 when this register is read.

PERDII

The path enhanced remote defect indication interrupt status (PERDII) bit is an event indicator. PERDII is set to logic 1 to indicate any change in the status of PERDIV (no defect to ERDI defect or ERDI defect to no defect). The interrupt status bit is independent of the interrupt enable bit. PERDII is cleared to logic 0 when this register is read.

COPERDII

The change of path enhanced remote defect indication interrupt status (COPERDII) bit is an event indicator. COPERDII is set to logic 1 to indicate a new ERDI-P value. The interrupt status bit is independent of the interrupt enable bit. COPERDII is cleared to logic 0 when this register is read.

PBIPEI

The path BIP-8 error interrupt status (PBIPEI) bit is an event indicator. PBIPEI is set to logic 1 to indicate a path BIP-8 error. The interrupt status bit is independent of the interrupt enable bit. PBIPEI is cleared to logic 0 when this register is read.

PREIEI

The path REI error interrupt status (PREIEI) bit is an event indicator. PREIEI is set to logic 1 to indicate a path REI error. The interrupt status bit is independent of the interrupt enable bit. PREIEI is cleared to logic 0 when this register is read.

Indirect Register 00H: TAPI Pointer Interpreter Configuration

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9		Unused	
Bit 8		Unused	
Bit 7	R/W	Reserved	0
Bit 6	R/W	TAPIBYPASS	0
Bit 5	R/W	NDFCNT	0
Bit 4	R/W	INVCNT	0
Bit 3	R/W	RELAYPAIS	0
Bit 2	R/W	JUST3DIS	0
Bit 1	R/W	SSEN	0
Bit 0		Unused	

The Pointer Interpreter Configuration Indirect Register is provided at TAPI r/w indirect address 00H.

SSEN

The SS bits enable (SSEN) bit selects whether or not the SS bits are taking into account in the pointer interpreter state machine. When SSEN is set to logic 1, the SS bits must be set to 10 for a valid NORM_POINT, NDF_ENABLE, INC_IND, DEC_IND or NEW_POINT indication. When SSEN is set to logic 0, the SS bits are ignored.

JUST3DIS

The “justification more than 3 frames ago disable” (JUST3DIS) bit selects whether or not the NDF_ENABLE, INC_IND or DEC_IND pointer justifications must be more than 3 frames apart to be considered valid. When JUST3DIS is set to logic 0, the previous NDF_ENABLE, INC_IND or DEC_IND indication must be more than 3 frames ago or the present NDF_ENABLE, INC_IND or DEC_IND indication is considered an INV_POINT indication. When JUST3DIS is set to logic 1, NDF_ENABLE, INC_IND or DEC_IND indication can be every frame.

RELAYPAIS

The relay path AIS (RELAYPAIS) bit selects the condition to enter the path AIS state in the pointer interpreter state machine. When RELAYPAIS is set to logic 1, the path AIS state is entered with 1 X AIS_ind indication. When RELAYPAIS is set to logic 0, the path AIS state is entered with 3 X AIS_ind indications. This configuration bit also affects the concatenation pointer interpreter state machine.

INVCNT

The invalid counter (INVCNT) bit selects the behavior of the consecutive INV_POINT event counter in the pointer interpreter state machine. When INVCNT is set to logic 1, the consecutive INV_POINT event counter is reset by 3 EQ_NEW_POINT indications. When INVCNT is set to logic 0, the counter is not reset by 3 EQ_NEW_POINT indications.

NDFCNT

The new data flag counter (NDFCNT) bit selects the behavior of the consecutive NDF_ENABLE event counter in the pointer interpreter state machine. When NDFCNT is set to logic 1, the NDF_ENABLE definition is enabled NDF + SS. When NDFCNT is set to logic 0, the NDF_ENABLE definition is enabled NDF + SS + offset value in the range 0 to 782 (764 in TU-3 mode). This configuration bit only changes the NDF_ENABLE definition for the consecutive NDF_ENABLE even counter to count towards LOP-P defect when the pointer is out of range, this configuration bit does not change the NDF_ENABLE definition for pointer justification.

TAPIBYPASS

The transmit add bus pointer interpreter bypass (TAPIBYPASS) bit disables the pointer interpreter on a per STS-1/STM-0 basis. When a logic 1 is written to TAPIBYPASS, the add bus pointer interpreter is disable for the corresponding STS-1/STM-0. When a logic 0 is written to TAPIBYPASS, the add bus pointer interpreter is enable for the corresponding STS-1/STM-0.

Indirect Register 01H: TAPI Error Monitor Configuration

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11	R/W	Reserved	0
Bit 10	R/W	IPREIBLK	0
Bit 9	R/W	IBER	0
Bit 8	R/W	PREIBLKACC	0
Bit 7	R/W	Reserved	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	PBIPEBLKACC	0
Bit 4	R/W	FSBIPDIS	0
Bit 3	R/W	PRDI10	0
Bit 2	R/W	PLMEND	0
Bit 1	R/W	PSL5	0
Bit 0	R/W	ALGO2	0

The Error Monitor Configuration Indirect Register is provided at TAPI r/w indirect address 01H.

ALGO2

The payload signal label algorithm 2 (ALGO2) bit selects the algorithm for the PSL monitoring. When ALGO2 is set to logic 1, the ITU compliant algorithm is (algorithm 2) is used to monitor the PSL. When ALGO2 is set to logic 0, the BELLCORE compliant algorithm (algorithm 1) is used to monitor the PSL. ALGO2 changes the PLU-P, PLM-P and PDI-P defect definitions but has no effect on UNEQ-P defect, accepted PSL and change of PSL definitions

PSL5

The payload signal label detection (PSL5) bit selects the path PSL persistence. When PSL5 is set to logic 1, a new PSL is accepted when the same PSL value is detected in the C2 byte for five consecutive frames. When PSL5 is set to logic 0, a new PSL is accepted when the same PSL value is detected in the C2 byte for three consecutive frames.

PLMEND

The payload label mismatch removal (PLMEND) bit controls the removal of a PLM-P defect when an UNEQ-P defect is declared. When PLMEND is set to logic 1, a PLM-P defect is terminated when an UNEQ-P defect is declared. When PLMEND is set to logic 0, a PLM-P defect is not terminated when an UNEQ-P defect is declared.

PRDI10

The path remote defect indication detection (PRDI10) bit selects the path RDI and path ERDI persistence. When PRDI10 is set to logic 1, path RDI and path ERDI are accepted when the same pattern is detected in bits 5,6,7 of the G1 byte for ten consecutive frames. When PRDI10 is set to logic 0, path RDI and path ERDI are accepted when the same pattern is detected in bits 5,6,7 of the G1 byte for five consecutive frames.

FSBIPDIS

The disable fixed stuff columns during BIP-8 calculation (FSBIPDIS) bit controls the path BIP-8 calculation for an STS-1 (VC-3) payload. When FSBIPDIS is set to logic 1, the fixed stuff columns are not part of the BIP-8 calculation when processing an STS-1 (VC-3) payload. When FSBIPDIS is set to logic 0, the fixed stuff columns are part of the BIP-8 calculation when processing an STS-1 (VC-3) payload.

PBIPEBLKACC

The path block BIP-8 errors accumulation (PBIPEBLKACC) bit controls the accumulation of path BIP-8 errors. When PBIPEBLKACC is set to logic 1, the path BIP-8 error accumulation represents block BIP-8 errors (a maximum of 1 error per frame). When PBIPEBLKACC is set to logic 0, the path BIP-8 error accumulation represents BIP-8 errors (a maximum of 8 errors per frame).

PREIBLKACC

The path block REI errors accumulation (PREIBLKACC) bit controls the accumulation of path REI errors from the path status (G1) byte. When PREIBLK is set to logic 1, the extracted path REI errors are interpreted as block BIP-8 errors (a maximum of 1 error per frame). When PREIBLK is set to logic 0, the extracted path REI errors are interpret as BIP-8 errors (a maximum of 8 errors per frame).

IBER

The inband error reporting (IBER) bit controls the inband regeneration of the path status (G1) byte. When IBER is set to logic 1, the path status byte is updated with the REI-P and the ERDI-P defects that must be returned to the far end. When IBER is set to logic 0, the path status byte is not altered.

IPREIBLK

The inband path REI block errors (IPREIBLK) bit controls the regeneration of the path REI errors in the path status (G1) byte. When IPREIBLK is set to logic 1, the path REI is updated with block BIP-8 errors (a maximum of 1 error per frame). When IPREIBLK is set to logic 0, the path REI is updated with BIP-8 errors (a maximum of 8 errors per frame).

Indirect Register 02H: TAPI Pointer Value and ERDI

Bit	Type	Function	Default
Bit 15	R	PERDIV[2]	X
Bit 14	R	PERDIV[1]	X
Bit 13	R	PERDIV[0]	X
Bit 12		Unused	
Bit 11	R	SSV[1]	X
Bit 10	R	SSV[0]	X
Bit 9	R	PTRV[9]	X
Bit 8	R	PTRV[8]	X
Bit 7	R	PTRV[7]	X
Bit 6	R	PTRV[6]	X
Bit 5	R	PTRV[5]	X
Bit 4	R	PTRV[4]	X
Bit 3	R	PTRV[3]	X
Bit 2	R	PTRV[2]	X
Bit 1	R	PTRV[1]	X
Bit 0	R	PTRV[0]	X

The Pointer Value Indirect Register is provided at TAPI r/w address 02H.

PTRV[9:0]

The path pointer value (PTRV[9:0]) bits represent the current STS (AU or TU3) pointer being process by the pointer interpreter state machine or by the concatenation pointer interpreter state machine.

SSV[1:0]

The SS value (SSV[1:0]) bits represent the current SS (DD) bits being processed by the pointer interpreter state machine or by the concatenation pointer interpreter state machine.

PERDIV[2:0]

The path enhanced remote defect indication value (PERDIV[2:0]) bits represent the filtered path enhanced remote defect indication value. PERDIV[2:0] is updated when the same ERDI pattern is detected in bits 5,6,7 of the G1 byte for five or ten consecutive frames (selectable with the PRDI10 register bit).

Indirect Register 03H: TAPI Captured and Accepted PSL

Bit	Type	Function	Default
Bit 15	R	CPSLV[7]	X
Bit 14	R	CPSLV[6]	X
Bit 13	R	CPSLV[5]	X
Bit 12	R	CPSLV[4]	X
Bit 11	R	CPSLV[3]	X
Bit 10	R	CPSLV[2]	X
Bit 9	R	CPSLV[1]	X
Bit 8	R	CPSLV[0]	X
Bit 7	R	APSLV[7]	X
Bit 6	R	APSLV[6]	X
Bit 5	R	APSLV[5]	X
Bit 4	R	APSLV[4]	X
Bit 3	R	APSLV[3]	X
Bit 2	R	APSLV[2]	X
Bit 1	R	APSLV[1]	X
Bit 0	R	APSLV[0]	X

The Accepted PSL and ERDI Indirect Register is provided at TAPI r/w address 03H.

APSLV[7:0]

The accepted path signal label value (APSLV[7:0]) bits represent the last accepted path signal label value. A new PSL is accepted when the same PSL value is detected in the C2 byte for three or five consecutive frames. (selectable with the PSL5 register bit).

CPSLV[7:0]

The captured path signal label value (CPSLV[7:0]) bits represent the last captured path signal label value. A new PSL is captured every frame from the C2 byte.

Indirect Register 04H: TAPI Expected PSL and PDI

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13	R/W	PDIRANGE	0
Bit 12	R/W	PDI[4]	0
Bit 11	R/W	PDI[3]	0
Bit 10	R/W	PDI[2]	0
Bit 9	R/W	PDI[1]	0
Bit 8	R/W	PDI[0]	0
Bit 7	R/W	EPSL[7]	0
Bit 6	R/W	EPSL[6]	0
Bit 5	R/W	EPSL[5]	0
Bit 4	R/W	EPSL[4]	0
Bit 3	R/W	EPSL[3]	0
Bit 2	R/W	EPSL[2]	0
Bit 1	R/W	EPSL[1]	0
Bit 0	R/W	EPSL[0]	0

The Expected PSL and PDI Indirect Register is provided at TAPI r/w indirect address 04H.

EPSL[7:0]

The expected path signal label (EPSL[7:0]) bits represent the expected path signal label. The expected PSL and the expected PDI validate the received or the accepted PSL to declare PLM-P, UNEQ-P and PDI-P defects according Table 3.

PDI[4:0], PDIRANGE

The payload defect indication (PDI[4:0]) bits and the payload defect indication range (PDIRANGE) bit determine the expected payload defect indication according to Table 4. When PDIRANGE is set to logic 1, the PDI range is enabled and the expected PDI range is from E1H to E0H+PDI[4:0]. When PDIRANGE is set to logic 0, the PDI range is disable and the expected PDI value is E0H+PDI[4:0]. The expected PSL and the expected PDI validate the received or the accepted PSL to declare PLM-P, UNEQ-P and PDI-P defects according Table 3.

Indirect Register 05H: TAPI Pointer Interpreter Status

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9		Unused	
Bit 8		Unused	
Bit 7		Unused	
Bit 6	R	NDF	X
Bit 5	R	ILLPTR	X
Bit 4	R	INVNDF	X
Bit 3	R	DISCOPA	X
Bit 2	R	CONCAT	X
Bit 1	R	ILLJREQ	X
Bit 0		Unused	

The Pointer Interpreter Status Indirect Register is provided at TAPI r/w indirect address 05H.

Note: The Pointer Interpreter Status bits are don’t care for slave time slots.

ILLJREQ

The illegal pointer justification request (ILLJREQ) signal is set high when a positive and/or negative pointer adjustment is received within three frames of a pointer justification event (inc_ind, dec_ind) or an NDF triggered active offset adjustment (NDF_enable).

CONCAT

The CONCAT bit is set high if the H1 and H2 pointer bytes received matche the concatenation indication (one of the five NDF_enable patterns in the NDF field, don't care in the size field, and all-ones in the pointer offset field).

DISCOPA

The discontinuous change of pointer alignment (DISCOPA) signal is set high when there is a pointer adjustment due to receiving a pointer repeated three times.

INVNDF

The invalid new data flag (INVNDF) signal is set high when an invalid NDF code is received.

ILLPTR

The illegal pointer offset (ILLPTR) signal is set high when the pointer received is out of the range. Legal values are from 0 to 782 (764 in TU3 mode). Pointer justification requests (inc_req, dec_req) and AIS indications (AIS_ind) are not considered illegal.

NDF

The new data flag (NDF) signal is set high when an enabled New Data Flag is received indicating a pointer adjustment (NDF_enabled indication).

Indirect Register 06H: TAPI Path BIP Error Counter

Bit	Type	Function	Default
Bit 15	R	PBIPE[15]	X
Bit 14	R	PBIPE[14]	X
Bit 13	R	PBIPE[13]	X
Bit 12	R	PBIPE[12]	X
Bit 11	R	PBIPE[11]	X
Bit 10	R	PBIPE[10]	X
Bit 9	R	PBIPE[9]	X
Bit 8	R	PBIPE[8]	X
Bit 7	R	PBIPE[7]	X
Bit 6	R	PBIPE[6]	X
Bit 5	R	PBIPE[5]	X
Bit 4	R	PBIPE[4]	X
Bit 3	R	PBIPE[3]	X
Bit 2	R	PBIPE[2]	X
Bit 1	R	PBIPE[1]	X
Bit 0	R	PBIPE[0]	X

The is Path BIP Error Counter register is provided at TAPI r/w indirect address 06H.

PBIPE[15:0]

The path BIP error (PBIPE[15:0]) bits represent the number of path BIP errors that have been detected in the B3 byte since the last accumulation interval. The error counters are transferred to the holding registers by a microprocessor write to the RHPP Counters Update register.

Indirect Register 07H: TAPI Path REI Error Counter

Bit	Type	Function	Default
Bit 15	R	PREIE[15]	X
Bit 14	R	PREIE[14]	X
Bit 13	R	PREIE[13]	X
Bit 12	R	PREIE[12]	X
Bit 11	R	PREIE[11]	X
Bit 10	R	PREIE[10]	X
Bit 9	R	PREIE[9]	X
Bit 8	R	PREIE[8]	X
Bit 7	R	PREIE[7]	X
Bit 6	R	PREIE[6]	X
Bit 5	R	PREIE[5]	X
Bit 4	R	PREIE[4]	X
Bit 3	R	PREIE[3]	X
Bit 2	R	PREIE[2]	X
Bit 1	R	PREIE[1]	X
Bit 0	R	PREIE[0]	X

The is Path BIP Error Counter register is provided at TAPI r/w indirect address 07H.

PREIE[15:0]

The path REI error (PREIE[15:0]) bits represent the number of path REI errors that have been extracted from the G1 byte since the last accumulation interval. The error counters are transferred to the holding registers by a microprocessor write to the RHPP Counters Update register.

Indirect Register 08H: TAPI Path Negative Justification Event Counter

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12	R	PNJE[12]	X
Bit 11	R	PNJE[11]	X
Bit 10	R	PNJE[10]	X
Bit 9	R	PNJE[9]	X
Bit 8	R	PNJE[8]	X
Bit 7	R	PNJE[7]	X
Bit 6	R	PNJE[6]	X
Bit 5	R	PNJE[5]	X
Bit 4	R	PNJE[4]	X
Bit 3	R	PNJE[3]	X
Bit 2	R	PNJE[2]	X
Bit 1	R	PNJE[1]	X
Bit 0	R	PNJE[0]	X

The is Path Negative Justification Event Counter register is provided at TAPI r/w indirect address 08H.

PNJE[12:0]

The Path Negative Justification Event (PNJE[12:0]) bits represent the number of Path Negative Justification Events that have occurred since the last accumulation interval. The event counters are transferred to the holding registers by a microprocessor write to RHPP Counters Update register.

Indirect Register 09H: TAPI Path Positive Justification Event Counter

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12	R	PPJE[12]	X
Bit 11	R	PPJE[11]	X
Bit 10	R	PPJE[10]	X
Bit 9	R	PPJE[9]	X
Bit 8	R	PPJE[8]	X
Bit 7	R	PPJE[7]	X
Bit 6	R	PPJE[6]	X
Bit 5	R	PPJE[5]	X
Bit 4	R	PPJE[4]	X
Bit 3	R	PPJE[3]	X
Bit 2	R	PPJE[2]	X
Bit 1	R	PPJE[1]	X
Bit 0	R	PPJE[0]	X

The is Path Positive Justification Event Counter register is provided at TAPI r/w indirect address 09H.

PPJE[12:0]

The Path Positive Justification Event (PPJE[12:0]) bits represent the number of Path Positive Justification Events that have occurred since the last accumulation interval. The event counters are transferred to the holding registers by a microprocessor write to RHPP Counters Update register.

Register 1302H: ADLL Reset

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9		Unused	
Bit 8		Unused	
Bit 7		Unused	
Bit 6		Unused	
Bit 5		Unused	
Bit 4		Unused	
Bit 3		Unused	
Bit 2		Unused	
Bit 1		Unused	
Bit 0		Unused	

Any write to the ADLL Reset Register will reset the Add Bus DLL

12 Test Features Description

Simultaneously asserting (low) the CSB, RDB and WRB inputs causes all digital output pins and the data bus to be held in a high-impedance state. This test feature may be used for board testing.

Test mode registers are used to apply test vectors during production testing of the SPECTRA-2488. Test mode registers (as opposed to normal mode registers) are selected when TRS (A[13]) is high.

Test mode registers may also be used for board testing. When all of the TSBs within the SPECTRA-2488 are placed in test mode 0, device inputs may be read and device outputs may be forced via the microprocessor interface (refer to the section "Test Mode 0" for details).

In addition, the SPECTRA-2488 also supports a standard IEEE 1149.1 five-signal JTAG boundary scan test port for use in board testing. All digital device inputs may be read and all digital device outputs may be forced via the JTAG test port.

Table 12 Test Mode Register Memory Map

Address	Register
0000H-1FFFH	Normal Mode Registers
2000	Master Test Register
2001	Test Mode Address Force Enable
2002	Test Mode Address Force Value
2003	RX Analog Test Mode Bus
2004	RX Analog Test Mode Bus
2005	TX Analog Test Mode Bus
2006	TX Analog Test Mode Bus
2007	Analog TIN Bus
2008-3FFF	Reserved For Test

12.1 Master Test and Test Configuration Registers

Notes on Test Mode Register Bits

1. Writing values into unused register bits has no effect. However, to ensure software compatibility with future, feature-enhanced versions of the product, unused register bits must be written with logic zero. Reading back unused bits can produce either a logic one or a logic zero; hence, unused register bits should be masked off by software when read.

2. Writable test mode register bits are not initialized upon reset unless otherwise noted.

Register 2000H: SPECTRA-2488 Master Test

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6		Unused	
Bit 5	R/W	PMCATST	X
Bit 4	R/W	PMCTST	X
Bit 3	R/W	DBCTRL	0
Bit 1	R/W	IOTST	0
Bit 1	R/W	HIZDATA	0
Bit 0	R/W	HIZIO	0

This register is used to enable SPECTRA-2488 test features. All bits, except PMCTST and PMCATST are reset to zero by a reset of the SPECTRA-2488 using the RSTB input. PMCTST and PMCATST are reset when CSB is logic 1. PMCTST and PMCATST can also be reset by writing a logic 0 to the corresponding register bit.

Access to this register is not affected by the Test Mode Address Force functions in registers 2001H and 2002H.

HIZIO, HIZDATA

The HIZIO and HIZDATA bits control the tri-state modes of the SPECTRA-2488. While the HIZIO bit is a logic one, all output pins of the SPECTRA-2488 except the data bus and output TDO are held tri-state. The microprocessor interface is still active. While the HIZDATA bit is a logic one, the data bus is also held in a high-impedance state which inhibits microprocessor read cycles. The HIZDATA bit is overridden by the DBCTRL bit.

IOTST

The IOTST bit is used to allow normal microprocessor access to the test registers and control the test mode in each TSB block in the SPECTRA-2488 for board level testing. When IOTST is a logic 1, all blocks are held in test mode and the microprocessor may write to a block's test mode 0 registers to manipulate the outputs of the block and consequently the device outputs (refer to the "Test Mode 0 Details" in the "Test Features" section).

DBCTRL

The DBCTRL bit is used to pass control of the data bus drivers to the CSB pin. When the DBCTRL bit is set to logic one and PMCTST is set to logic one, the CSB pin controls the output enable for the data bus. While the DBCTRL bit is set, holding the CSB pin high causes the SPECTRA-2488 to drive the data bus and holding the CSB pin low tri-states the data bus. The DBCTRL bit overrides the HIZDATA bit. The DBCTRL bit is used to measure the drive capability of the data bus driver pads.

PMCTST

The PMCTST bit is used to configure the SPECTRA-2488 for PMC's manufacturing tests. When PMCTST is set to logic one, the SPECTRA-2488 microprocessor port becomes the test access port used to run the PMC "canned" manufacturing test vectors. The PMCTST can be cleared by setting CSB to logic one or by writing logic zero to the bit.

PMCATST

The PMCATST bit is used to configure the analog portion of the SPECTRA-2488 for PMC's manufacturing tests. The PMCATST can be cleared by setting CSB to logic one or by writing logic zero to the bit.

Register 2001H: SPECTRA-2488 Test Mode Address Force Enable

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 1		Unused	X
Bit 1		Unused	X
Bit 0	R/W	TM_A_EN	X

This register is used to force the address pins to a certain value. These bits are valid when either PMCTST or IOTST is set to logic 1. The TM_A[X] bit is forced when TM_A_EN is logic 1. Otherwise, the A[X] pin is used.

Access to this register is not affected by the Test Mode Address Force functions in registers 2001H and 2002H.

TM_A_EN

When TM_A_EN is logic 1 and either PMCTST or IOTST is logic 1, the TM_A[X] register bit replaces the input pin A[X]. Like PMCTST and PMCATST, TM_A_EN bits are cleared only when CSB is logic 1 or when they are written to logic 0.

Register 2002H: SPECTRA-2488 Test Mode Address Force Value

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 1		Unused	X
Bit 1	R/W	TM_A[11]	X
Bit 0	R/W	TM_A[10]	X

This register is used to force the address pins to a certain value. These bits are valid when either PMCTST or IOTST is set to logic 1. The TM_A[X] bit is forced when TM_A_EN is logic 1. Otherwise, the A[X] pin is used.

Access to this register is not affected by the Test Mode Address Force functions in registers 2001H and 2002H.

TM_A[11:10]

When TM_A_EN is logic 1 and either PMCTST or IOTST is logic 1, the TM_A[X] bit replaces the input pin A[X]. Like PMCTST and PMCATST, TM_A[X] bits are cleared only when CSB is logic 1 or when they are written to logic 0.

Register 2003H: SPECTRA-2448 RX Analog Test Mode Bus

Bit	Type	Function	Default
Bit 15	R/W	TM_RX[15]	X
Bit 14	R/W	TM_RX[14]	X
Bit 13	R/W	TM_RX[13]	X
Bit 12	R/W	TM_RX[12]	X
Bit 11	R/W	TM_RX[11]	X
Bit 10	R/W	TM_RX[10]	X
Bit 9	R/W	TM_RX[9]	X
Bit 8	R/W	TM_RX[8]	X
Bit 7	R/W	TM_RX[7]	X
Bit 6	R/W	TM_RX[6]	X
Bit 5	R/W	TM_RX[5]	X
Bit 4	R/W	TM_RX[4]	X
Bit 3	R/W	TM_RX[3]	X
Bit 1	R/W	TM_RX[2]	X
Bit 1	R/W	TM_RX[1]	X
Bit 0	R/W	TM_RX[0]	X

This register is used to enable test mode in the analog blocks. These bits are valid when PMCATST is set to logic 1.

Access to this register is not affected by the Test Mode Address Force functions in registers 2001H and 2002H.

TM_RX[15:0]

When TM_RX[X] and PMCATST are logic 1, the analog PECL receiver is configured for its manufacturing test mode. Like PMCTST and PMCATST, TM_RX[X] bits are cleared only when CSB is logic 1 or when they are written to logic 0.

Register 2004H: SPECTRA-2448 RX Analog Test Mode Bus

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9		Unused	
Bit 8		Unused	
Bit 7		Unused	
Bit 6		Unused	
Bit 5		Unused	
Bit 4		Unused	
Bit 3	R/W	TM_RX[19]	X
Bit 1	R/W	TM_RX[18]	X
Bit 1	R/W	TM_RX[17]	X
Bit 0	R/W	TM_RX[16]	X

This register is used to enable test mode in the analog blocks. These bits are valid when PMCATST is set to logic 1.

Access to this register is not affected by the Test Mode Address Force functions in registers 2001H and 2002H.

TM_RX[19:16]

When TM_RX[X] and PMCATST are logic 1, the analog PECL receiver is configured for its manufacturing test mode. Like PMCTST and PMCATST, TM_RX[X] bits are cleared only when CSB is logic 1 or when they are written to logic 0.

Register 2005H: SPECTRA-2448 TX Analog Test Mode Bus

Bit	Type	Function	Default
Bit 15	R/W	TM_TX[15]	X
Bit 14	R/W	TM_TX[14]	X
Bit 13	R/W	TM_TX[13]	X
Bit 12	R/W	TM_TX[12]	X
Bit 11	R/W	TM_TX[11]	X
Bit 10	R/W	TM_TX[10]	X
Bit 9	R/W	TM_TX[9]	X
Bit 8	R/W	TM_TX[8]	X
Bit 7	R/W	TM_TX[7]	X
Bit 6	R/W	TM_TX[6]	X
Bit 5	R/W	TM_TX[5]	X
Bit 4	R/W	TM_TX[4]	X
Bit 3	R/W	TM_TX[3]	X
Bit 1	R/W	TM_TX[2]	X
Bit 1	R/W	TM_TX[1]	X
Bit 0	R/W	TM_TX[0]	X

This register is used to enable test mode in the analog blocks. These bits are valid when PMCATST is set to logic 1.

Access to this register is not affected by the Test Mode Address Force functions in registers 2001H and 2002H.

TM_TX[15:0]

When TM_TX[X] and PMCATST are logic 1, the analog PECL transmitter is configured for its manufacturing test mode. Like PMCTST and PMCATST, TM_TX[X] bits are cleared only when CSB is logic 1 or when they are written to logic 0.

Register 2006H: SPECTRA-2448 TX Analog Test Mode Bus

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9		Unused	
Bit 8		Unused	
Bit 7		Unused	
Bit 6		Unused	
Bit 5		Unused	
Bit 4		Unused	
Bit 3		Unused	
Bit 1	R/W	TM_TX[18]	X
Bit 1	R/W	TM_TX[17]	X
Bit 0	R/W	TM_TX[16]	X

This register is used to enable test mode in the analog blocks. These bits are valid when PMCATST is set to logic 1.

Access to this register is not affected by the Test Mode Address Force functions in registers 2001H and 2002H.

TM_TX[18:16]

When TM_TX[X] and PMCATST are logic 1, the analog PECL transmitter is configured for its manufacturing test mode. Like PMCTST and PMCATST, TM_TX[X] bits are cleared only when CSB is logic 1 or when they are written to logic 0.

Register 2007H: SPECTRA-2448 Analog TIN Bus

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9		Unused	
Bit 8		Unused	
Bit 7		Unused	
Bit 6		Unused	
Bit 5		Unused	
Bit 4		Unused	
Bit 3	R/W	ATIN[3]	X
Bit 1	R/W	ATIN[2]	X
Bit 1	R/W	ATIN[1]	X
Bit 0	R/W	ATIN[0]	X

This register is used to force test input in the analog blocks. These bits are valid when PMCATST is set to logic 1.

Access to this register is not affected by the Test Mode Address Force functions in registers 2001H and 2002H.

ATIN[3:0]

Like PMCTST and PMCATST, ATIN[X] bits are cleared only when CSB is logic 1 or when they are written to logic 0.

12.2 JTAG Test Port

The SPECTRA-2488 JTAG Test Access Port (TAP) allows access to the TAP controller and the 4 TAP registers: instruction, bypass, device identification and boundary scan. Using the TAP, device input logic levels can be read, device outputs can be forced, the device can be identified and the device scan path can be bypassed. For more details on the JTAG port, please refer to the Operations section.

Table 13 Instruction Register (Length - 3 bits)

Instructions	Selected Register	Instruction Codes, IR[2:0]
EXTEST	Boundary Scan	000
IDCODE	Identification	001
SAMPLE	Boundary Scan	010
BYPASS	Bypass	011
BYPASS	Bypass	100
STCTEST	Boundary Scan	101
BYPASS	Bypass	110
BYPASS	Bypass	111

Table 14 Identification Register

Length	32 bits
Version Number	0H
Part Number	5315H
Manufacturer's Identification Code	0CDH
Device Identification	053150CDH

Table 15 Boundary Scan Register

Name	Register Bit	cell Type	Dev ID	Name	Register Bit	cell Type	Dev ID
ADPV[1]	436	IN_CELL	L	TPOHV[1]	217	IN_CELL	-
APAISV[1]	435	IN_CELL	L	TPOHENV[1]	216	IN_CELL	-
OEB_DJ0J1V[1]	434	OUT_CELL	L	OEB_TPOHRDYV[1]	215	OUT_CELL	-
DJ0J1V[1]	433	OUT_CELL	L	TPOHRDYV[1]	214	OUT_CELL	-
OEB_DPLV[1]	432	OUT_CELL	L	OEB_TOHCLKV[2]	213	OUT_CELL	-
DPLV[1]	431	OUT_CELL	H	TOHCLKV[2]	212	OUT_CELL	-
OEB_DD1[0]	430	OUT_CELL	L	OEB_TOHFPV[2]	211	OUT_CELL	-
DD1[0]	429	OUT_CELL	H	TOHFPV[2]	210	OUT_CELL	-
OEB_DD1[1]	428	OUT_CELL	L	TTOHV[2]	209	IN_CELL	-
DD1[1]	427	OUT_CELL	L	TTOHENV[2]	208	IN_CELL	-
OEB_DD1[2]	426	OUT_CELL	H	TPOHV[2]	207	IN_CELL	-
DD1[2]	425	OUT_CELL	H	TPOHENV[2]	206	IN_CELL	-
OEB_DD1[3]	424	OUT_CELL	L	OEB_TPOHRDYV[2]	205	OUT_CELL	-
DD1[3]	423	OUT_CELL	L	TPOHRDYV[2]	204	OUT_CELL	-
OEB_DD1[4]	422	OUT_CELL	L	OEB_TOHCLKV[3]	203	OUT_CELL	-
DD1[4]	421	OUT_CELL	H	TOHCLKV[3]	202	OUT_CELL	-
OEB_DD1[5]	420	OUT_CELL	L	OEB_TOHFPV[3]	201	OUT_CELL	-
DD1[5]	419	OUT_CELL	H	TOHFPV[3]	200	OUT_CELL	-
OEB_DD1[6]	418	OUT_CELL	L	TTOHV[3]	199	IN_CELL	-
DD1[6]	417	OUT_CELL	H	TTOHENV[3]	198	IN_CELL	-
OEB_DD1[7]	416	OUT_CELL	L	TPOHV[3]	197	IN_CELL	-
DD1[7]	415	OUT_CELL	L	TPOHENV[3]	196	IN_CELL	-

OEB_DDPV[1]	414	OUT_CELL	L	OEB_TPOHRDYV[3]	195	OUT_CELL	-
DDPV[1]	413	OUT_CELL	L	TPOHRDYV[3]	194	OUT_CELL	-
OEB_DALARMV[1]	412	OUT_CELL	H	OEB_TOHCLKV[4]	193	OUT_CELL	-
DALARMV[1]	411	OUT_CELL	H	TOHCLKV[4]	192	OUT_CELL	-
AJ0J1_FPV[2]	410	IN_CELL	L	OEB_TOHFPV[4]	191	OUT_CELL	-
APLV[2]	409	IN_CELL	L	TOHFPV[4]	190	OUT_CELL	-
AD2[0]	408	IN_CELL	H	TTOHV[4]	189	IN_CELL	-
AD2[1]	407	IN_CELL	H	TTOHENV[4]	188	IN_CELL	-
AD2[2]	406	IN_CELL	L	TPOHV[4]	187	IN_CELL	-
AD2[3]	405	IN_CELL	H	TPOHENV[4]	186	IN_CELL	-
AD2[4]	404	IN_CELL	-	OEB_TPOHRDYV[4]	185	OUT_CELL	-
AD2[5]	403	IN_CELL	-	TPOHRDYV[4]	184	OUT_CELL	-
AD2[6]	402	IN_CELL	-	OEB_TSLDCLK	183	OUT_CELL	-
AD2[7]	401	IN_CELL	-	TSLDCLK	182	OUT_CELL	-
ADPV[2]	400	IN_CELL	-	TSLD	181	IN_CELL	-
APAISV[2]	399	IN_CELL	-	OEB_TLDCLK	180	OUT_CELL	-
OEB_DJ0J1V[2]	398	OUT_CELL	-	TLDCLK	179	OUT_CELL	-
DJ0J1V[2]	397	OUT_CELL	-	TLD	178	IN_CELL	-
OEB_DPLV[2]	396	OUT_CELL	-	OEB_PGMTCLK	177	OUT_CELL	-
DPLV[2]	395	OUT_CELL	-	PGMTCLK	176	OUT_CELL	-
OEB_DD2[0]	394	OUT_CELL	-	TFPON_TFPI4	175	IN_CELL	-
DD2[0]	393	OUT_CELL	-	TFPOP_TFPI3	174	IN_CELL	-
OEB_DD2[1]	392	OUT_CELL	-	OEB_TCLKV[4]	173	OUT_CELL	-
DD2[1]	391	OUT_CELL	-	TCLKV[4]	172	OUT_CELL	-
OEB_DD2[2]	390	OUT_CELL	-	TDCLKV[4]	171	IN_CELL	-
DD2[2]	389	OUT_CELL	-	TDN0_TD40	170	OUT_CELL	-
OEB_DD2[3]	388	OUT_CELL	-	TDP0_TD41	169	OUT_CELL	-
DD2[3]	387	OUT_CELL	-	TDN1_TD42	168	OUT_CELL	-
OEB_DD2[4]	386	OUT_CELL	-	TDP1_TD43	167	OUT_CELL	-
DD2[4]	385	OUT_CELL	-	TDN2_TD44	166	OUT_CELL	-
OEB_DD2[5]	384	OUT_CELL	-	TDP2_TD45	165	OUT_CELL	-
DD2[5]	383	OUT_CELL	-	TDN3_TD46	164	OUT_CELL	-
OEB_DD2[6]	382	OUT_CELL	-	TDP3_TD47	163	OUT_CELL	-
DD2[6]	381	OUT_CELL	-	OEB_RCLKV[4]	162	OUT_CELL	-
OEB_DD2[7]	380	OUT_CELL	-	RCLKV[4]	161	OUT_CELL	-
DD2[7]	379	OUT_CELL	-	SDV[4]	160	IN_CELL	-
OEB_DDPV[2]	378	OUT_CELL	-	RDCLKV[4]	159	IN_CELL	-
DDPV[2]	377	OUT_CELL	-	TDN4_RD40	158	IN_CELL	-
OEB_DALARMV[2]	376	OUT_CELL	-	TDP4_RD41	157	IN_CELL	-
DALARMV[2]	375	OUT_CELL	-	TDN5_RD42	156	IN_CELL	-
AJ0J1_FPV[3]	374	IN_CELL	-	TDP5_RD43	155	IN_CELL	-
APLV[3]	373	IN_CELL	-	TDN6_RD44	154	IN_CELL	-
AD3[0]	372	IN_CELL	-	TDP6_RD45	153	IN_CELL	-
AD3[1]	371	IN_CELL	-	TDN7_RD46	152	IN_CELL	-
AD3[2]	370	IN_CELL	-	TDP7_RD47	151	IN_CELL	-
AD3[3]	369	IN_CELL	-	OEB_TCLKV[3]	150	OUT_CELL	-
AD3[4]	368	IN_CELL	-	TCLKV[3]	149	OUT_CELL	-
AD3[5]	367	IN_CELL	-	TDCLKV[3]	148	IN_CELL	-
AD3[6]	366	IN_CELL	-	TDN8_TD30	147	OUT_CELL	-
AD3[7]	365	IN_CELL	-	TDP8_TD31	146	OUT_CELL	-
ADPV[3]	364	IN_CELL	-	TDN9_TD32	145	OUT_CELL	-
APAISV[3]	363	IN_CELL	-	TDP9_TD33	144	OUT_CELL	-
OEB_DJ0J1V[3]	362	OUT_CELL	-	TDN10_TD34	143	OUT_CELL	-
DJ0J1V[3]	361	OUT_CELL	-	TDP10_TD35	142	OUT_CELL	-
OEB_DPLV[3]	360	OUT_CELL	-	TDN11_TD36	141	OUT_CELL	-
DPLV[3]	359	OUT_CELL	-	TDP11_TD37	140	OUT_CELL	-
OEB_DD3[0]	358	OUT_CELL	-	OEB_RCLKV[3]	139	OUT_CELL	-
DD3[0]	357	OUT_CELL	-	RCLKV[3]	138	OUT_CELL	-
OEB_DD3[1]	356	OUT_CELL	-	SDV[3]	137	IN_CELL	-
DD3[1]	355	OUT_CELL	-	RDCLKV[3]	136	IN_CELL	-
OEB_DD3[2]	354	OUT_CELL	-	TDN12_RD30	135	IN_CELL	-
DD3[2]	353	OUT_CELL	-	TDP12_RD31	134	IN_CELL	-
OEB_DD3[3]	352	OUT_CELL	-	TDN13_RD32	133	IN_CELL	-
DD3[3]	351	OUT_CELL	-	TDP13_RD33	132	IN_CELL	-
OEB_DD3[4]	350	OUT_CELL	-	TDN14_RD34	131	IN_CELL	-
DD3[4]	349	OUT_CELL	-	TDP14_RD35	130	IN_CELL	-
OEB_DD3[5]	348	OUT_CELL	-	TDN15_RD36	129	IN_CELL	-
DD3[5]	347	OUT_CELL	-	TDP15_RD37	128	IN_CELL	-
OEB_DD3[6]	346	OUT_CELL	-	TFPIN_TFPI2	127	IN_CELL	-
DD3[6]	345	OUT_CELL	-	TFPIP_TFPI1	126	IN_CELL	-
OEB_DD3[7]	344	OUT_CELL	-	OEB_PGMRCLK	125	OUT_CELL	-
DD3[7]	343	OUT_CELL	-	PGMRCLK	124	OUT_CELL	-
OEB_DDPV[3]	342	OUT_CELL	-	OEB_TCLKV[2]	123	OUT_CELL	-
DDPV[3]	341	OUT_CELL	-	TCLKV[2]	122	OUT_CELL	-
OEB_DALARMV[3]	340	OUT_CELL	-	TDCLKV[2]	121	IN_CELL	-
DALARMV[3]	339	OUT_CELL	-	RDN0_TD20	120	OUT_CELL	-
AJ0J1_FPV[4]	338	IN_CELL	-	RDP0_TD21	119	OUT_CELL	-

APLV[4]	337	IN_CELL	-	RDN1_TD22	118	OUT_CELL	-
AD4[0]	336	IN_CELL	-	RDP1_TD23	117	OUT_CELL	-
AD4[1]	335	IN_CELL	-	RDN2_TD24	116	OUT_CELL	-
AD4[2]	334	IN_CELL	-	RDP2_TD25	115	OUT_CELL	-
AD4[3]	333	IN_CELL	-	RDN3_TD26	114	OUT_CELL	-
AD4[4]	332	IN_CELL	-	RDP3_TD27	113	OUT_CELL	-
AD4[5]	331	IN_CELL	-	OEB_RCLKV[2]	112	OUT_CELL	-
AD4[6]	330	IN_CELL	-	RCLKV[2]	111	OUT_CELL	-
AD4[7]	329	IN_CELL	-	SDV[2]	110	IN_CELL	-
ADPV[4]	328	IN_CELL	-	RDCLKV[2]	109	IN_CELL	-
APAISV[4]	327	IN_CELL	-	RDN4_RD20	108	IN_CELL	-
OEB_DJ0J1V[4]	326	OUT_CELL	-	RDP4_RD21	107	IN_CELL	-
DJ0J1V[4]	325	OUT_CELL	-	RDN5_RD22	106	IN_CELL	-
OEB_DPLV[4]	324	OUT_CELL	-	RDP5_RD23	105	IN_CELL	-
DPLV[4]	323	OUT_CELL	-	OEB_TCLKV[1]	104	OUT_CELL	-
OEB_DD4[0]	322	OUT_CELL	-	TCLKV[1]	103	OUT_CELL	-
DD4[0]	321	OUT_CELL	-	TDCLKV[1]	102	IN_CELL	-
OEB_DD4[1]	320	OUT_CELL	-	RDN6_RD24	101	IN_CELL	-
DD4[1]	319	OUT_CELL	-	RDP6_RD25	100	IN_CELL	-
OEB_DD4[2]	318	OUT_CELL	-	RDN7_RD26	99	IN_CELL	-
DD4[2]	317	OUT_CELL	-	RDP7_RD27	98	IN_CELL	-
OEB_DD4[3]	316	OUT_CELL	-	RDN8_TD10	97	OUT_CELL	-
DD4[3]	315	OUT_CELL	-	RDP8_TD11	96	OUT_CELL	-
OEB_DD4[4]	314	OUT_CELL	-	RDN9_TD12	95	OUT_CELL	-
DD4[4]	313	OUT_CELL	-	RDP9_TD13	94	OUT_CELL	-
OEB_DD4[5]	312	OUT_CELL	-	RDN10_TD14	93	OUT_CELL	-
DD4[5]	311	OUT_CELL	-	RDP10_TD15	92	OUT_CELL	-
OEB_DD4[6]	310	OUT_CELL	-	RDN11_TD16	91	OUT_CELL	-
DD4[6]	309	OUT_CELL	-	RDP11_TD17	90	OUT_CELL	-
OEB_DD4[7]	308	OUT_CELL	-	OEB_RCLKV[1]	89	OUT_CELL	-
DD4[7]	307	OUT_CELL	-	RCLKV[1]	88	OUT_CELL	-
OEB_DDPV[4]	306	OUT_CELL	-	OEB_OOF	87	OUT_CELL	-
DDPV[4]	305	OUT_CELL	-	OOF	86	OUT_CELL	-
OEB_DALARMV[4]	304	OUT_CELL	-	SDV[1]	85	IN_CELL	-
DALARMV[4]	303	OUT_CELL	-	RDCLKV[1]	84	IN_CELL	-
ACK	302	IN_CELL	-	RDN12_RD10	83	IN_CELL	-
ACMP	301	IN_CELL	-	RDP12_RD11	82	IN_CELL	-
DJ0REF	300	IN_CELL	-	RDN13_RD12	81	IN_CELL	-
DCMP	299	IN_CELL	-	RDP13_RD13	80	IN_CELL	-
DCK	298	IN_CELL	-	RDN14_RD14	79	IN_CELL	-
OEB_SALM1	297	OUT_CELL	-	RDP14_RD15	78	IN_CELL	-
SALM1	296	OUT_CELL	-	RDN15_RD16	77	IN_CELL	-
OEB_B3E1	295	OUT_CELL	-	RDP15_RD17	76	IN_CELL	-
B3E1	294	OUT_CELL	-	OEB_D[15]	75	OUT_CELL	-
OEB_RALMV[1]	293	OUT_CELL	-	D[15]	74	IO_CELL	-
RALMV[1]	292	OUT_CELL	-	OEB_D[14]	73	OUT_CELL	-
OEB_ROHCLKV[1]	291	OUT_CELL	-	D[14]	72	IO_CELL	-
ROHCLKV[1]	290	OUT_CELL	-	OEB_D[13]	71	OUT_CELL	-
OEB_ROHFPV[1]	289	OUT_CELL	-	D[13]	70	IO_CELL	-
ROHFPV[1]	288	OUT_CELL	-	OEB_D[12]	69	OUT_CELL	-
OEB_RTOHV[1]	287	OUT_CELL	-	D[12]	68	IO_CELL	-
RTOHV[1]	286	OUT_CELL	-	OEB_D[11]	67	OUT_CELL	-
OEB_RPOHV[1]	285	OUT_CELL	-	D[11]	66	IO_CELL	-
RPOHV[1]	284	OUT_CELL	-	OEB_D[10]	65	OUT_CELL	-
OEB_RPOHENV[1]	283	OUT_CELL	-	D[10]	64	IO_CELL	-
RPOHENV[1]	282	OUT_CELL	-	OEB_D[9]	63	OUT_CELL	-
OEB_RRCPDATV[1]	281	OUT_CELL	-	D[9]	62	IO_CELL	-
RRCPDATV[1]	280	OUT_CELL	-	OEB_D[8]	61	OUT_CELL	-
OEB_SALM2_B3E2	279	OUT_CELL	-	D[8]	60	IO_CELL	-
SALM2_B3E2	278	OUT_CELL	-	OEB_D[7]	59	OUT_CELL	-
OEB_RALMV[2]	277	OUT_CELL	-	D[7]	58	IO_CELL	-
RALMV[2]	276	OUT_CELL	-	OEB_D[6]	57	OUT_CELL	-
OEB_ROHCLKV[2]	275	OUT_CELL	-	D[6]	56	IO_CELL	-
ROHCLKV[2]	274	OUT_CELL	-	OEB_D[5]	55	OUT_CELL	-
OEB_ROHFPV[2]	273	OUT_CELL	-	D[5]	54	IO_CELL	-
ROHFPV[2]	272	OUT_CELL	-	OEB_D[4]	53	OUT_CELL	-
OEB_RTOHV[2]	271	OUT_CELL	-	D[4]	52	IO_CELL	-
RTOHV[2]	270	OUT_CELL	-	OEB_D[3]	51	OUT_CELL	-
OEB_RPOHV[2]	269	OUT_CELL	-	D[3]	50	IO_CELL	-
RPOHV[2]	268	OUT_CELL	-	OEB_D[2]	49	OUT_CELL	-
OEB_RPOHENV[2]	267	OUT_CELL	-	D[2]	48	IO_CELL	-
RPOHENV[2]	266	OUT_CELL	-	OEB_D[1]	47	OUT_CELL	-
OEB_RRCPDATV[2]	265	OUT_CELL	-	D[1]	46	IO_CELL	-
RRCPDATV[2]	264	OUT_CELL	-	OEB_D[0]	45	OUT_CELL	-
OEB_SALM3_B3E3	263	OUT_CELL	-	D[0]	44	IO_CELL	-
SALM3_B3E3	262	OUT_CELL	-	A[13]	43	IN_CELL	-
OEB_RALMV[3]	261	OUT_CELL	-	A[12]	42	IN_CELL	-

RALMV[3]	260	OUT_CELL	-	A[11]	41	IN_CELL	-
OEB_ROHCLKV[3]	259	OUT_CELL	-	A[10]	40	IN_CELL	-
ROHCLKV[3]	258	OUT_CELL	-	A[9]	39	IN_CELL	-
OEB_ROHFPV[3]	257	OUT_CELL	-	A[8]	38	IN_CELL	-
ROHFPV[3]	256	OUT_CELL	-	A[7]	37	IN_CELL	-
OEB_RTOHV[3]	255	OUT_CELL	-	A[6]	36	IN_CELL	-
RTOHV[3]	254	OUT_CELL	-	A[5]	35	IN_CELL	-
OEB_RPOHV[3]	253	OUT_CELL	-	A[4]	34	IN_CELL	-
RPOHV[3]	252	OUT_CELL	-	A[3]	33	IN_CELL	-
OEB_RPOHENV[3]	251	OUT_CELL	-	A[2]	32	IN_CELL	-
RPOHENV[3]	250	OUT_CELL	-	A[1]	31	IN_CELL	-
OEB_RRCPDATV[3]	249	OUT_CELL	-	A[0]	30	IN_CELL	-
RRCPDATV[3]	248	OUT_CELL	-	CSB	29	IN_CELL	-
OEB_SALM4_B3E4	247	OUT_CELL	-	ALE	28	IN_CELL	-
SALM4_B3E4	246	OUT_CELL	-	RDB	27	IN_CELL	-
OEB_RALMV[4]	245	OUT_CELL	-	WRB	26	IN_CELL	-
RALMV[4]	244	OUT_CELL	-	RSTB	25	IN_CELL	-
OEB_ROHCLKV[4]	243	OUT_CELL	-	QUAD622	24	IN_CELL	-
ROHCLKV[4]	242	OUT_CELL	-	OEB_INTB	23	OUT_CELL	-
OEB_ROHFPV[4]	241	OUT_CELL	-	INTB	22	OUT_CELL	-
ROHFPV[4]	240	OUT_CELL	-	TRCPDATV[4]	21	IN_CELL	-
OEB_RTOHV[4]	239	OUT_CELL	-	TRCPFPV[4]	20	IN_CELL	-
RTOHV[4]	238	OUT_CELL	-	TRCPCLKV[4]	19	IN_CELL	-
OEB_RPOHV[4]	237	OUT_CELL	-	TRCPDATV[3]	18	IN_CELL	-
RPOHV[4]	236	OUT_CELL	-	TRCPFPV[3]	17	IN_CELL	-
OEB_RPOHENV[4]	235	OUT_CELL	-	TRCPCLKV[3]	16	IN_CELL	-
RPOHENV[4]	234	OUT_CELL	-	TRCPDATV[2]	15	IN_CELL	-
OEB_RRCPDATV[4]	233	OUT_CELL	-	TRCPFPV[2]	14	IN_CELL	-
RRCPDATV[4]	232	OUT_CELL	-	TRCPCLKV[2]	13	IN_CELL	-
OEB_RSLDCLK	231	OUT_CELL	-	TRCPDATV[1]	12	IN_CELL	-
RSLDCLK	230	OUT_CELL	-	TRCPFPV[1]	11	IN_CELL	-
OEB_RSLD	229	OUT_CELL	-	TRCPCLKV[1]	10	IN_CELL	-
RSLD	228	OUT_CELL	-	AJ0J1_FPV[1]	9	IN_CELL	-
OEB_RLDCLK	227	OUT_CELL	-	APLV[1]	8	IN_CELL	-
RLDCLK	226	OUT_CELL	-	AD1[0]	7	IN_CELL	-
OEB_RLD	225	OUT_CELL	-	AD1[1]	6	IN_CELL	-
RLD	224	OUT_CELL	-	AD1[2]	5	IN_CELL	-
OEB_TOHCLKV[1]	223	OUT_CELL	-	AD1[3]	4	IN_CELL	-
TOHCLKV[1]	222	OUT_CELL	-	AD1[4]	3	IN_CELL	-
OEB_TOHFPV[1]	221	OUT_CELL	-	AD1[5]	2	IN_CELL	-
TOHFPV[1]	220	OUT_CELL	-	AD1[6]	1	IN_CELL	-
TTOHV[1]	219	IN_CELL	-	AD1[7]	0	IN_CELL	-
TTOHENV[1]	218	IN_CELL	-				

Notes

1. When set high, INTB will be set to high impedance.

12.2.1 Boundary Scan Cells

In the following diagrams, CLOCK-DR is equal to TCK when the current controller state is SHIFT-DR or CAPTURE-DR, and unchanging otherwise. The multiplexer in the center of the diagram selects one of four inputs, depending on the status of select lines G1 and G2. The ID Code bit is as listed in the Boundary Scan Register table located above.

Figure 11 Input Observation Cell (IN_CELL)

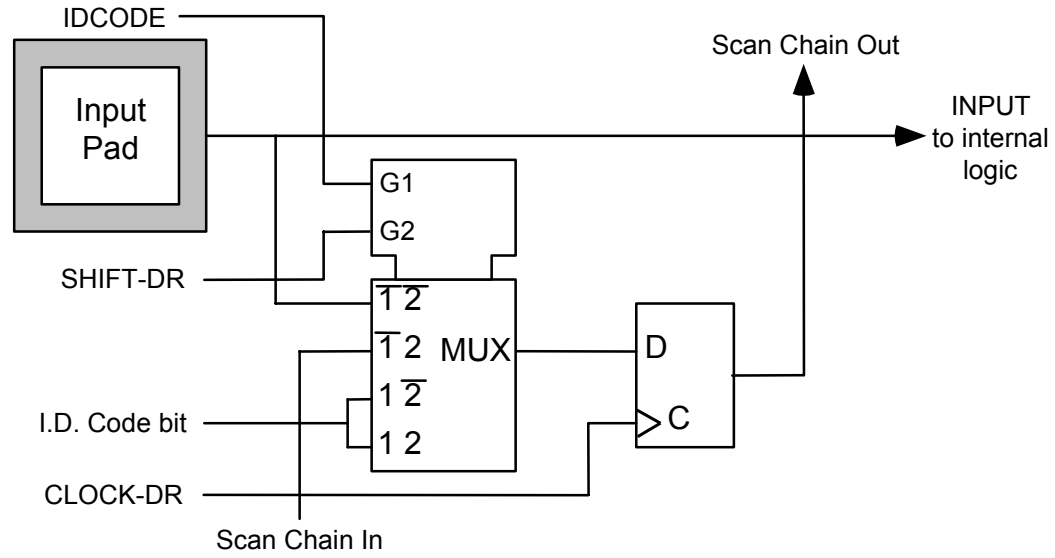


Figure 12 Output Cell (OUT_CELL)

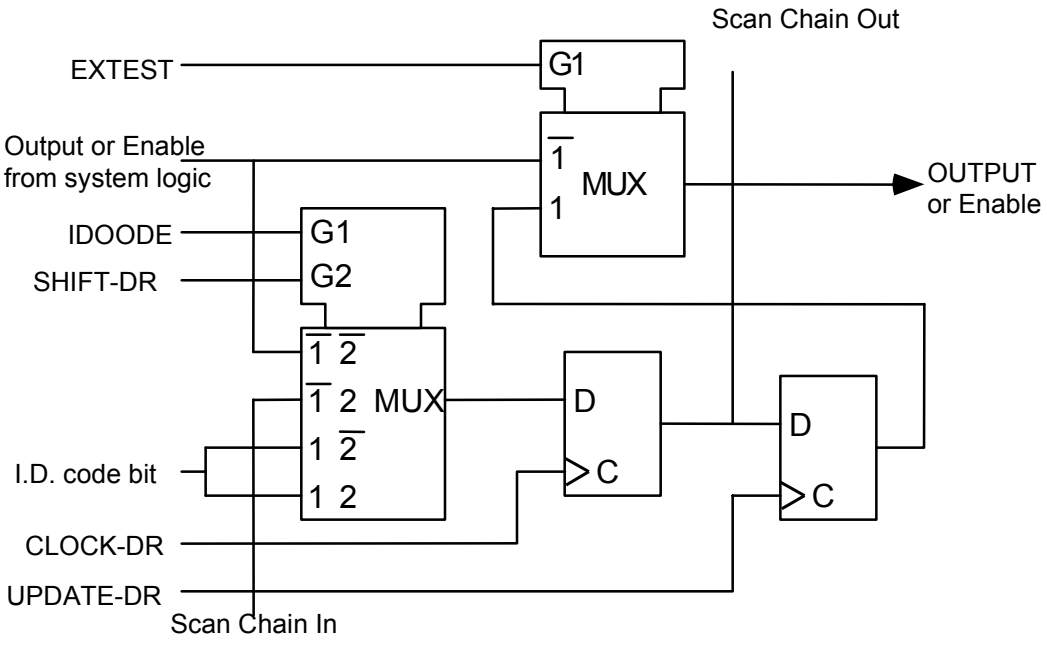


Figure 13 Bidirectional Cell (IO_CELL)

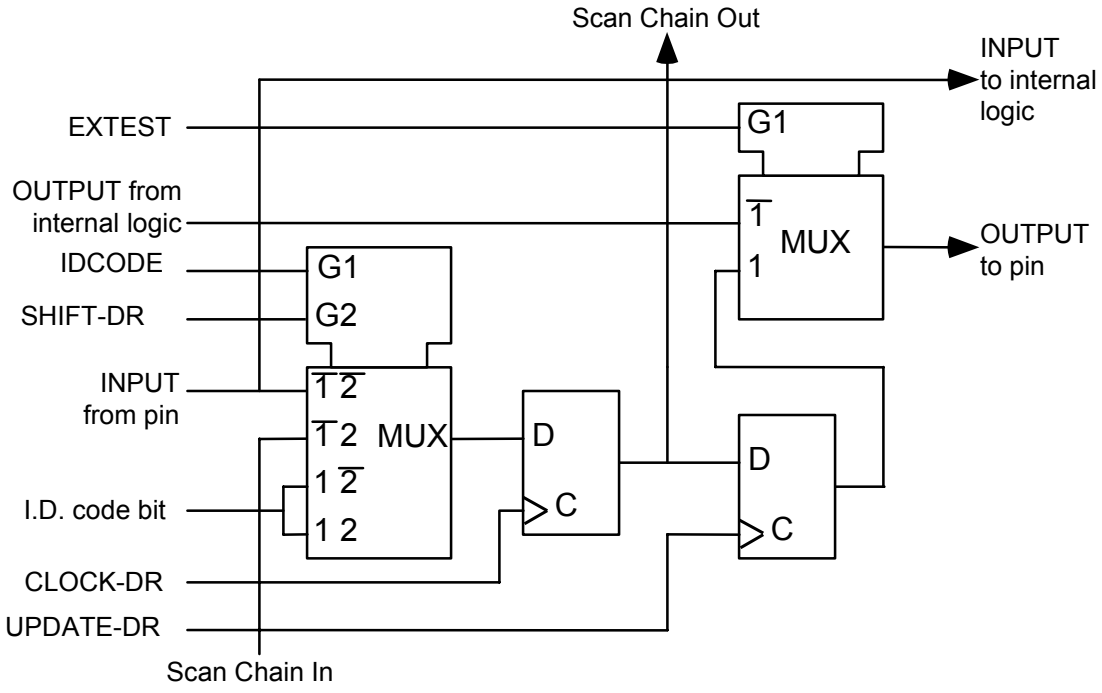
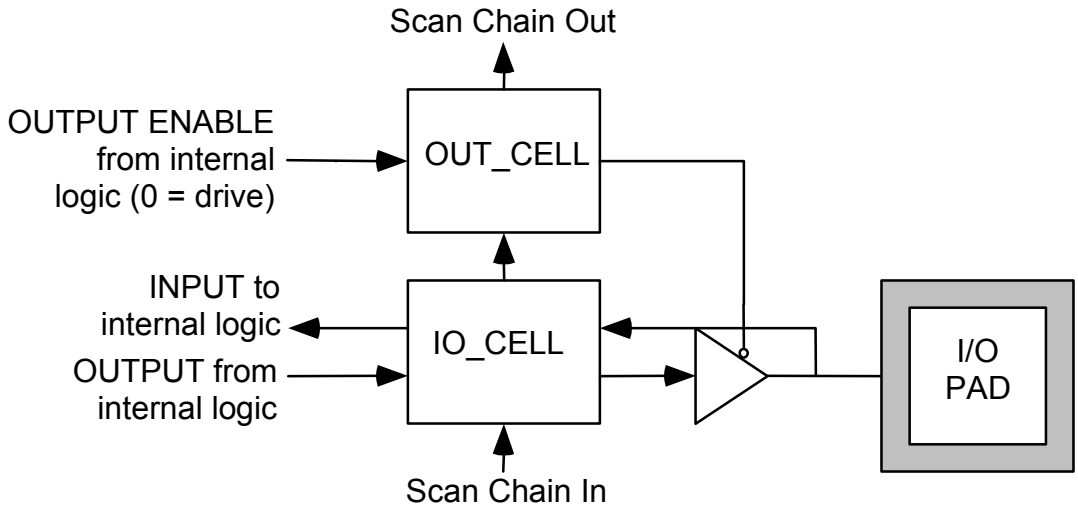


Figure 14 Layout of Output Enable and Bidirectional Cells



13 Operation

This section presents Configuration Options, PCB design recommendations, operating details for the JTAG boundary scan feature and interface details for system side devices.

The SPECTRA-2488 is a SONET/SDH PAYLOAD EXTRACTOR/ALIGNER device. It processes the section, line, path overhead of an STS-48/48c (STM-16/AU4-16c/AU4-12c/AU4-8c/ AU4-4c/AU4/AU3/TU3) or quad STS-12/12c (STM-4/AU4-4c/AU4/AU3/TU3) stream. The SPECTRA-2488 supports a rich set of line, path and system configuration options.

13.1 Transport and Path Overhead Bytes

Under normal operating conditions, the SPECTRA-2488 processes the complete transport overhead present in an STS-48c/48 or quad STS-12/12c(STM-4) stream. The byte positions processed by the SPECTRA-622 are indicated below.

Figure 15 STS-12 (STM-4) on RTOH 1-4/TTOH1-4

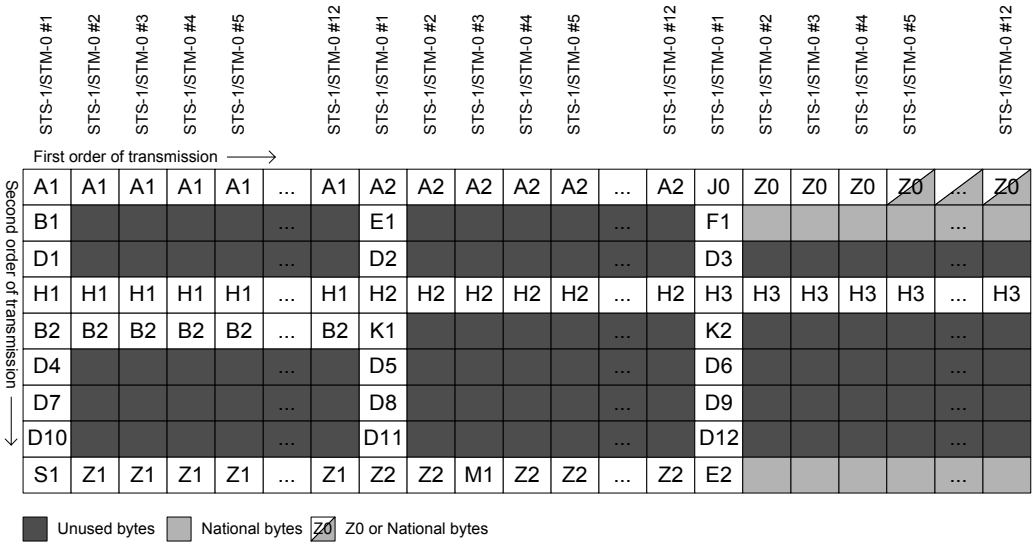


Figure 16 STS-48 (STM-16) on RTOH1/TTOH1

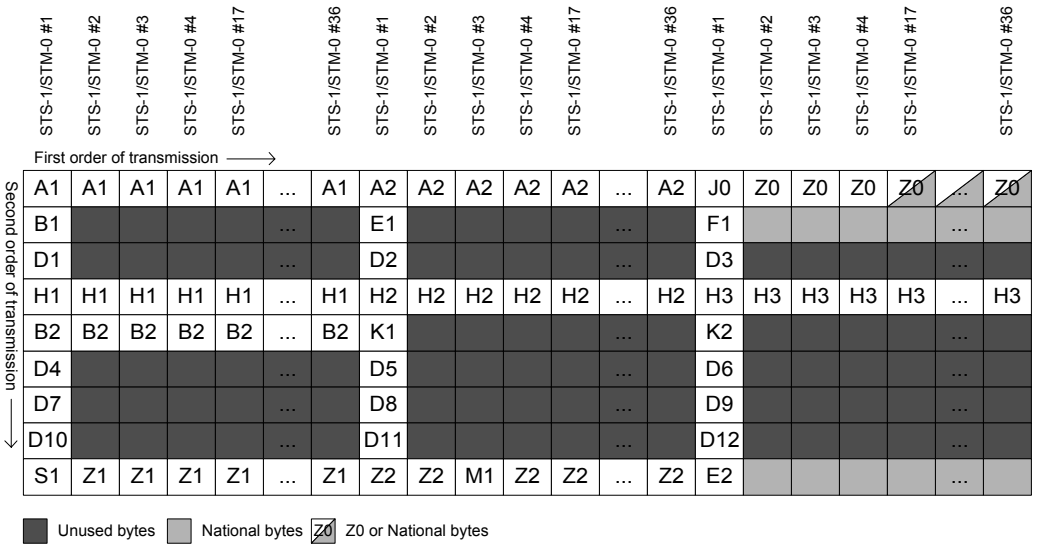


Figure 17 STS-48 (STM-16) on RTOH2/TTOH2

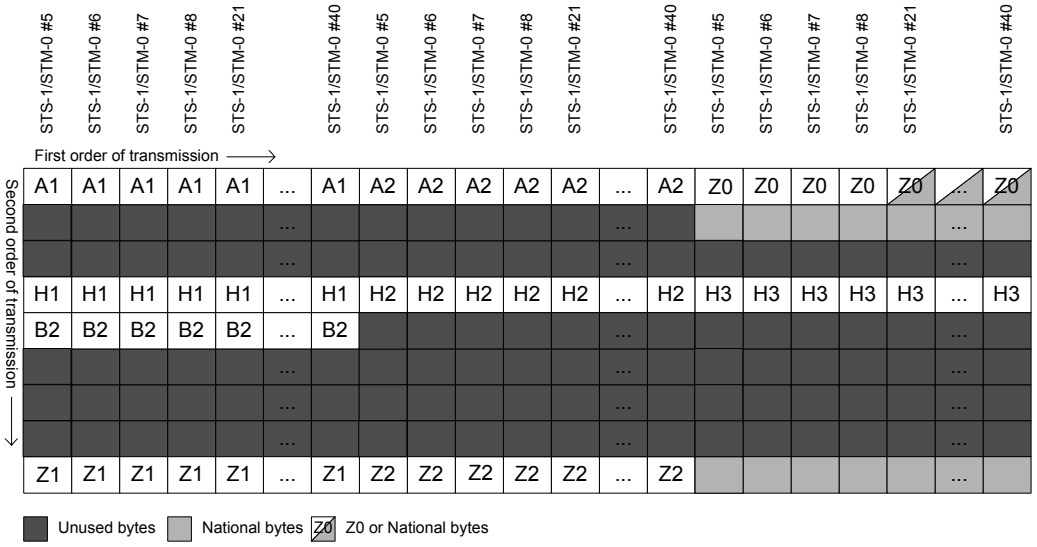


Figure 18 STS-48 (STM-16) on RTOH3/TTOH3

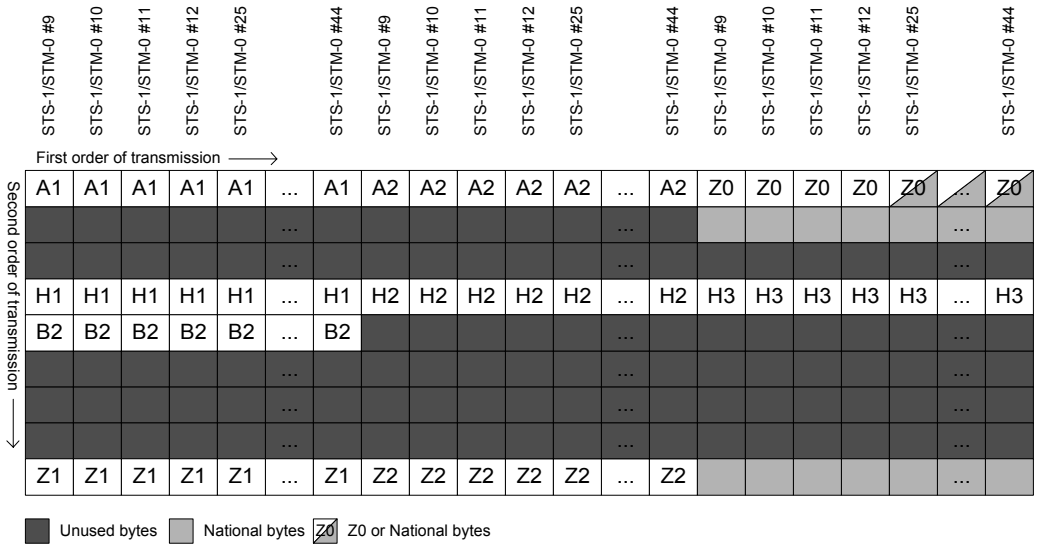
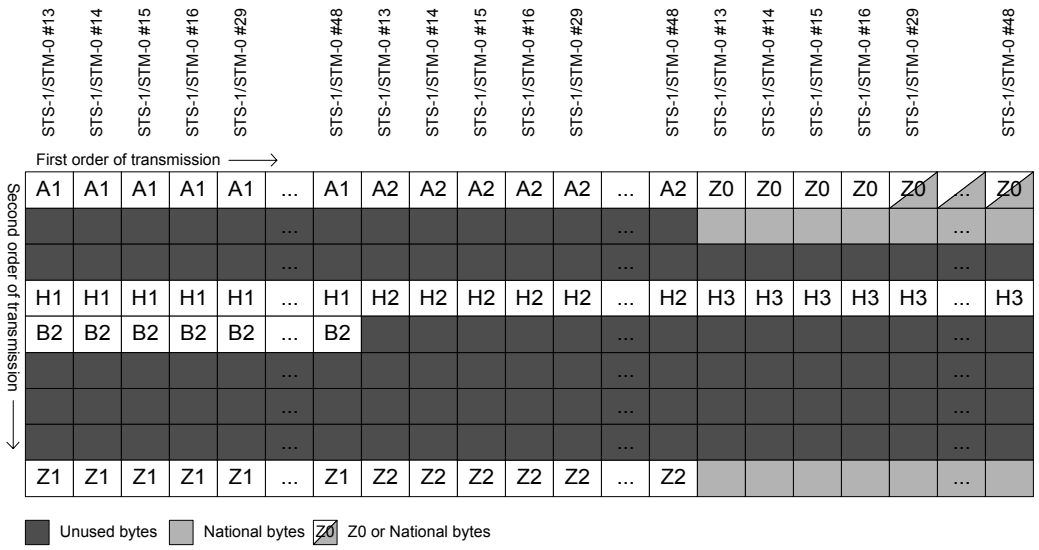


Figure 19 STS-48 (STM-16) on RTOH4/TTOH4



Transport Overhead Bytes

All receive transport overhead bytes are extracted and presented onto the RTOH port. All transmit transport overhead bytes can be inserted via the TTOH port.

A1, A2: The frame alignment bytes (A1, A2) locate the SONET/SDH frame in the serial stream. These bytes are used to byte align the received data.

J0 The J0 byte is currently defined as the section trace byte for SONET/SDH. J0 byte is not scrambled by the frame synchronous scrambler. The received section trace message is processed by the SECTION RTTP block and also available on the RTOH port. The transmit section trace message can be programmed in the SECTION TTTP, via the TTOH port or the TRMP block.

Z0: The Z0 bytes are currently defined as the section growth bytes for SONET/SDH. Z0 bytes are not scrambled by the frame synchronous scrambler. The received section growth bytes are extracted and available on the RTOH port. The transmit section growth bytes can be inserted via the TTOH port or the TRMP block.

B1: The section bit interleaved parity byte provides a section error monitoring function. In the transmit direction, the TRMP block calculates the B1 code over all bits of the previous frame after scrambling. The calculated code is then placed in the current frame before scrambling. In the receive direction, the RRMP block calculates the B1 code over the current frame and compares this calculation with the B1 byte received in the following frame. B1 errors are accumulated in the error event counter of the RRMP block .

D1 - D3: The section data communications channel provides a 192 kbit/s data communications channel for network element to network element communications. In the transmit direction, the section DCC byte is inserted from a dedicated 192 kbit/s input, TLD and/or TSLD port. Section DCC can also be inserted via the TTOH port or the TRMP block. In the receive direction, the section DCC is extracted on a dedicated 192 kbit/s output, RLD and/or RSLD port. Section DCC is also extracted on the RTOH port.

H1, H2: The pointer value bytes locate the J1 path overhead byte in the SONET/SDH frame. In the transmit direction, the SVCA block inserts a valid pointer with pointer adjustments to accommodate plesiochronous timing offsets between the line and system references. In the receive direction, the pointer is interpreted by the RHPP block to locate the payload. The loss of pointer state is entered when a valid pointer cannot be found. Path AIS state is entered when H1, H2 contain an all ones pattern.

H3: The pointer action bytes contain synchronous payload envelope data when a negative stuff event occurs. An all zero pattern is inserted in the transmit direction unless a negative stuff event occurs. This byte is ignored in the receive direction unless a negative stuff event is detected.

B2: The line bit interleaved parity bytes provide a line error monitoring function. In the transmit direction, the TRMP block calculates the B2 codes. The calculated code is then placed in the next frame. In the receive direction, the RRMP block calculates the B2 codes over the current frame and compares this calculation with the B2 codes receive in the following frame. B2 errors are accumulated in the error event counter of the RRMP block.

K1, K2: The K1 and K2 bytes provide the automatic protection switching channel. The K2 byte is also used to identify line layer maintenance signals. Line RDI is indicated when bits 6, 7, and 8 of the K2 byte are set to the pattern '110'. Line AIS is indicated when bits 6, 7, and 8 of the K2 byte are set to the pattern '111'. In the transmit direction, the K1 and K2 bytes can be inserted via the TTOH port or the TRCP ports. The TRMP block also provides register control for the K1 and K2 bytes block. In the receive direction, the RRMP block provides register access to the filtered APS channel. Protection switch byte failure alarm detection is provided. The K2 byte is also determines the presence of the line AIS, or the line RDI maintenance signals

D4 - D12: The line data communications channel provides a 576 kbit/s data communications channel for network element to network element communications. In the transmit direction, the line DCC byte is inserted from a dedicated 576 kbit/s input, TLD. Line DCC can also be inserted via the TTOH port or the TRMP block. In the receive direction, the line DCC is extracted on a dedicated 576 kbit/s output, RLD. Line DCC is also extracted on the RTOH port.

S1: The S1 byte provides the synchronization status message. Bits 5 through 8 of the synchronization status byte identifies the synchronization source of the SONET/SDH signal. Bits 1 through 4 are currently undefined. In the transmit direction, the synchronization status message is inserted from the TRMP block. In the receive direction, the TRMP block provides register access to the synchronization status byte. The S1 byte is also available on the RTOH port.

Z1: The Z1 bytes are allocated for future growth. In the transmit direction, the Z1 growth bytes can be inserted via the TTOH port or the TRMP block. In the receive direction, the Z1 growth bytes are extracted and available on the RTOH port.

M1: The M1 byte provides a line remote error indication (REI) function for remote performance monitoring. In the transmit direction, the M1 byte is internally generated. The number of B2 errors detected in the previous interval is insert from the receive RRMP block or the TRCP port. In the receive direction, a legal REI value is added to the line REI event counter in the RRMP block.

Z2: The Z2 bytes are allocated for future growth. In the transmit direction, Z2 growth bytes can be inserted via the TTOH port or the TRMP block. In the receive direction, Z1 growth bytes are extracted and available on the RTOH port.

Path Overhead Bytes

All receive path overhead bytes are extracted and presented onto the RPOH port. All transmit path overhead bytes can be inserted via the TPOH port.

J1: The Path Trace byte is used to repetitively transmit a 64-byte CLLI message (for SONET/SDH networks), or a 16-byte E.164 address (for SDH networks). When not used, this byte should be set to transmit continuous null characters. Null is defined as the ASCII code, 0x00. The received section trace message is processed by the PATH RTTP block and also available on the RPOH port. The transmit section trace message can be programmed in the PATH TTTP, via the TPOH port or the THPP block.

B3: The path bit interleaved parity byte provides a path error monitoring function. In the transmit direction, the THPP block calculates the B3 code. The calculated code is then placed in the next frame. In the receive direction, the RHPP block calculates the B3 code and compares this calculation with the B3 code received in the following frame. B3 errors are accumulated in an error event counter of the RHPP.

C2: The path signal label indicator identifies the equipped payload type. In the transmit direction, the C2 byte can be inserted via the TPOH port or the THPP block. In the receive direction, the C2 byte is processed by the RHPP block for path signal label mismatch and unstable alarms and also for unequipped and payload defect indication alarms. The C2 byte is also available on the RPOH port.

G1: The path status byte provides a path remote error indication (REI) function, and a path remote defect indication (RDI) function. Three bits are allocated for remote defect indications: bit 5 (the path RDI bit), bit 6 (the auxiliary path RDI bit) and bit 7 (Enhanced RDI bit). Taken together these bits provide a eight state path RDI code that can be used to categorize path defect indications. In the transmit direction, the REI and RDI codes are internally generated. The RDI code is inserted from the receive RHPP block or the TRCP port. The number of B3 errors detected in the previous interval is inserted from the THPP block or the TRCP port. In the receive direction, a legal path REI value is added to the path REI event counter in the RHPP block.

H4: The multi-frame indicator byte is a payload specific byte. In the transmit direction, the H4 byte can be inserted via the TPOH port or the THPP block. In the receive direction, the H4 byte is extracted and available on the RPOH port..

Z3 Z4 Z5: The Z3, Z4 and Z5 bytes are allocated for future growth. In the transmit direction, the growth bytes can be inserted via the TPOH port or the THPP block. In the receive direction, the growth bytes are extracted and available on the RPOH port.

13.2 Accessing Indirect Registers

Indirect registers are used to conserve address space in the SPECTRA-2488. Indirect registers are accessed by writing the indirect address register. The following steps should be followed for writing to indirect registers:

1. Read the BUSY bit. If it is equal to logic 0, continue to step 2. Otherwise, continue polling the BUSY bit.

2. Write the desired configurations for the channel into the indirect data registers.

3. Write the channel number (indirect address) to the indirect address register with RWB set to logic 0.

4. Read BUSY. Once it equals 0, the indirect write has been completed.

The following steps should be followed for reading indirect registers:

1. Read the BUSY bit. If it is equal to logic 0, continue to step 2. Otherwise, continue polling the BUSY bit.

2. Write the channel number (indirect address) to the indirect address register with RWB set to logic 1.

3. Read the BUSY bit. If it is equal to logic 0, continue to 4. Otherwise, continue polling the BUSY bit.

4. Read the indirect data registers to find the state of the register bits for the selected channel number.

Note: Maximum busy bit set time is 22 clock cycles except for the STSI block which is 10 clock cycles.

13.3 Interrupt Service Routine

The SPECTRA-2488 will assert INTB to logic 0 when a condition that is configured to produce an interrupt occurs. To find which condition caused this interrupt to occur, the procedure outlined below should be followed:

1. Read the SP2488 Interrupt Status registers at address 0010H to 0013H to find the functional block(s) which caused the interrupt. The interrupt status bits point to the functional block(s) which caused the hardware interrupt.

2. Find the register address of the corresponding block that caused the interrupt and read its Interrupt Status registers. The interrupt functional block and interrupt source identification register bits from step 1 are cleared once these register(s) have been read and the interrupt(s) identified.

3. Service the interrupt(s).

4. If the INTB pin is still logic 0, then there are still interrupts to be serviced and steps 1 to 3 need to be repeated. Otherwise, all interrupts have been serviced. Wait for the next assertion of INTB.

13.4 Using the Performance Monitoring Features

The performance monitor counters within the different blocks are provided for performance monitoring purposes. All performance monitor counters have been sized to not saturate if polled every second. The counters will saturate and not roll over if they reach their maximum value.

Each block's counters can be accumulated independently if one of the registers which contain the latched counter values is written to. A device update of all the counters can be done by writing to the SPECTRA-2488 global performance monitor update register (register 0000H). After this register is written to, the TIP bit in this register can be polled to determine when all the counter values have been transferred and are ready to be read.

13.5 Translation from AU4/3x(TUG3/TU3/VC3) into 3x(AU3/VC3)

On the Receive side, the SPECTRA-2488 can be configure to translate AU4/3x(TUG3/TU3/VC3) payloads into 3x(AU3/VC3) payloads to bridge between SDH compliant and SONET compliant networks. The RHPP block interprets the AU4 pointer and terminates the VC4 POH overhead. The RHPP TU3 block interprets the TU3 pointer and terminates the VC3 POH overhead. Then, the SVCA block moves the VC3 fixed stuff columns from columns 1,2 to columns 30,59 (the contains is lost). While performing rate adaptation, the SVCA block also generates three independent AU3 pointers for the DROP TelecomBus interface.

AU3/VC3 (Receive Side) => AU3/VC3 (DROP TelecomBus Interface)

1. Default setting in the RHPP Payload Configuration Register (0102H, 0502H, 0902H or 0D02H) for AU3 pointer interpretation..

2. Default setting in the RHPP TU3 Payload Configuration Register (0182H, 0582H, 0982H or 0D82H) for no TU3 pointer interpretation.

3. Default setting in the SVCA Payload Configuration Register (0202H, 0602H, 0A02H or 0E02H) for AU3 processing.

AU4/VC4 (Receive Side) => AU4/VC4 (DROP TelecomBus Interface)

1. Set the STS3C[4:1] bits in the RHPP Payload Configuration Register (0102H, 0502H, 0902H or 0D02H) for AU4 pointer interpretation..

2. Default setting in the RHPP TU3 Payload Configuration Register (0182H, 0582H, 0982H or 0D82H) for no TU3 pointer interpretation.

3. Set the STS3C[4:1] bits in the SVCA Payload Configuration Register (0202H, 0602H, 0A02H or 0E02H) for AU4 processing.

AU4/3x(TUG3/TU3/VC3) (Receive Side) => 3x(AU3/VC3) (DROP TelecomBus Interface)

1. Set the STS3C[4:1] bits in the RHPP Payload Configuration Register (0102H, 0502H, 0902H or 0D02H) for AU4 pointer interpretation..

2. Set the TUG3[4:1] bits in the RHPP TU3 Payload Configuration Register (0182H, 0582H, 0982H or 0D82H) for TU3 pointer interpretation.

3. Set the STS3C[4:1] and the TUG3[4:1] bits in the SVCA Payload Configuration Register (0202H, 0602H, 0A02H or 0E02H) for AU4/TU3=>AU3 translation.

13.6 Translation from 3x(AU3/VC3) into AU4/3x(TUG3/TU3/VC3)

On the ADD Telecombus interface, the SPECTRA-2488 can be configure to translate 3x(AU3/VC3) payloads into AU4/3x(TUG3/TU3/VC3) payloads to bridge between SONET compliant and SDH compliant networks. The SVCA block moves the VC3 fixed stuff columns from columns 30,59 to columns 1,2 (the contains is lost). While performing rate adaptation, the SVCA block also generates three independent TU3 pointers and a fix AU4 pointer for the transmit side. The THPP TU3 block inserts the VC3 POH overhead.The THPP block inserts the VC4 POH overhead.

AU3/VC3 (ADD TelecomBus Interface) => AU3/VC3 (Transmit Side)

1. Default setting in the SVCA Payload Configuration Register (1202H, 1602H, 1A02H or 1E02H) for AU3 processing.

2. Default setting in the THPP TU3 Payload Configuration Register (1182H, 1582H, 1982H or 1D82H) for no TU3 POH insertion.

3. Default setting in the THPP Payload Configuration Register (1102H, 1502H, 1902H or 1D02H) for AU3 POH insertion..

AU4/VC4 (ADD TelecomBus Interface) => AU4/VC4 (Transmit Side)

1. Set the STS3C[4:1] bits in the SVCA Payload Configuration Register (1202H, 1602H, 1A02H or 1E02H) for AU4 processing.

2. Default setting in the THPP TU3 Payload Configuration Register (1182H, 1582H, 1982H or 1D82H) for no TU3 POH insertion.

3. Set the STS3C[4:1] bits in the THPP Payload Configuration Register (1102H, 1502H, 1902H or 1D02H) for AU4 POH insertion..

3x(AU3/VC3) (ADD TelecomBus Interface) => AU4/3x(TUG3/TU3/VC3) (Transmit Side)

1. Set the STS3C[4:1] and the TUG3[4:1] bits in the SVCA Payload Configuration Register (1202H, 1602H, 1A02H or 1E02H) for AU3 => AU4/TU3 translation.

2. Set the TUG3[4:1] bits in the THPP TU3 Payload Configuration Register (1182H, 1582H, 1982H or 1D82H) for TU3 POH insertion.

3. Set the STS3C[4:1] bits in the THPP Payload Configuration Register (1102H, 1502H, 1902H or 1D02H) for AU4 POH insertion..

13.7 Bit Error Rate Monitor

The SPECTRA-2488 provides two BERM blocks. One can be dedicated to monitoring the Signal Degrade (SD) error rates and the other dedicated to monitoring the Signal Fail (SF) error rates.

The Bit Error Rate Monitor (BERM) block counts and monitors line BIP errors over programmable periods of time (window size). It can monitor to declare an alarm or to clear it if the alarm is already set. A different threshold must be used to declare or clear the alarm, whether or not those two operations are performed at the same BER. The following tables list the recommended content of the BERM registers for different speeds (OC-N) and error rates (BER). Both BERMs in the SBER block are equivalent and are programmed similarly. In a normal application they will be set to monitor different BER.

When the SF/SD CMODE bit is 1, this indicates that the clearing monitoring is recommended to be performed using a window size that is 8 times longer than the declaration window size. When the SF/SD CMODE bit is 0 this indicates that the clearing monitoring is recommended to be performed using a window size equal to the declaration window size. In all cases the clearing threshold is calculated for a BER that is 10 times lower than the declaration BER, as required in the references. The tables indicate the declare BER, the evaluation period and the recommended CMODE and associated thresholds.

The Saturation threshold is not listed in the table, and is programmed with the value 0xFFFFFF by default, deactivating saturation. Saturation capabilities are provided to allow the user to address issues associated with error bursts. It enables the user to determine a ceiling value at which the error counters will saturate, letting error bursts pass through within a frame or sub window period.

Table 16 Recommended BERM Settings For Different OC and BER Rates, Meeting Bellcore Objectives

OC	Monitored Declare BER	Objective Met For Switching Time (s)	SF/SD CMODE	SF/SD SAP (hex)	SF/SD DECTH (hex)	SF/SD CLRTH (hex)
12	10^{-3}	0.008	0	00000007	000828	0001AE
12	10^{-4}	0.008	0	00000007	00016E	000036
12	10^{-5}	0.025	0	00000016	000073	000014
12	10^{-6}	0.250	0	000000DE	000075	000014
12	10^{-7}	2.500	0	000008AE	000075	000014
12	10^{-8}	21.000	0	000048EA	000061	000012

OC	Monitored Declare BER	Objective Met For Switching Time (s)	SF/SD CMODE	SF/SD SAP (hex)	SF/SD DECTH (hex)	SF/SD CLRTH (hex)
12	10^{-9}	167.000	0	000243DC	00004B	00000F
48	10^{-3}	0.008	0	00000007	002116	000677
48	10^{-4}	0.008	0	00000007	0005F8	0000C1
48	10^{-5}	0.008	0	00000007	000095	000019
48	10^{-6}	0.063	0	00000037	000074	000014
48	10^{-7}	0.625	0	0000022B	000075	000014
48	10^{-8}	5.200	0	0000120E	000060	000011
48	10^{-9}	42.000	0	000091D5	00004C	00000F

Table 17 Recommended BERM Settings For Different OC and BER Rates, Meeting Bellcore and ITU Requirements.

OC	Monitored Declare BER	Requirement Met For Switching Time (s)	SF/SD CMODE	SF/SD SAP (hex)	SF/SD DECTH (hex)	SF/SD CLRTH (hex)
12	10^{-3}	0.01	0	00000008	00093C	0001F7
12	10^{-4}	0.10	0	0000002B	00091D	00012C
12	10^{-5}	1.00	0	00000192	000922	00011C
12	10^{-6}	10.00	0	00000F98	000922	00011B
12	10^{-7}	100.00	0	00009BD6	000922	00011A
12	10^{-8}	1,000.00	0	00061647	000922	00011A
12	10^{-9}	10,000.00	0	003CDEAD	000922	00011A
48	10^{-3}	0.01	0	00000008	0025A5	00077B
48	10^{-4}	0.10	0	0000002B	002554	000465
48	10^{-5}	1.00	0	00000192	00256F	000426
48	10^{-6}	10.00	0	00000F98	002570	000420
48	10^{-7}	100.00	0	00009BD6	002571	00041F
48	10^{-8}	1,000.00	0	00061647	002571	00041F
48	10^{-9}	10,000.00	0	003CDEAD	002571	00041F

13.8 Setting up Timeslot Assignments In The STSI

The STSI blocks in the SPECTRA-2488 (ASTSI and DSTSI) can be used to rearrange the position of the system side SONET/SDH timeslots. Each block buffers 48 timeslots and rearranges them as desired before outputting them. The STSI blocks allow user configuration of timeslot mappings, basic bypass of timeslots, and predefined mappings for standard TelecomBus interfaces.

13.8.1 Standard TelecomBus Timeslot Map

The standard TelecomBus Timeslot Map at the SPECTRA-2488 system side interface is shown in Table 18. The following discussion references AD[x][7:0] and DD[x][7:0], but can also apply to their associated control signals.

Payload bytes from the SONET/SDH stream are labeled by Sx,y. Within Sx,y, the STS-3/STM-1 number is given by 'x' and the column number within the STS-3/STM-1 is given by 'y'. With such a mapping, an STS-12c/STM-4c data stream will be transferred across one complete AD[x][7:0] or DD[x][7:0] bus.

Table 18 Standard TelecomBus Timeslot Map

AD[1][7:0] DD[1][7:0]	S1,1	S2,1	S3,1	S4,1	S1,2	S2,2	S3,2	S4,2	S1,3	S2,3	S3,3	S4,3
AD[2][7:0] DD[2][7:0]	S5,1	S6,1	S7,1	S8,1	S5,2	S6,2	S7,2	S8,2	S5,3	S6,3	S7,3	S8,3
AD[3][7:0] DD[3][7:0]	S9,1	S10,1	S11,1	S12,1	S9,2	S10,2	S11,2	S12,2	S9,3	S10,3	S11,3	S12,3
AD[4][7:0] DD[4][7:0]	S13,1	S14,1	S15,1	S16,1	S13,2	S14,2	S15,2	S16,2	S13,3	S14,3	S15,3	S16,3

13.8.2 Custom Timeslot Mappings

If the ASTSISW[1:0] or DSTSISW[1:0] bits are set to 'b00, then the corresponding STSI block will be set for custom timeslot mapping. This permits the user to swap the position of or multicast any STS-1/STM-0 timeslot.

The channels must still fit into the required system side timeslot map in a manner which is required by a channel of such a rate. For example, an STS-3c channel which occupied system side timeslots S1,1 and S1,2 and S1,3 in Table 18 can be moved to line side timeslots S7,1 and S7,2 and S7,3. The analogous mapping can be done from the line side timeslots to the system side timeslots.

The following procedure shows how the ASTSI block can be programmed to perform such a remapping of timeslots. Page 0 of the ASTSI block is configured in the example.

1. Set ASTSISW[1:0] equal to 'b00.

2. For the ASTSI, the base address STSI_BASE is 1220H.

3. Read BUSY in the STSI Indirect Address register at STSI_BASE + 00H. If it is logic 0, proceed to step 4. Otherwise, poll BUSY until it is logic 0.

4. Write 0010H to the STSI Indirect Data register at STSI_BASE + 01H to set TSIN[3:0] to 1 and DINSEL[1:0] to 0. This selects the AD[1][7:0] timeslot S1,1 as the input timeslot.

5. Write 0031H to the STSI Indirect Address register at STSI_BASE + 00H to set TSOUT[3:0] to 3 and DOUTSEL[1:0] to 1. This selects the position S7,1 on the output line side timeslot in the page 0 mapping of the ASTSI.

6. Read BUSY in the STSI Indirect Address register at STSI_BASE + 00H. If it is logic 0, proceed to step 7. Otherwise, poll BUSY until it is logic 0.

7. Write 0050H to the STSI Indirect Data register at STSI_BASE + 01H to set TSIN[3:0] to 5 and DINSEL[1:0] to 0. This selects the AD[1][7:0] timeslot S1,2 as the input timeslot.

8. Write 0071H to the STSI Indirect Address register at STSI_BASE + 00H to set TSOUT[3:0] to 7 and DOUTSEL[1:0] to 1. This selects the position S7,2 on the output line side timeslot in the page 0 mapping of the ASTSI.

9. Read BUSY in the STSI Indirect Address register at STSI_BASE + 00H. If it is logic 0, proceed to step 10. Otherwise, poll BUSY until it is logic 0.

10. Write 0090H to the STSI Indirect Data register at STSI_BASE + 01H to set TSIN[3:0] to 9 and DINSEL[1:0] to 0. This selects the AD[1][7:0] timeslot S1,3 as the input timeslot.

11. Write 00B1H to the STSI Indirect Address register at STSI_BASE + 00H to set TSOUT[3:0] to BH and DOUTSEL[1:0] to 1. This selects the position S7,3 on the output line side timeslot in the page 0 mapping of the ASTSI.

12. Go back to step 1 if you want to configure more timeslot mappings.

13.8.3 Active and Standby Pages in The STSI Blocks

The STSI blocks contain 2 pages of configurations: an active page, and an inactive page. Selection of the page in use in the ASTSI is done by the ACMP input signal. Selection of the page in use in the DSTSI is done by the DCMP input signal.

The existence of an active page and an inactive page allows the user to set-up an alternate timeslot mapping on multiple devices or multiple STSI blocks before performing a global switch to the new mapping. The swapping of the page in use is done at transport frame boundaries. The ACMP and DCMP are sampled at the J0 locations defined by PL equal logic zero and J0J1 equal logic one.

13.9 PRBS Generator and Monitor (PRGM)

A pseudo-random (using the $X^{23}+X^{18}+1$ polynomial) or incrementing pattern can be inserted/extracted in the SONET/SDH payload. The user has the option to monitor a programmable sequence in all the B1 byte positions. The complement of these values are also monitored in the E1 byte positions. This is used to check for misconfiguration of STS-1 cross-connect fabrics. If a known STS-1 originated from a particular STS-1 port, the source can be programmed to send a B1 pattern that would be monitored at the other end.

13.9.1 Mixed Payload (STS-12c, STS-3c, and STS-1)

Each PRGM is designed to process the payload of a STS-12/STM-4 frame in a time-multiplexed manner. Each time division (12 STS-1 paths) can be programmed to a granularity of a STS-1. It is possible to process one STS-12c/STM-4c, twelve STS-1/STM-0 or four STS-3c/STM-1 or a mix of STS-1/STM-0 and STS-3c/STM-1 as long as the aggregate data rate is not more than one STS-12/STM-4 equivalent. The mixed payload configuration can support the three STS-1/STM-0 and STS-3c/STM-1 combinations shown below:

- three STS-1/STM-0 with three STS-3c/STM-1
- six STS-1/STM-0 with two STS-3c/STM-1
- nine STS-1/STM-0 with one STS-3c/STM-1.

The STS-1 path that each one of the payload occupies, cannot be chosen randomly. They must be placed on STS-3c/STM-1 boundaries (group of three STS-1).

13.9.2 Synchronization

Before being able to monitor the correctness of the PRBS payload, the monitor must synchronize to the incoming PRBS. The process of synchronization involves synchronizing the monitoring LFSR to the transmitting LFSR. Once the two are synchronized the monitoring LFSR is able to generate the next expected PRBS bytes. When receiving sequential PRBS bytes (STS-12c/VC-4-4c), the LFSR state is determined after receiving 3 PRBS bytes (24 bits of the sequence). The last 23 of 24 bits (excluding MSB of first received byte) would give the complete LFSR state. The 8 newly generated LFSR bits after a shift by 8 (last 8 XOR products) will produce the next expected PRBS byte.

In master/slave configuration of the monitor (processing STS-24c/VC-4-8c, STS-36c/VC-4-12c or STS-48c/VC-4-16c) more bytes are needed to recover the LFSR state, because the slaves needs a few bytes to be synchronized with the J1 byte indicator.

The implemented algorithm requires four PRBS bytes of the same payload to ascertain the LFSR state. From this recovered LFSR state the next expected PRBS byte is calculated.

An Out of Synchronization and Synchronized State is defined for the monitor. While in progress of synchronizing to the incoming PRBS stream, the monitor is out of synchronization and remains in this state until the LFSR state is recovered and the state has been verified by receiving 4 consecutive PRBS bytes without error. The monitor will then change to the Synchronized State and remains in that state until forced to resynchronize via the RESYNC register bit or upon receiving 4 erred bytes. When forced to resynchronize, the monitor changes to the Out of Synchronization State and tries to regain synchronization.

Upon detecting 4 consecutive PRBS byte errors, the monitor will enter the Out of Synchronization State and automatically try to resynchronize to the incoming PRBS stream. Once synchronized to the incoming stream, it will take 4 consecutive non-erred PRBS bytes to change back into the Synchronized State. The auto synchronization is useful when the input frame alignment of the monitored stream changes. The realignment will affect the PRBS sequence causing all input PRBS bytes to mismatch and forcing the need for a resynchronization of the monitor. The auto resynchronization does this, detecting a burst of errors and automatically re-synchronizing.

13.9.3 Master/Slave Configuration for STS-24c/36c/48c or STM-8c/12c/16c Payloads

To monitor STS-24c/36c/48c or STM-8c/12c/16c payloads, a master/slave configuration is available where each monitor receives 1/n of the concatenated stream. In the case of a STS-48c/STM-16c, 4 PRGMs are used in a master/slave configuration. Because the payload is four bytes interleaved, after a group of four consecutive bytes, a jump in the sequence takes place. The number of bytes that must be skipped can be determined using the number of PRGMs in the master/slave configuration. For example, to process an STS-48c/STM-16c, the number of sequence to skip is (4 PRGMS * 4 bytes) – 3 = 13. So, 13 sequences will be skipped after each group of four consecutive bytes.

The PRBS monitor can be re-initialize by the user by writing in a normal register of the master PRGM. Since all the slave PRGMs use the LFSR state of the previous PRGM in the chain, they will be re-initialize too.

13.9.4 Error Detection and Accumulation

By comparing the received PRBS byte with the calculated PRBS byte, the monitor is able to detect bit errors in the payload. A bit error is detected on a comparison mismatch of the two bytes. All bit errors are accumulated in a 16 bit error counter. The error counter will saturate at its maximum value of FFFFh, ie it will not wrap around to 0000h if further PRBS byte errors are encountered. The counter is readable via the PRGM Monitor Error Count. An indirect read to that register will initiate a transfer of the error counter into the registers for reading. The error counter is cleared when transferred into the registers and the accumulation starts at zero.

Bit errors are accumulated only when the monitor is in synchronized state. To enter the synchronize state, the monitor must have synchronized to the incoming PRBS stream and received 4 consecutive bytes without errors. Once synchronized, the monitor falls out of synchronization when forced to by programming high the RESYNC register bit, or once it detects 4 consecutive PRBS byte errors. When out of synchronization, detected errors are not accumulated.

13.10 Path Unequipped Configuration

The THPP can be configure to insert all zeros in a payload when the path is define as unequipped.

Setting a payload unequipped for a:

STS-24C/36C/48C : set UNEQ to logic one and UNEQV to logic zero for path 1 of the master and slave(s) THPP(s).

STS-12C : set UNEQ to logic one and UNEQV to logic zero for path 1 of the THPP.

STS-3C : set UNEQ to logic one and UNEQV to logic zero for the corresponding STS-3C (VC-4) path 1, 2, 3 or 4 of the THPP.

STS-1 : set UNEQ to logic one and UNEQV to logic zero for the corresponding STS-1 (VC-3) path of the THPP.

TUG-3 : set UNEQ to logic one and UNEQV to logic zero for the corresponding VC-3 path of the TU3 THPP.

Note: If, for an unequipped path, the add bus signals (AJ0J1, APL and APAIS) are not valid, the SVCA must be held in reset for the corresponding path in order to avoid AIS-P generation.

Note: For an unequipped path, the THPP fixed stuff columns overwrite must be disable for the corresponding path in order to generate a valid B3.

13.11 Clocking Options

The SPECTRA-2488 supports several clocking modes. Figure 20 and Figure 21 represent abstractions of the clocking topology.

Figure 20 OC-48 Conceptual Clocking Structure

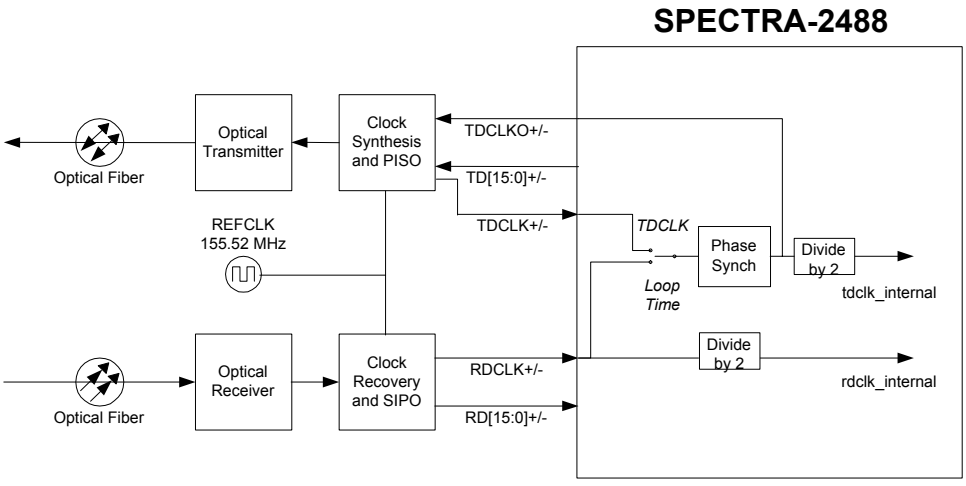
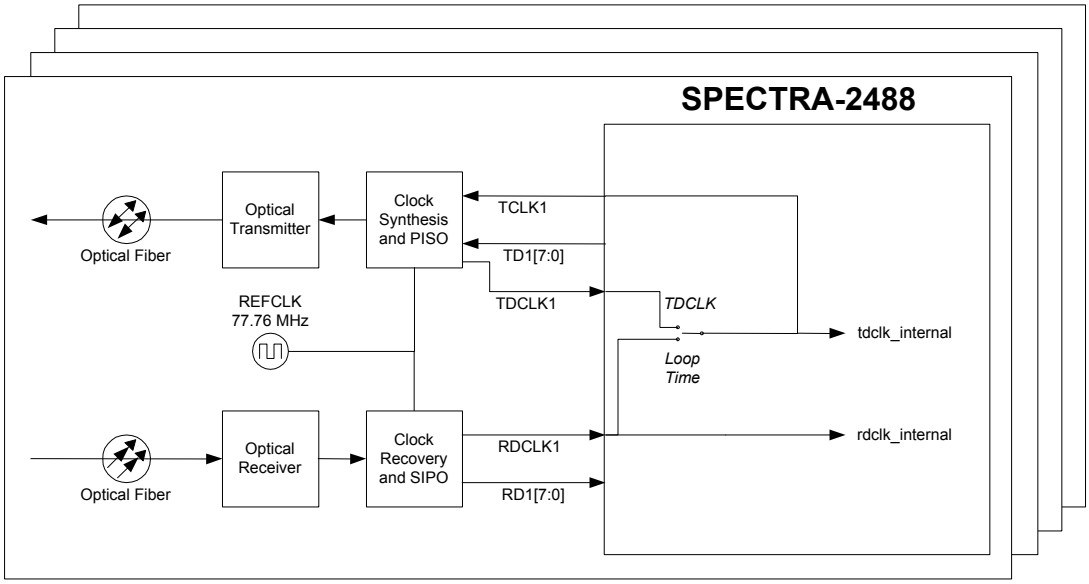


Figure 21 OC-12 Conceptual Clocking Structure



The external transmit clock is provided for all public user network interfaces (UNIs) and for private UNIs and private network node interfaces (NNIs) that are not synchronized to the recovered clock.

The transmit clock in a public UNI must conform to SONET Network Element (NE) requirements specified in Bellcore GR-253-CORE. These requirements include jitter generation, short term clock stability, phase transients during synchronization failure, and holdover. The reference clock source, 77.76 MHz in quad OC-12 mode and 155.52 MHz in single OC-48 mode, is typically a VCO (or temperature compensated VCXO) locked to a primary reference source for public UNI applications. The accuracy of this clock source should be within ±20 ppm of the reference frequency to comply with the SONET/SDH network element free-run accuracy requirements.

The transmit clock in a private UNI or a private NNI may be locked to an external reference or may free-run. The simplest implementation requires an oscillator free-running at the reference.

The loop time mode is provided for private UNIs and private NNIs that require synchronization to the recovered clock. In single OC-48 mode, the loop time mode is selected by setting the LPTDCLK bit of the Loop Timing Configuration register. In quad OC-12 mode, the loop time mode is selected independently for each slice by setting the LPTDCLK1-4 bits of the Loop Timing Configuration register. Normally, the transmit clock is locked to the receive data. In the event of a loss of signal condition, the transmit clock is synthesized from the reference clock.

In single OC-48 mode, the 155.52 MHz line clocks are divided by 2 to generate the internal clocks. In Loop Time mode, each divider may select a different edge of the line clock to produce its internal clock. The PHSYNC bit of the Loop Timing Configuration register can be enable to synchronize the rising edges of the internal clocks.

13.12 Loopback Operation

The SPECTRA-2488 supports three loopback functions: line side line loopback, line side system loopback and system side line loopback. The system side loopback mode is configurable for each path while the line side loopback modes are configurable for each slice.

The loopback modes are activated by the LLLBEN, LSLBEN, SLLBEN bits contained in the SPECTRA-2488 top-level registers.

The line side line loopback (LLLBEN) connects the high speed receive data to the high speed transmit data, and can be used for line side investigations (including the external clock recovery and clock synthesis but excluding all the SPECTRA-2488 processing). While in this mode, the entire receive path is operating normally.

Note: For proper operation, RDCLK must be muxed over TDCLK (bit 0 and 5 of register 0003H for single mode operation, bit 1 to 4 of register 0003H for quad mode operation).
Note: For proper operation after the loopback is enable, the transmit and receive datastreams must be manually frame aligned. This can be accomplish by forcing a new frame alignment using the FOOF bit in the RRMP block (Register 0080H for single mode operation and registers 0080H, 0480H, 0880H and 0C80H for quad mode operation)

The line side system loopback (LSLBEN) connects the high speed transmit data to the high speed receive data, and can be used for system side investigations (excluding the external clock recovery and clock synthesis but including all the SPECTRA-2488 path processing). While in this mode, the entire receive and transmit path are operating normally.

Note: For proper operation, TDCLK must be muxed over RDCLK (bit 12 to 15 of register 000CH for single and quad mode of operation).

The system side line loopback (SLLBEN) connects the DROP TelecomBus to the ADD TelecomBus, and can be used for line side investigations (including the external clock recovery and clock synthesis, and including the SPECTRA-2488 path processing). While in this mode, the entire receive path is operating normally. To perform this loopback, DCK and ACK must be synchronous.

Note: For proper operation when the AJ0J1_FP port contains no valid framing, the AFPEN mode (bit 14 of register 0016H) must be configure and the AFPMASK mask (bit 15 of register 001DH) must be enable.

13.13 Elastic Store Disable Operation

The SPECTRA-2488 may run in a fully synchronous mode between the line and system interfaces. In this mode the payload elastic store may be bypassed to disable all path processing on the ingress or egress frames.

When active, the elastic store disable function disables the following functions:

- Frequency adaptation between the line clock and system clock by generating new STS-1/3c/12c/24c/36c/48c (AU3/4/4-4c/4-16c orTU3) pointers.

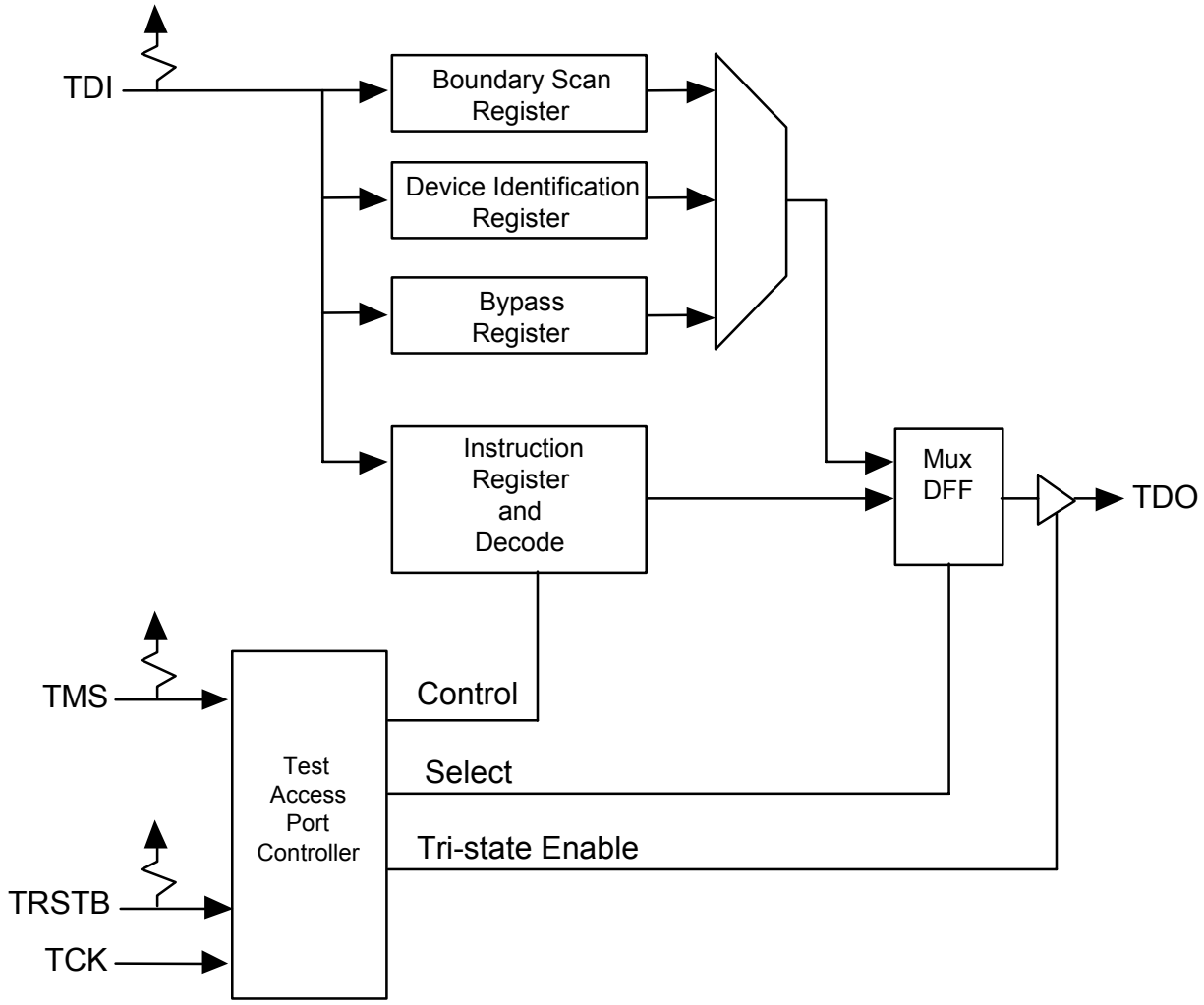
- Frame re-alignment on the system side reference (DJ0REF) or on the line side reference (TFPI).
- TU-3 to AU-3 and AU-3 to TU-3 conversion.
- Path AIS insertion.
- Path AIS indication on the TelecomBus DROP interface.
- Path overhead insertion on the transmit line side.
- ERDI-P and REI-P insertion on the line transmit side.

When running synchronously with elastic store disabled, the line clocks must be fed to the system clocks. In single OC-48 mode, RCLK1 must be fed to DCK and TCLK1 must be fed to ACK. In quad OC-12 mode, only one channel can be used synchronously. Again, RCLK1 must be fed to DCK and TCK1 must be fed to ACK.

13.14 JTAG Support

The SPECTRA-2488 supports the IEEE Boundary Scan Specification as described in the IEEE 1149.1 standards. The Test Access Port (TAP) consists of the five standard pins, TRSTB, TCK, TMS, TDI and TDO used to control the TAP controller and the boundary scan registers. The TRSTB input is the active-low reset signal used to reset the TAP controller. TCK is the test clock used to sample data on input, TDI and to output data on output, TDO. The TMS input is used to direct the TAP controller through its states. The basic boundary scan architecture is shown below.

Figure 22 Boundary Scan Architecture



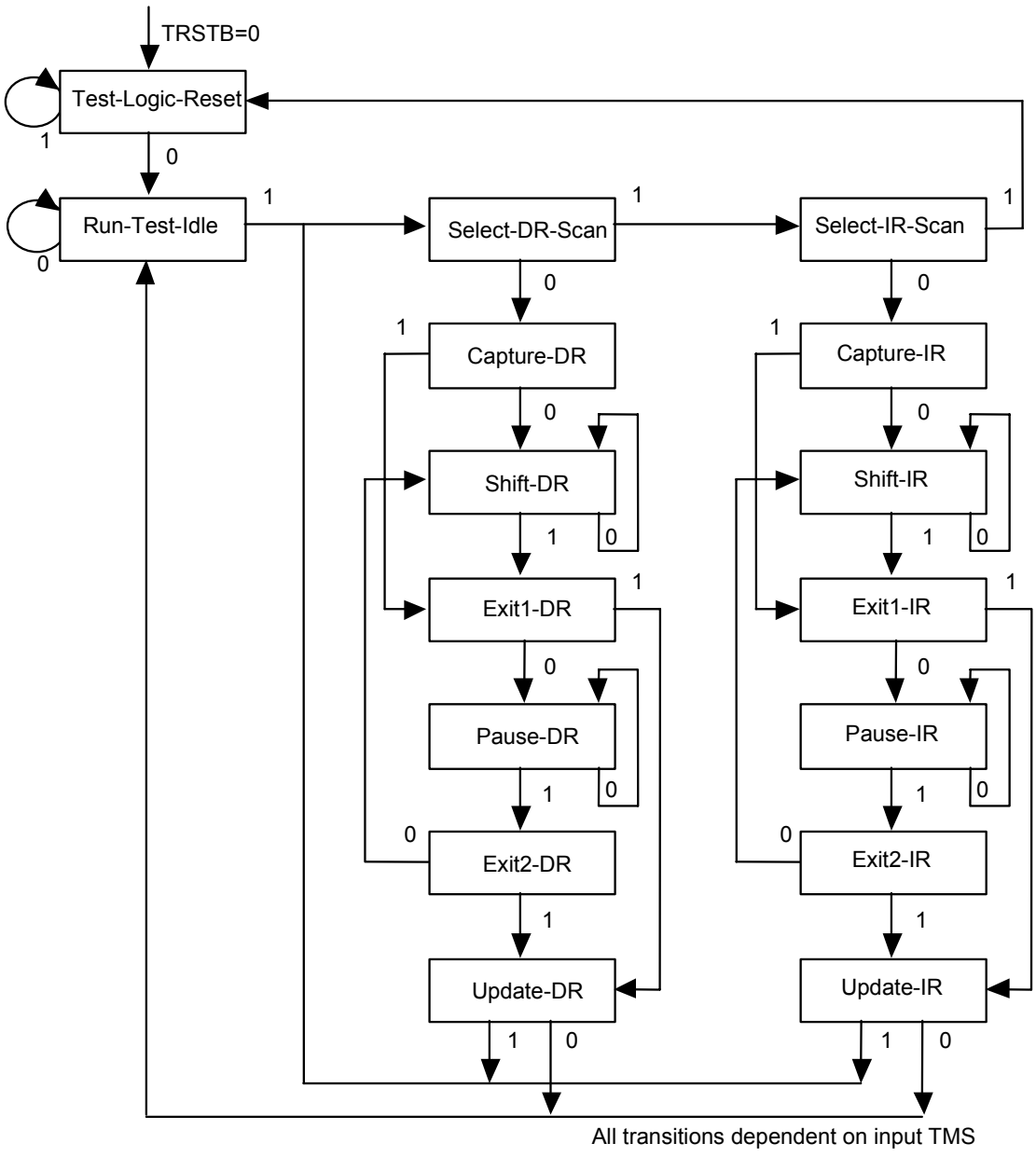
The boundary scan architecture consists of a TAP controller, an instruction register with instruction decode, a bypass register, a device identification register and a boundary scan register. The TAP controller interprets the TMS input and generates control signals to load the instruction and data registers. The instruction register with instruction decode block is used to select the test to be executed and/or the register to be accessed. The bypass register offers a single-bit delay from primary input, TDI to primary output, TDO. The device identification register contains the device identification code.

The boundary scan register allows testing of board inter-connectivity. The boundary scan register consists of a shift register place in series with device inputs and outputs. Using the boundary scan register, all digital inputs can be sampled and shifted out on primary output, TDO. In addition, patterns can be shifted in on primary input, TDI and forced onto all digital outputs.

13.14.1 TAP Controller

The TAP controller is a synchronous finite state machine clocked by the rising edge of primary input, TCK. All state transitions are controlled using primary input, TMS. The finite state machine is described below.

Figure 23 TAP Controller Finite State Machine



13.14.2 States

Test-Logic-Reset

The test logic reset state is used to disable the TAP logic when the device is in normal mode operation. The state is entered asynchronously by asserting input, TRSTB. The state is entered synchronously regardless of the current TAP controller state by forcing input, TMS high for 5 TCK clock cycles. While in this state, the instruction register is set to the IDCODE instruction.

Run-Test-Idle

The run test/idle state is used to execute tests.

Capture-DR

The capture data register state is used to load parallel data into the test data registers selected by the current instruction. If the selected register does not allow parallel loads or no loading is required by the current instruction, the test register maintains its value. Loading occurs on the rising edge of TCK.

Shift-DR

The shift data register state is used to shift the selected test data registers by one stage. Shifting is from MSB to LSB and occurs on the rising edge of TCK.

Update-DR

The update data register state is used to load a test register's parallel output latch. In general, the output latches are used to control the device. For example, for the EXTEST instruction, the boundary scan test register's parallel output latches are used to control the device's outputs. The parallel output latches are updated on the falling edge of TCK.

Capture-IR

The capture instruction register state is used to load the instruction register with a fixed instruction. The load occurs on the rising edge of TCK.

Shift-IR

The shift instruction register state is used to shift both the instruction register and the selected test data registers by one stage. Shifting is from MSB to LSB and occurs on the rising edge of TCK.

Update-IR

The update instruction register state is used to load a new instruction into the instruction register. The new instruction must be scanned in using the Shift-IR state. The load occurs on the falling edge of TCK.

The Pause-DR and Pause-IR states are provided to allow shifting through the test data and/or instruction registers to be momentarily paused.

Boundary Scan Instructions

The following is a description of the standard instructions. Each instruction selects a serial test data register path between input, TDI and output, TDO.

13.14.3 Instructions

BYPASS

The bypass instruction shifts data from input, TDI to output, TDO with one TCK clock period delay. The instruction is used to bypass the device.

EXTEST

The external test instruction allows testing of the interconnection to other devices. When the current instruction is the EXTEST instruction, the boundary scan register is place between input, TDI and output, TDO. Primary device inputs can be sampled by loading the boundary scan register using the Capture-DR state. The sampled values can then be viewed by shifting the boundary scan register using the Shift-DR state. Primary device outputs can be controlled by loading patterns shifted in through input TDI into the boundary scan register using the Update-DR state.

SAMPLE

The sample instruction samples all the device inputs and outputs. For this instruction, the boundary scan register is placed between TDI and TDO. Primary device inputs and outputs can be sampled by loading the boundary scan register using the Capture-DR state. The sampled values can then be viewed by shifting the boundary scan register using the Shift-DR state.

IDCODE

The identification instruction is used to connect the identification register between TDI and TDO. The device's identification code can then be shifted out using the Shift-DR state.

STCTEST

The single transport chain instruction is used to test out the TAP controller and the boundary scan register during production test. When this instruction is the current instruction, the boundary scan register is connected between TDI and TDO. During the Capture-DR state, the device identification code is loaded into the boundary scan register. The code can then be shifted out output, TDO using the Shift-DR state.

13.15 Board Design Recommendations

The noise environment and signal integrity are often the limiting factors in system performance. Therefore, the following board design guidelines must be followed in order to ensure proper operation:

1. Use a single plane for both digital and analog grounds.

2. Provide separate +3.3 volt analog transmit, +3.3 volt analog receive, and +3.3 volt digital supplies, but otherwise connect the supply voltages together at one point close to the connector where +3.3 volts is brought to the card.

3. Provide separate +1.8 volt analog transmit, +1.8 volt analog receive, and +1.8 volt digital supplies, but otherwise connect the supply voltages together at one point close to the connector where +1.8 volts is brought to the card.

4. Ferrite beads are not advisable in digital switching circuits because inductive spiking (di/dt noise) is introduced into the power rail. Simple RC filtering is the best approach provided care is taken to ensure the IR drop in the resistance does not lower the supply voltage below the recommended operating voltage.

5. High-frequency decoupling capacitors are recommended for the analog power pins as close to the package pin as possible. Separate decoupling is required to prevent the transmitter from coupling noise into the receiver and to prevent transients from coupling into some reference circuitry. See the section on Power Supplies for more details.

6. The high speed signals (RDCLK+/-, RFP+/-, RD+/-, TDCLK+/-, TFPI+/-, TDCLKO+/-, TD+/-, and TFPO+/-) must be routed with 50 ohm controlled impedance circuit board traces and must be terminated with a matched load. Normal TTL-type design rules are not recommended and will reduce the performance of the device. See the section on interfacing to ECL and PECL devices for more details.

Please refer to the SPECTRA-2488 reference design (PMC-2000179, PMC-2000185) for further recommendations

13.16 Power Up Sequence

Due to ESD protection structures in the pads it is necessary to exercise caution when powering a device up or down. ESD protection devices behave as diodes between power supply pins and from I/O pins to power supply pins. Under extreme conditions it is possible to blow these ESD protection devices or trigger latch up.

In order for the SPECTRA-2488 to operate correctly, all 3.3V power supplies (AVDH, QAVD and VDDO) must be on before the 1.8V supplies (AVDL and VDDI).

The recommended power supply sequencing follows:

1. To prevent damage to the ESD protection on the device inputs the maximum DC input current specification must be respected. This is accomplished by either ensuring that the VDDO power is applied before input pins are driven or by increasing the source impedance of the driver so that the maximum driver short circuit current is less than the maximum DC input current specification.

2. QAVD power must be supplied either after VDDO or simultaneously with VDDO to prevent current flow through the ESD protection devices which exist between QAVD and VDDO power supplies. To prevent forward biasing the ESD protection diode between QAVD and VDDO supplies, the differential voltage measured between these power supplies must be less than 0.5 volt.

   This recommended differential voltage is to include peak to peak noise on the QAVD and VDDO power supplies as digital noise will otherwise be coupled into the analog circuitry. Current limiting can be accomplished by using an off chip three terminal voltage regulator supplied by a quiet high voltage supply.

3. AVDH power must be supplied either after QAVD and VDDO or simultaneously with QAVD and VDDO or it must be current limited to the maximum latchup current specification. (100 mA). To prevent forward biasing the ESD protection diode between AVDH and QAVD supplies, the differential voltage measured between these power supplies must be less than 0.5 volt.

   This recommended differential voltage is to include peak to peak noise on the AVDH and QAVD power supplies as digital noise will otherwise be coupled into the analog circuitry. Current limiting can be accomplished by using an off chip three terminal voltage regulator supplied by a quiet high voltage supply. The relative power sequencing of the multiple AVDH power supplies is not important.

4. AVDL power must be supplied either after VDDI or simultaneously with VDDI or it must be current limited to the maximum latchup current specification. (100 mA). To prevent forward biasing the ESD protection diode between AVDL and VDDI supplies, the differential voltage measured between these power supplies must be less than 0.5 volt.

   This recommended differential voltage is to include peak to peak noise on the AVDL and VDDI power supplies as digital noise will otherwise be coupled into the analog circuitry. Current limiting can be accomplished by using an off chip three terminal voltage regulator supplied by a quiet high voltage supply. The relative power sequencing of the multiple AVDL power supplies is not important.

5. Power down the device in the reverse sequence. Use the above current limiting technique for the analog power supplies. Small offsets in VDDO/AVDH and VDDI/AVDL discharge times will not damage the device.

Please refer to the SPECTRA-2488-reference design (PMC-2000179, PMC-2000185) for further recommendations.

Note: Analog is very tolerant of noise - no regulator required.

Note: Since on any board there is always a delay between different devices activating, the SPECTRA-2488 is able to sustain +/-100 ma drive on its input pins for less then 100 ms while powering up.

13.17 Interfacing to ECL or PECL Devices

Only a few passive components are required to convert the signals to ECL (or PECL) logic levels. Figure 24 illustrates the recommended configurations for ECL voltage levels..

The combination of the 49.9 Ω and 63.4 Ω resistors divide the voltage down to a nominally 800mV swing. The 49.9 Ω resistors also terminate the signals.

The RDCLK, RFP, TDCLK and TFPI input signals should be terminated as the RD input signals. The TDCLKO and TFPO output signals should be terminated as the TD output signals.

Figure 24 Interfacing SPECTRA-2488 PECL to 3.3V Devices

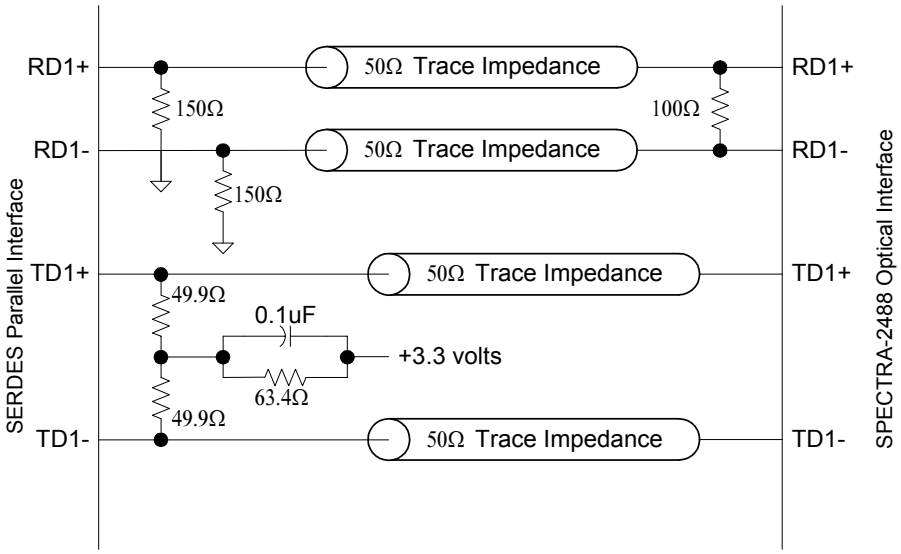
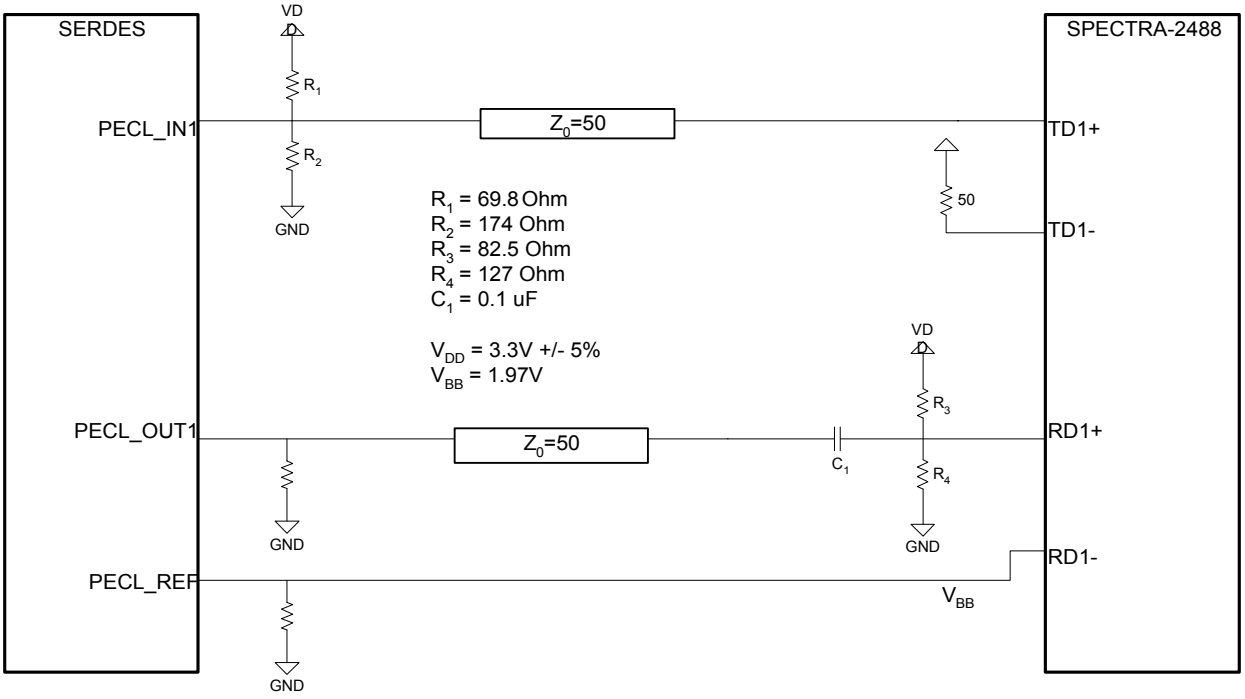


Figure 25 Interfacing SPECTRA-2488 differential PECL to single ended PECL Devices



NOTES:
If no PECL reference from SERDES exists, V_{BB} can be supplied to RD1- with a simple resistor divider between V_{DD} and GND. VDD of the receive side Thevenin termination must be the same as the VDD for the SERDES device.

Figure 25 illustrates the recommended configurations to interface the SPECTRA-2488 differential PECL to single ended PECL Devices.

Please refer to the SPECTRA-2488 reference design (PMC-2000179, PMC-2000185) for further recommendations.

14 Functional Timing

14.1 ADD Parallel TelecomBus

Figure 26 shows the timing of the ADD TelecomBus interface. Timing is provided by ACLK. SONET/SDH data is carried in the AD[*X*][7:0], where '*X*' denotes one of the four sections of the Incoming TelecomBus. The bytes are arranged in order of transmission in an STS-12/STM-4 stream. Each transport/section overhead byte is labeled by Sx,y and type. Payload bytes are labeled by Sx,y and Bn, where 'n' is the active offset of the byte.

A timeslot naming strategy and assignment on an AD[*X*][7:0] bus is shown in Figure 26. Within Sx,y, the STS-3/STM-1 number is given by 'x' and the column number within the STS-3/STM-1 is given by 'y'. The APL[*X*] signal is set high to mark payload bytes and is set low at all other bytes. The composite transport frame and payload frame signal AJ0J1[*X*] is set high with APL[*X*] set low to mark the J0 byte of a transport frame. AJ0J1[*X*] is set high with APL[*X*] also set high to mark the J1 byte of all the streams within AD[*X*][7:0].

High order streams in AIS alarm are indicated by the APAIS[*X*] signal. Assertion of the AIS alarm will cause the cell/packet delineation blocks to lose alignment. The ACMP signal selects the active connection memory page in the Time-slot Interchange block. It is only valid at the J0 byte position and is ignored at all other positions within the transport frame. The J0 byte position on all four buses must be aligned.

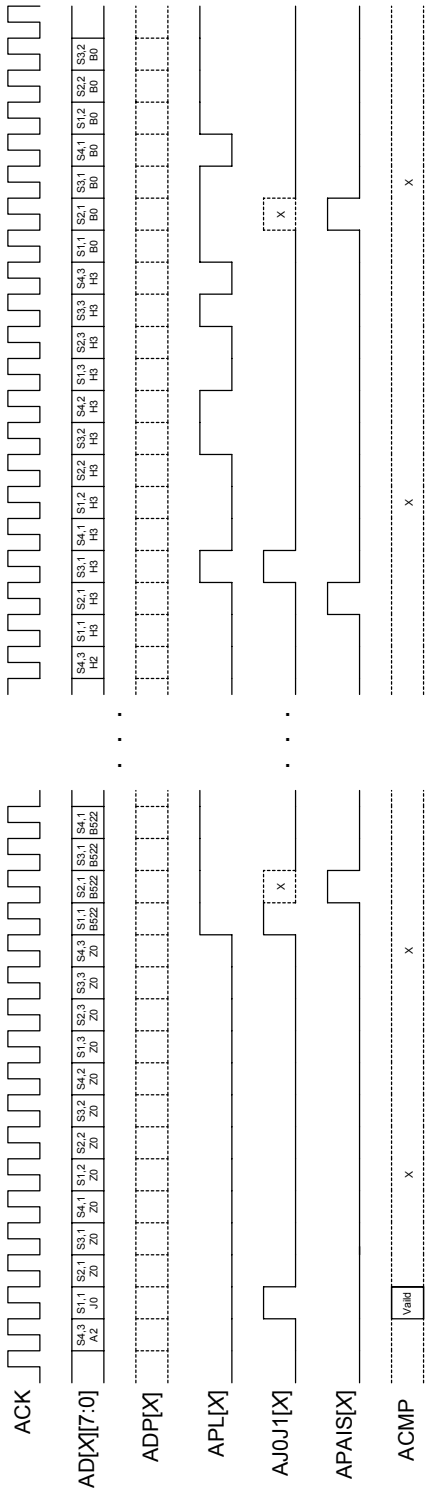
In Figure 26, timeslots numbers S1,x, S2,y, and S4,z are configured as STS-1/STM-0 operation. Timeslot number S3,n is configured for STS-3c/STM-1 operation. Stream S1,1 (STM-1 #1, AU3 #1) is shown to have an active offset of 522 by the high level on APL[*X*] and AJ0J1[*X*] at byte S1,1/B522. Stream S2,1 (STM-1 #2, AU3 #1) is shown to be in high-order path AIS (APAIS[*X*] set high at bytes S2,1/Z0, S2,1/B522, S2,1/H3 and S2,1/B0). STM-1 #3 is a configured in AU4 mode and is shown to undergo a negative pointer justification event, changing its active offset from 0 to 782. This is shown by AJ0J1[*X*] being set high at byte S3,1/H3 and APL[*X*] being set high at bytes S3,1/H3, S3,2/H3 and S3,3/H3.

For the case where an STS-48c/STM-16c is carried on the four buses AD[X][7:0], the J0 indication is expected on all four buses (AJ0J1[X] = 1 and APL[X] = 0) at the same time. The J1 indication is expected only on the first bus (AJ0J1[1] = 1 and APL[1] = 1, AJ0J1[4:2] = 0 and APL[1] = 1).

ACMP is sampled at the clock cycle where the J0 indication is given (AJ0J1[*X*] is logic 1 and APL[*X*] is logic 0). ACMP is used to select the incoming memory page in the STSI when the parallel TelecomBus is in use.

The arrangement shown in Figure 26 is for illustrative purposes only; other configurations, alarm conditions, active offsets and justification events, etc. are possible.

Figure 26 ADD Parallel TelecomBus Timing



14.2 DROP Parallel TelecomBus

Figure 27 shows the timing of the DROP TelecomBus interface. Timing is provided by DCLK. SONET/SDH data is carried in the DD[*X*][7:0], where '*X*' denotes one of the four sections of the DROP TelecomBus. The bytes are arranged in order of transmission in an STS-12/STM-4 stream. The STSI block can be used to rearrange timeslots between the system side and the line side of the SPECTRA-2488.

The timeslot naming strategy and assignment is shown in Figure 27. Each transport/section overhead byte is labeled by Sx,y and type. Payload bytes are labeled by Sx,y and Bn, where 'n' is the active offset of the byte. Within Sx,y, the STS-3/STM-1 number is given by 'x' and the column number within the STS-3/STM-1 is given by 'y'. The DPL[*X*] signal is set high to mark payload bytes and is set low at all other bytes. All four DJ0J1[4:1] signals are set high with all four DPL[4:1] signals set low to mark the J0 byte of a transport frame. DJ0J1[*X*] is set high with DPL[*X*] also set high to mark the J1 byte of all the streams within DD[*X*][7:0]. High order streams in alarm are indicated by the DALARM[*X*] signal.

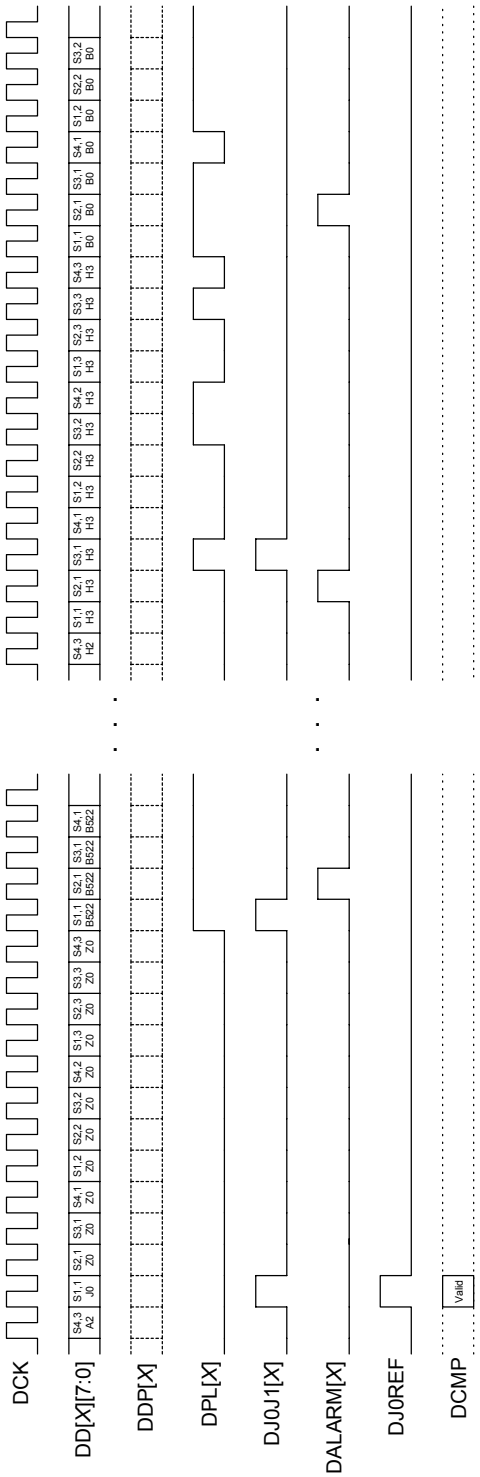
In Figure 27, timeslots S1,x, S2,y, and S4,z are configured for STS-1/STM-0 operation. Timeslot S3,n is configured for STS-3c/STM-1 operation. Stream S1,1 (STM-1 #1, AU3 #1) is shown to have an active offset of 522 by the high level on DPL[*X*] and DJ0J1[*X*] at byte S1,1/B522. Stream S2,1 (STM-1 #2, AU3 #1) is shown to be in high-order path alarm (DALARM[*X*] set high at bytes S2,1/Z0, S2,1/B522, S2,1/H3 and S2,1/B0). STM-1 #3 is a configured in AU4 mode and is shown to undergo a negative pointer justification event, changing its active offset from 0 to 782. This is shown by DJ0J1[*X*] being set high at byte S3,1/H3 and DPL[*X*] being set high at bytes S3,1/H3, S3,2/H3 and S3,3/H3. Stream S4,1 is shown to undergo a positive pointer justification event as indicated by the low level on DPL[*X*] at byte S4,1/B0.

For the case where an STS-48c/STM-16c is carried on the four buses DD[4:1][7:0], the J0 indication is given on all four buses (DJ0J1[X] = 1 and DPL[X] = 0) at the same time. The J1 indication is given only on the first bus (DJ0J1[1] = 1 and DPL[1] = 1, DJ0J1[4:2] = 0 and DPL[1] = 1).

DCMP is sampled at the clock cycle where the J0 indication is given (DJ0J1[*X*] is logic 1 and DPL[*X*] is logic 0). DCMP is used to select the incoming memory page in the STSI when the parallel TelecomBus is in use.

The arrangement shown in Figure 27 is for illustrative purposes only; other configurations, alarm conditions, active offsets and justification events, etc. are possible.

Figure 27 DROP Parallel TelecomBus



14.3 Receive Transport Overhead

Figure 28 RTOH output timing

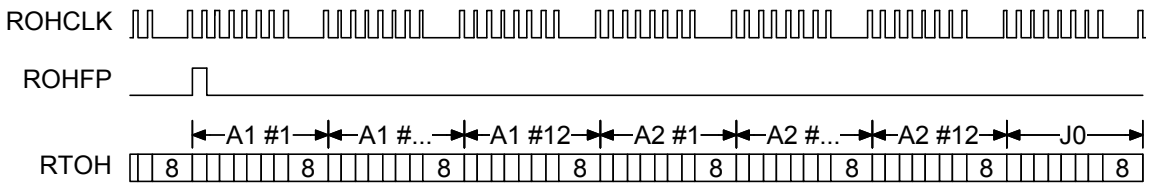


Figure 29 RTOH and ROHFP output timing

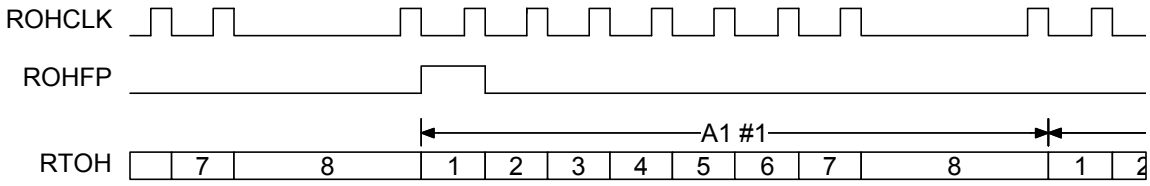


Figure 28 shows the receive transport overhead (RTOH) functional timings. ROHCLK is a 20.736 MHz clock generated by gapping a 25.92 MHz clock (33% high duty cycle). 2592 bits (9x3x12 bytes) are output on RTOH between two ROHFP assertions.

Figure 29 shows that RTOH and ROHFP are aligned with the falling edge of ROHCLK. The rising edge of ROHCLK should be used to sample RTOH and ROHFP. Sampling ROHFP high identifies the MSB of the first A1 byte on RTOH.

14.4 Receive Section and Line DCC

Figure 30 RLD and RSLD output timing

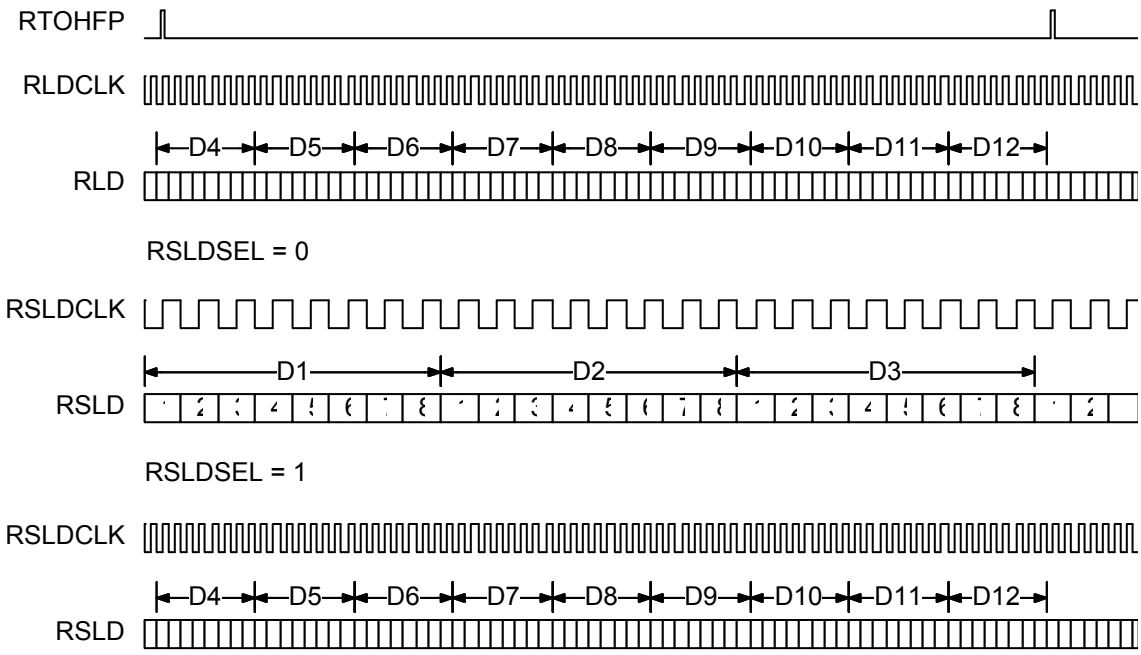
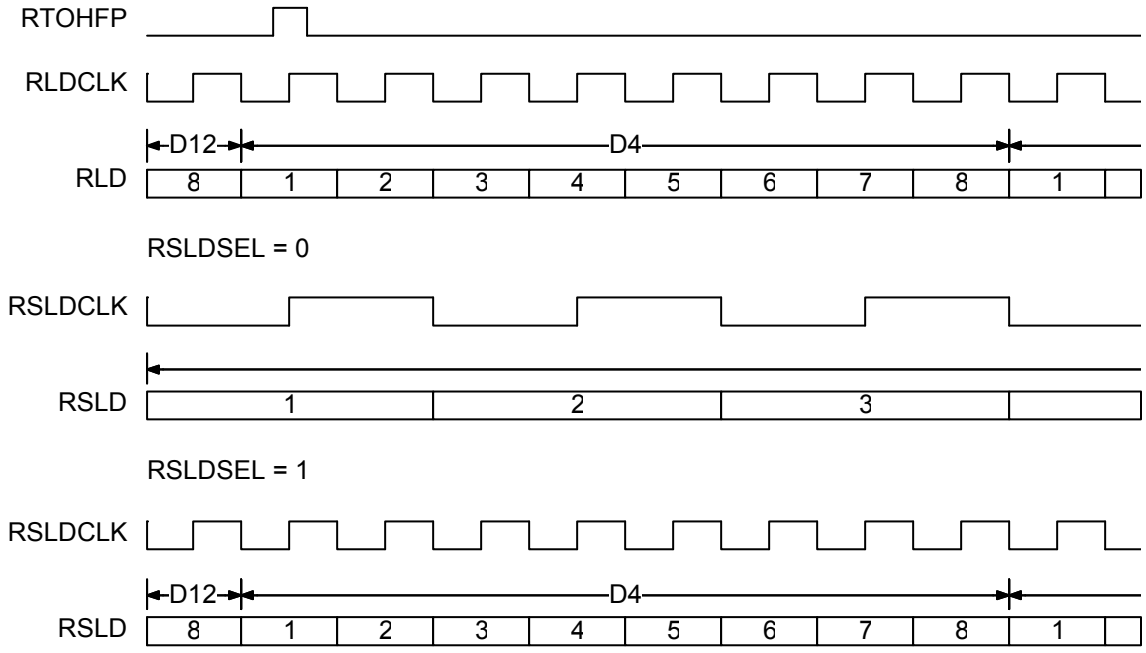


Figure 30 and Figure 31 show the receive line DCC (RLD) and the receive section/line DCC (RSLD) functional output timings. RLD and RLDCLK are carrying the line DCC bytes (D4-D12). When RSLDSEL is set to zero, RSLD and RSLDCLK are carrying the section DCC bytes (D1-D3). When RSLDSEL is set to one, RSLD and RSLDCLK are carrying the line DCC bytes (D4-D12).

Figure 31 RLD, RSLD and ROHFP output timing



RLDCLK is a 576 KHz clock and RLD is aligned with the falling edge of RLDCLK. The rising edge of RLDCLK should be used to sample RLD and ROHFP. Sampling ROHFP high identifies the MSB of the D4 byte on the RLD output.

RSLDCLK is a 192 KHz clock when carrying the section DCC and a 576 KHz clock when carrying the line DCC. RSLD is aligned with the falling edge of RSLDCLK. The rising edge of RSLDCLK should be used to sample RSLD and ROHFP. Sampling ROHFP high identifies the MSB of the D1 or D4 byte on the RSLD output.

14.5 Receive Path Overhead Port

Figure 32 shows the receive path overhead (RPOH) functional timings. The RPOH port (RPOH, RPOHEN and B3E) is used to output the POH bytes of the STS (VC) payloads and the path BIP-8 errors. The POH bytes are output on RPOH MSB first in the same order that they are received. Since ROHFP is synchronized on the transport frame, zero, one or two path overhead can be output per path per frame. RPOHEN is used to indicate new POH bytes on RPOH. RPOHEN is either asserted or de asserted for the nine POH bytes. The path BIP-8 errors are output on B3E at the same time the path trace byte is output on RPOH. Optionally, block BIP-8 errors can be output on B3E.

Note: RPOHEN will be asserted to validate zero, one or two opportunities per path per frame out of three opportunities. RPOHEN opportunities will alternate from path to path and from frame to frmae based on pointer movement.

Figure 32 shows that RPOH and RPOHEN are aligned with the falling edge of ROHCLK. The rising edge of ROHCLK should be used to sample RPOH and RPOHEN. Sampling ROHFP high identifies the MSB of the path trace byte of STS-1/STM-0 #1 on RPOH and the first possible path BIP-8 error of STS-1/STM-0 #1 on B3E.

Figure 32 RPOH Output Timing

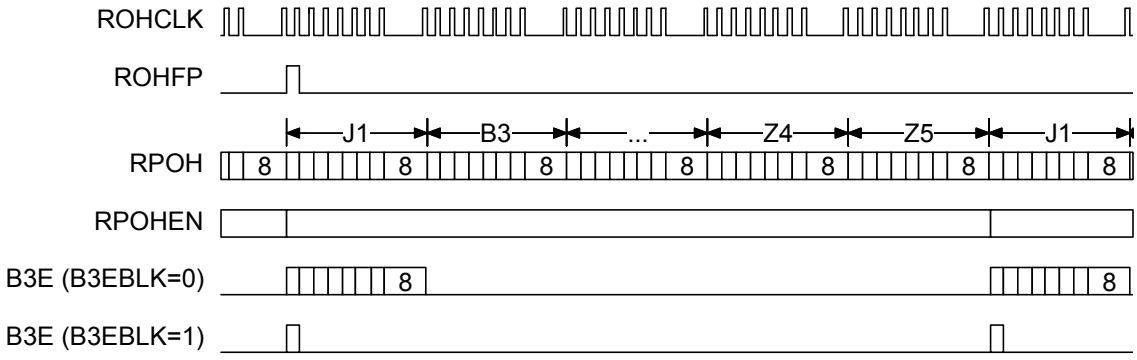
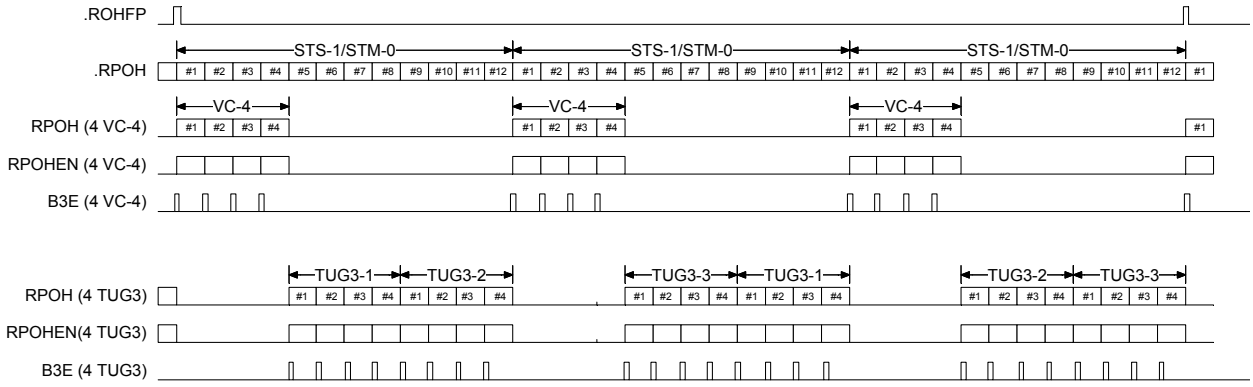


Figure 33 shows the STS-1/STM-0 time slots assignment on RPOH. Since ROHFP is synchronized on the transport frame, zero, one or two path overhead can be output per path per frame. To avoid loosing any POH bytes, three time slots are assigned per path per frame. In STS (AU) mode, the time slots are repeatedly assigned from STS-1/STM-0 #1 to #12. Figure 33 shows the case of a STM-4 data stream carrying four VC-4 payloads. Only the master VC-4 STS-1/STM-0 time slots contain valid POH bytes. Figure 33 shows the case of four VC-4 payloads carrying four TUG3 payloads. Both the master and the slave VC-4 STS-1/STM-0 time slots contain valid POH bytes.

Figure 33 RPOH STS-1/STM-0 Time Slots Output Timing



14.6 Transmit Transport Overhead

Figure 34 TTOH and TTOHEN Input Timing

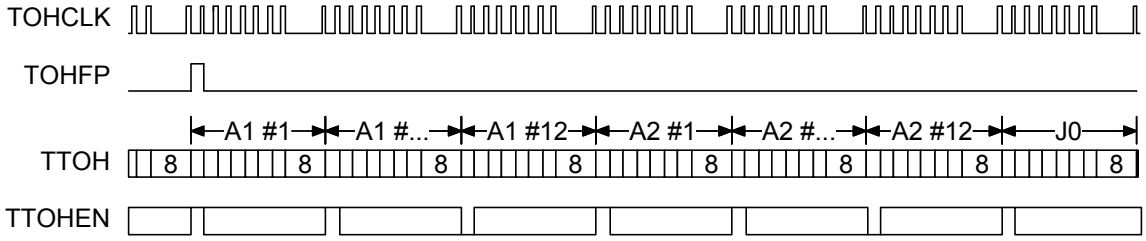


Figure 35 TTOH and TOHFP Input Timing

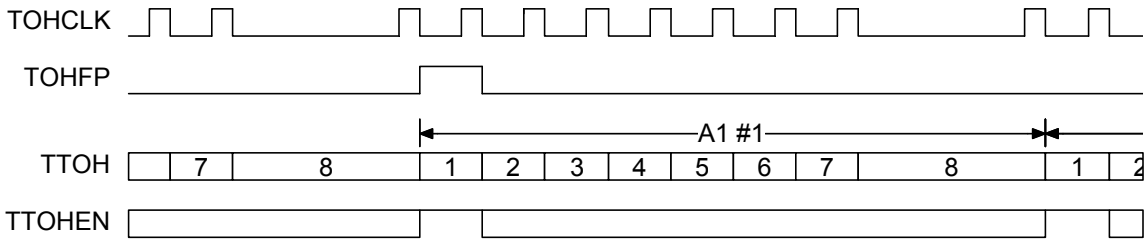


Figure 34 shows the transmit transport overhead (TTOH) functional timings. TOHCLK is a 20.736 MHz clock generated by gapping a 25.92 MHz clock (33% high duty cycle). 2592 bits (9x3x12 bytes) are input on TOH between two TOHFP assertions.

TTOHEN is used to validate the insertion of the corresponding byte on TTOH. When TTOHEN is sampled high on the MSB of the byte, the byte will be inserted in the transport overhead. When TTOHEN is sampled low on the MSB of the byte, the byte is not inserted. TTOH and TTOHEN are sampled with the rising edge of TOHCLK. TOHFP is aligned with the falling edge of TOHCLK. The rising edge of TOHCLK should be used to sample TOHFP. Sampling TOHFP high identifies the MSB of the first A1 byte on TTOH.

14.7 Transmit Section and Line DCC

Figure 36 TLD and TSLD Input Timing

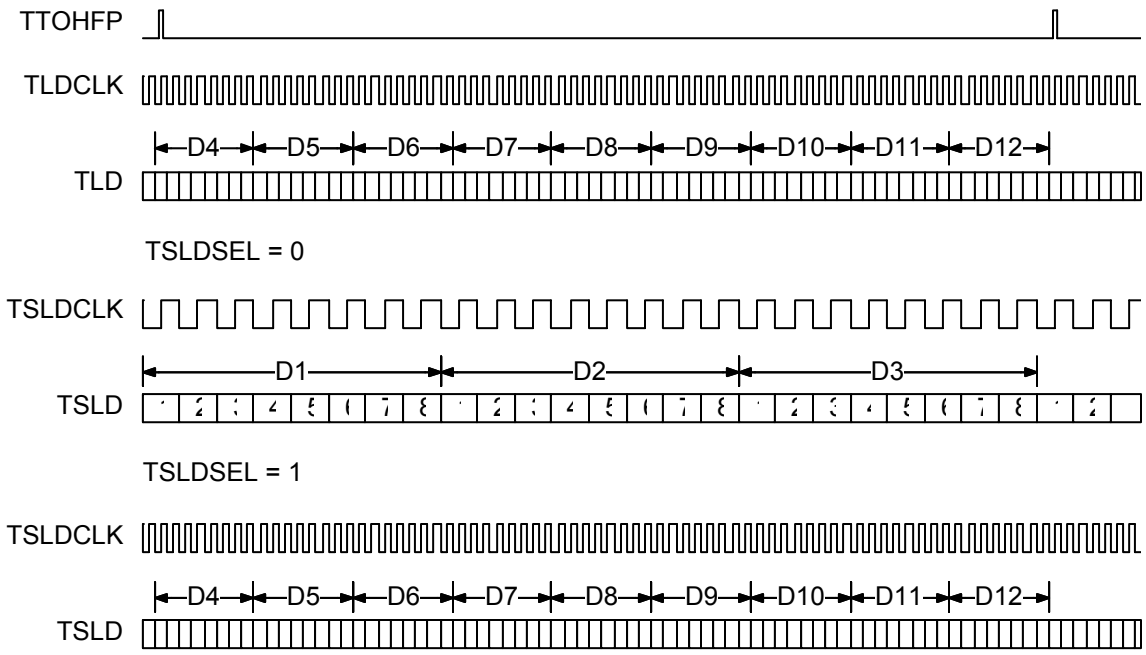
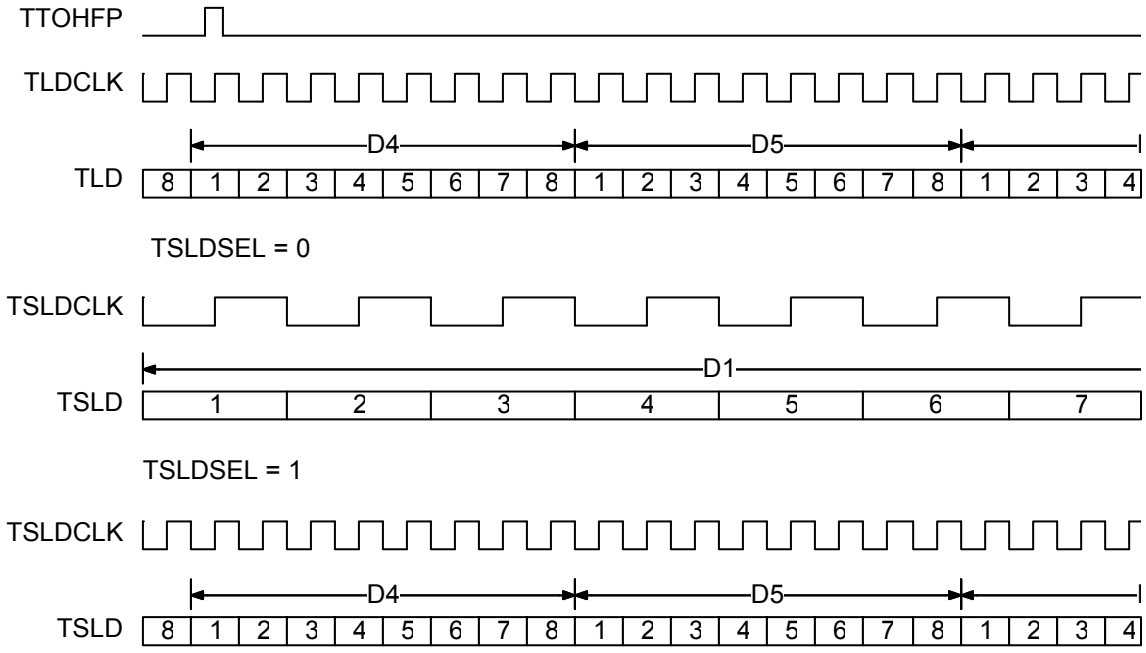


Figure 36 and Figure 37 show the transmit line DCC (TLD) and the transmit section/line DCC (TSLD) functional input timings. TLD and TLDCLK are carrying the line DCC bytes (D4-D12). When TSLDSEL is set to zero, TSLD and TSLDCLK are carrying the section DCC bytes (D1-D3). When TSLDSEL is set to one, TSLD and TSLDCLK are carrying the line DCC bytes (D4-D12).

Figure 37 TLD, TSLD and TOHFP Input Timing



TLDCLK is a 576 KHz clock. TSLDCLK is a 192 KHz clock when carrying the section DCC and a 576 KHz clock when carrying the line DCC. TLD and TSLD are sampled with the rising edge of TLDCLK and TSLDCLK. TLDCLK and TSLDCLK are generated such that the rising edge of TLDCLK and TSLDCLK can be used by external logic to sample TOHFP with proper setup and hold time. Sampling TOHFP high identifies the MSB of the D4 byte on TLD and the MSB of the D1 or D4 byte on TSLD.

14.8 Transmit Path Overhead

Figure 38 shows the transmit path overhead (TPOH) functional timings. The TPOH port (TPOH, TPOHEN and TPOHRDY) is used to input the POH bytes of the STS (VC) payloads. The POH bytes are input on TPOH MSB first in the same order that they are transmit. Since TOHFP is synchronized on the transport frame, zero, one or two path overhead can be input per path per frame.

TPOHRDY is asserted to indicate that the SPECTRA is ready to receive POH bytes. TPOHEN is used to validate the insertion of the corresponding byte on TPOH. If TPOHRDY is logic high and TPOHEN is sampled high on the MSB of the byte, the byte will be inserted in the path overhead. When TPOHEN is sampled low on the MSB of the byte, the byte is not inserted in the output stream. If TPOHRDY is logic low and TPOHEN is sample high on the MSB of the byte, the byte will not be inserted in the path overhead and must be represented at the next opportunity.

TPOH and TPOHEN are sampled with the rising edge of TOHCLK. TPOHRDY is aligned with the falling edge of TOHCLK. The rising edge of TOHCLK should be used to sample TPOHRDY. Sampling TOHFP high identifies the MSB of the path trace byte of STS-1/STM-0 #1 on TPOH.

Figure 38 RPOH Input Timing

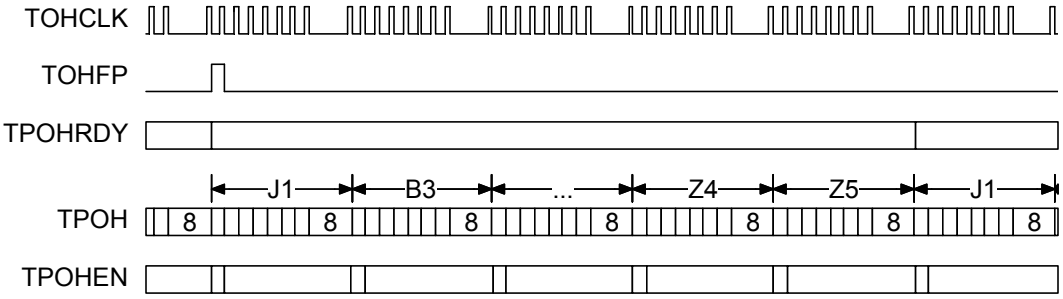
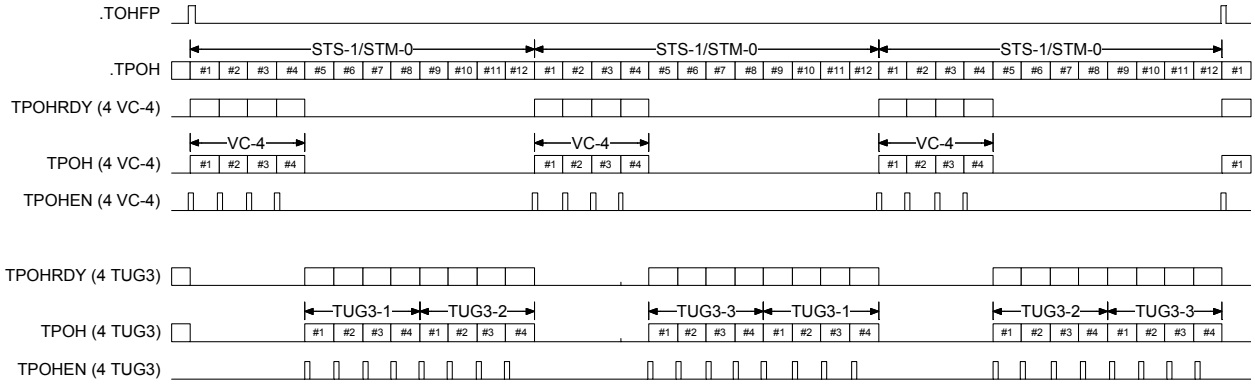


Figure 39 shows the STS-1/STM-0 time slots assignment on TPOH. Since TOHFP is synchronized on the transport frame, zero, one or two path overhead can be input per path per frame. To avoid loosing any POH bytes, three time slots are assigned per path per frame. In STS (AU) mode, the time slots are repeatedly assigned from STS-1/STM-0 #1 to #12. Figure 39 shows the case of a STM-4 data stream carrying four VC-4 payloads. Only the master VC-4 STS-1/STM-0 time slots contain valid POH bytes. Figure 39 shows the case of four VC-4 payloads carrying four TUG3 payloads. Both the master and the slave VC-4 STS-1/STM-0 time slots contain valid POH bytes.

Figure 39 TPOH STS-1/STM-0 Time Slots Input Timing



14.9 Receive Ring Control Port

Figure 40 shows the receive ring control port (RRCP) functional timings. RRCPDAT serially outputs all the section, line and path defects detected in the receive data stream. Since ROHFP is synchronized on the transport frame two path overheads are output per path per frame.

RRCPDAT is aligned with the falling edge of ROHCLK. The rising edge of ROHCLK should be used to sample RRCPDAT. Sampling ROHFP high with ROHCLK identifies the OOF defect on RRCP. Table 19 defines RRCP in function of the bit position.

Figure 40 RRCP Output Timing

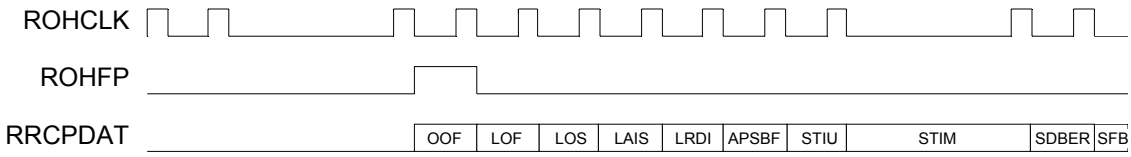


Table 19 Ring Control Port Bit Definition

Bit Position	Type	Defect
1	Section	OOF
2	Section	LOF
3	Section	LOS
4	Section	LAIS
5	Section	LRDI
6	Section	APSBF
7	Section	STIU
8	Section	STIM
9	Section	SDBER
10	Section	SFBER
11-12	Section	GROWTH[1:0]
13-16	Section	0
17-32	Section	APS[15:0]
33-40	Section	LBIPCNT[7:0]
41	Section	LRDIINS
42-64	Section	0
65	Path	PLOP
66	Path	PAIS
67	Path	PPLU
68	Path	PPLM
69	Path	PUNEQ
70	Path	PPDI
71	Path	PRDI
72	Path	PERDI
73-75	Path	PERDIV[2:0]
76	Path	PTIU
77	Path	PTIM

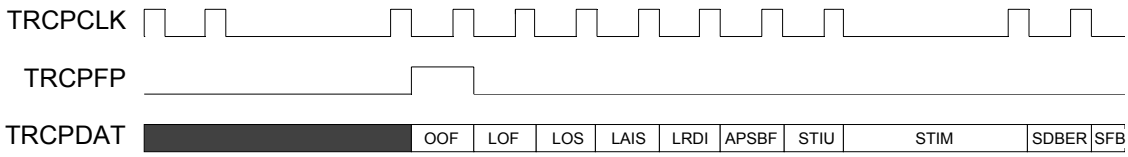
Bit Position	Type	Defect
78-79	Path	PGROWTH[1-0]
80	Path	0
81-84	Path	PBIPCNT[3:0]
85-87	Path	PERDIINS[2:0]
88-96	Path	0
97-128	Path	STS-1/STM-0 #2
...	...	...
417-448	Path	STS-1/STM-0 #12
449-480	TU3 Path	TU3 STS-1/STM-0 #1
...	...	...
801-832	TU3 Path	TU3 STS-1/STM-0 #12
833-864	Path	STS-1/STM-0 #1
...	...	...
1185-1216	Path	STS-1/STM-0 #12
1217-1248	TU3 Path	TU3 STS-1/STM-0 #1
...	...	...
1569-1600	TU3 Path	TU3 STS-1/STM-0 #12
1601-2592	None	0

14.10 Transmit Ring Control Port

Figure 41 shows the transmit ring control port (TRCP) functional timings. TRCPDAT serially inputs all the section, line and path defects detected in the receive data stream. The TRCP port is usually connected to the RRCP port of a mate SPECTRA. TRCP is not restricted to a RRCP port as long as the format and the timings between TRCPCLK, TRCPFP and TRCPDAT are met.

Sampling TRCPFP high with TRCPCLK identifies the OOF defect on TRCPDAT. TRCPFP must be asserted to initiate TRCPDAT capture. Only the first 1600 bits, after TRCPFP assertion, are considered valid and part of the ring control port. Table 19 defines TRCPDAT in function of the bit position.

Figure 41 TRCP Input Timing

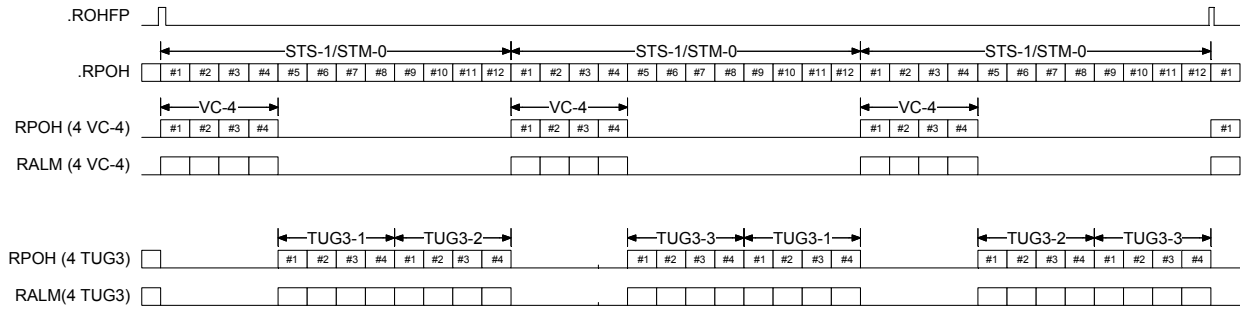


14.11 Receive Path Alarm

Figure 42 shows the receive path alarm (RALM) functional timings. RALM is used to output the "ORing" of the enabled path defects Figure 42 shows the STS-1/STM-0 time slots assignment on RALM which is identical to RPOH. Each STS-1/STM-0 time slot is either high or low for 72 ROHCLK clock cycles (9 POH bytes x 8 bits).

RALM is aligned with the falling edge of ROHCLK. The rising edge of ROHCLK should be used to sample RALM. Sampling ROHFP high identifies STS-1/STM-0 #1 on RALM.

Figure 42 RALM Output Timing



15 Absolute Maximum Ratings

Maximum rating are the worst case limits that the device can withstand without sustaining permanent damage. They are not indicative of normal mode operation conditions.

Table 20 Absolute Maximum Ratings

Storage Temperature	-40°C to +125°C
3.3V Supply Voltage	-0.3V to +4.6V
1.8V Supply Voltage	-0.3V to +2.5V
Voltage on Any Digital Pin	-0.3V to V_{VDDO}+0.3V
Voltage on Any PECL Pin	-0.3V to +3.46V
Static Discharge Voltage	±1000 V
Latch-Up Current	±100 mA
DC Input Current	±20 mA
Lead Temperature	+230°C
Absolute Maximum Junction Temperature	+150°C
Overshoot Tolerance on Input Pins	-2.0 V to VDDO+2.0V less 10 ns, 100 mA max
Maximum Overshoot on Output Pins	-2.0 V to VDDO+2.0V less 10 ns, 20 mA max

Notes on Absolute Maximum Ratings:

1. Most output pins require termination circuitry.

16 D.C. Characteristics

T_A = -40°C to T_J = +125°C, $V_{VDDI} = V_{VDDItypical} \pm 5\%$, $V_{VDDO} = V_{DDOtypical} \pm 5\%$
$V_{AVDL} = V_{AVDLtypical} \pm 5\%$, $V_{AVDH} = V_{AVDHtypical} \pm 5\%$
(Typical Conditions: T_C = 25°C, $V_{VDDI} = V_{AVDL}$ =1.8V, $V_{VDDO} = V_{AVDH}$ = 3.3V)

Table 21 D.C. Characteristics

Symbol	Parameter	Min	Typ	Max	Units	Conditions
V_{VDDI}	Power Supply	1.71	1.8	1.89	Volts	
V_{VDDO}	Power Supply	3.14	3.3	3.46	Volts	
V_{AVDL}	Power Supply	1.71	1.8	1.89	Volts	
V_{AVDH}	Power Supply	3.14	3.3	3.46	Volts	
V_{IL}	Input Low Voltage			0.8	Volts	Guaranteed Input Low voltage
V_{IH}	Input High Voltage	2.0			Volts	Guaranteed Input High voltage
V_{OL}	Output or Bi-directional Low Voltage			0.4	Volts	Guaranteed output Low voltage at VDDO=2.97V and IOL=maximum rated for pad.
V_{OH}	Output or Bi-directional High Voltage	2.4			Volts	Guaranteed output High voltage at VDDO=2.97V and IOH=maximum rated current for pad.
V_{ST-}	Schmidt Trigger Input Low Voltage			0.8	Volts	Applies to RSTB, TRSTB, CSB, TCK, RDCLK1-4, TDCLK1-4, DCK, ACK and TRCPCLK1-4.
V_{ST+}	Schmidt Trigger Input High Voltage	2.2			Volts	Applies to RSTB, TRSTB, CSB, TCK, RDCLK1-4, TDCLK1-4, DCK, ACK and TRCPCLK1-4.
V_{TH}	Schimdt Trigger Input Hysteresis Voltage		0.5		Volts	Applies to RSTB, TRSTB, CSB, TCK, RDCLK1-4, TDCLK1-4, DCK, ACK and TRCPCLK1-4.
V_{PECLI-}	Input PECL Low Differential Voltage	V_{AVDH} – 1.810		V_{AVDH} - 1.475	Volts	Applies to PECL inputs
V_{PECLI+}	Input PECL High Differential Voltage	V_{AVDH} - 1.165		V_{AVDH} - 0.880	Volts	Applies to PECL inputs
$V_{PECLIcm}$	Input PECL Common Mode	V_{AVDH} - 1.490		V_{AVDH} - 1.180	Volts	Applies to PECL inputs
V_{PECLO-}	Output PECL Low Differential Voltage	V_{AVDH} - 1.810	1.59	V_{AVDH} - 1.620	Volts	Applies to PECL outputs

Symbol	Parameter	Min	Typ	Max	Units	Conditions
V_{PECLO+}	Output PECL High Differential Voltage	V_{AVDH} – 1.025	2.34	V_{AVDH} – 0.880	Volts	Applies to PECL outputs
I_{ILPU}	Input Low Current	-200	-50	-15	µA	VIL = GND. Notes 1 and 3.
I_{IHPU}	Input High Current	-10	0	+10	µA	VIH = VDDO. Notes 1 and 3.
I_{IL}	Input Low Current	-10	0	+10	µA	VIL = GND. Notes 2 and 3.
I_{IH}	Input High Current	-10	0	+10	µA	VIH = VDDO. Notes 2 and 3.
C_{IN}	Input Capacitance		5		pF	tA=25°C, f = 1 MHz
C_{OUT}	Output Capacitance		5		pF	tA=25°C, f = 1 MHz
C_{IO}	Bi-directional Capacitance		5		pF	tA=25°C, f = 1 MHz

Notes on D.C. Characteristics:

1. Since the total power of the chip is greater than the spec of the SBGA package (3 Watts),a heat sink must be used.
2. Input pin or bi-directional pin with internal pull-up resistor.
3. Input pin or bi-directional pin without internal pull-up resistor.
4. Negative currents flow into the device (sinking), positive currents flow out of the device (sourcing).

17 Power Information

17.1 Power Requirements

Table 22 Power Requirements

Conditions	Parameter	Typ[1,3]	High[4]	Max[2]	Units
OC48 All serial links, parallel buses, PRBS generators and PRBS monitors running.	IDDOP (VDDI)	1.77	—	2.100	A
	IDDOP (VDDO)	0.239	—	0.287	A
	IDDOP (RAVDL)	0.022	—	0.060	A
	IDDOP (TAVDL)	0.055	—	0.059	A
	IDDOP (RAVDH)	0.017	—	0.024	A
	IDDOP (TAVDH)	0.182	—	0.192	A
	IDDOP (CAVDH)	0.0058	—	0.0062	A
	IDDOP (QAVDH)	0.00057	—	0.0015	A
	Total Power	4.792	5.456	—	W
4xOC12[5]	IDDOP (VDDI)	1.75			A
	IDDOP (VDDO)	0.376			A
	IDDOP (RAVDL)	1E-6			A
	IDDOP (TAVDL)	1E-6			A
	IDDOP (RAVDH)	0.00384			A
	IDDOP (TAVDH)	6E-6			A
	IDDOP (CAVDH)	0.00107			A
	IDDOP (QAVDH)	0.00057			A
	Total Power	4.4089			W

Notes:

1. Typical IDD values are calculated as the mean value of current under the following conditions: typically processed silicon, nominal supply voltage, Tj=60 °C, outputs loaded with 30 pF, and a normal amount of traffic or signal activity. These values are suitable for evaluating typical device performance in a system.
2. Max IDD values are currents guaranteed by the production test program and/or characterization over process for operating currents at the maximum operating voltage and operating temperature that yields the highest current (including outputs loaded to 30pF).
3. Typical power values are calculated using the formula:

   $$\text{Power} = \sum i(\text{VDDNomi} \times \text{IDDTypi})$$

   Where i denotes all the various power supplies on the device, VDDNomi is the nominal voltage for supply i, and IDDTypi is the typical current for supply i (as defined in note 1 above). These values are suitable for evaluating typical device performance in a system.

4. High power values are a “normal high power” estimate, calculated using the formula:

   Power = ∑i(VDDMaxi x IDDHighi)

   Where i denotes all the various power supplies on the device, VDDMaxi is the maximum operating voltage for supply i, and IDDHighi is the current for supply i. IDDHigh values are calculated as the mean value plus two sigmas (2σ) of measured current under the following conditions: Tj=105° C, outputs loaded with 30 pF. These values are suitable for evaluating board and device thermal characteristics.

5. Since OC48 mode, by design, is higher power than 4xOC12 mode, the max power numbers are tested in the production test program for this mode.

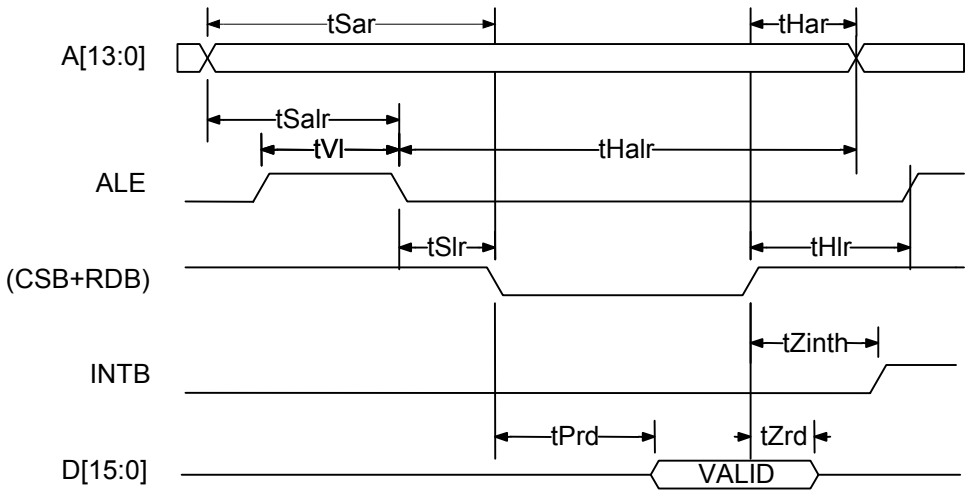
18 Microprocessor Interface Timing Characteristics

T_A = -40°C to T_J = +125°C, $V_{VDDI} = V_{VDDItypical} \pm 5\%$, $V_{VDDO} = V_{DDOtypical} \pm 5\%$
$V_{AVDL} = V_{AVDLtypical} \pm 5\%$, $V_{AVDH} = V_{AVDHtypical} \pm 5\%$
(Typical Conditions: T_C = 25°C, $V_{VDDI} = V_{AVDL}$ =1.8V, $V_{VDDO} = V_{AVDH}$ = 3.3V)

Table 23 Microprocessor Interface Read Access (Figure 43)

Symbol	Parameter	Min	Max	Units
TS_{AR}	Address to Valid Read Set-up Time	10		ns
TH_{AR}	Address to Valid Read Hold Time	5		ns
TS_{ALR}	Address to Latch Set-up Time	10		ns
TH_{ALR}	Address to Latch Hold Time	10		ns
TV_{L}	Valid Latch Pulse Width	5		ns
TS_{LR}	Latch to Read Set-up	0		ns
TH_{LR}	Latch to Read Hold	5		ns
TP_{RD}	Valid Read to Valid Data Propagation Delay		70	ns
TZ_{RD}	Valid Read Negated to Output Tri-state		20	ns
TZ_{INTH}	Valid Read Negated to INTB High (WCIMODE=0)		50	ns

Figure 43 Intel Microprocessor Interface Read Timing



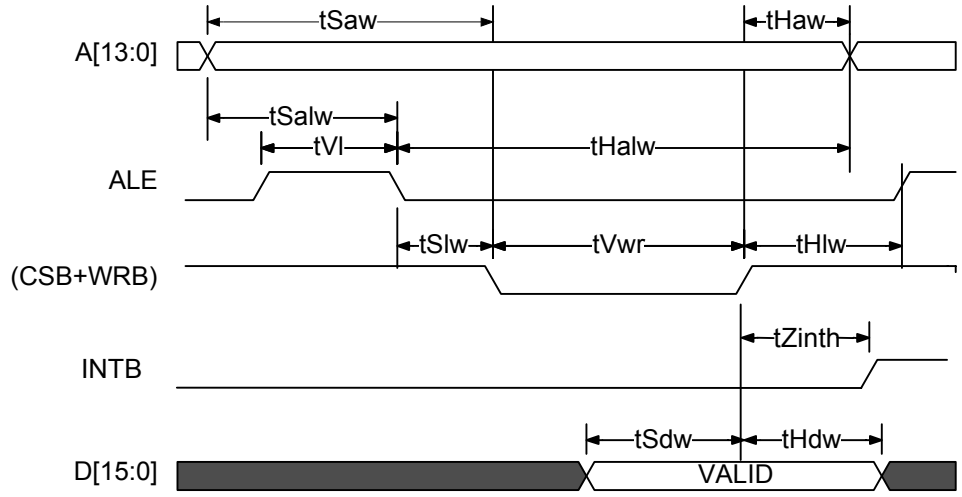
Notes on Microprocessor Interface Read Timing:

1. Output propagation delay time is the time in nanoseconds from the 1.4 Volt point of the reference signal to the 1.4 Volt point of the output.
2. Output propagation delays are measured with a 100 pF load on the Microprocessor Interface data bus, (D[15:0]).
3. A valid read cycle is defined as a logical OR of the CSB and the RDB signals.
4. In non-multiplexed address/data bus architectures, ALE should be held high so parameters tS_{ALR}, tH_{ALR}, tV_L, tS_{LR}, and tH_{LR} are not applicable.
5. Parameter tH_{AR} is not applicable if address latching is used.
6. When a set-up time is specified between an input and a clock, the set-up time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.
7. When a hold time is specified between an input and a clock, the hold time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.

Table 24 Microprocessor Interface Write Access (Figure 44)

Symbol	Parameter	Min	Max	Units
TS_{AW}	Address to Valid Write Set-up Time	10		ns
TS_{DW}	Data to Valid Write Set-up Time	20		ns
TS_{ALW}	Address to Latch Set-up Time	10		ns
TH_{ALW}	Address to Latch Hold Time	10		ns
TV_{L}	Valid Latch Pulse Width	5		ns
TS_{LW}	Latch to Write Set-up	0		ns
TH_{LW}	Latch to Write Hold	5		ns
TH_{DW}	Data to Valid Write Hold Time	5		ns
TH_{AW}	Address to Valid Write Hold Time	5		ns
TV_{WR}	Valid Write Pulse Width	40		ns
TZ_{INTH}	Valid Write to INTB High (WCIMODE=1)		50	ns

Figure 44 Intel Microprocessor Interface Write Timing



Notes on Microprocessor Interface Write Timing:

1. A valid write cycle is defined as a logical OR of the CSB and the WRB signals.
2. In non-multiplexed address/data bus architectures, ALE should be held high so parameters tS_{ALW}, tH_{ALW}, tV_{L}, tS_{LW}, and tH_{LW} are not applicable.
3. Parameter tH_{AW} is not applicable if address latching is used.
4. When a set-up time is specified between an input and a clock, the set-up time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.

5. When a hold time is specified between an input and a clock, the hold time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.

18.1 A.C. TIMING CHARACTERISTICS

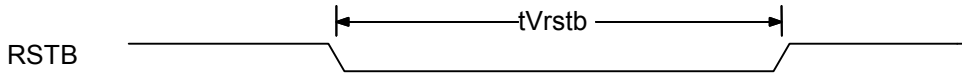
T_A = -40°C to T_J = +125°C, $V_{VDDI} = V_{VDDItypical} \pm 5\%$, $V_{VDDO} = V_{DDOtypical} \pm 5\%$
$V_{AVDL} = V_{AVDLtypical} \pm 5\%$, $V_{AVDH} = V_{AVDHtypical} \pm 5\%$
(Typical Conditions: T_C = 25°C, $V_{VDDI} = V_{AVDL}$ =1.8V, $V_{VDDO} = V_{AVDH}$ = 3.3V)

18.1.1 System Miscellaneous Timing

Table 25 System Miscellaneous Timing (Figure 45)

Symbol	Description	Min	Max	Units
tVRSTB	RSTB input pulse width	100		ns

Figure 45 System Miscellaneous Timing Diagram



18.1.2 Single OC-48 Line Interface Timing

Table 26 RDCLK+/- Input Timing

Symbol	Description	Min	Max	Units
$f_{RDCLK+/-}$	RDCLK+/- Frequency (nominally 155.52MHz)	155	156	MHz
$tHI_{RDCLK+/-}$	RDCLK+/- Hi Pulse Width	2.5		ns
$tLO_{RDCLK+/-}$	RDCLK+/- Low Pulse Width	2.5		ns
tS_{SD}	SD Set-up time to RDCLK+/- rising edge	2		ns
tH_{SD}	SD Hold time to RDCLK+/- rising edge	0		ns
$tS_{RD+/-}$	RD[15:0]+/- Set-up time to RDCLK+/- rising edge	2		ns
$tH_{RD+/-}$	RD[15:0]+/- Hold time to RDCLK+/- rising edge	0		ns
$tS_{RFP+/-}$	RFP+/- Set-up time to RDCLK+/- rising edge	2		ns
$tH_{RFP+/-}$	RFP+/- Hold time to RDCLK+/- rising edge	0		ns

Figure 46 RDCLK+/- Input Timing Diagram

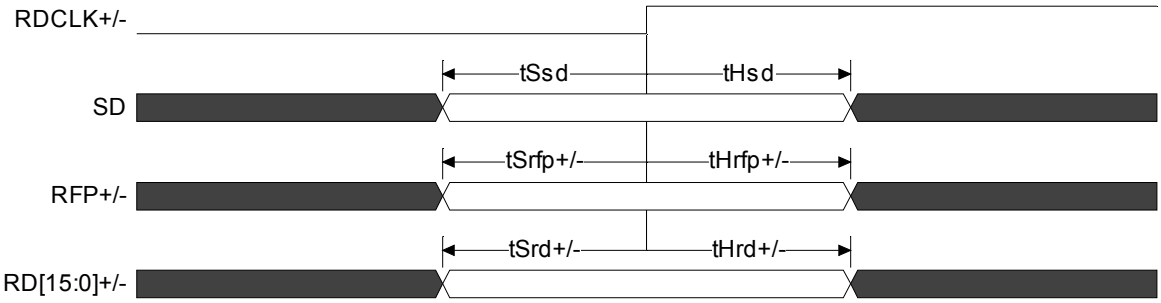


Table 27 RCLK1 Output Timing

Symbol	Description	Min	Max	Units
tP_{OOF}	RCLK1 rising edge to OOF valid	1	7	ns

Figure 47 RCLK1 Output Timing Diagram

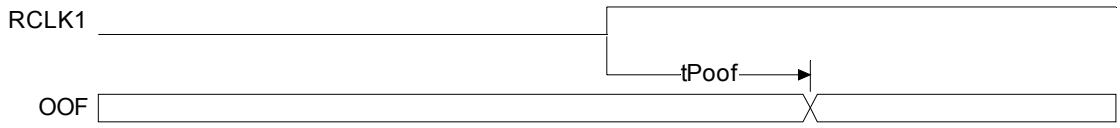


Table 28 TDCLK+/- Input Timing

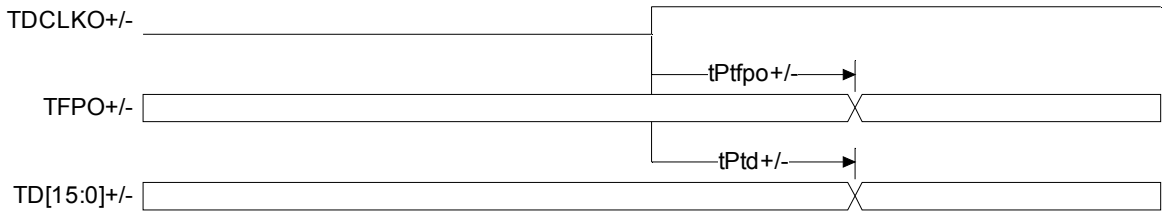
Symbol	Description	Min	Max	Units
fTDCLK+/-	TDCLK+/- Frequency (nominally 155.52MHz)			
tHITDCLK+/-	TDCLK+/- Hi Pulse Width	2.5		ns
tLOTDCLK+/-	TDCLK+/- Low Pulse Width	2.5		ns
$tS_{TFPI+/-}$	TFPI+/- Set-up time to TDCLK+/- rising edge	2		ns
$tH_{TFPI+/-}$	TFPI+/- Hold time to TDCLK+/- rising edge	0		ns

Figure 48 TDCLK+/- Input Timing Diagram

Table 29 TDCLKO+/- Output Timing

Symbol	Description	Min	Max	Units
tPTD+/-	TDCLKO+/- rising edge to TD[15:0]+/- valid	1	3.25	ns
tPTFPO+/-	TDCLKO+/- rising edge to TFPO+/- valid	1	3	ns

Figure 49 TDCLKO+/- Output Timing Diagram



Notes on Input Timing:

1. When a set-up time is specified between an input and a clock, the set-up time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.
2. When a hold time is specified between an input and a clock, the hold time is the time in nanoseconds from the 1.4 Volt point of the clock to the 1.4 Volt point of the input.

Notes on Output Timing:

1. Output propagation delay time is the time in nanoseconds from the 1.4 Volt point of the reference signal to the 1.4 Volt point of the output.
2. Output propagation delays are measured with a 30 pF load on the outputs except when otherwise specified.

18.1.3 Quad OC-12 Line Interface Timing

Table 30 RDCLK1-4 Input Timing

Symbol	Description	Min	Max	Units
fRDCLK	RDCLK1-4 Frequency (nominally 77.76MHz)	77	78	MHz
tHIRDCLK	RDCLK1-4 Hi Pulse Width	5		ns
tLORDCLK	RDCLK1-4 Low Pulse Width	5		ns
tS_{SD}	SD1-4 Set-up time to RDCLK1-4 rising edge	3		ns
tH_{SD}	SD1-4 Hold time to RDCLK1-4 rising edge	0.25		ns
tS_{RD}	RD[7:0]1-4 Set-up time to RDCLK1-4 rising edge	3		ns
tH_{RD}	RD[7:0]1-4 Hold time to RDCLK1-4 rising edge	0.15		ns

Figure 50 RDCLK1-4 Input Timing Diagram

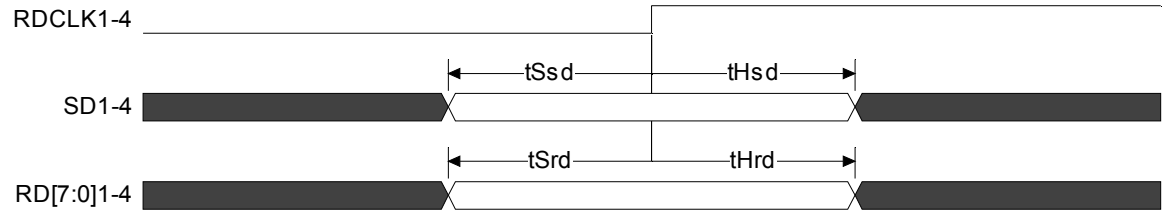


Table 31 TDCLK1-4 Input Timing

Symbol	Description	Min	Max	Units
fTDCLK	TDCLK1-4 Frequency (nominally 77.76Hz)	77	78	MHz
tHITDCLK	TDCLK1-4 Hi Pulse Width	5		ns
tLOTDCLK	TDCLK1-4 Low Pulse Width	5		ns
tS_{TFPI}	TFPI1-4 Set-up time to TDCLK1-4 rising edge	3		ns
tH_{TFPI}	TFPI1-4 Hold time to TDCLK1-4 rising edge	0		ns

Figure 51 TDCLK1-4 Input Timing Diagram

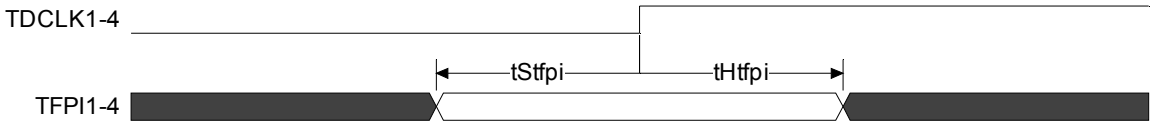
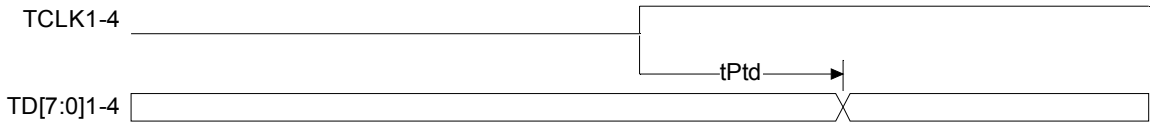


Table 32 TCLK1-4- Output Timing

Symbol	Description	Min	Max	Units
tP_{TD}	TCLK1-4 rising edge to TD[7:0]1-4 valid	1	7	ns

Figure 52 TDCLK1-4 Output Timing Diagram



Notes on Input Timing:

1. When a set-up time is specified between an input and a clock, the set-up time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.
2. When a hold time is specified between an input and a clock, the hold time is the time in nanoseconds from the 1.4 Volt point of the clock to the 1.4 Volt point of the input.

Notes on Output Timing:

1. Output propagation delay time is the time in nanoseconds from the 1.4 Volt point of the reference signal to the 1.4 Volt point of the output.
2. Output propagation delays are measured with a 30 pF load on the outputs except when otherwise specified.

18.1.4 Receive Overhead Port Timing

Table 33 ROHCLK1-4 Output Timing

Symbol	Description	Min	Max	Units
tPRRCPDAT	ROHCLK1-4 falling edge to RRCPDAT1-4 valid	-7	7	ns
tPSALM	ROHCLK1-4 falling edge to SALM1-4 valid	-7	7	ns
tPRALM	ROHCLK1-4 falling edge to RALM1-4 valid	-7	7	ns
tPROHFP	ROHCLK1-4 falling edge to ROHFP1-4 valid	-7	7	ns
tPRTOH	ROHCLK1-4 falling edge to RTOH1-4 valid	-7	7	ns
tPRPOH	ROHCLK1-4 falling edge to RPOH1-4 valid	-7	7	ns
tPRPOHEN	ROHCLK1-4 falling edge to RPOHEN1-4 valid	-7	7	ns
tPB3E	ROHCLK1-4 falling edge to B3E1-4 valid	-7	7	ns

Figure 53 ROHCLK1-4 Output Timing Diagram

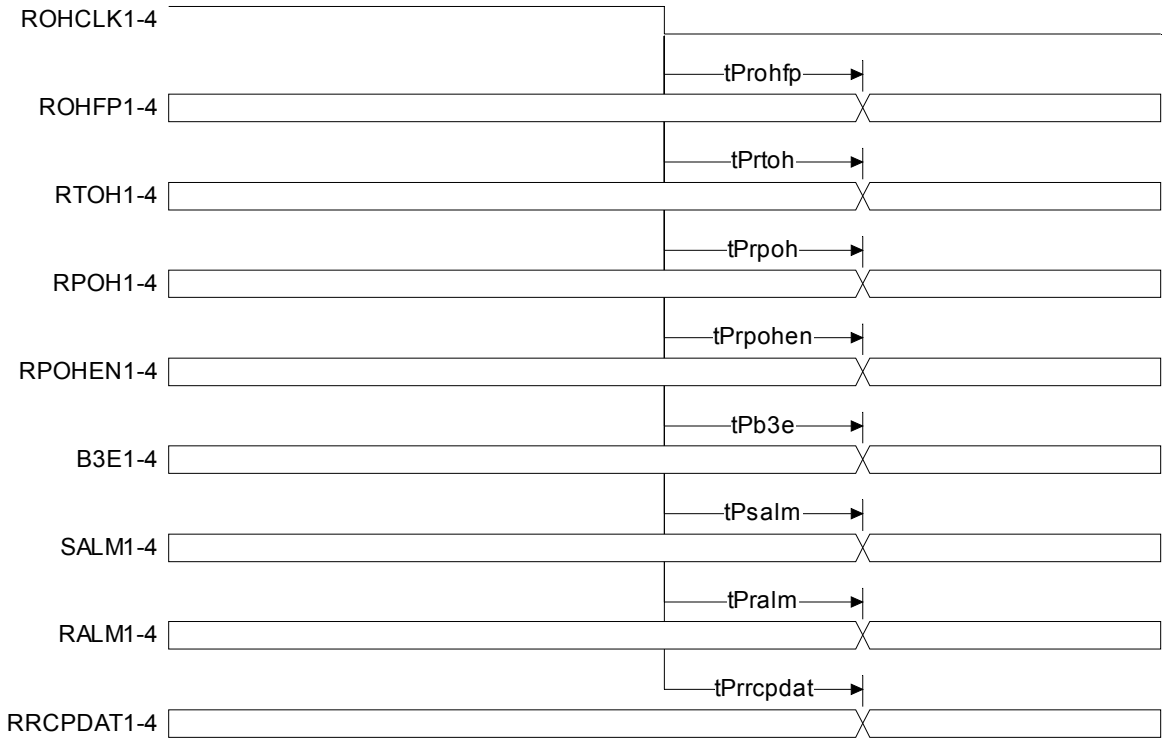


Table 34 RSLDCLK Output Timing

Symbol	Description	Min	Max	Units
tPRSLD	RSLDCLK falling edge to RSLD valid	-7	7	ns

Figure 54 RSLDCLK Output Timing Diagram

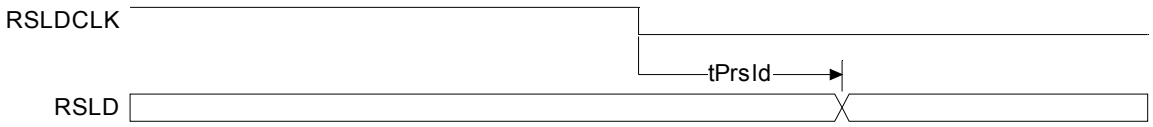
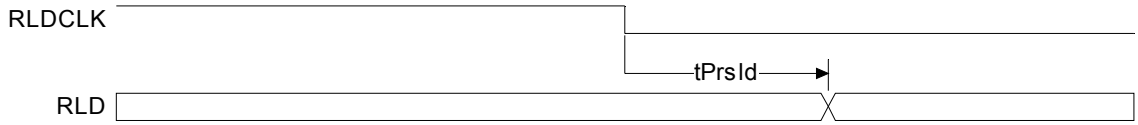


Table 35 RLDCLK Output Timing

Symbol	Description	Min	Max	Units
tP_{RLD}	RLDCLK falling edge to RLD valid	-7	7	ns

Figure 55 RLDCLK Output Timing Diagram



Notes on Input Timing:

1. When a set-up time is specified between an input and a clock, the set-up time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.
2. When a hold time is specified between an input and a clock, the hold time is the time in nanoseconds from the 1.4 Volt point of the clock to the 1.4 Volt point of the input.

Notes on Output Timing:

1. Output propagation delay time is the time in nanoseconds from the 1.4 Volt point of the reference signal to the 1.4 Volt point of the output.
2. Output propagation delays are measured with a 30 pF load on the outputs except when otherwise specified.

18.1.5 Transmit Overhead Port Timing

Table 36 TOHCLK1-4 Input Timing

Symbol	Description	Min	Max	Units
tSTTOH	TTOH1-4 Set-up time to TOHCLK1-4 rising edge	14		ns
tHTTOH	TTOH1-4 Hold time to TOHCLK1-4 rising edge	0		ns
tSTTOHEN	TTOHEN1-4 Set-up time to TOHCLK1-4 rising edge	14		ns
tHTTOHEN	TTOHEN1-4 Hold time to TOHCLK1-4 rising edge	0		ns
tSTPOH	TPOH1-4 Set-up time to TOHCLK1-4 rising edge	14		ns
tHTPOH	TPOH1-4 Hold time to TOHCLK1-4 rising edge	0		ns
tSTPOHEN	TPOHEN1-4 Set-up time to TOHCLK1-4 rising edge	14		ns
tHTPOHEN	TPOHEN1-4 Hold time to TOHCLK1-4 rising edge	0		ns

Figure 56 TOHCLK1-4 Input Timing Diagram

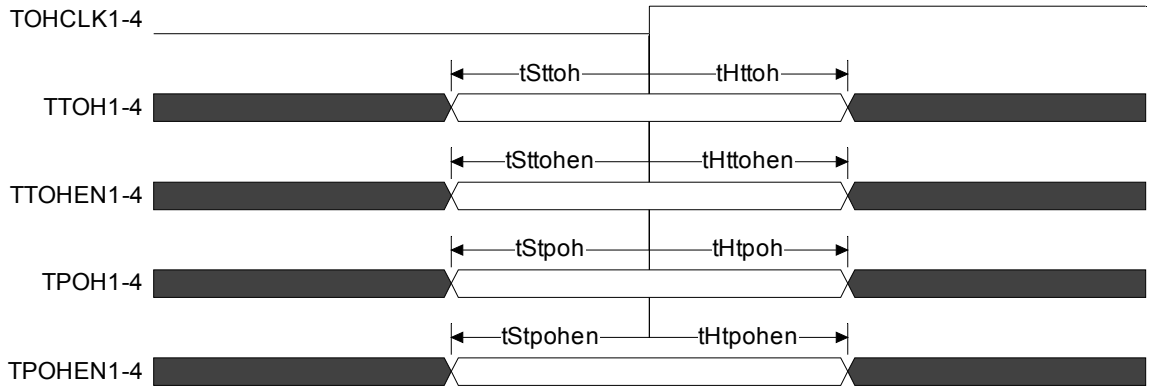


Table 37 TOHCLK1-4 Output Timing

Symbol	Description	Min	Max	Units
tPTOHFP	TOHCLK1-4 falling edge to TOHFP1-4 valid	-7	7	ns
tPTPOHRDY	TOHCLK1-4 falling edge to TPOHRDY1-4 valid	-7	7	ns

Figure 57 TOHCLK1-4 Output Timing Diagram

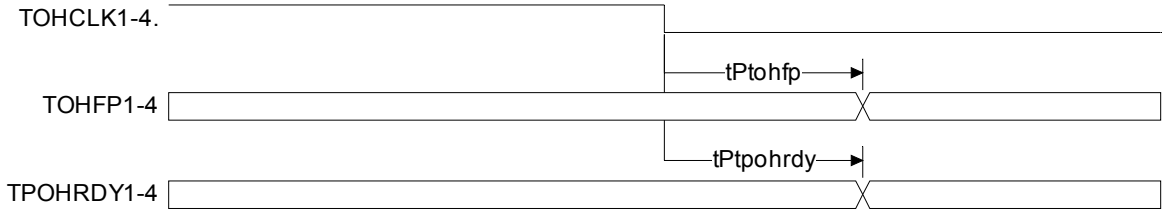


Table 38 TSLDCLK Input Timing

Symbol	Description	Min	Max	Units
tSTSLD	TSLD Set-up time to TSLDCLK rising edge	14		ns
tHTSLD	TSLD Hold time to TSLDCLK rising edge	0		ns

Figure 58 TSLDCLK Input Timing Diagram

Table 39 TLDCLK Input Timing

Symbol	Description	Min	Max	Units
tS_{TLD}	TLD Set-up time to TLDCLK rising edge	14		ns
tH_{TLD}	TLD Hold time to TLDCLK rising edge	0		ns

Figure 59 TLDCLK Input Timing Diagram

Notes on Input Timing:

1. When a set-up time is specified between an input and a clock, the set-up time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.
2. When a hold time is specified between an input and a clock, the hold time is the time in nanoseconds from the 1.4 Volt point of the clock to the 1.4 Volt point of the input.

Notes on Output Timing:

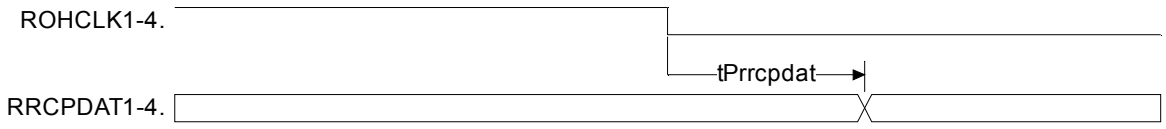
3. Output propagation delay time is the time in nanoseconds from the 1.4 Volt point of the reference signal to the 1.4 Volt point of the output.
4. Output propagation delays are measured with a 30 pF load on the outputs except when otherwise specified.

18.1.6 Receive Ring Control Port Timing

Table 40 ROHCLK1-4 Output Timing

Symbol	Description	Min	Max	Units
TPRRCPDAT	ROHCLK1-4 falling edge to RRCPDAT1-4 valid	-7	7	ns

Figure 60 TRCPCLK1-4 Input Timing Diagram



Notes on Input Timing:

1. When a set-up time is specified between an input and a clock, the set-up time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.
2. When a hold time is specified between an input and a clock, the hold time is the time in nanoseconds from the 1.4 Volt point of the clock to the 1.4 Volt point of the input.

Notes on Output Timing:

1. Output propagation delay time is the time in nanoseconds from the 1.4 Volt point of the reference signal to the 1.4 Volt point of the output.

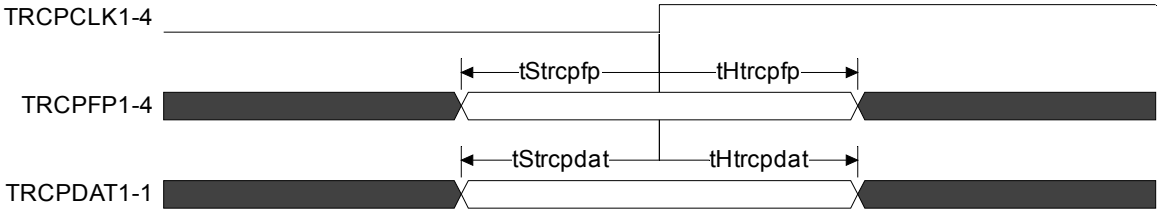
2. Output propagation delays are measured with a 30 pF load on the outputs except when otherwise specified.

18.1.7 Transmit Ring Control Port Timing

Table 41 TRCPCLK1-4 Input Timing

Symbol	Description	Min	Max	Units
tSTRCPFP	TRCPFP1-4 Set-up time to TRCPCLK1-4 rising edge	10		ns
tHTRCPFP	TRCPFP1-4 Hold time to TRCPCLK1-4 rising edge	5		ns
tSTRCPDAT	TRCPDAT1-4 Set-up time to TRCPCLK1-4 rising edge	10		ns
tHTRCPDAT	TRCPDAT1-4 Hold time to TRCPCLK1-4 rising edge	5		ns

Figure 61 TRCPCLK1-4 Input Timing Diagram



Notes on Input Timing:

1. When a set-up time is specified between an input and a clock, the set-up time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.
2. When a hold time is specified between an input and a clock, the hold time is the time in nanoseconds from the 1.4 Volt point of the clock to the 1.4 Volt point of the input.

Notes on Output Timing:

1. Output propagation delay time is the time in nanoseconds from the 1.4 Volt point of the reference signal to the 1.4 Volt point of the output.
2. Output propagation delays are measured with a 30 pF load on the outputs except when otherwise specified.

18.1.8 System Interface Timing

Table 42 ACK Input Timing

Symbol	Description	Min	Max	Units
fACK	ACK Frequency (nominally 77.76MHz)	77	78	MHz
tHIACK	ACK Hi Pulse Width	5		ns
tLOACK	ACK Low Pulse Width	5		ns
tS_{AJ0J1_FP}	AJ0J1/AFP1-4 Set-up time to ACK rising edge	3		ns
tH_{AJ0J1_FP}	AJ0J1/AFP1-4 Hold time to ACK rising edge	0		ns
tS_{ADP}	ADP1-4 Set-up time to ACK rising edge	3		ns
tH_{ADP}	ADP1-4 Hold time to ACK rising edge	0		ns
tS_{AD}	AD1-4[7:0] Set-up time to ACK rising edge	3.25		ns

Symbol	Description	Min	Max	Units
tH_{AD}	AD1-4[7:0] Hold time to ACK rising edge	0		ns
tS_{APL}	APL1-4 Set-up time to ACK rising edge	3		ns
tH_{APL}	APL1-4 Hold time to ACK rising edge	0		ns
tS_{APAIS}	APAIS1-4 Set-up time to ACK rising edge	3		ns
tH_{APAIS}	APAIS1-4Hold time to ACK rising edge	0		ns
tS_{ACMP}	ACMP Set-up time to ACK rising edge	3		ns
tH_{ACMP}	ACMP Hold time to ACK rising edge	0		ns

Figure 62 ACK Input Timing Diagram

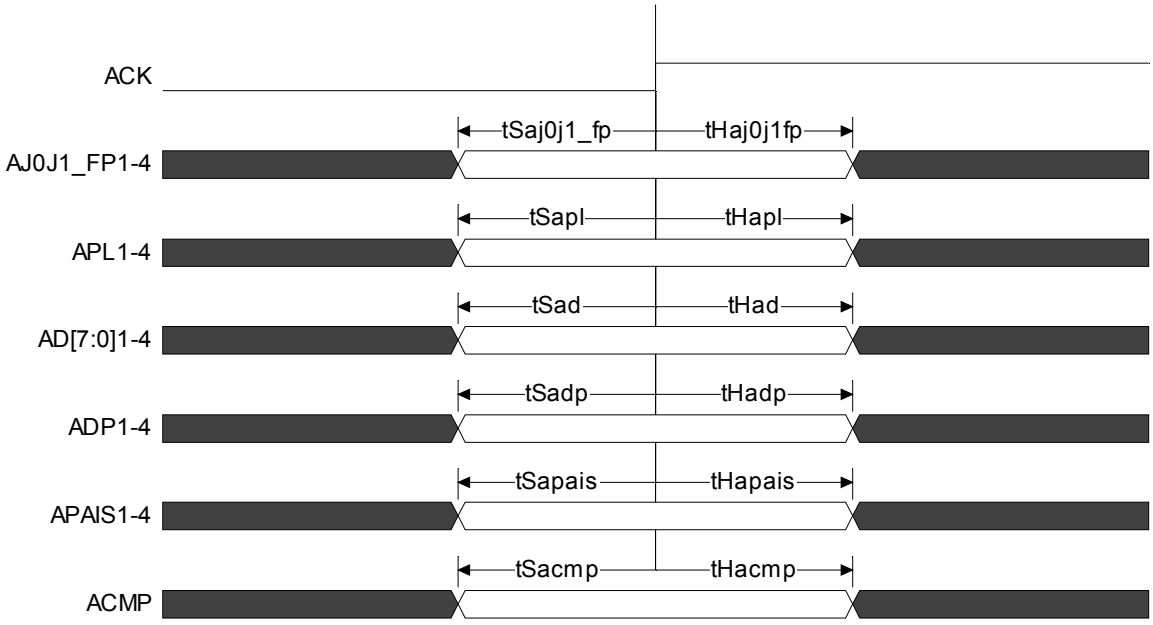


Table 43 DCK Input Timing

Symbol	Description	Min	Max	Units
fDCK	DCK Frequency (nominally 77.76MHz)	77	78	MHz
tHIDCK	DCK Hi Pulse Width	5		ns
tLODCK	DCK Low Pulse Width	5		ns
tS_{DJ0REF}	DJ0REF Set-up time to DCK rising edge	3		ns
tH_{DJ0REF}	DJ0REF Hold time to DCK rising edge	0		ns
tS_{DCMP}	DCMP Set-up time to DCK rising edge	3		ns
tH_{DCMP}	DCMP Hold time to DCK rising edge	0		ns

Figure 63 DCK Input Timing Diagram

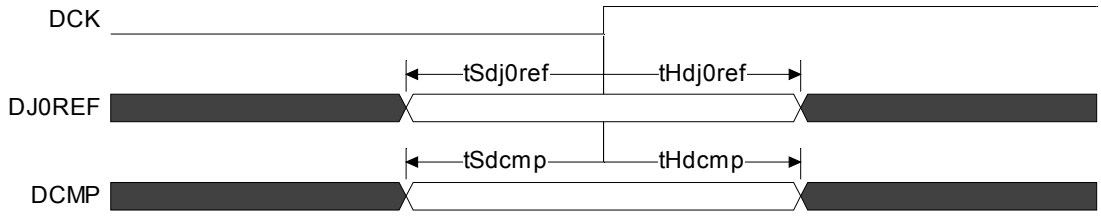
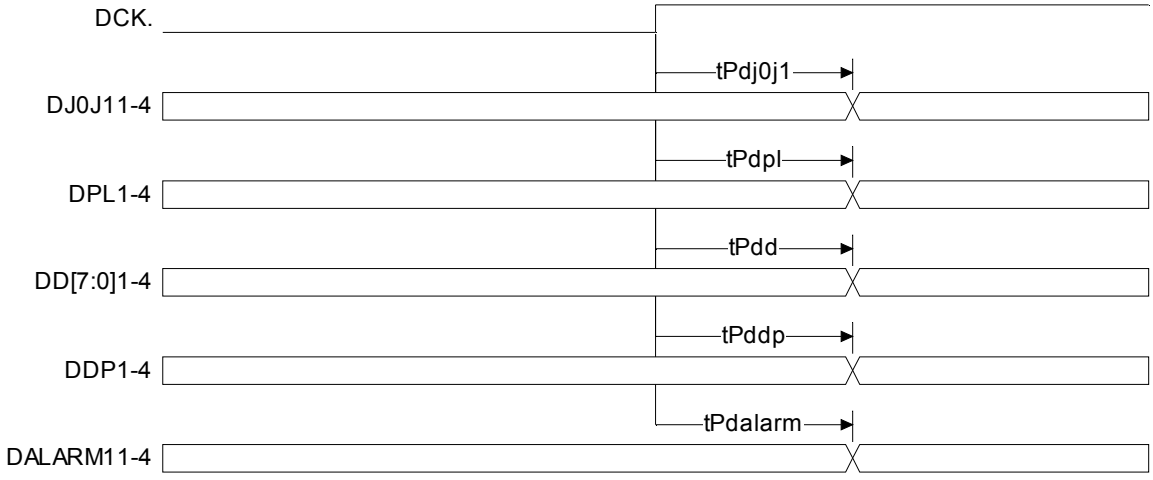


Table 44 DCK Output Timing

Symbol	Description	Min	Max	Units
tPDJ0J1	DCK rising edge to DJ0J11-4 valid	1	7	ns
tPDD	DCK rising edge to DD1-4[7:0] valid	1	7	ns
tPDDP	DCK rising edge to DDP1-4 valid	1	7	ns
tPDPL	DCK rising edge to DPL1-4 valid	1	7	ns
tPDALARM	DCK rising edge to DALARM1-4 valid	1	7	ns

Figure 64 DCK Output Timing Diagram



Notes on Input Timing:

1. When a set-up time is specified between an input and a clock, the set-up time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.
2. When a hold time is specified between an input and a clock, the hold time is the time in nanoseconds from the 1.4 Volt point of the clock to the 1.4 Volt point of the input.

Notes on Output Timing:

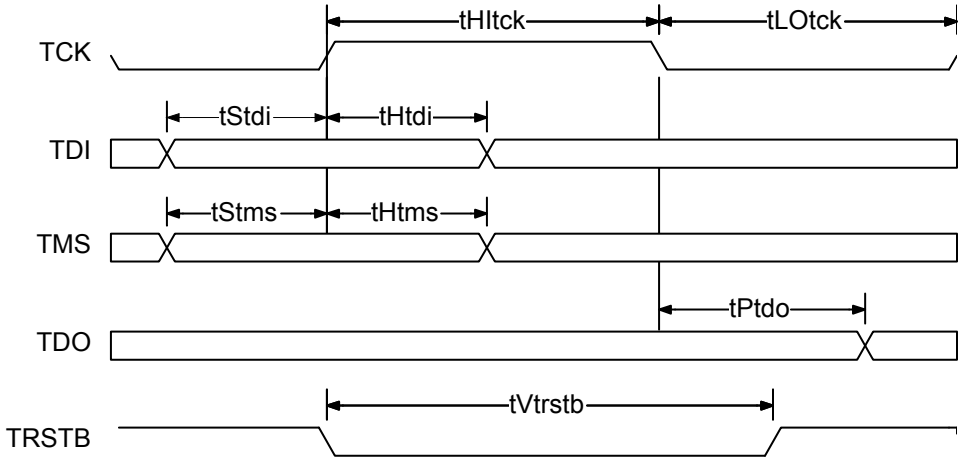
1. Output propagation delay time is the time in nanoseconds from the 1.4 Volt point of the reference signal to the 1.4 Volt point of the output.
2. Output propagation delays are measured with a 30 pF load on the outputs except when otherwise specified.

18.1.9 JTAG Test Port Timing

Table 45 JTAG Port Interface (Figure 65)

Symbol	Description	Min	Max	Units
fTCK	TCK Frequency		4	MHz
tHITCK	TCK HI Pulse Width	100		ns
tHITCK	TCK LO Pulse Width	100		ns
tSTMS	TMS Set-up time to TCK	25		ns
tHTMS	TMS Hold time to TCK	25		ns
tSTDI	TDI Set-up time to TCK	25		ns
tHTDI	TDI Hold time to TCK	25		ns
tPTDO	TCK Low to TDO Valid	2	25	ns
tVTRSTB	TRSTB Pulse Width	100		ns

Figure 65 JTAG Port Interface Timing



Notes on Input Timing:

1. When a set-up time is specified between an input and a clock, the set-up time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.
2. When a hold time is specified between an input and a clock, the hold time is the time in nanoseconds from the 1.4 Volt point of the clock to the 1.4 Volt point of the input.

Notes on Output Timing:

1. Output propagation delay time is the time in nanoseconds from the 1.4 Volt point of the reference signal to the 1.4 Volt point of the output.
2. Output propagation delays are measured with a 30 pF load on the outputs except when otherwise specified.

19 Thermal Information

This product is designed to operate over a wide temperature range when used with a heat sink and is suited for outside plant equipment[1].

Table 46 Outside Plant Thermal Information

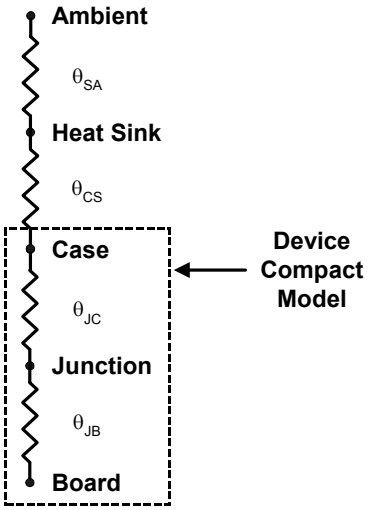
Maximum long-term operating junction temperature (T_J) to ensure adequate long-term life.	105 °C
Maximum junction temperature (T_J) for short-term excursions with guaranteed continued functional performance[2]. This condition will typically be reached when the local ambient temperature reaches 85 °C.	125 °C
Minimum ambient temperature (T_A)	-40 °C

Table 47 Device Compact Model[3]

θ_{JC}	0.1 °C/W
θ_{JB}	7.0 °C/W

Table 48 Heat Sink Requirements

$\theta_{SA}+\theta_{CS}$[4]	[(105-70)/P]-θ_{JC} °C/W[5]
θ_{SA} and θ_{CS} are required for long-term operation	



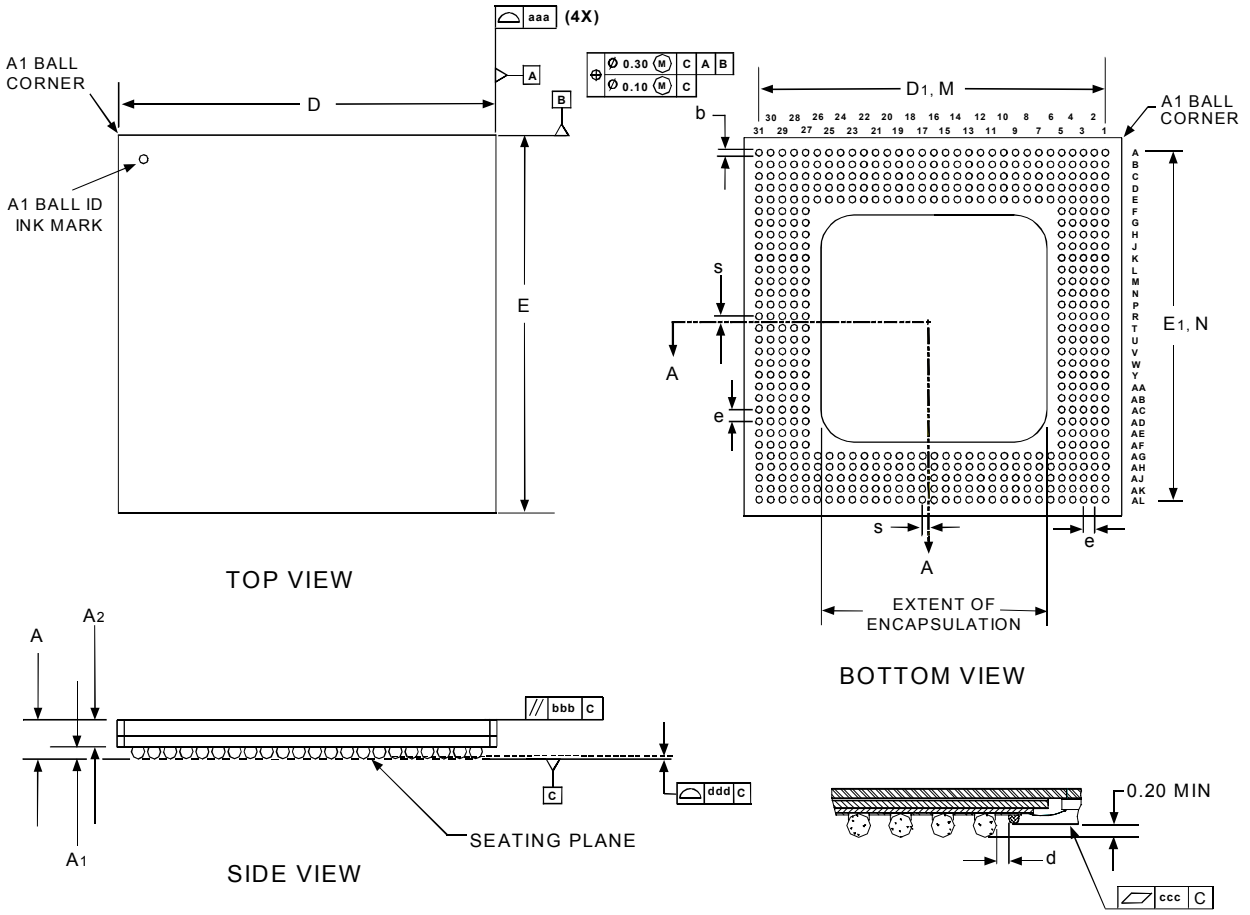
Operating power is dissipated in the package at the worst-case power supply. Power depends upon the operating mode. Please refer to 'High' power values in section 17.1 Power Requirements.

Notes

1. The minimum ambient temperature requirement for Outside Plant Equipment meets the minimum ambient temperature requirement for Industrial Equipment
2. Short-term is used as defined in Telcordia Technologies Generic Requirements GR-63-Core Core.
3. θ_{JC}, the junction-to-case thermal resistance, is a measured nominal value plus two sigma. θ_{JB}, the junction-to-board thermal resistance, is obtained by simulating conditions described in JEDEC Standard JESD 51-8.
4. θ_{SA} is the thermal resistance of the heat sink to ambient. θ_{CS} is the thermal resistance of the heat sink attached material. The maximum θ_{SA} required for the airspeed at the location of the device in the system with all components in place.
5. In this formula, obtain power (P) in watts from section 17.1 Power Requirements.

20 Mechanical Information

Figure 66 Mechanical Drawing 520 Pin Super Ball Grid Array (SBGA)



NOTES: 1) ALL DIMENSIONS IN MILLIMETER.
2) DIMENSION aaa DENOTES PACKAGE BODY PROFILE.
3) DIMENSION bbb DENOTES PARALLEL.
4) DIMENSION ccc DENOTES FLATNESS.
5) DIMENSION ddd DENOTES COPLANARITY.

PACKAGE TYPE : 520 THERMALLY ENHANCED BALL GRID ARRAY - SBGA																
BODY SIZE : 40 x 40 x 1.54 MM																
Dim.	A	A_1	A_2	D	D_1	E	E_1	M,N	b	d	e	aaa	bbb	ccc	ddd	S
Min.	1.30	0.50	0.80	39.90	38.00	39.90	38.00		0.60	0.5	-	-	-	-		-
Nom.	1.51	0.60	0.91	40.00	38.10	40.00	38.10	31x31	0.75	-	1.27	-	-	-		0.00
Max.	1.70	0.70	1.00	40.10	38.20	40.10	38.20		0.90	-	-	0.20	0.25	0.20	0.20	-